LT1310

1.5A Boost DC/DC Converter with Phase-Locked Loop

December 2001

FEATURES

- Synchronizable or Constant Frequency Low Noise Output
- Synchronizable Up to 4.5MHz
- Wide Input Voltage Range: 2.8V to 18V
- Low Profile Surface Mount Solution (All Ceramic Capacitors)
- Low V_{CESAT} Switch: 240mV at 1A
- Adjustable Output from V_{IN} to 35V
- Small Thermally Enhanced 10-Lead MSOP Package

APPLICATIONS

- Instruments
- Avionics
- Data Acquisition
- Communications
- Imaging
- Ultrasound

DESCRIPTION

The LT®1310 boost DC/DC converter combines a 1.5A current mode PWM switcher with an integrated phase-lock loop, allowing the user to set the switching frequency anywhere from 10kHz to 4.5MHz. Intended for use in applications where switching frequency must be accurately controlled, the LT1310 can generate 12V at up to 400mA from a 5V input.

Switching frequency is set with an external capacitor, and the device can be operated in either free-running or phase-locked mode. A wide capture range of nearly 2:1 allows the free-running frequency to be set using standard 10% tolerance NP0 dielectric capacitors.

The LT1310 is available in the tiny thermally enhanced 10-lead MSOP package.

TYPICAL APPLICATION

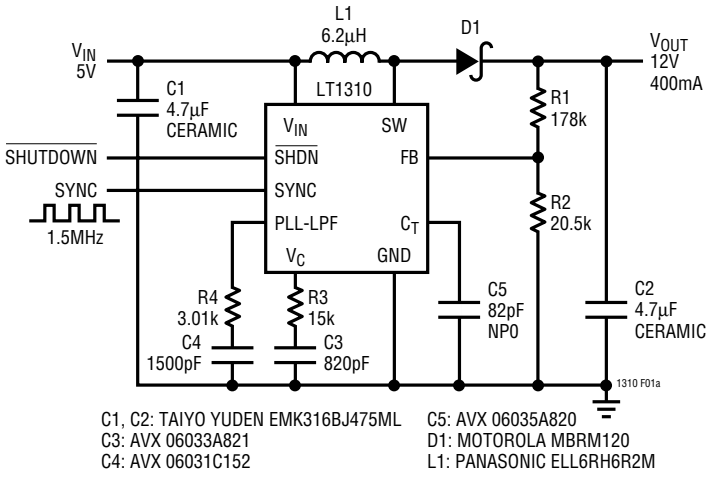
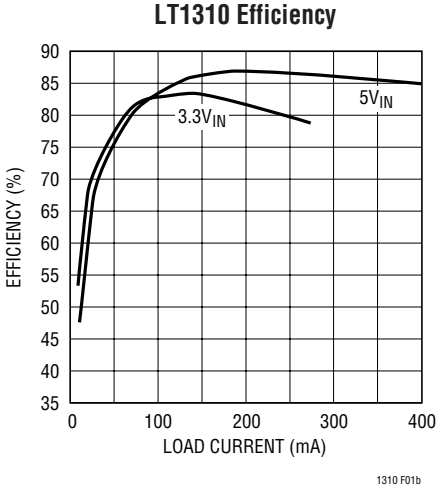


Figure 1. 5V to 12V Converter Synchronized at 1.5MHz

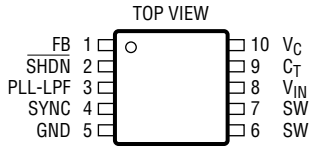


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} 18V
$\overline{SHDN}$ 18V
SYNC 18V
FB 5V
C_T 5V
V_C 2V
PLL-LPF 2V
SW 36V
Operating Temperature Range (Note 2) .. –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



MSE EXPOSED PAD PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 40°C/W

EXPOSED PAD IS GROUND
(MUST BE SOLDERED TO PCB)

ORDER PART NUMBER
LT1310EMSE
MSE PART MARKING
LTRZ

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V, $V_{\overline{SHDN}}$ = 3.3V, unless otherwise noted. (Note 2)

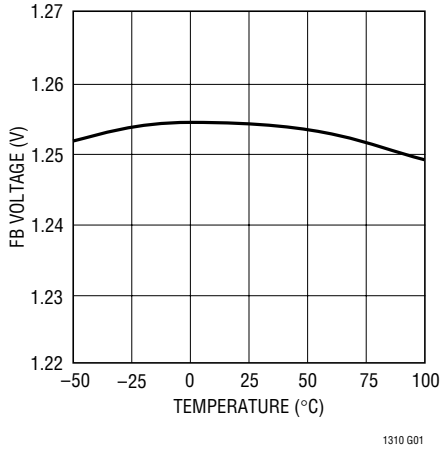
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Undervoltage Lockout					2.8	V
Maximum Input Voltage					18	V
Feedback Voltage		 ●	1.242 1.236	1.255	1.268 1.268	V V
FB Pin Bias Current				60	150	nA
Reference Line Regulation	V_{IN} = 2.9V to 18V			0.01	0.05	%/V
Error Amplifier Transconductance	ΔI = 5μA			350		μA/V
Error Amplifier Voltage Gain				200		V/V
SW Current Limit			1.5	2.1	2.8	A
SW Saturation Voltage	I_{SW} = 1A			0.240	0.320	V
SW Maximum Duty Cycle	C_T = 220pF C_T = 47pF		80 78	84 83		% %
SW Minimum On Time	I_{SW} = 150mA, V_C = 0.25V			70		ns
VCO Frequency	C_T = 220pF, PLL-LPF = High C_T = 220pF, PLL-LPF = High C_T = 220pF, PLL-LPF = Low C_T = 47pF, PLL-LPF = High	 ● 	0.950 0.800 	1.10 500 3.3	1.25 1.30 630 	MHz MHz kHz Mhz
Frequency Foldback	C_T = 220pF, PLL-LPF = High, FB = 0V			200		kHz
PLL Lock Range	C_T = 220pF, Maximum C_T = 220pF, Minimum (Percent Change from Max)		0.950 –40	1.10 –50	1.25 	MHz %
Supply Current	$\overline{SHDN}$ = High $\overline{SHDN}$ = Low			11.5 	15 1	mA μA
SW Leakage Current	Switch Off, SW = 3.3V			0.1	5	μA
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 2.4V			35	65	μA
$\overline{SHDN}$ Pin High	Active Mode		2.4			V
$\overline{SHDN}$ Pin Low	Shutdown Mode				0.4	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

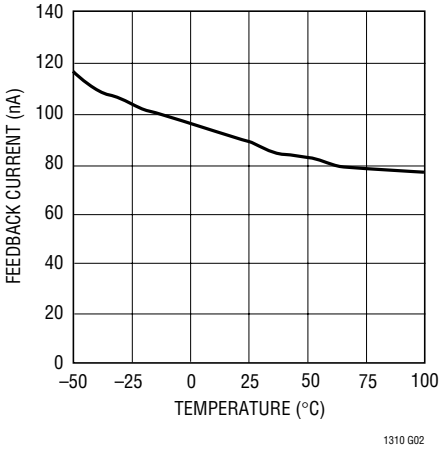
Note 2: The LT1310E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, chacterization and correlation with statistical process controls.

TYPICAL PERFORMANCE CHARACTERISTICS

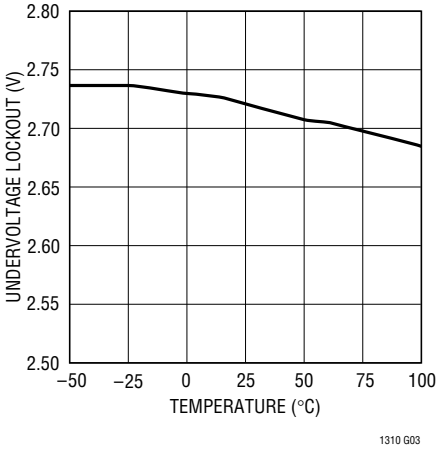
Feedback Voltage



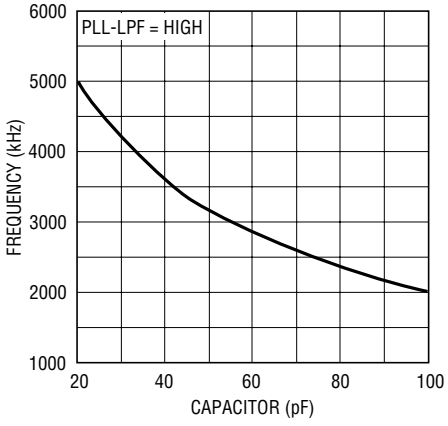
Feedback Pin Current



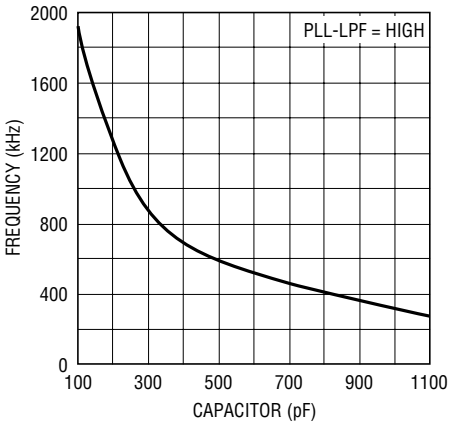
Undervoltage Lockout



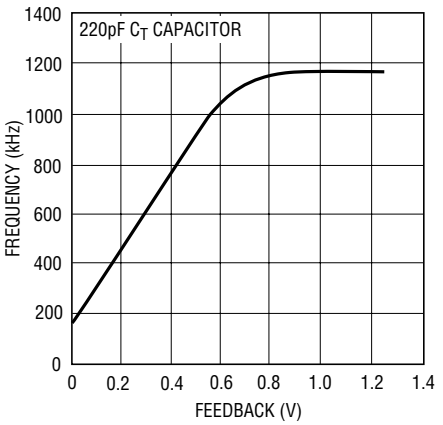
Oscillator Frequency vs C_T Capacitor



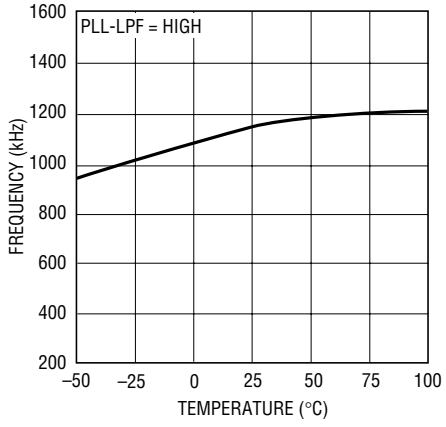
Oscillator Frequency vs C_T Capacitor



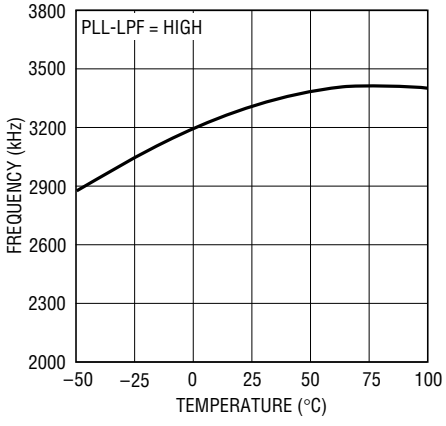
Oscillator Frequency vs Feedback Voltage



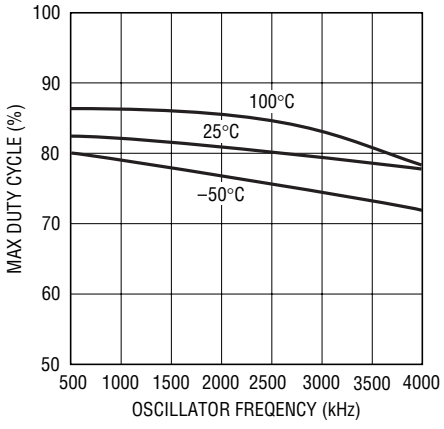
Oscillator Frequency 220pF Capacitor on C_T Pin



Oscillator Frequency 47pF Capacitor on C_T Pin

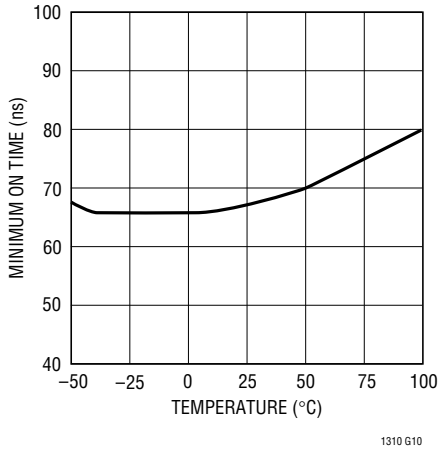


Maximum Duty Cycle vs Oscillator Frequency

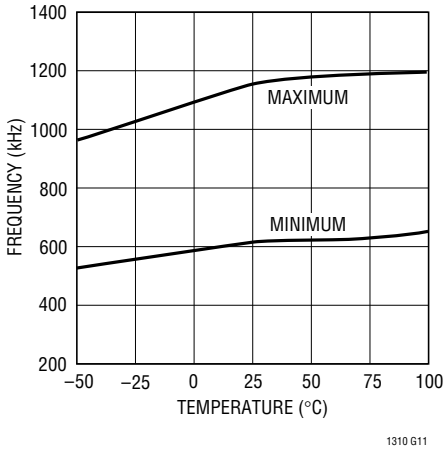


TYPICAL PERFORMANCE CHARACTERISTICS

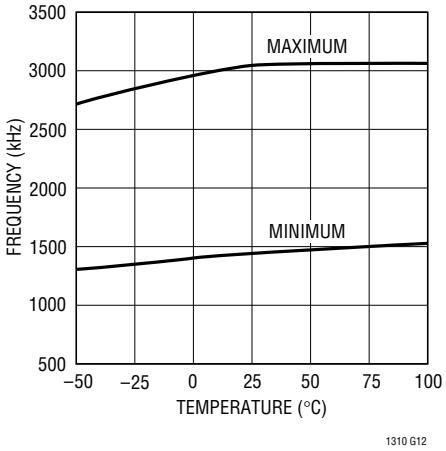
Switch Minimum On Time



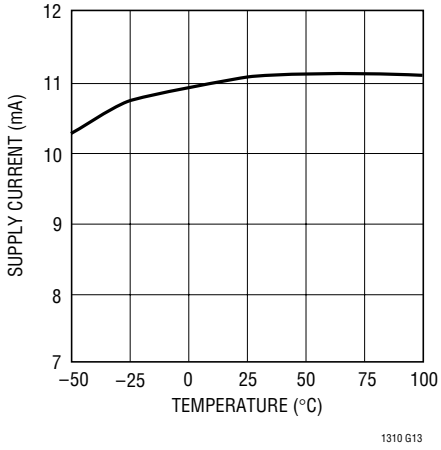
PLL Lock Range
220pF Capacitor on C_T Pin



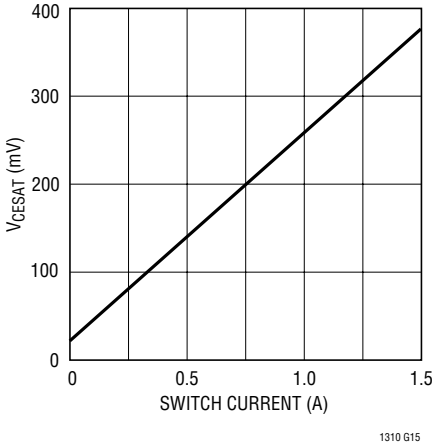
PLL Lock Range
47pF Capacitor on C_T Pin



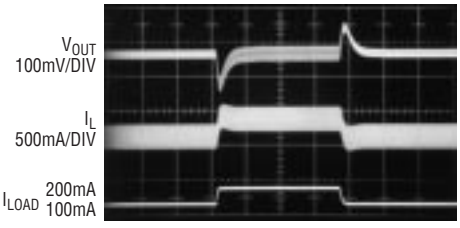
Supply Current



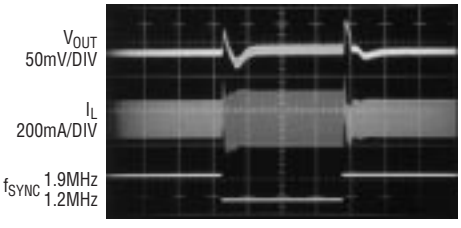
Switch V_{CESAT}



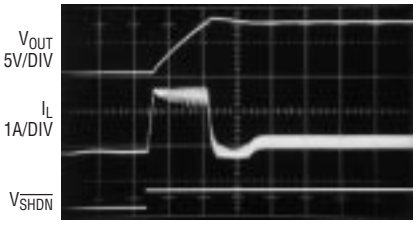
Transient Response



PLL Response



Start-Up Response



PIN FUNCTIONS

FB (Pin 1): Feedback Pin for Error Amplifier. Connect the resistor divider here to set output voltage according to the formula:

$V_{OUT} = 1.255(1 + R1/R2)$

Minimize trace area at this pin.

$\overline{SHDN}$ (Pin 2): Shutdown Pin. For active mode, tie this pin to a voltage between 2.4V and 18V. To disable the part and go into low current mode, pull this pin below 0.4V.

PLL-LPF (Pin 3): Phase Locked-Loop Filter Pin. This is the output of the phase detector and also the input to the voltage controlled oscillator (VCO). Connect an RC filter here. Typically, R = 3k and C = 1500pF. If the part is not externally synchronized (no sync signal), pull this pin to V_{IN} through a 10k resistor (PLL-LPF = HIGH). This drives the oscillator to its maximum frequency.

SYNC (Pin 4): Frequency Synchronization Pin. Inject the external synchronizing signal here. This signal must be ground referred and have a minimum amplitude of 1.2V. The phase detector is edge triggered and when locked the rising edge of the sync signal will be aligned with the turn-on of the power transistor.

GND (Pin 5, Exposed Pad): Ground. **Tie both Pin 5 and the exposed pad directly to local ground plane**. The ground metal to the exposed pad should be wide for better heat dissipation. Multiple vias (local ground plane ↔ ground backplane) placed close to the exposed pad can further aid in reducing thermal resistance.

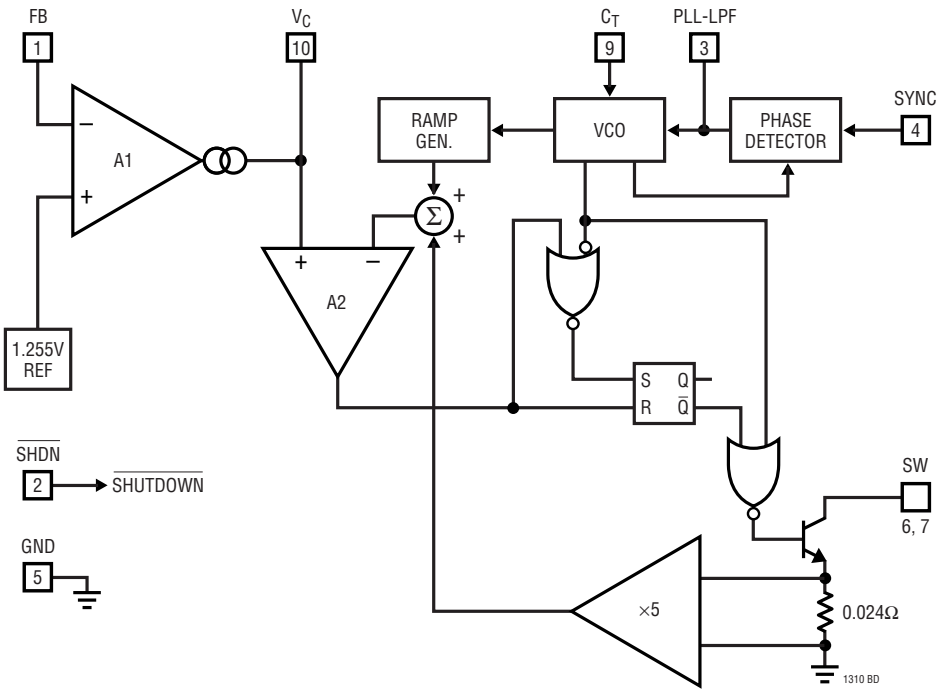
SW (Pins 6, 7): Switch Pin. Connect inductor/diode here. Minimize trace area at this pin to keep EMI down.

V_{IN} (Pin 8): Supply Pin. Must be bypassed as close as possible to the pin.

C_T (Pin 9): Timing Capacitor Pin for VCO. Place the timing capacitor from this pin to ground to set the frequency range for the oscillator. Minimize trace at this pin to reduce stray capacitance.

V_C (Pin 10): Compensation Pin for Error Amplifier. Tie an RC network here to compensate the voltage feedback loop.

BLOCK DIAGRAM



OPERATION

To understand operation, refer to the Block Diagram. The LT1310 contains a boost switching regulator that can be phase locked to an external synchronizing signal. The boost regulator uses current mode control and contains a 1.5A NPN power transistor. This type of control uses two feedback loops. The main control loop sets output voltage and operates as follows: a load step causes V_{OUT} and the FB voltage to be slightly perturbed. The error amplifier A1 responds to this change in FB by driving the V_C pin either higher or lower. Because switch current is proportional to the V_C pin voltage, this change causes the switch current to be adjusted until V_{OUT} is once again satisfied. Loop compensation is taken care of by an RC network from the V_C pin to ground. Inside this main loop is another that sets current limit on a cycle-by-cycle basis. This loop utilizes current comparator A2 to control peak current. The oscillator issues a set pulse to the flip-flop at the beginning of each cycle, turning the switch on. With the switch now in the ON state, the SW pin is effectively connected to ground. Current ramps up in the inductor linearly at a rate of V_{IN}/L. Switch current is set by the V_C pin voltage and when the voltage across R_{SENSE} trips the current comparator, a reset pulse will be generated and the switch will be turned off. Since the inductor is now loaded up with current, the SW pin will fly high until it is clamped by the catch diode, D1. Current will flow through the diode decreasing at a rate of $(V_{OUT} – V_{IN})/L$ until the oscillator issues a new set pulse, causing the cycle to repeat.

The LT1310 is phase lockable up to 4.5MHz, giving the user precise control over switching frequency. The phase detector compares the incoming sync signal to the internal oscillator signal. If the switching frequency is lower than the sync signal, or if the phase lags the sync signal, then the phase detector output will source current into the PLL-LPF pin, driving it higher. The PLL-LPF pin is also the input to the voltage controlled oscillator. If the sync signal is slower than the switching frequency, the PLL-LPF pin will sink current until the PLL-LPF pin voltage drops. When locked, the PLL-LPF pin rests at a voltage between 0V and 1.3V. The PLL-LPF pin is capable of sinking or sourcing approximately 30μA.

C_T Selection for Operating Frequency

The LT1310's internal voltage controlled oscillator frequency range is set by an external timing capacitor, C_T. A graph for selecting C_T vs operating frequency is shown in Figure 3. The VCO frequency is proportional to the PLL-LPF pin voltage with maximum frequency corresponding to maximum PLL-LPF pin voltage. For Figure 2, the PLL-LPF pin is pulled high with a 10k resistor to V_{IN}.

When using Figure 3's graph for synchronizable applications, choose C_T according to a frequency value approximately 33% above your center frequency. For this case, the PLL-LPF pin will be driven by the internal phase detector and should be connected only to the RC filter shown in Figure 1.

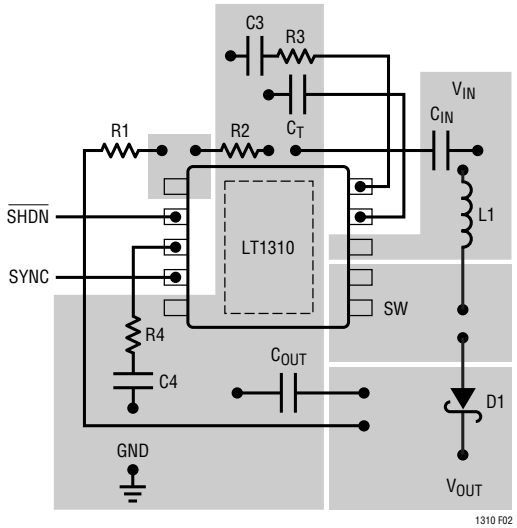


Figure 2. Suggested Layout

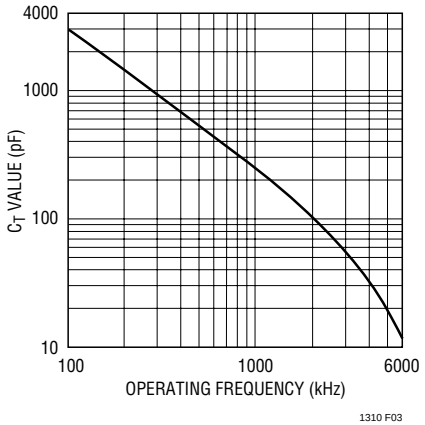
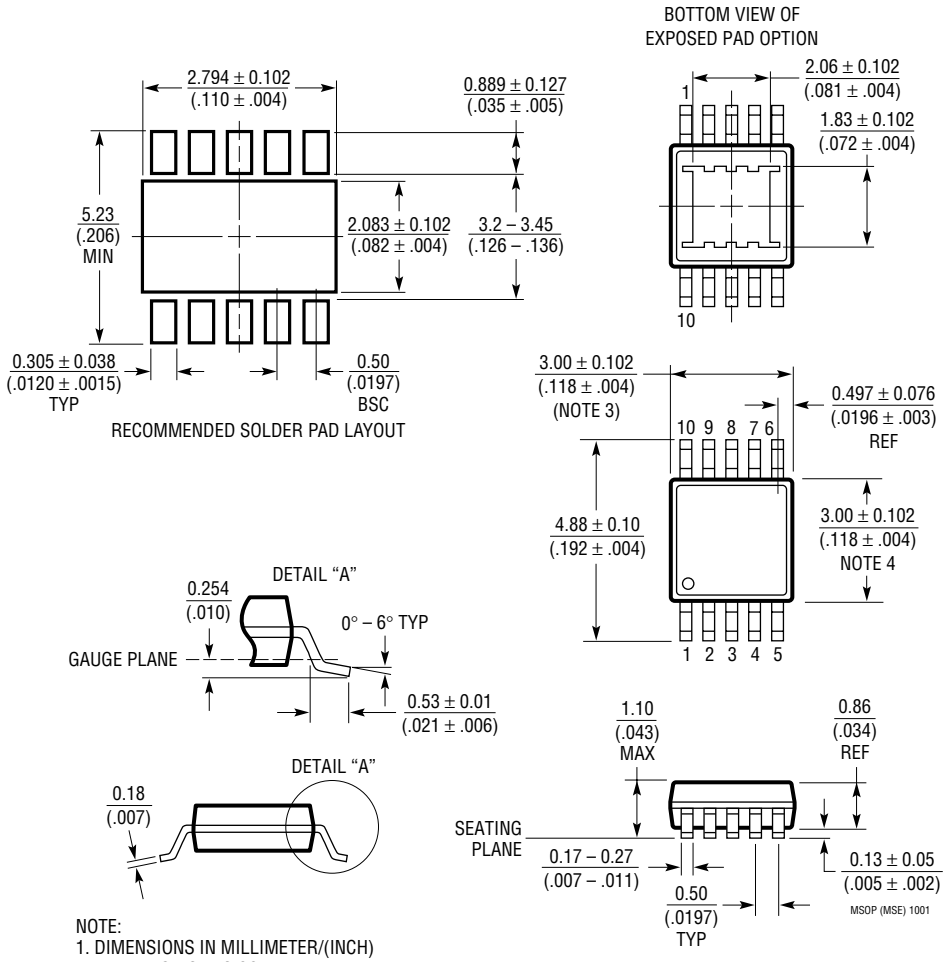


Figure 3. C_T vs Operating Frequency

PACKAGE DESCRIPTION

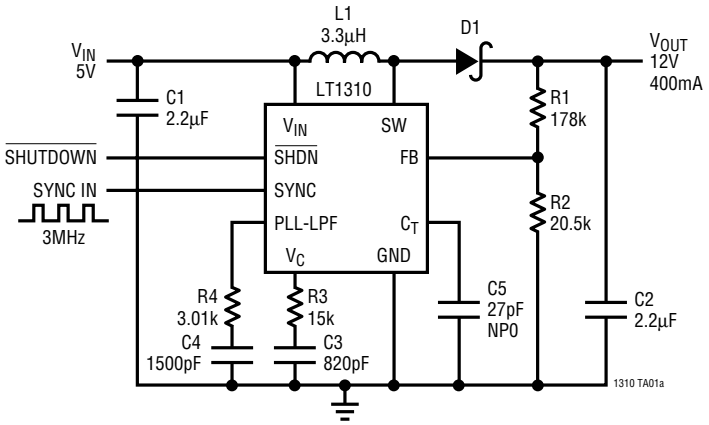
MSE Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1663)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

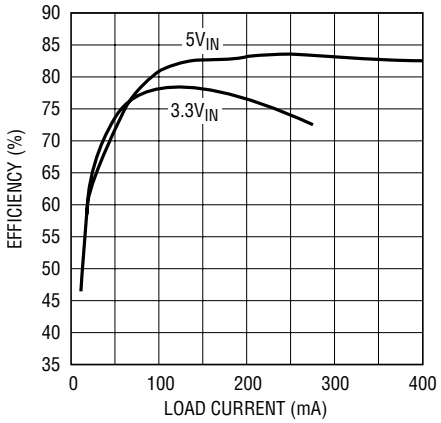
TYPICAL APPLICATION

3MHz 5V to 12V Converter



C1, C2: TAIYO YUDEN LMK212BJ225MG
D1: MOTOROLA MBRM120
L1: PANASONIC ELL6RH3R3M

Efficiency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1767	Monolithic 1.5A, 1.25MHz Step-Down Switching Regulator	V_{IN}: 3V to 25V, Current Mode, 8-Lead MSOP
LT1930	1A, 1.2MHz/2.2MHz Step-Up DC/DC Converters in ThinSOT™	12V at 300mA from 5V Input, ThinSOT Package
LT1946	1.2MHz Boost DC/DC Converter with 1.5A Switch and Soft-Start	8V at 430mA from 3.3V Input, 8-Lead MSOP Package
LTC3402	2A, 3MHz Micropower Synchronous Boost Converter	97% Efficiency, 10-Lead MSOP Package

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