DATA SHEET

PCA9518

Expandable 5-channel I^2C hub

Product data

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Philips
Semiconductors

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Expandable 5-channel I²C hub PCA9518

DESCRIPTION

The PCA9518 is a BiCMOS integrated circuit intended for application in I²C and SMBus systems.

While retaining all the operating modes and features of the I²C system, it permits extension of the I²C-bus by buffering both the data (SDA) and the clock (SCL) lines, thus enabling virtually unlimited buses of 400 pF.

The I²C-bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9518 enables the system designer to divide the bus into an unlimited number of segments off of a hub where any segment to segment transition sees only one repeater delay and is multiple master capable on each segment.

Using multiple PCA9518 parts, any width hub (in multiples of five)[1] can be implemented using the expansion pins.

FEATURES

- Expandable 5 channel, bi-directional buffer
- I²C-bus and SMBus compatible
- Active high individual repeater enable inputs
- Open-drain input/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates standard mode and fast mode I²C devices and multiple masters
- Powered-off high impedance I²C pins
- Operating supply voltage range of 3.0 V to 3.6 V
- 5 V tolerant I²C and enable pins
- 0 to 400 kHz clock frequency[2]
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101.
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA.
- Package offerings: SO and TSSOP

PIN CONFIGURATION

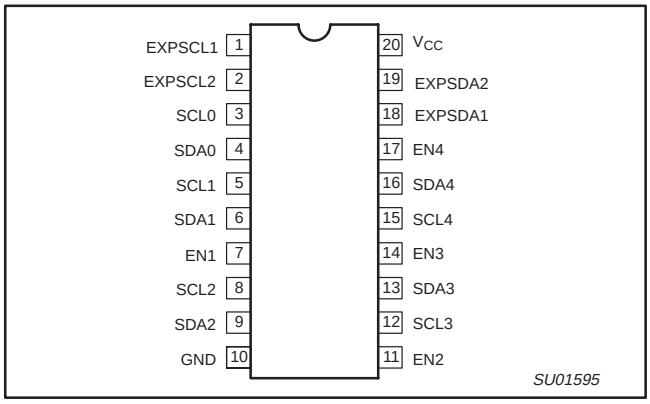


Figure 1. Pin configuration

PIN DESCRIPTION

PIN	SYMBOL	FUNCTION
1	EXPSCL1	Expandable serial clock pin 1
2	EXPSCL2	Expandable serial clock pin 2
3	SCL0	Serial clock bus 0
4	SDA0	Serial data bus 0
5	SCL1	Serial clock bus 1
6	SDA1	Serial data bus 1
7	EN1	Active High Bus 1 enable Input
8	SCL2	Serial clock bus 2
9	SDA2	Serial data bus 2
10	GND	Supply ground
11	EN2	Active High Bus 2 enable Input
12	SCL3	Serial clock bus 3
13	SDA3	Serial data bus 3
14	EN3	Active High Bus 3 enable Input
15	SCL4	Serial clock bus 4
16	SDA4	Serial data bus 4
17	EN4	Active High Bus 4 enable Input
18	EXPSDA1	Expandable serial data pin 1
19	EXPSDA2	Expandable serial data pin 2
20	V_{CC}	Supply power

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
20-pin plastic SO	–40 to +85 °C	PCA9518D	PCA9518D	SOT163-1
20-pin plastic TSSOP	–40 to +85 °C	PCA9518PW	PCA9518	SOT360-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

1. Only four ports per device are available if individual Enable is required.
2. The maximum system operating frequency may be less than 400 KHz because of the delays added by the repeater.

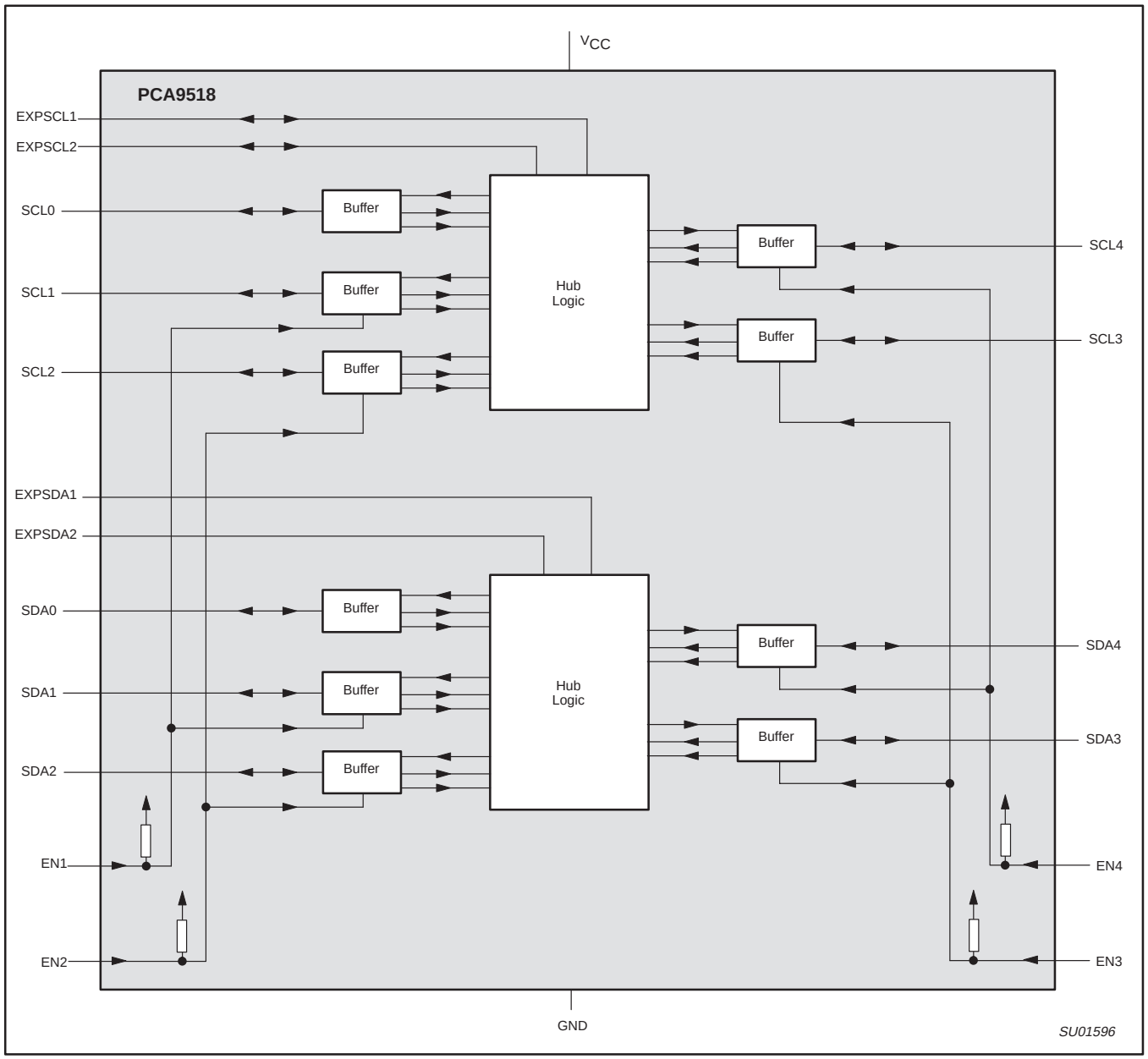


Figure 2. Block Diagram: PCA9518

A more detailed view of Figure 2 buffer is shown in Figure 3.

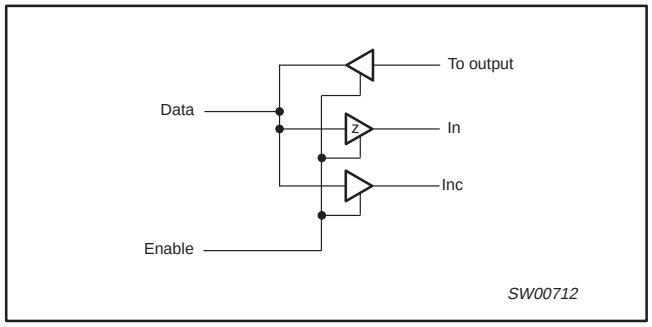


Figure 3.

The output pull-down voltage of each internal buffer is set for approximately 0.5 V, while the input threshold of each internal buffer is set about 0.07 V lower, when the output is internally driven low. This prevents a lock-up condition from occurring.

FUNCTIONAL DESCRIPTION

The PCA9518 BiCMOS integrated circuit is a five way hub repeater, which enables I²C and similar bus systems to be expanded in increments of five with only one repeater delay and no functional degradation of system performance.

The PCA9518 BiCMOS integrated circuit contains five multi-directional, open drain buffers specifically designed to support the standard low-level-contention arbitration of the I²C-bus. Except during arbitration or clock stretching, the PCA9518 acts like a pair of non-inverting, open drain buffers, one for SDA and one for SCL.

Enable

The enable pins EN1 through EN4 are active high and have internal pull-up resistors. Each enable pin ENn controls its associated SDAn and SCLn ports. When low, the ENn pin blocks the inputs from SDAn and SCLn, as well as disabling the output drivers on the SDAn and SCLn pins. The enable pins should only change state when both the global bus and the local port are in an idle state to prevent system failures.

The active high enable pins allow the use of open drain drivers which can be wire-ORed to create a distributed enable where either centralized control signal (master) or spoke signal (submaster) can enable the channel when it is idle.

Expansion

The PCA9518 includes 4 open drain I/O pins used for expansion. Two expansion pins, EXPSDA1 and EXPSDA2 are used to communicate the internal state of the serial data within each hub to the other hubs. The EXPSDA1 pins of all hubs are connected together to form an open drain bus. Similarly, all EXPSDA2 pins, EXPSCL1 pins, and all EXPSCL2 pins are connected together forming a 4-wire bus between hubs.

When it is necessary to be able to deselect every port, each expansion device only contributes 4 ports which can be enabled or disables because the fifth does not have an enable pin.

Pull-up resistors are required on the EXPXXXX[3] pins even if only one PCA9518 is used.

I²C Systems

As with the standard I²C system, pull-up resistors are required to provide the logic HIGH levels on the Buffered bus. (Standard open-collector or open-drain configuration of the I²C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part is designed to work with standard mode (0 to 100 kHz) and fast mode (0 to 400 kHz) I²C devices in addition to SMBus devices. Standard mode I²C devices only specify 3 mA output drive, this limits the termination current to 3 mA in a generic I²C system where standard mode devices and multiple masters are possible. Please see Application Note AN255 *"I²C & SMBus Repeaters, Hubs and Expanders"* for additional information on sizing resistors.

APPLICATION INFORMATION

A typical application is shown in Figure 4. In this example, the system master is running on a 3.3 V I²C-bus while the slaves are connected to a 3.3 V or 5 V bus. All buses run at 100 kHz unless slave 3, 4 and 5 are isolated from the bus. Then the master bus and slave 1, 2 and 6 can run at 400 kHz.

Any segment of the hub can talk to any other segment of the hub. Bus masters and slaves can be located on any segment with 400 pF load allowed on each segment.

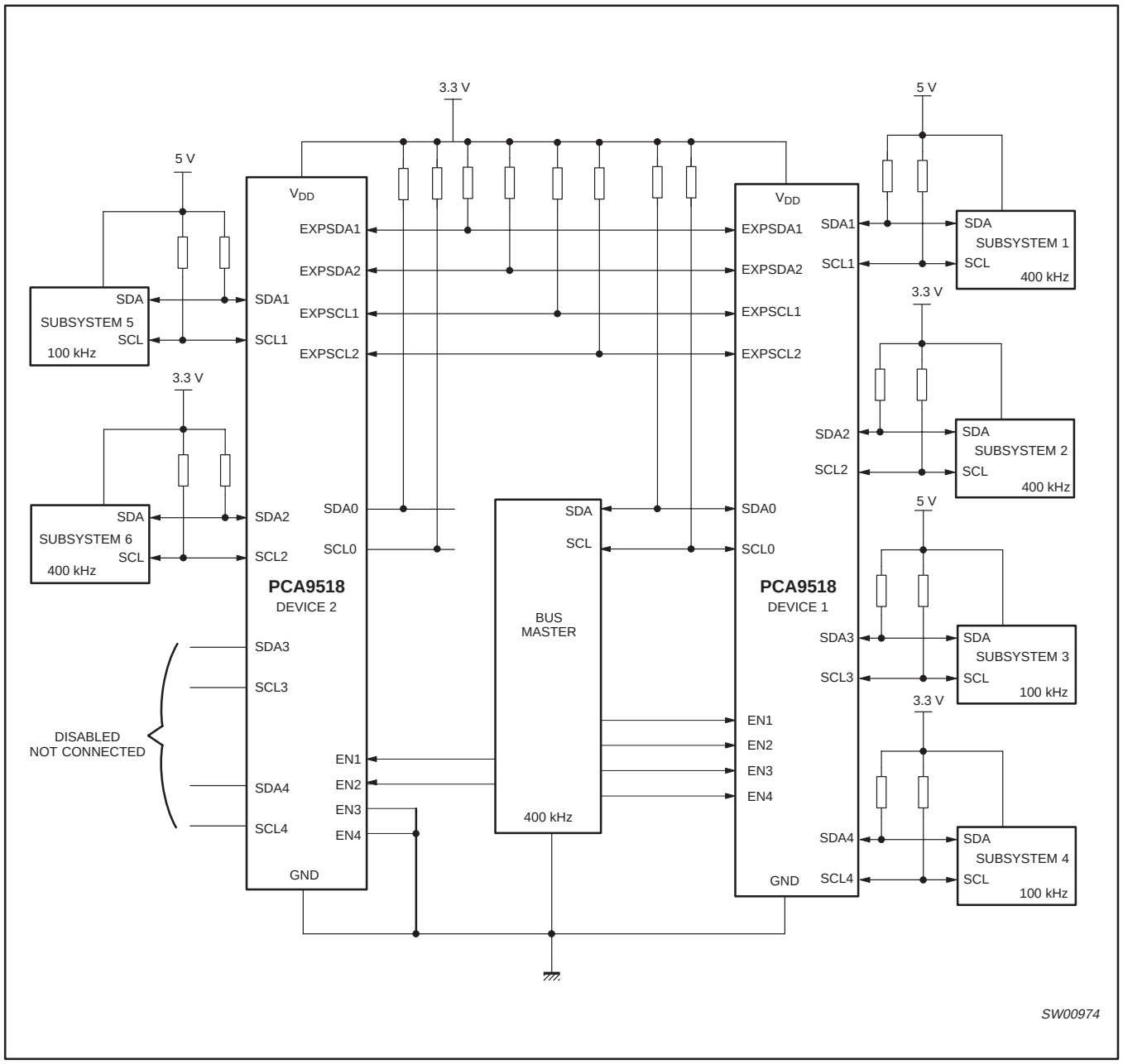
The PCA9518 is 5 V tolerant so it does not require any additional circuitry to translate between the different bus voltages.

When one port of the PCA9518 is pulled low by a device on the I²C bus, a CMOS hysteresis type input detects the falling edge and drives the EXPXXX1 line low, when the EXPXXX1 voltage is less than1/2V_{CC}, the other ports are pulled down to the V_{OL} of the PCA9518 which is typically 0.5 V.

In order to illustrate what would be seen in a typical application, refer to Figure 5. If the bus master in Figure 4 were to write to the slave through the PCA9518, we would see the waveform shown in Figure 5. This looks like a normal I²C transmission except for the small foot preceding each clock low to high transition and proceeding each data low to high transition for the master. The foot height is the difference between the low level driven by the master and the higher voltage low level driven by the PCA9518 repeater. Its width corresponds to an effective clock stretching coming from the PCA9518 which delays the rising edge of the clock. That same magnitude of delay is seen on the rising edge of the data. The foot on the rising edge of the data is extended through the 9th clock pulse as the PCA9518 repeats the acknowledge from the slave to the master. The clock of the slave looks normal except the V_{OL} is the ~0.5 V level generated by the PCA9518. The SDA at the slave has a particularly interesting shape during the 9th clock cycle where the slave pulls the line below the value driven by the PCA9518 during the acknowledge and then returns to the PCA9518 level creating a foot before it completes the low to high transition. SDA lines other than the one with the master and the one with the slave have a uniform low level driven by the PCA9518 repeater.

The other four waveforms are the expansion bus signals and are included primarily for timing reference points. All timing on the expansion bus is with respect to 0.5 V_{CC}. EXPSDA1 is the expansion bus that is driven low whenever any SDA pin falls below 0.3 V_{CC}. EXPSDA2 is the expansion bus that is driven low whenever any pin is ≤0.4 V. EXPSCL1 is the expansion bus that is driven low whenever any SCL pin falls below 0.3 V_{CC}. EXPSCL2 is the expansion bus that is driven low whenever any SCL pin is ≤0.4 V. The EXPSDA2 returns high after the SDA pin that was the last one being held below 0.4 V by an external driver starts to rise. The last SDA to rise above 0.4 V is held down by the PCA 9518 to ~0.5 V until after the delay of the circuit which determines that it was the last to rise, then it is allowed to rise above the ~0.5 V level driven by the PCA9518. Considering the bus 0 SDA to be the last one to go above 0.4 V, then the EXPSDA1 returns to high after the EXPSDA2 is high and either the bus 0 SDA rise time is 1 μs or, when the bus 0 SDA reaches 0.7 V_{CC}, whichever occurs first. After both EXPSDA2 and EXPSDA1 are high the rest of the SDA lines are allowed to rise. The same description applies for the EXPSCL1, EXPSCL2, and SCL pins.

3. XXXX is SDA1, SDA2, SCL1, or SCL2
XXX is SDA or SCL



NOTE:
1. Only two of the five channels on the PCA9518 Device 2 are being used. EN3 and EN4 are connected to GND to disable channels 3 and 4. SDA0 and SCL0 must be pulled-up to V_{CC} since there is no enable pin.

Figure 4. Typical application: Multiple expandable 5-channel I²C hubs

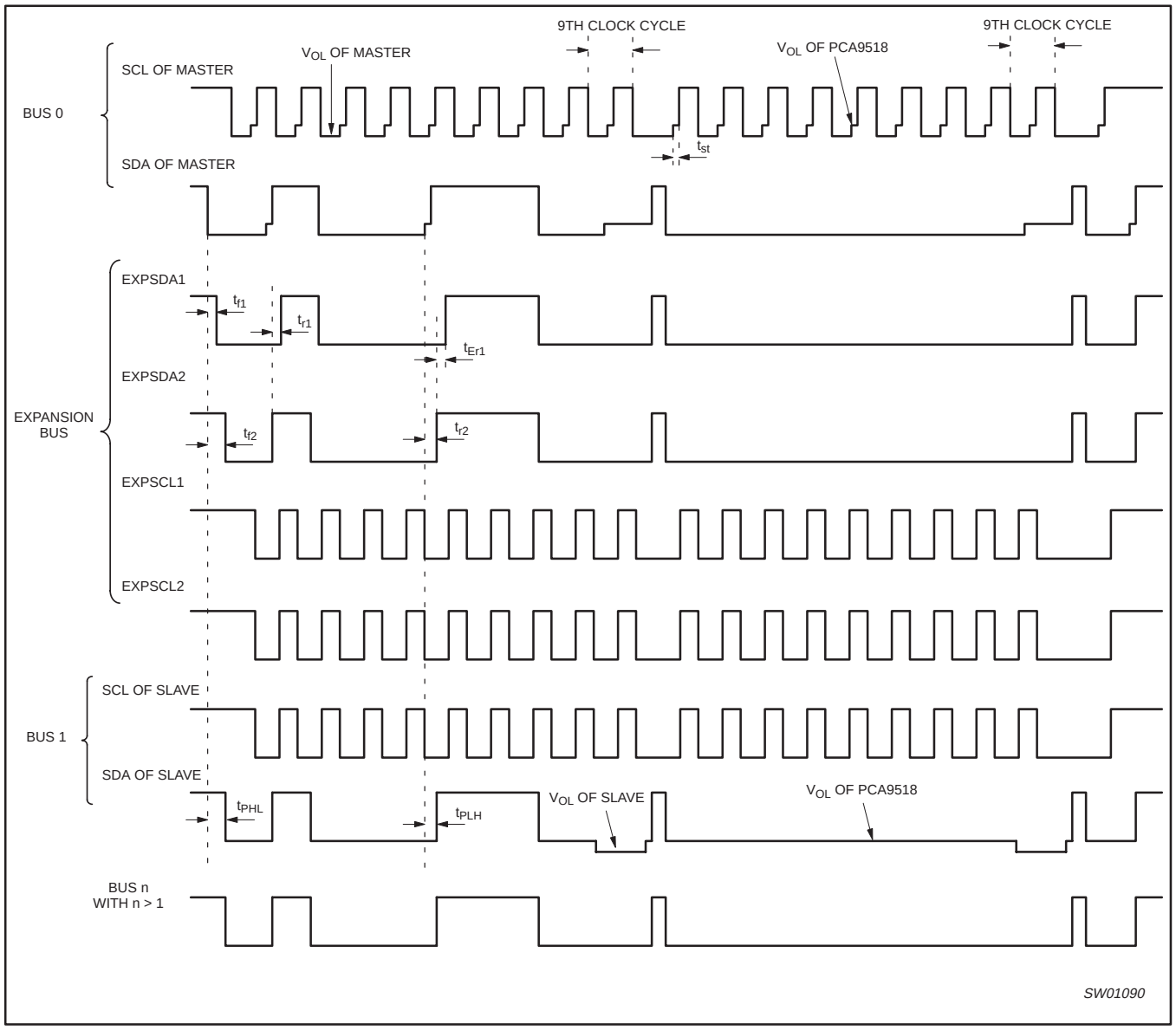


Figure 5. Bus waveforms

It is important to note that any arbitration or clock stretching events on Bus 1 require that the V_{OL} of the devices on Bus 1 be 70 mV below the V_{OL} of the PCA9518 (see $V_{OL} – V_{ilc}$ in the DC Characteristics section) to be recognized by the PCA9518 and then transmitted to Bus 0.

ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Voltages with respect to pin GND.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
V_{CC} to GND	Supply voltage range V_{CC}	–0.5	+7	V
V_{bus}	Voltage range I^2C-bus, SCL or SDA	–0.5	+7	V
I	DC current (any pin)	—	50	mA
P_{tot}	Power dissipation	—	300	mW
T_{stg}	Storage temperature range	–55	+125	°C
T_{amb}	Operating ambient temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.0 to 3.6 V; GND = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Supplies						
V_{CC}	DC supply voltage		3.0	3.3	3.6	V
I_{CCH}	Quiescent supply current, both channels HIGH	V_{CC} = 3.6 V; SDAn = SCLn = V_{CC}	—	7.5	10	mA
I_{CCL}	Quiescent supply current, both channels LOW	V_{CC} = 3.6 V; one SDA and one SCL = GND, other SDA and SCL open	—	9	11	mA
I_{CCLc}	Quiescent supply current in contention	V_{CC} = 3.6 V; SDAn = SCLn = GND	—	9	11	mA
Input SCL; input/output SDA						
V_{IH}	High-level input voltage, SCL, SDA		0.7 V_{CC}	—	5.5	V
V_{IL}	Low-level input voltage, SCL, SDA (Note 1)		–0.5	—	0.3 V_{CC}	V
V_{ILc}	Low-level input voltage contention, SCL, SDA (Note 1)		–0.5	—	0.4	V
V_{IK}	Input clamp voltage	I_I = –18 mA	—	—	–1.2	V
I_I	Input leakage current	V_I = 3.6 V	—	—	±1	μA
I_{IL}	Input current LOW, SDA, SCL	V_I = 0.2 V, SDA, SCL	—	—	5	μA
V_{OL}	Low level output, SCL, SDA	I_{OL} = 0[2] or 6 mA	0.47	0.52	0.6	V
V_{OL}–V_{ILc}	Low level input voltage below output low level voltage	Guaranteed by design	—	—	70	mV
C_I	Input capacitance	V_I = 3 V or 0 V	—	6	8	pF
Enable 1–4						
V_{IL}	LOW level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH level input voltage		2.0	—	5.5	V
I_{IL}	Input current LOW	V_I = 0.2 V, EN1–EN4	—	10	30	μA
I_{LI}	Input leakage current		–1	—	1	μA
C_I	Input capacitance	V_I = 3.0 V or 0 V	—	3	7	pF
Expansion Pins						
V_{IH}	HIGH level input voltage, EXP*		0.55 V_{CC}	—	5.5	V
V_{IL}	LOW level input voltage, EXP*		–0.5	—	0.45 V_{CC}	V
I_{IL}	Input current LOW, EXP*	V_I = 0.2 V, EXP*	—	—	5	μA
V_{OL}	Low level output, EXP*	I_{OL} = 12 mA	—	—	0.5	V
C_I	Input capacitance	V_I = 3.0 V or 0 V	—	6	8	pF

NOTE:
1. V_{IL} specification is for the enable input and the first low level seen by the SDAx/SCLx lines. V_{ILc} is for the second and subsequent low levels seen by the SDAx/SCLx lines
2. Test performed with I_{OL} = 10 μA

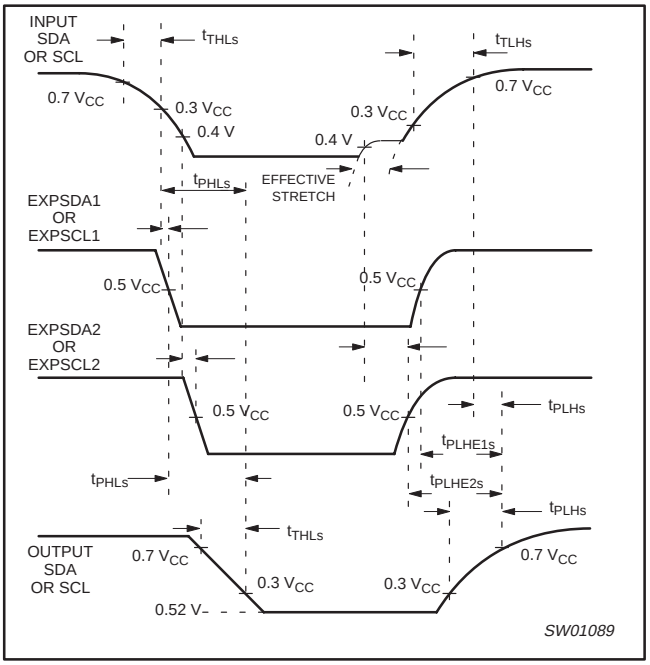
AC ELECTRICAL CHARACTERISTICS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS[3]			UNIT
			MIN	TYP	MAX	
t_{PHLs}	Propagation delay SDA to SDAn or SCL to SCLn	Waveform 1; Note 2	105	202	389	ns
t_{PLHs}	Propagation delay SDA to SDAn or SCL to SCLn	Waveform 1; Note 3	110	259	265	ns
t_{PHLE1s}	Propagation delay EXPSDA1 to SDA or EXPSCL1 to SCL	Waveform 1	109	193	327	ns
t_{PLHE1s}	Propagation delay EXPSDA1 to SDA or EXPSCL1 to SCL	Waveform 1	130	153	179	ns
t_{PLHE2s}	Propagation delay EXPSDA2 to SDA or EXPSCL2 to SCL	Waveform 1	160	234	279	ns
t_{THLs}	Transition time, SDA/SCL	Waveform 1	58	110	187	ns
t_{TLHs}	Transition time, SDA/SCL	Waveform 1	—	0.85 RC	—	ns
t_{SET}	Enable to Start condition		300	—	—	ns
t_{HOLD}	Enable after Stop condition		300	—	—	ns

NOTES:

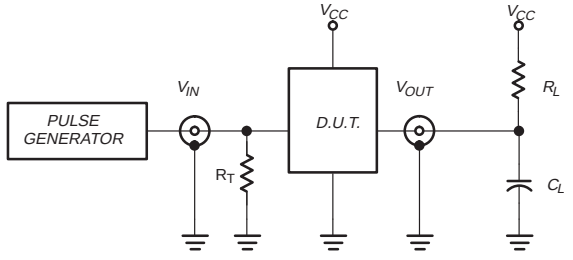
1. The SDA and SCL propagation delays are dominated by rise times or fall times. The fall times are mostly internally controlled and are only sensitive to load capacitance. The rise times are RC time constant controlled and therefor a specific nmerical value can only be given for fixed RC time constants.
2. The SDA high to low propagation delay, t_{PLHs}, includes the fall time from V_{CC} to 0.5 VCC of the EXPSDA1 or EXPSCL1 pins and the SDA or SCL fall time from the quisent high (usually V_{CC}) to below 0.3 V_{CC}. The SDA and SCL outputs have edge rate control circuits included which make the fall time almost independent of load capacitance.
3. The SDA or SCL low to high propagation delay includes the rise time constant from the quisent low to 0.5 V_{CC} for the EXPSDA1 or EXPSCL2, the rise time constant for the quisent low to 0.5 V_{CC} for the EXPSDA1 or EXPSCL1, and the rise time constant from the quisent external driven low to 0.7 V_{CC} for the SDA or SCL output. All of these rise times are RC time constants determined by the external R and total C for the various nodes.

AC WAVEFORMS



Waveform 1.

TEST CIRCUIT



Test Circuit for Open Drain Outputs

DEFINITIONS

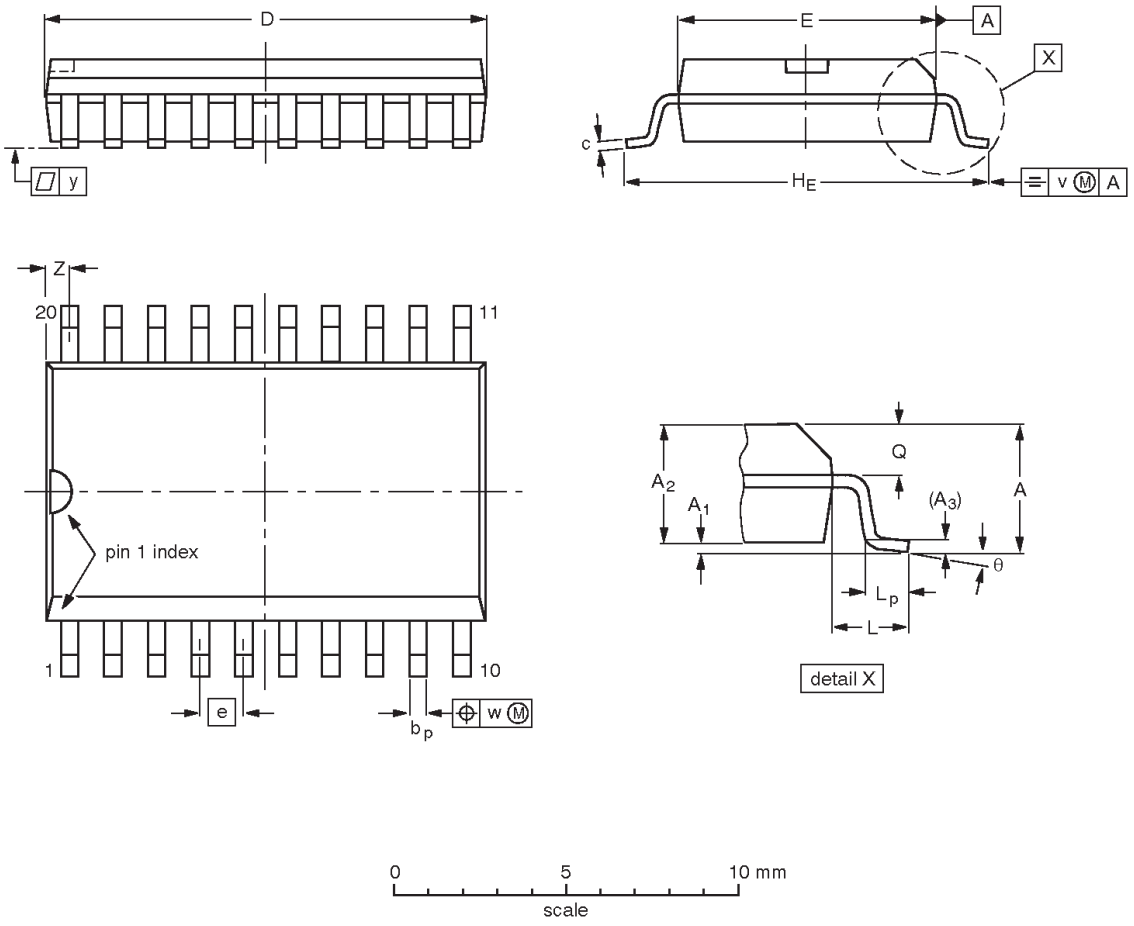
R_L = *Load resistor; 1.1 k for I²C and 500 Ω for EXP.*

C_L = *Load capacitance includes jig and probe capacitance; 100 pF for I²C and 100 pF for EXP*

R_T = *Termination resistance should be equal to Z_{OUT} of pulse generators.*

SW01088

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

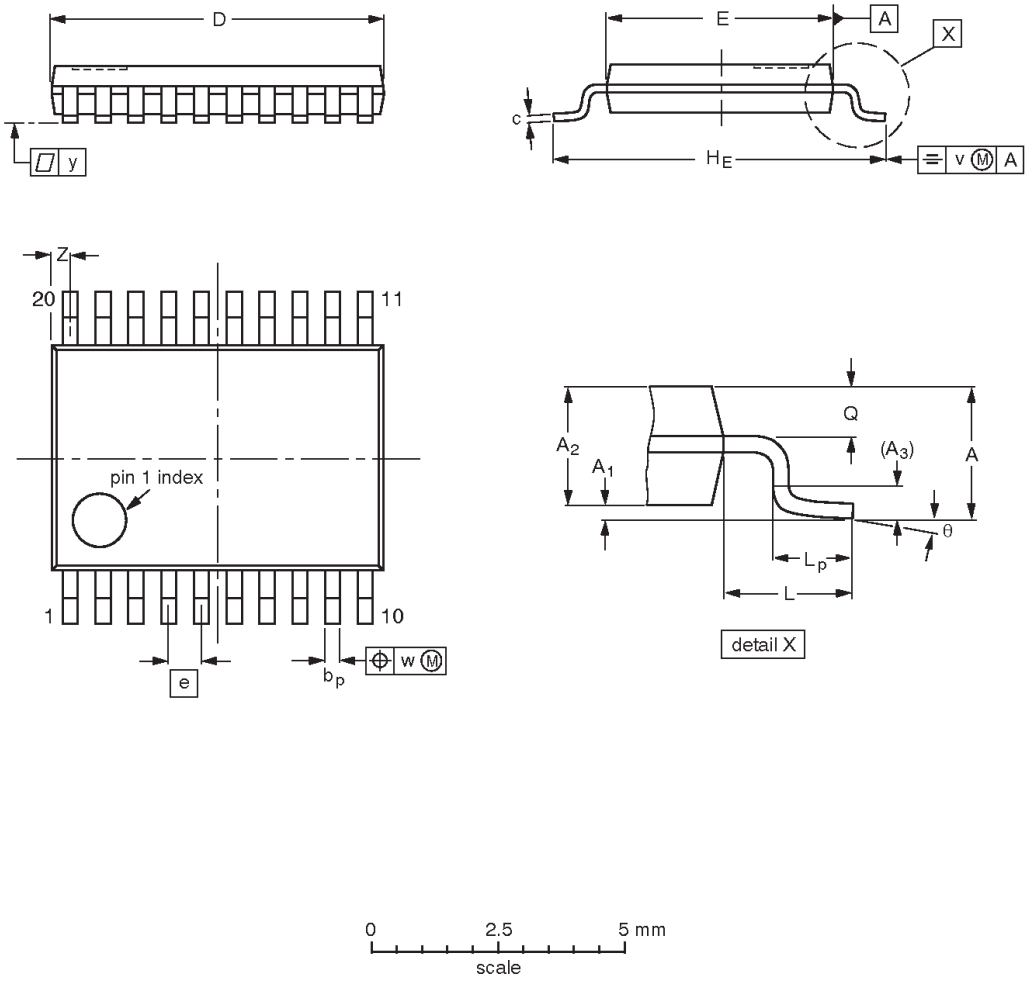
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				~~97-05-22~~ 99-12-27

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153				~~95-02-04~~ 99-12-27

Expandable 5-channel I²C hub PCA9518

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Data sheet status[1]	Product status[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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