10 Device Specifications

10.1 Absolute Maximum Ratings

Ambient temperature under bias (T_A) ..... 0 °C to + 70 °C
Storage temperature (T_{ST}) ..... – 65 °C to + 150 °C

Voltage on V_{CC} pins with respect to ground (V_{SS}) ..... – 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 V to V_{CC} + 0.5 V

Input current on any pin during overload condition ..... – 10 mA to + 10 mA
Absolute sum of all input currents during overload condition ..... | 100 mA |

Power dissipation ..... TBD

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

10.2 DC Characteristics

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB-C504
T_A = – 40 to 85 °C for the SAF-C504
T_A = – 40 to 110 °C for the SAH-C504
T_A = – 40 to 125 °C for the SAK-C504

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$, RESET, $\overline{CTRAP}$)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage (RESET, $\overline{CTRAP}$)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except XTAL1, RESET and $\overline{CTRAP}$)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL1	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage to RESET and $\overline{CTRAP}$	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage (ports 1, 2, 3, COUT3)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage (port 0, ALE, $\overline{PSEN}$)	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 80 µA, I_{OH} = – 10 µA
Output high voltage (ports 1,3 pins in push-pull mode and COUT3)	V_{OH1}	0.9 V_{CC}	–	V	I_{OH} = – 800 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{OH2}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 800 µA [2], I_{OH} = – 80 µA [2]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	– 10	– 50	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$)	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	–	10	pF	f_c = 1 MHz, T_A = 25 °C
Overload current	I_{OV}	–	± 5	mA	[7] [8]

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ. [9]	max.		
Power supply current:					
Active mode, 12 MHz [4]	I_{CC}	16	TBD	mA	V_{CC} = 5 V, [4]
Idle mode, 12 MHz [5]	I_{CC}	8	TBD	mA	V_{CC} = 5 V, [5]
Active mode, 24 MHz [4]	I_{CC}	25	TBD	mA	V_{CC} = 5 V, [4]
Idle mode, 24 MHz [5]	I_{CC}	13	TBD	mA	V_{CC} = 5 V, [5]
Active mode, 40 MHz [4]	I_{CC}	38	TBD	mA	V_{CC} = 5 V, [4]
Idle mode, 40 MHz [5]	I_{CC}	17	TBD	mA	V_{CC} = 5 V, [5]
Power-down mode	I_{PD}	1	50	µA	V_{CC} = 2...5.5 V [3]

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (power-down mode) is measured under following conditions:
$\overline{EA}$ = Port0 = V_{CC} ; RESET = V_{SS} ; XTAL2 = N.C.; XTAL1 = V_{SS} ; V_{AGND} = V_{SS} ; all other pins are disconnected.

4) I_{CC} (active mode) is measured with:
XTAL1 driven with t_{CLCH} , t_{CHCL} = 5 ns , V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
$\overline{EA}$ = Port0 = Port1 = RESET = V_{CC} ; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{CLCH} , t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS} ; Port0 = V_{CC} ; all other pins are disconnected;

6) $I_{CC\,max}$ at other frequencies is given by:
active mode: TBD
idle mode: TBD
where f_{osc} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

7) Overload conditions occur if the standard operating conditions are exeeded, ie. the voltage on any pin exeeds the specified range (i.e. V_{OV} > V_{CC} + 0.5 V or V_{OV} < V_{SS} – 0.5 V). The supply voltage V_{CC} and V_{SS} must remain within the specified limits. The absolute sum of input currents on all port pins may not exceed 50 mA.

8) Not 100 % tested, guaranteed by design characterization

9) The typical I_{CC} values are periodically measured at T_A = +25 °C but not 100 % tested.

10.3 A/D Converter Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V
4V ≤ V_{AREF} ≤ V_{CC} + 0.1 V;
V_{SS} – 0.1 V ≤ V_{AGND} ≤ V_{SS} + 0.2 V;

T_A = 0 to 70 °C for the SAB-C504
T_A = – 40 to 85 °C for the SAF-C504
T_A = – 40 to 110 °C for the SAH-C504
T_A = – 40 to 125 °C for the SAK-C504

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	1)
Sample time	t_S	–	64 x t_{IN} 32 x t_{IN} 16 x t_{IN} 8 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 2)
Conversion cycle time	t_{ADCC}	–	384 x t_{IN} 192 x t_{IN} 96 x t_{IN} 48 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 3)
Total unadjusted error	T_{UE}	–	± 2	LSB	V_{SS} + 0.5V ≤ V_{IN} ≤ V_{CC} – 0.5V 4)
		–	± 4	LSB	V_{SS} < V_{IN} < V_{SS} + 0.5V V_{CC} – 0.5V < V_{IN} < V_{CC} 4)
Internal resistance of reference voltage source	R_{AREF}	–	t_{ADC} / 250 – 0.25	kΩ	t_{ADC} in [ns] 5) 6)
Internal resistance of analog source	R_{ASRC}	–	t_S / 500 – 0.25	kΩ	t_S in [ns] 2) 6)
ADC input capacitance	C_{AIN}	–	50	pF	6)

Notes see next page.

Clock calculation table :

Clock Prescaler Ratio	ADCL1, 0		t_{ADC}	t_S	t_{ADCC}
÷ 32	1	1	32 x t_{IN}	64 x t_{IN}	384 x t_{IN}
÷ 16	1	0	16 x t_{IN}	32 x t_{IN}	192 x t_{IN}
÷ 8	0	1	8 x t_{IN}	16 x t_{IN}	96 x t_{IN}
÷ 4	0	0	4 x t_{IN}	8 x t_{IN}	48 x t_{IN}

Further timing conditions : t_{ADC} min = 500 ns
t_{IN} = 2 / f_{OSC} = 2 t_{CLCL}

Notes:

1) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) During the sample time the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time for the calibration. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{CC} = 4.9 V. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100 % tested, but guaranteed by design characterization.

10.4 AC Characteristics for C504-L / C504-2R

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB-C504
T_A = – 40 to 85 °C for the SAF-C504
T_A = – 40 to 110 °C for the SAH-C504
T_A = – 40 to 125 °C for the SAK-C504

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	127	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	43	–	$t_{CLCL} - 40$	–	ns
Address hold after ALE	t_{LLAX}	30	–	$t_{CLCL} - 23$	–	ns
ALE low to valid instr in	t_{LLIV}	–	233	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	58	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	215	–	$3t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	150	–	$3t_{CLCL} - 100$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} *)	–	63	–	$t_{CLCL} - 20$	ns
Address valid after $\overline{PSEN}$	t_{PXAV} *)	75	–	$t_{CLCL} - 8$	–	ns
Address to valid instr in	t_{AVIV}	–	302	–	$5t_{CLCL} - 115$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the C504 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for C504-L / C504-2R (cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	114	–	$2t_{CLCL} - 53$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5t_{CLCL} - 165$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	294	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

10.5 AC Characteristics for C504-L24 / C504-2R24

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V T_A = 0 to 70 °C for the SAB-C504
T_A = – 40 to 85 °C for the SAF-C504

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		24-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 24 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	43	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	17	–	$t_{CLCL} - 25$	–	ns
Address hold after ALE	t_{LLAX}	17	–	$t_{CLCL} - 25$	–	ns
ALE low to valid instr in	t_{LLIV}	–	80	–	$4t_{CLCL} - 87$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	22	–	$t_{CLCL} - 20$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	95	–	$3t_{CLCL} - 30$	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	60	–	$3t_{CLCL} - 65$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} *)	–	32	–	$t_{CLCL} - 10$	ns
Address valid after $\overline{PSEN}$	t_{PXAV} *)	37	–	$t_{CLCL} - 5$	–	ns
Address to valid instr in	t_{AVIV}	–	148	–	$5t_{CLCL} - 60$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the C504 to devices with float times up to 37 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for C504-L24 / C504-2R24 (cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		24-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 24 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	180	–	$6t_{CLCL} - 70$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	180	–	$6t_{CLCL} - 70$	–	ns
Address hold after ALE	t_{LLAX2}	56	–	$2t_{CLCL} - 27$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	118	–	$5t_{CLCL} - 90$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0		0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	63	–	$2t_{CLCL} - 20$	ns
ALE to valid data in	t_{LLDV}	–	200	–	$8t_{CLCL} - 133$	ns
Address to valid data in	t_{AVDV}	–	220	–	$9t_{CLCL} - 155$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	75	175	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$	t_{AVWL}	67	–	$4t_{CLCL} - 97$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	17	67	$t_{CLCL} - 25$	$t_{CLCL} + 25$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	$t_{CLCL} - 37$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	170	–	$7t_{CLCL} - 122$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	15	–	$t_{CLCL} - 27$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 24 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	41.7	294	ns
High time	t_{CHCX}	12	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	12	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	12	ns
Fall time	t_{CHCL}	–	12	ns

10.6 AC Characteristics for C504-L40 / C504-2R40

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V T_A = 0 to 70 °C for the SAB-C504
T_A = – 40 to 85 °C for the SAF-C504

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	35	–	$2t_{CLCL} - 15$	–	ns
Address setup to ALE	t_{AVLL}	10	–	$t_{CLCL} - 15$	–	ns
Address hold after ALE	t_{LLAX}	10	–	$t_{CLCL} - 15$	–	ns
ALE low to valid instr in	t_{LLIV}	–	55	–	$4t_{CLCL} - 45$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	10	–	$t_{CLCL} - 15$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	60	–	$3t_{CLCL} - 15$	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	25	–	$3t_{CLCL} - 50$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} *)	–	20	–	$t_{CLCL} - 5$	ns
Address valid after $\overline{PSEN}$	t_{PXAV} *)	20	–	$t_{CLCL} - 5$	–	ns
Address to valid instr in	t_{AVIV}	–	65	–	$5t_{CLCL} - 60$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	– 5	–	– 5	–	ns

*) Interfacing the C504 to devices with float times up to 25 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

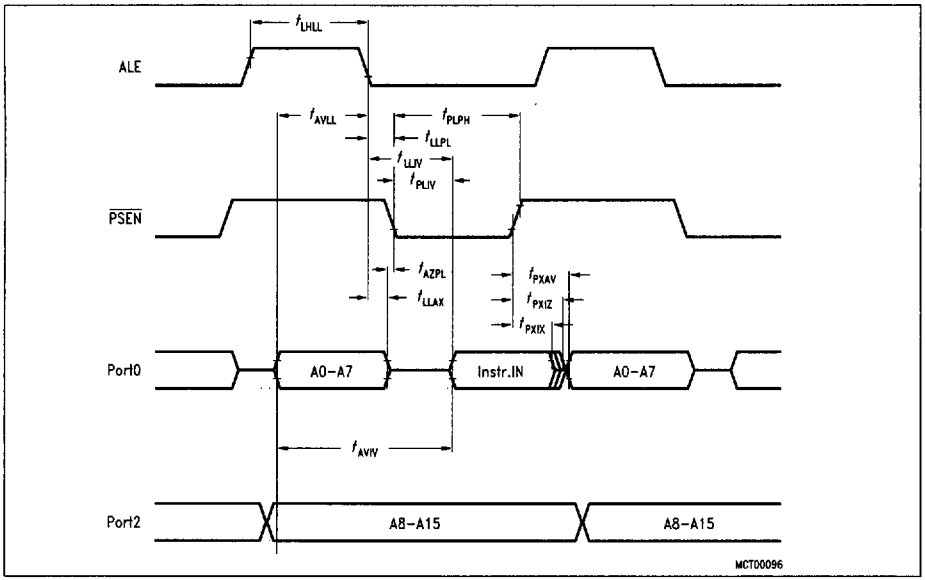
AC Characteristics for C504-L40 / C504-2R40 (cont'd)

External Data Memory Characteristics

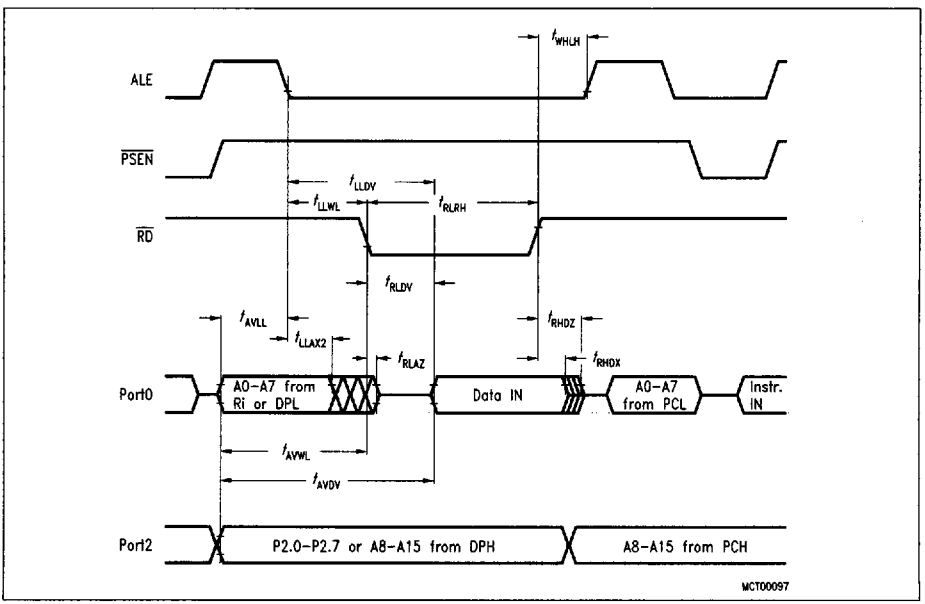
Parameter	Symbol	Limit Values				Unit
		40-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	120	–	$6t_{CLCL} - 30$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	120	–	$6t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX2}	35	–	$2t_{CLCL} - 15$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	75	–	$5t_{CLCL} - 50$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0		0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	38	–	$2t_{CLCL} - 12$	ns
ALE to valid data in	t_{LLDV}	–	150	–	$8t_{CLCL} - 50$	ns
Address to valid data in	t_{AVDV}	–	150	–	$9t_{CLCL} - 75$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	60	90	$3t_{CLCL} - 15$	$3t_{CLCL} + 15$	ns
Address valid to $\overline{WR}$	t_{AVWL}	70	–	$4t_{CLCL} - 30$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	$t_{CLCL} - 15$	$t_{CLCL} + 15$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	$t_{CLCL} - 20$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	125	–	$7t_{CLCL} - 50$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	–	$t_{CLCL} - 20$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

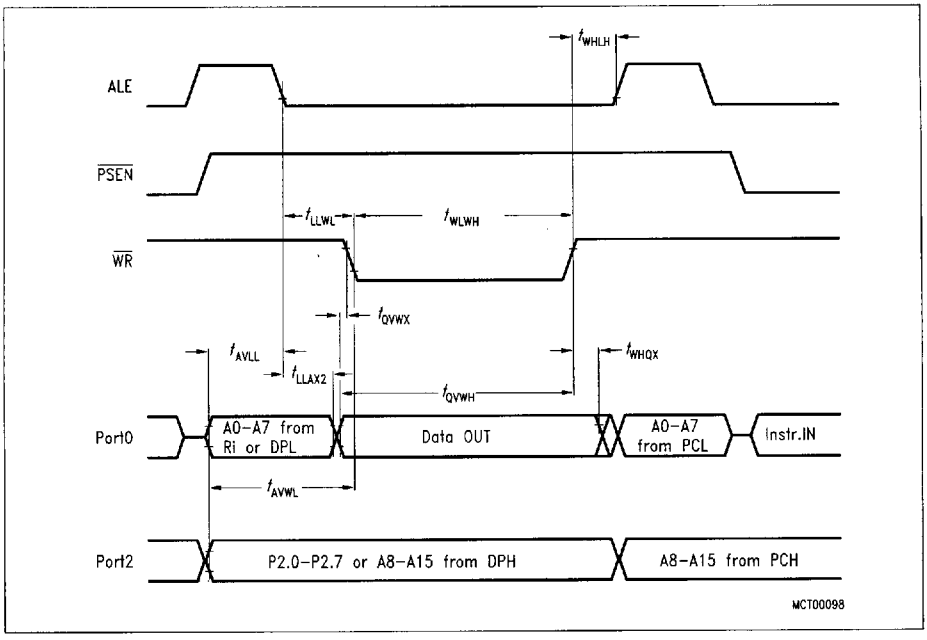
Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 40 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	25	294	ns
High time	t_{CHCX}	10	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	10	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	10	ns
Fall time	t_{CHCL}	–	10	ns



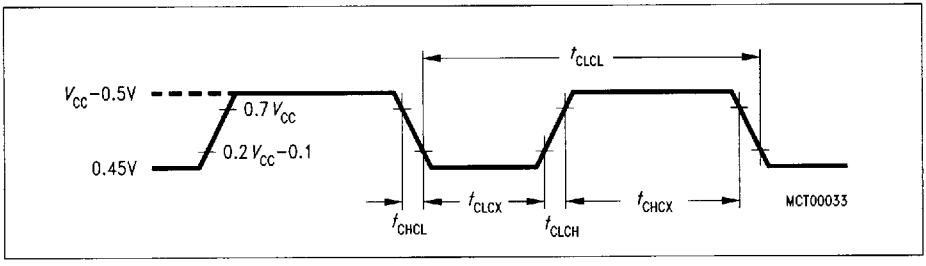
Program Memory Read Cycle



Data Memory Read Cycle



Data Memory Write Cycle

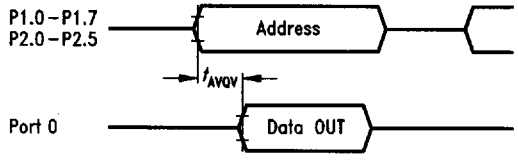


External Clock Cycle

10.7 ROM Verification Characteristics for C504-2R

ROM Verification Mode 1

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	10 t_{CLCL}	ns



Address: P1.0 – P1.7 = A0 – A7
P2.0 – P2.5 = A8 – A13
Data: P0.0 – P0.7 = D0 – D7

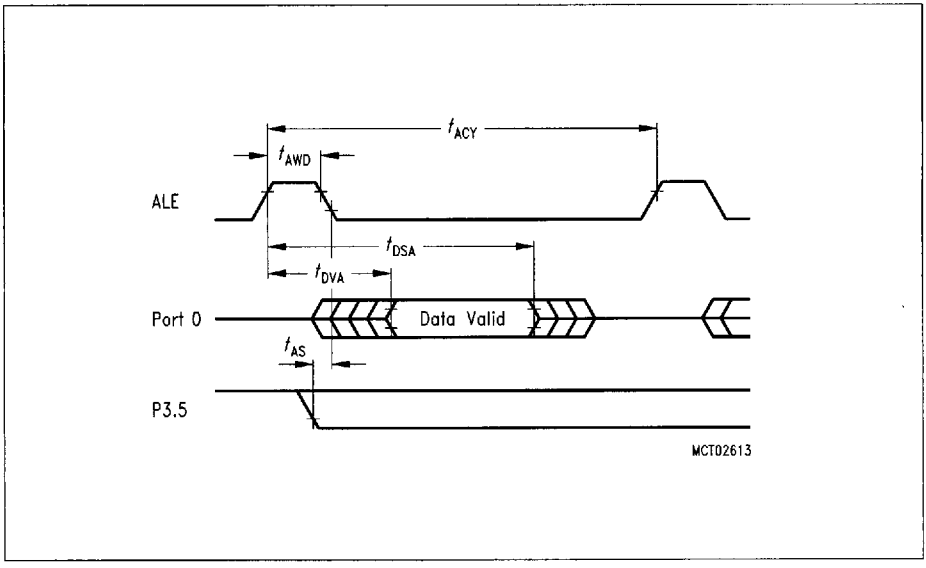
Inputs: P2.6, P2.7, $\overline{PSEN}$ = V_{SS}
ALE, $\overline{EA}$ = V_{IH}
RESET = V_{IH1}

MCT02629

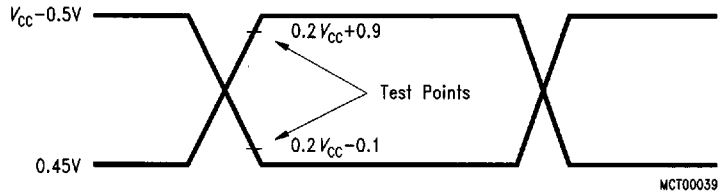
ROM Verification Mode 1

ROM Verification Mode 2

Parameter	Symbol	Limit Values			Unit
		min.	typ	max.	
ALE pulse width	t_{AWD}	–	2 t_{CLCL}	–	ns
ALE period	t_{ACY}	–	12 t_{CLCL}	–	ns
Data valid after ALE	t_{DVA}	–	–	4 t_{CLCL}	ns
Data stable after ALE	t_{DSA}	8 t_{CLCL}	–	–	ns
P3.5 setup to ALE low	t_{AS}	–	t_{CLCL}	–	ns
Oscillator frequency	$1/t_{CLCL}$	4	–	6	MHz

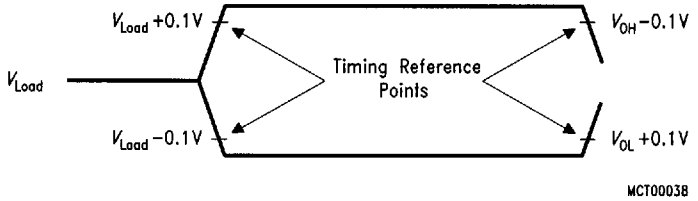


ROM Verification Mode 2



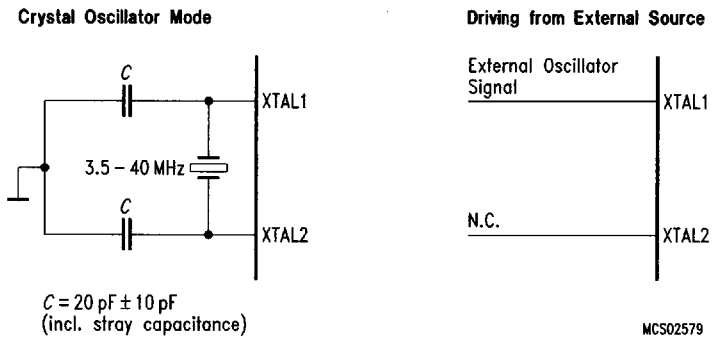
AC Inputs during testing are driven at $V_{CC} - 0.5$ V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA

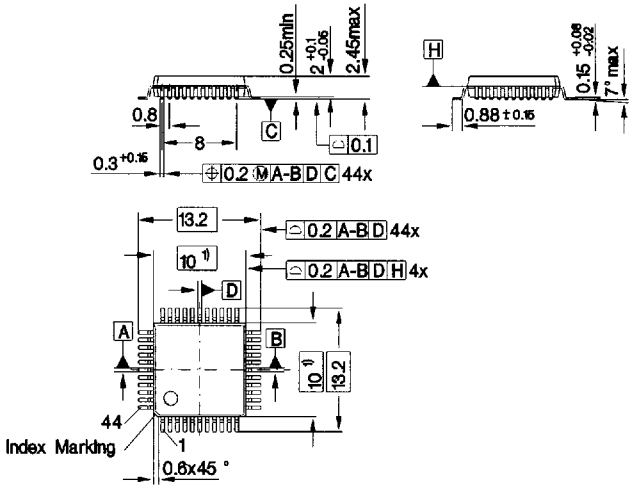
AC Testing : Float Waveforms



Recommended Oscillator Circuits for Crystal Oscillator

10.8 Package Information

P-MQFP-44 (SMD)
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPM05622

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".
SMD = Surface Mounted Device

Dimensions in mm