

T-35-25

# TOPAZ

SEMICONDUCTOR

## SD204, SD205

### N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

#### ORDERING INFORMATION

Sorted Chips in Waffle Pack	SD204CHP	SD205CHP
TO-205AF (TO-39) Package	SD204HD	SD205HD
Description	6.0 ohm, 25V	6.0 ohm, 25V

#### FEATURES

- Low Capacitance— $c_{iss}$  11pF typ.
- Inherently Temperature Stable by Design
- TTL Logic Compatible Input— $V_{GS(th)}$  2.0V (max)

#### APPLICATIONS

- Broadband RF Power Amplifiers
- High Speed Switches and Drivers
- Pulse Amplifiers and Logic Buffers
- CMOS and TTL to High Current Interface

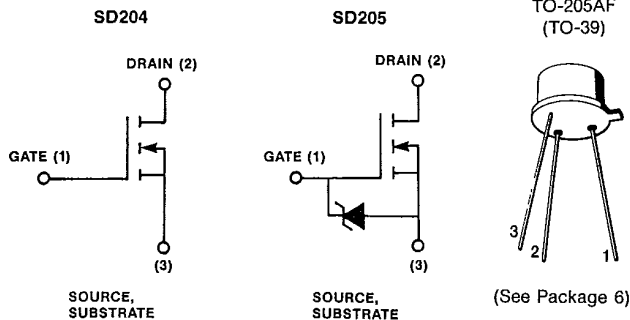
#### ABSOLUTE MAXIMUM RATINGS ( $T_A = +25^\circ\text{C}$ unless otherwise specified)

$V_{DS}$ Drain-Source Voltage	+25V
$V_{DG}$ Drain-Gate Voltage	+25V
$V_{GS}$ Gate-Source (Forward) Voltage	+20V
Gate-Source (Reverse) Voltage	-0.3V
$I_D$ Continuous Drain Current (Note 1)	0.3A
Continuous Drain Current (Note 2)	0.7A
Peak Pulsed Drain Current	1.0A
$P_D$ Continuous Power Dissipation	
$T_A = +25^\circ\text{C}$ (Note 1, Note 3)	1.0W
$T_C = +25^\circ\text{C}$ (Note 1, Note 4)	6.25W
Power Derating Factors (Note 1)	
Free Air	10mW/ $^\circ\text{C}$
Infinite Heat Sink	62.5mW/ $^\circ\text{C}$

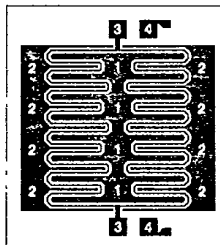
Thermal Resistance (Note 1)	
$\theta_{ja}$ Junction to Ambient	100 $^\circ\text{C}/\text{W}$
$\theta_{jc}$ Junction to Case	16 $^\circ\text{C}/\text{W}$
$T_{op}$ Operating Junction Temperature Range	-55 to +125 $^\circ\text{C}$
$T_{stg}$ Storage Temperature Range	-55 to +150 $^\circ\text{C}$

- Note 1: Not applicable to chips. Final value depends on mounting.  
 Note 2: Pulse Test 80 $\mu\text{Sec}$ , 1% Duty Cycle  
 Note 3: Free Air  
 Note 4: Infinite Heat Sink

#### SCHEMATIC DIAGRAM



#### CHIP CONFIGURATION



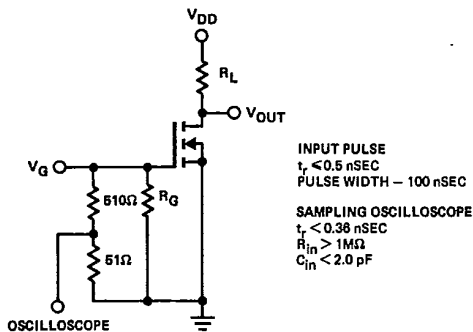
1—Drain 2—Source 3—Gate 4—Diode  
 Minimum bonding required. One Drain, One Source (left), One Source (right), One Gate. Bond Gate and Adjacent Diode to Common Point to Connect Protective Diode.

Size: .040 x .044 x .013 Inch.  
 Body (Substrate) is backside contact.

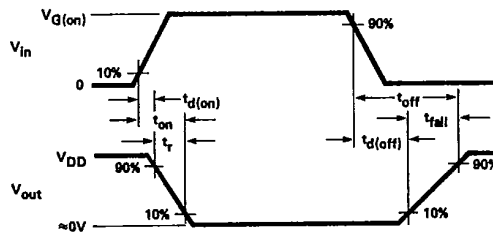
**ELECTRICAL CHARACTERISTICS** (T<sub>A</sub> = +25°C unless otherwise noted)

#	CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	BV <sub>DSS</sub>	Drain Source Breakdown Voltage	25			V	I <sub>D</sub> = 1.0μA, V <sub>GS</sub> = 0
2	V <sub>GS(th)</sub>	Gate Source Threshold Voltage	0.5		2.0	V	I <sub>D</sub> = 1mA, V <sub>DS</sub> = V <sub>GS</sub>
3	I <sub>D(on)</sub>	Drain-Source ON Current	1.0			nA	V <sub>DS</sub> = 10V (Note 1) V <sub>GS</sub> = 10V
4	I <sub>DSS</sub>	Drain-Source OFF Leakage Current			1.0		V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0
5	r <sub>DS(on)</sub>	Drain-Source ON Resistance			8.0	ohms	V <sub>GS</sub> = 5V I <sub>D</sub> = 50mA (Note 1)
6					6.0		V <sub>GS</sub> = 10V I <sub>D</sub> = 500mA (Note 1)
7					6.0		
8	I <sub>GSS</sub>	Gate Body Leakage Current	SD205		1.0	μA	V <sub>GS</sub> = 20V, V <sub>DS</sub> = 0
8A			SD204		±10	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0
9	g <sub>fs</sub>	Common-Source Forward Transconductance	100			mmhos	V <sub>DS</sub> = 15V, I <sub>D</sub> = 200mA f = 1KHz (Note 1)
10	C <sub>iss</sub>	Common-Source Input Capacitance		11	13	pF	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0 f = 1MHz
11	C <sub>oss</sub>	Common-Source Output Capacitance			8.0		
12	C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance			3.0		
13	t <sub>d(on)</sub>	Turn-On Delay Time		<1.0	2.0		
14	t <sub>r</sub>	Rise Time		1.0	3.0	nS	V <sub>DD</sub> = 10V, V <sub>G(on)</sub> = 10V R <sub>L</sub> = 133Ω, R <sub>G</sub> = 51Ω
15	t <sub>off</sub>	Turn-off Time		3.0	5.0		
16	NF	Common-Source Noise Figure			4.5		
17	G <sub>PS</sub>	Common-Source Power Gain	9.0				V <sub>DS</sub> = 10V, I <sub>D</sub> = 100mA f = 300MHz

**SWITCHING TIMES TEST CIRCUIT**



**TEST WAVEFORMS**

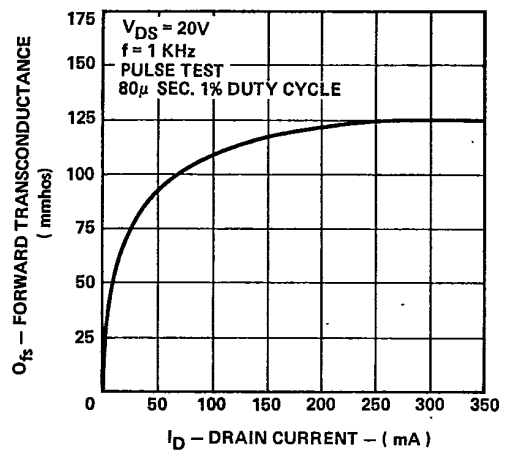


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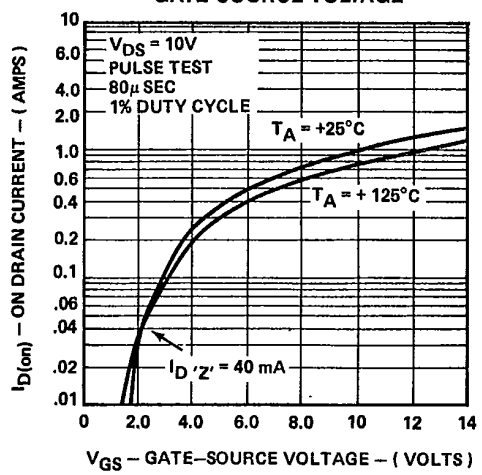


**TYPICAL PERFORMANCE CHARACTERISTICS** ( $T_A = +25^\circ\text{C}$  unless otherwise specified)

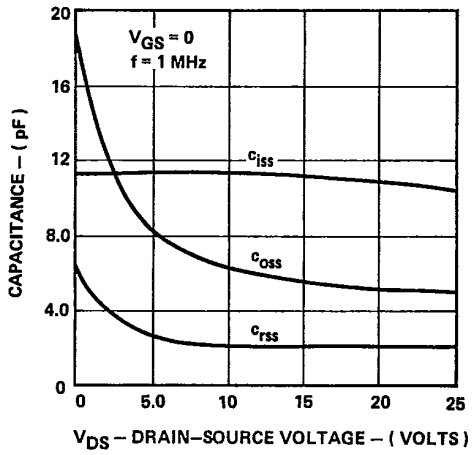
**FORWARD TRANSCONDUCTANCE**  
—VS—  
**ON DRAIN CURRENT**



**ON DRAIN CURRENT**  
—VS—  
**GATE-SOURCE VOLTAGE**



**CAPACITANCES**  
—VS—  
**DRAIN-SOURCE VOLTAGE**



**DRAIN-SOURCE ON RESISTANCE**  
—VS—  
**GATE-SOURCE VOLTAGE**

