1. General Description

The EM78M611 is a series of Universal Serial Bus 8-bit RISC Multi-Time Programming (MTP) microcontrollers. It is specifically designed for USB low speed device application and to support legacy device such as PS/2 keyboard. The EM78M611 also support one device address and three endpoints. With no firmware involved, these series of microcontrollers can automatically identify and decode Standard USB Command to EndPoint Zero.

The EM78M611 is implemented on a RISC architecture. It has eight-level stack and eight interrupt sources. Each device has 144 bytes of general purpose SRAM and 6K bytes of program ROM, and is embedded with 4 bytes of E^2PROM. The EM78M611 has up to 11 pins with the capacity of sinking large current.

These series of chips have many powerful features, including **:**

- Dual Clock mode which allows the device to run on very low power saving frequency
- Pattern Detect Application function which is used in a serial transmission to count waveform width
- Width Modulation that can generate a duty-cycle-programmable signal
- 24-channel AD converter with up to 10 bits resolution.

2. Features

- Operating voltage 4.4V ~ 5.25V
- Low-cost solution for low-speed USB devices, such as keyboard, joystick, and Gamepad.
- USB Specification Compliance
  - Universal Serial Bus Specification Version 1.1
  - USB Device Class Definition for Human Interface Device (HID), Firmware Specification Version 1.1
  - Support 1 device address and 3 endpoints
- USB Application
  - P75(D-) has an internal pull-high resistor (1.5K Ohm)
  - USB protocol handling
  - USB device state handling
  - Identifying and decoding of Standard USB commands to EndPoint Zero

- PS/2 Application Support
  - Auto-detects PS/2 or USB port
  - Build-in PS/2 port interface for keyboard and mouse
- Built-in 8-bit RISC MCU
  - 8 level stacks for subroutine and interruption
  - Eight available interruptions
  - 8-bit real time clock/counter (TCC) with overflow interruption
  - Built-in RC oscillator free running for WatchDog Timer and Dual clock mode
  - Two independent programmable prescalers for WDT and TCC
  - Two methods of saving power**:**
    1. Power-down mode (SLEEP mode)
    2. Dual clock mode.
  - Two clocks per instruction cycle
  - Multi-time programmable
- I/O Ports
  - Up to 11 LED sink pins
  - Each GPIO pin of Ports 5, 6, 8, P90~P93, P95, and P96; has an internal programmable pull-high resistor (25K Ohm)
  - Each GPIO pin of Port 6, P74~P77, and Port 9 can wakeup the MCU from sleep mode by input state change
- Internal Memory
  - Built-in 6K*13 bits Program ROM
  - Built-in 144 bytes general purpose registers (SRAM)
  - Built-in USB Application FIFOs.
  - Built-in 4 bytes E2PROM
- Operation Frequency
  - Normal Mode**:** MCU runs at the external oscillator frequency; 6MHz or 12MHz
  - Dual Clock Mode**:** MCU runs at the frequency of 256KHz (or 32KHz, 4KHz, 500Hz), emitted by the internal oscillator with the external ceramic resonator (or crystal) turned off to save power.
- Built-in Pattern Detect Application for serial signal transmission
- Built-in Pulse Width Modulation (PWM)
  - Up to 2 channels PWM function on P.92 (PWM1) and P.93 (PWM2).

- Up to 8-bit resolution PWM output
- Up to 8 selections of duty cycles

■ Built-in 24-Channel Analog-to-Digital Converter (ADC)
- Up to 24 channels
- Up to 10 bits resolution
- 4 ADC conversion rates**:** 256K/12K/64K/32K

■ Built-in 3.3V Voltage Regulator
- For MCU power supply
- Pull-up source for the external USB resistor on D-pin.

■ Package Type**:**
- 40 pin PDIP (EM78M611(A/B/C/D) AP)
- 44 pin QFP (EM78M611(A/B/C/D) AQ)
- 20 pin PDIP/SOP (EM78M611(A/B/C/D) BP/BM)
- 20 pin SSOP (EM78M611(A/B/C/D) DM)
- 24 pin PDIP/SOP (EM78M611(A/B/C/D) CP/CM)

3. Type Definition

The EM78M611 series has 4 types of packaging. Each type is divided into 4 modules, namely; original, with E^2PROM, with A/D converter, and with both E^2PROM and A/D converter. The Table 3.1 below summarizes which series of the EM78611 belong to which module.

Original	With E^2PROM	With A/D Converter	With Both
EM78M611A＊＊	EM78M611B＊＊	EM78M611C＊＊	EM78M611D＊＊

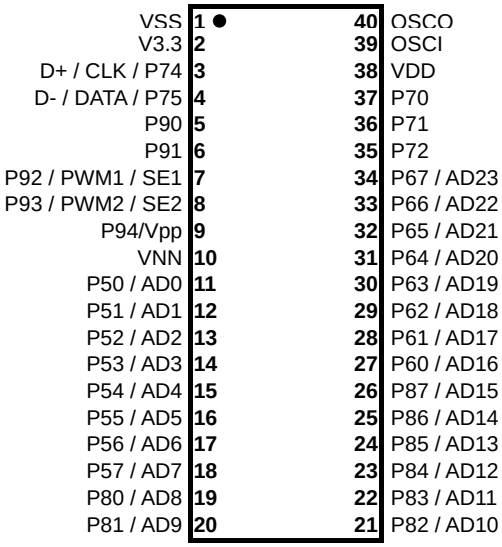
Table 3-1 Packaging Summary of EM78M611 Series IC

4. Applications

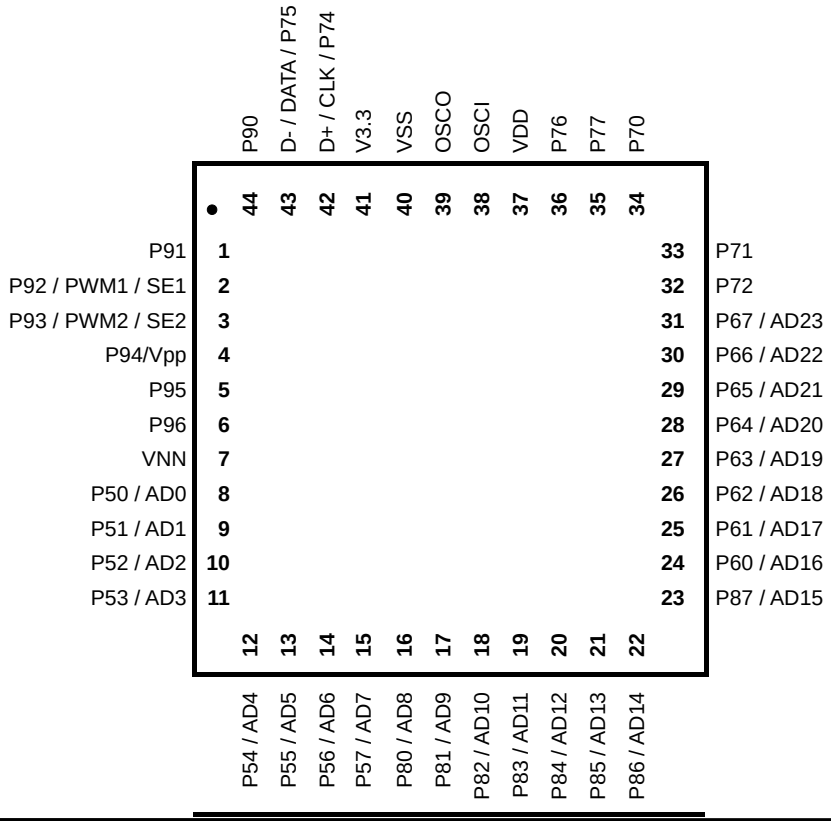
- USB Keyboard only.
- USB and PS/2 both compatible with Keyboard.
- USB Keyboard with USB Mouse.
- USB Joystick.

5. Pin Configuration

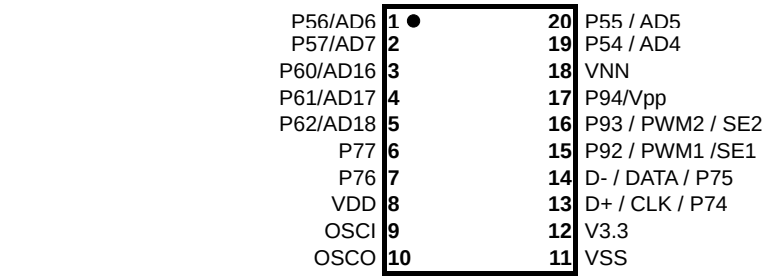
EM78M611AP (40-Pin DIP)



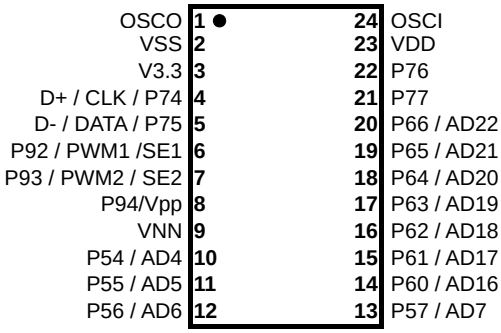
EM78M611AQ (44-Pin QFP)



EM78M611BP/BM/DM (20-Pin PDIP/SOP/SSOP)



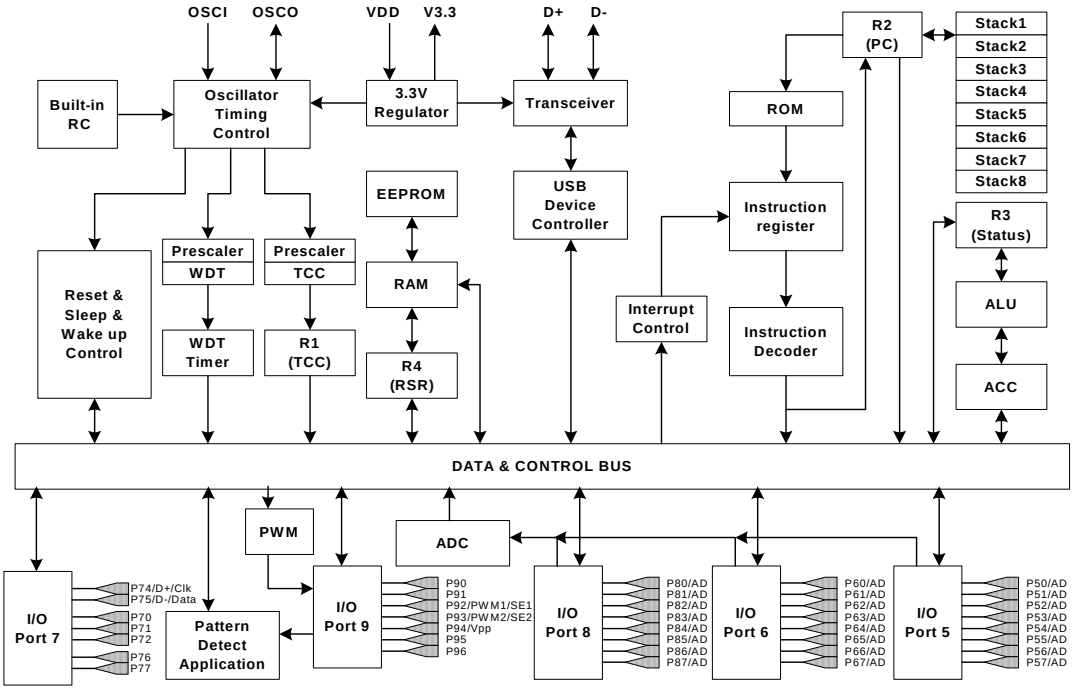
EM78M611CP/CM (24-Pin PDIP/SOP)



6. Pin Description

Pin Number	I/O	Function
P50 ~ P57 P60 ~ P67 P80 ~ P87	I/O	GPIO pins. These pins can be pulled-high internally through software control.
AD0 ~ AD23	I	Analog to Digital Converter input pins.
P90 ~ P93 P95 ~ P96	I/O	GPIO pins. These pins can be pulled-high internally through software control or LED sink pins.
PWM1 ~ PWM2	O	PWM output pins
SE1 ~ SE2	I	Serial Signal input pins.
P70 ~ P72, P76, P77	I/O	LED sink pins. P76, P77 will have an internal pulled-high resistor when the EM78M611 is running under PS/2 mode.
D+ / CLK / P74	I/O	USB plus data line interface or CLK for PS/2 keyboard. When the EM78M611 is running under PS/2 mode, this pin will have an internal pulled-high resistor (2.2K Ohm), with V_{DD}=5.0V.
D- / DATA / P75	I/O	USB minus data line interface or DATA for PS/2 keyboard. When the EM78M611 is running under PS/2 mode, this pin will have an internal pulled-high resistor (2.2K Ohm), with V_{DD}=5.0V. When the EM78M611 is running under USB mode, this pin will have an internal pulled-high resistor, 1.5k Ohm, with $V_{3.3}$=3.3V.
OSCI	I	6MHz / 12MHz ceramic resonator or crystal input.
OSCO	O	Return path for 6-MHz / 12MHz ceramic resonator or crystal.
VDD	PWR	Power supply pin.
GND	PWR	Ground pin.
V_{NN}	I	MTP program Pin
P94/V_{PP}	I	Input only I/O. MTP program pin.
$V_{3.3}$	PWR	3.3v regulator output.

7. Block Diagram



8. Function Description

The EM78M611memory is organized into four spaces, namely; User Program memory in 6K*13 bits ROM space, Data Memory in 144 bytes SRAM space, E^2PROM space, and USB Application FIFOs for EndPoint0, EndPoint1, and EndPoint2. Furthermore, several registers are used for special purposes.

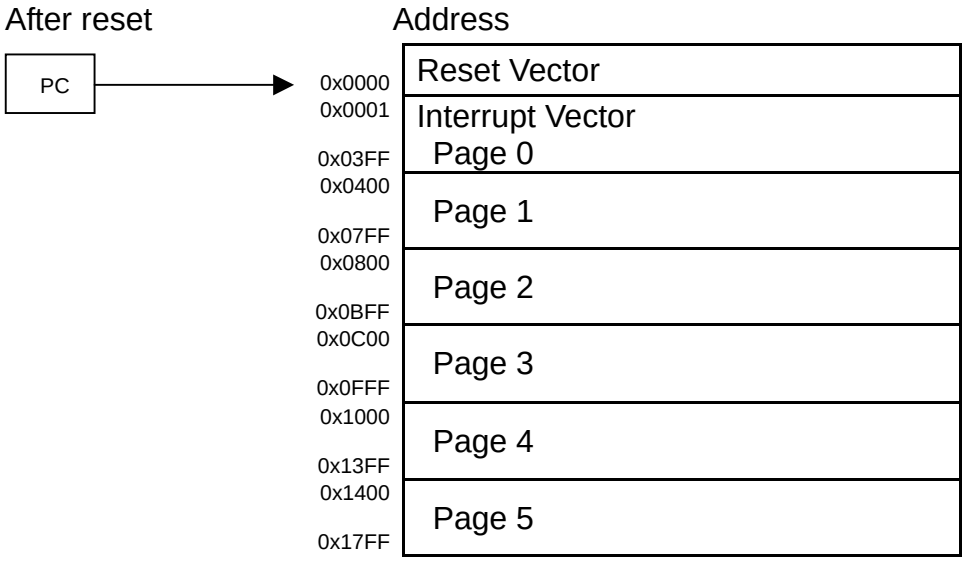
8.1 Program Memory

The program space of the EM78M611 is 6K bytes, and is divided into six pages. Each page is 1K bytes long. After Reset, the 13-bit Program Counter (PC) points to location zero of the program space.

The Interrupt Vector is at 0x0001 and accommodates TCC interrupt, RF1(SE1) timing counter interrupt, RF2(SE2) timing counter interrupt, P74~P77 State Changed interrupt, EndPoint 0 interrupt, USB Suspend interrupt, USB Reset interrupt, and USB Host Resume interrupt.

After an interrupt, the MCU will fetch the next instruction from the corresponding address as

illustrated in the following diagram.



8.2 Data Memory

The Data Memory has 144 bytes SRAM space. It is also equipped with USB Application FIFO space for USB Application. The Figure 8.1 (next page) shows the organization of the Data Memory Space.

8.2.1 Special Purpose Register

When the microcontroller executes instruction, specific registers are invoked for assistance, such as; Status Register which records the calculation status, Port I/O Control Registers which control the I/O pins' direction, etc. EM78M611 provides a lot of other special purpose registers for different functions.

Note that Special Control Registers can only be read or written by two instructions: IOR and IOW.

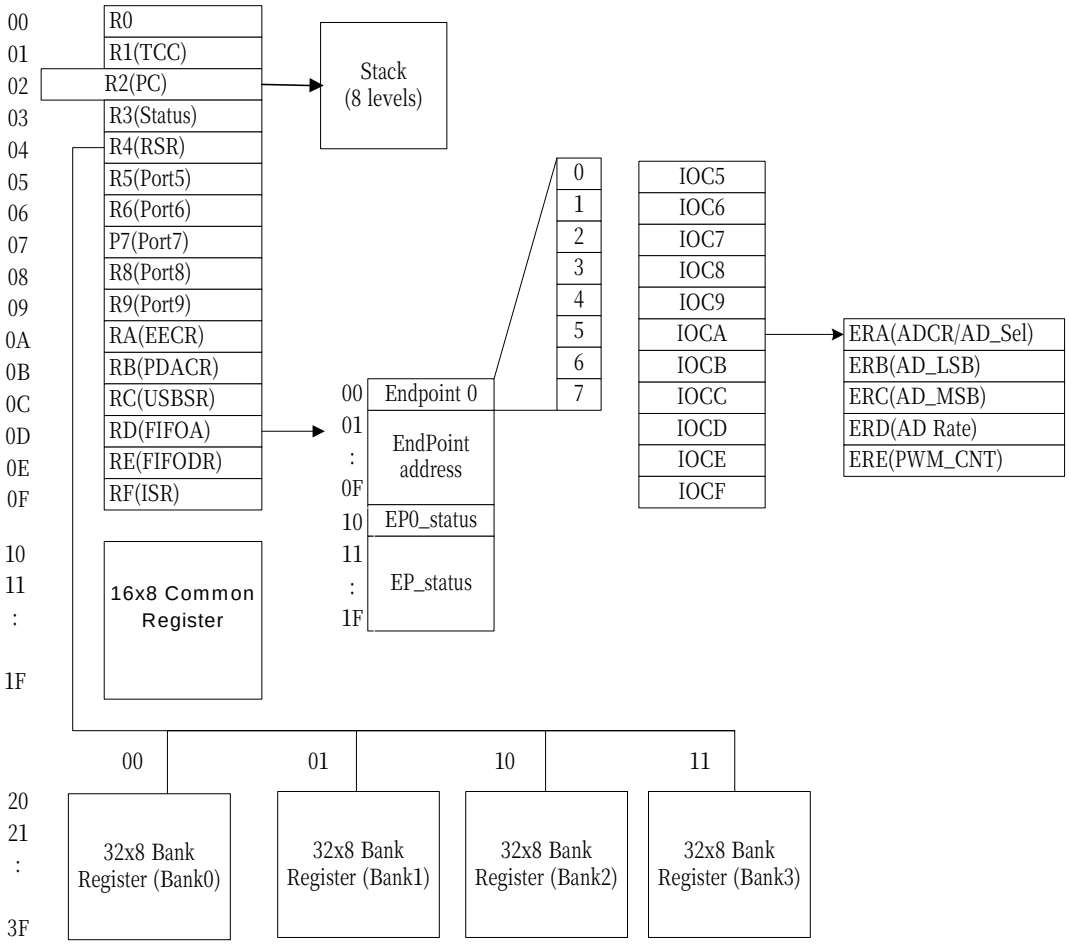


Fig 8.1 The Organization of EM78M611 Data RAM

8.2.1.1 Operation Registers

The following sections will introduce each of the Operation Registers of the Special Purpose Registers. The Operation Registers are arranged according to the order of registers' address. Note that some registers are read only, while others are both readable and writable.

R0 (Indirect Addressing Register) *Default Value: (0B_0000_0000)*

R0 is not a physically implemented register. Its major function is to be an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses the data pointed by the RAM Select Register (R4).

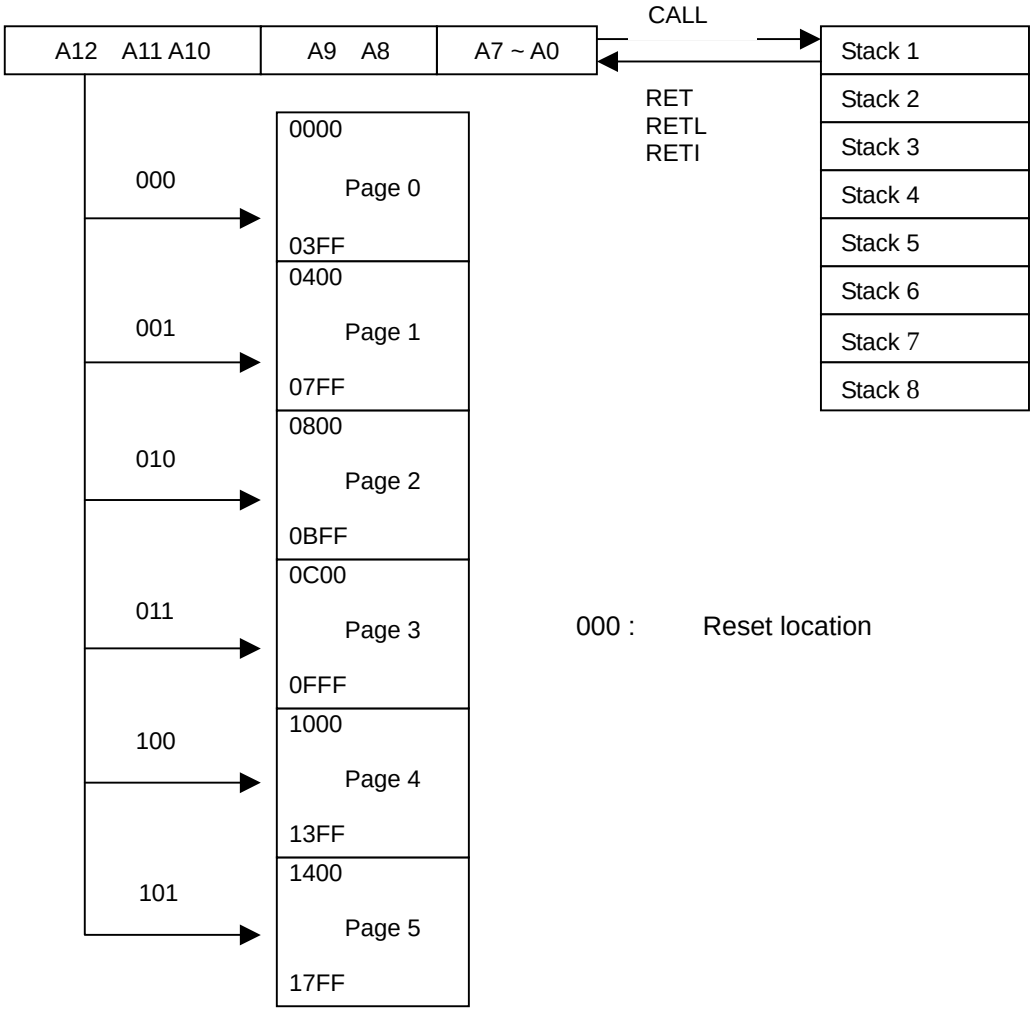
R1 (Time / Clock Counter) *Default Value: (0B_0000_0000)*

This register TCC, is an 8-bit timer or counter. It is readable and writable as any other register.

After Power-on reset and WatchDog reset, the initial value of this register is 0x00.

R2 (Program Counter & Stack) *Default Value: (0B_0000_0000)*

The EM78M611 Program Counter is a 13-bit long register that allows accessing 6k bytes of Program Memory with 8 level stacks. The eight LSB bits, A0~A7, are located at R2, while the three MSB bits, A12~A10, are located at R3. The Program Counter is cleared after Power-on reset or WatchDog reset. The first instruction that is executed after a reset is located at address 00h.



R3 (Status Register) *Default Value:(0B_0001_1XXX)*

7	6	5	4	3	2	1	0
PS2	PS1	PS0	T	P	Z	DC	C

R3 [0] Carry flag.

R3 [1] Auxiliary carry flag.

R3 [2] Zero flag. It will be set to 1 when the result of an arithmetic or logic operation is zero.

R3 [3] Power down flag. It will be set to 1 during Power-on phase or by "WDTC" command and cleared when the MCU enters into Power down mode. It remains in previous state after WatchDog Reset.

1: Power-on.

0: Power down

R3 [4] Time-out flag. It will be set to 1 during Power-on phase or by "WDTC" command. It is reset to 0 by WDT time-out.

1: WatchDog timer no overflow.

0: WatchDog timer overflow.

The various states of Power down flag and Time-out flag at different conditions are shown below:

T	P	Condition
1	1	Power-on reset
1	1	WDTC instruction
0	*P	WDT time-out
1	0	Power down mode
1	0	Wakeup caused by port change during Power down mode

*P: Previous status before WDT reset

R3 [5-7] Page selection bits. These three bits are the used to select the page of program memory.

PS2	PS1	PS0	Program Memory Page [Address]
0	0	0	Page 0 [0000-03FF]
0	0	1	Page 1 [0400-07FF]
0	1	0	Page 2 [0800-0BFF]
0	1	1	Page 3 [0C00-0FFF]
1	0	0	Page 4 [1000-13FF]
1	0	1	Page 5 [1400-17FF]

R4 (RAM Select Register) *Default Value: (0B_00XX_XXXX)*

7	6	5	4	3	2	1	0
BK1	BK0	Ad5	Ad4	Ad3	Ad2	Ad1	Ad0

R4 (RAM select register) contains the address of the registers.

R4 [0~5] are used to select registers in 0x00h~0x3Fh. The address 0x00~0x1F is common space. After 0x1Fh, SRAM are divided into four banks. Use Bank Select Register.

R4 [6,7] to select the registers bank (refer to the table below).The following are two examples:

(1) R4=00*01100* and R4=10*01100* point to the same register 0x0Ch. Since 0x0Ch is in the common space, Bit 6 and Bit 7 are meaningless.

(2) R4=01*11100* points to the register 0x3C in Bank 2.

R4[7]Bk1	R4[6]Bk0	RAM Bank #
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

R5 (Port5 I/O register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
P57	P56	P55	P54	P53	P52	P51	P50

R6 (Port 6 I/O register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
P67	P66	P65	P64	P63	P62	P61	P60

R7 (Port7 I/O register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
P77	P76	D- / P75 / DATA	D+ / P74 / CLK	-	P72	P71	P70

R8 (Port 8 I/O register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
P87	P86	P85	P84	P83	P82	P81	P80

R9 (Port 9 I/O register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
-	P96	P95	P94	P93	P92	P91	P90

RA (E^{2}PROM Control Register) *Default Value: (0B_0000_0011)*

RA is a command register for E^{2}RPOM control. For detailed usage of this register, refer to Section 8.2.3 which describes the E^{2}RPOM embedded in the EM78M611.

RB (Pattern Detect Application Control Register) *Default Value: (0B_0000_0000)*

RB is a control register for controlling the Pattern Detect Application function. For the detailed description of this register, refer to Section 8.7.2 which describes the PDA function.

RC (USB Application Status Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
EP0_W	EP0_R	EP1_R	EP2_R	EP2_W	Host_Suspend	EP0_Busy	Stall

RC [0] Stall flag While MCU receives an unsupported command or invalid parameters from host, this bit will be set to 1 by the firmware to notify the UDC to return a STALL handshake. When a successful SETUP transaction is received, this bit is cleared automatically. This bit is readable and writable.

RC [1] EP0_Busy flag When this bit is equal to "1," it indicates that the UDC is writing data into the EP0'FIFO or reading data from it. During this time, the firmware will avoid accessing the FIFO until UDC finishes writing or reading. This bit is only readable.

RC [2] Host Suspend flag If this bit is equal to 1, it indicates that USB bus has no traffic for the specified period of 3.0 ms. This bit will also be cleared automatically when there is bus activity. This bit is only readable.

RC [3] EP2_W flag This bit is set when the UDC receives a successful data from USB Host to EP2. Upon detecting that this bit is equal to One, the firmware will execute a read sequence to the EP2's FIFO, then clear this bit. Otherwise, the subsequent data from USB Host won't be accepted by the UDC.

RC [4,5,6] EP0_R / EP1_R / EP2_R flag These three bits inform the UDC to read the data written by the firmware from the FIFO. Then the UDC will send the data to the Host automatically. After UDC finishes reading the data from the FIFO, this bit will be cleared automatically.

Therefore, before writing data into FIFO's, the firmware will first check this bit to avoid overwriting the data. These two bits can only be set by the firmware and cleared by the hardware.

RC [7] EP0_W flag After the UDC completes writing data to the FIFO, this bit will be set automatically. The firmware will clear it as soon as it gets the data from EP0's FIFO. Only when this bit is cleared that the UDC will be able to write a new data into the FIFO.

Therefore, before the firmware can write a data into the FIFO, this bit must first be set by the firmware to prevent UDC from writing data at the same time. This bit is both readable and writable.

RD (USB Application FIFO Address Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
0	0	0	UAD4	UAD3	UAD2	UAD1	UAD0

RD [0~4] USB Application FIFO address registers. These five bits are the address pointer of USB Application FIFO.

RD [5~7] Undefined registers. The default value is zero.

RE (USB Application FIFO Data Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
UD7	UD6	UD5	UD4	UD3	UD2	UD1	UD0

RE (USB Application FIFO data register) contains the data in the register of which address is pointed by RD.

RF (Interrupt Status Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
USB Host Resume_IF	SE2_IF	SE1_IF	Port7 state change_1F	USB Reset_IF	USB Suspend_IF	EP0_IF	TCC_IF

RF [0] TCC Overflow interrupt flag. It will be set while TCC overflows, and is cleared by the firmware.

RF [1] EndPoint Zero interrupt flag. It will be set when the EM78M611 receives Vender /Customer Command to EndPoint Zero. This bit is cleared by the firmware.

RF [2] USB Suspend interrupt flag. It will be set when the EM78M611 finds the USB Suspend Signal on USB bus. This bit is cleared by the firmware.

RF [3] USB Reset interrupt flag. It will be set when the host issues the USB Reset signal.

RF [4] Port 7 State Change interrupt flag. It will be set at P.74 ~ P.77 State Change when the EM78M611 is not running under USB mode.

RF [5,6] SE1 / SE2 Pattern Detection interrupt flag. These two flags are used for Pattern detecting application.

RF [7] USB Host Resume interrupt flag. It will be set only under Dual clock mode when the USB suspend signal becomes low.

8.2.1.2 Control Registers

Some special purpose registers are available for special control purposes. Except for the Accumulator (A), these registers must be read and written by special instructions. One of these registers, CONT, can only be read by the instruction "CONTR" and written by "CONTW" instruction. The other special control registers can be read by the instruction "IOR" and written by the instruction "IOW."

The following paragraphs only describe the general functions of the control registers. For more detailed description, refer to Sections 8.7 to 8.9 of this spec.

A (Accumulator Register)

The accumulator is an 8-bit register that holds operands and results of arithmetic calculations. It is not addressable.

CONT (Control Register) *Default Value: (0B_0011_1111)*

7	6	5	4	3	2	1	0
LED	/INT	TSR2	TSR1	TSR0	PSR2	PSR1	PSR0

Except for Bit-6 (Interrupt enable control bit), CONT register can be read by the instruction "CONTR" and written by the instruction “CONTW."

CONT [0~2] WatchDog Timer prescaler bits. These three bits are used as the prescaler of WatchDog Timer.

CONT [3~5] TCC Timer prescaler bits.

The relationship between the prescaler value and these bits are shown below:

PSR2/TSR2	PSR1/TSR1	PSR0/TSR0	TCC Rate	WDT Rate
0	0	0	1: 2	1: 1
0	0	1	1: 4	1: 2
0	1	0	1: 8	1: 4
0	1	1	1: 16	1: 8
1	0	0	1: 32	1: 16
1	0	1	1: 64	1: 32
1	1	0	1: 128	1: 64
1	1	1	1: 256	1: 128

CONT [6] Interrupt enable control bit. This bit toggles Interrupt function between enable and disable. It is set to 1 by the interrupt disable instruction "DISI" and reset by the interrupt enable instructions "ENI" or "RETI."

0: Enable the Interrupt function.

1: Disable the Interrupt function.

Note that this bit can be read only by the instruction "CONTR"

CONT [7] LED bit. This bit is used to enable the LED sink capacity of P76 and P77.

0: Disable the LED sink capacity of P76, P77.

1: Enable the LED sink capacity of P76, P77.

IOC5 ~IOC9 I/O Port Direction Control Registers

These are I/O port (Port5 ~ Port7) direction control registers. Each bit controls the I/O direction of three I/O ports respectively. When these bits are set to 1, the relative I/O pins become input pins. Similarly, the I/O pins becomes outputs when the relative control bits are cleared.

1: Input direction.

0: Output direction.

IOCA (Operation Mode Control Register) *Default Value: (0B_1100_0000)*

7	6	5	4	3	2	1	0
Dual_Frq.1	Dual_Frq.0	-	-	ExReg_Sel	PDA	PS/2	USB

IOCA [0,1] These two bits are used to select the operation mode. EM78M611 can auto-detect the type of port device being attached. After identifying the port, the firmware will set these two bits to enter into a proper operation mode. The definition of these two control registers is described in the table below.

IOCA[1]	IOCA[0]	Operation Mode
0	0	Detect Mode
0	1	USB Mode
1	0	PS/2 Mode
1	1	USB Test Mode

IOCA [2] Pattern Detect Application function enable bit. This bit is used to enable the Pattern Detect Application (PDA) function. For the details about this function please refer Section 8.7.

0: Disable PDA function.

1: Enable PDA function.

IOCA [3] Extra control register select bit. The five extra control registers (ERA, ERB, ERC, ERD, and ERD) are located in 0xA~0xE. To access these five registers, set the bit as follows**:**

0: Select RA ~ RE.

1: Select Extra Control registers – ERA ~ ERE.

IOCA [6,7] Selects the operation frequency in Dual Clock Mode. Four frequencies are available and can be chosen as Dual Clock Mode for running the MCU program.

Dual_Frq.1	Dual_Frq.0	Frequency
0	0	500Hz
0	1	4kHz
1	0	32kHz
1	1	256kHz

IOCB (Port 9 Wake-up Pin Select Register) *Default Value: (0B_1111_1111)*

7	6	5	4	3	2	1	0
1	/P96	/P95	/P94	/P93	/P92	/P91	/P90

IOCB [0~6] These bits are used to select which of the Port 9 pins is to be assigned to wakeup the MCU while in Power down mode.

0: Enable the function.

1: Disable the function.

IOCB [7] Undefined. The default value is Zero.

IOCC (Port 9 LED Sink Capacity Control Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
0	P96	P95	0	P93	P92	P91	P90

IOCC [0~3,5,6] LED sink control bit. These bits are used to enable the LED sink capacity of P90 ~ P93, P95, and P96.

0: Disable the LED sink capacity of respective pin.

1: Enable the LED sink capacity of respective pin.

IOCC [4,7] Undefined. The default value is Zero.

IOCD (Port 9 Pull High Control Register) *Default Value: (0B_1111_1111)*

7	6	5	4	3	2	1	0
1	/PH96	/PH95	1	/PH93	/PH92	/PH91	/PH90

IOCD [0~6] These bits control the 200KOhm pull-high resistor of individual pins in Port 9.

1: Disable the function of pull-high.

0: Enable the function of pull-high.

IOCE (Special Function Control Register) *Default Value: (0B_1101_01111)*

7	6	5	4	3	2	1	0
/Dual clock	/WUE	WTE	RUN	Device_Resume	/PU8	/PU6	/PU5

IOCE [0,1,2] Port 5, Port 6, and Port 8 pull-high control bits.

1: Disable

0: Enable

IOCE [3] Device Resume control bit. Writing this bit to “1” can generate Device Resume signal on USB bus. As long as the USB bus is not idle, this bit will be cleared at the same time.

IOCE [4] Run bit. This bit can be cleared by the firmware and set during power-on, or by the hardware at the falling edge of wake-up signal. When this bit is cleared, the clock system is disabled and the MCU enters into Power down mode. At the transition of wake-up signal from high to low, this bit is set to enable the clock system.

1: Run mode. The EM78M611 is working normally.

0: Sleep mode. The EM78M611 is in power down mode.

IOCE [5] WatchDog Timer enable bit. The bit disable/enables the WatchDog Timer.

1: Enable WDT.

0: Disable WDT.

IOCE [6] Enable the wake-up function as triggered by port-changed. This bit is set by UDC.

1: Disable the wake-up function.

0: Enable the wake-up function.

IOCE [7] Dual clock Control bit. This bit is used to select the frequency of system clock. When this bit is cleared, the MCU will run on very low frequency for power saving and the UDC will stop working.

1: Selects EM78M611 to run on normal frequency.

0: Selects to run on slow frequency.

IOCF (Interrupt Mask Register) *Default Value：(0B_0000_0000)*

7	6	5	4	3	2	1	0
USB Host Resume_IE	SE2_IE	SE1_IE	Port7 state change_1E	USB Reset_IE	USB Suspend_IE	EP0_IE	TCC_IE

IOCF [0~7] TCC / EP0 / USB Suspend / USB Reset / Port 7 State Change / SE1 / SE2 / USB Host Resume interrupt enable bits. These eight bits control the function of TCC interrupt, EP0 interrupt, USB Suspend interrupt, USB Reset interrupt, Port7 State Change interrupt, SE1 pattern detection interrupt, SE2 pattern detection interrupt and USB Host Resume interrupt respectively. Individual interrupt is enabled by setting its associated control bit in the IOCF to "1."

1: Enable Interrupt.

0: Disable Interrupt.

Only when the global interrupt is enabled by the ENI instruction that the individual interrupt will work. After DISI instruction, any interrupt will not work even if the respective control bits of IOCF are set to 1.

The USB Host Resume Interrupt works only under Dual clock mode. This is because when the MCU is under sleep mode, it will be waked up by the UDC Resume signal automatically.

8.2.1.3 Extra Control Register

Five extra control registers are available to control special functions. The five registers are ERA (AD Control register), ERB (AD_LSB), ERC (AD_MSB), ERD (AD_Rate), and ERE (PWM Control register).

Remember to set IOCA[3] before accessing these five registers. The operating method is same as other control registers.

More detailed descriptions of the registers are provided in Section 8.7 to 8.9.

8.2.2 USB Application FIFOs

For USB Application, EM78M611 provides an 8-byte First-In-First-Out (FIFO) buffer for each endpoint. The buffer cannot be accessed directly. However, a corresponding Data Byte Pointer register for each endpoint is made available to address the individual byte of the FIFO buffer. The content of the individual byte will map to a special register.

8.2.3 E^2PROM

Four bytes of E^2PROM are located in the R2C ~ R2F of Bank 3. The stored data of E^2PROM are not erased when the power is off and can be read and rewritten by firmware. In some special case of application, for example, cordless keyboard controller, it can store important data, such as the cordless keyboard's device identical number.

There is a control register, RA (address **:** 0x0A in Bank1) that controls the E^2PROM, that is, to read, write, or to erase the data from E^2PROM. Writing a command into this register will execute an action to E^2PROM. The command value is defined in the following table. Note that there is an execution time lapse for each command. Before writing the next command into the control register, allow enough time for the E^2PROM to finish the previous command.

Command Value	Action	Execution Time
0B_0000_0000	Read	1ms
0B_0000_0001	Write	9ms
0B_0000_0010	Erase	128ms
0B_0000_0011	Disable	N.A.

8.3 USB Application

EM78M611 is designed specially for USB device application and has many powerful functions that help the firmware to free itself from complex situation in various aspects of USB application.

8.3.1 Auto-Detect PS/2 or USB Mode

When the EM78M611 is connected to the bus, it will auto-detect and identify which type of bus (USB or PS/2) it is connected to. The condition that influences auto-detect function is described below**:**

1. After a Power-on reset, the initial value of IOCA [0,1] is 0b00. Thus the operation mode is "Detect mode" and the D+ and D- IO pins are internal pulled high by 200KOhm to VDD.
2. The firmware checks the state of R7 [4,5]. If the state of this two bit is 0b00, set the IOCA [0] to "1" to define the "USB mode." Otherwise, set the IOCA [1] to "1," to define "PS/2 mode."

3. When the operation mode is defined as “USB mode,” the D- IO pin will be internal pulled high by a 1.5KOhm resistor to 3.3V, which is output from a built-in regulator.

4. If the operation mode is in “PS/2 mode,” both of the PS/2 interface IO pins are internal pulled high by a 2.2KOhm resistor to VDD.

***{NOTE}** If the auto-detect function is not used, the firmware should set the operation mode, either USB mode or PS/2 mode, in the beginning of program.*

An additional mode, “USB Test Mode” is also available. This mode has no load on D+ and D- IO pins, and can only be used in USB Application case. Therefore, an external 1.5KOhm resistor is needed to pull up D- IO pin to 3.3V.

Under PS/2 mode, both PS/2 pins are programmed to generate an interrupt. After setting the P.74 ~ P.77 State changed Interrupt Enable bit, the MCU will interrupt while the state of these four pins changes.

8.3.2 USB Device Controller

The USB Device Controller (UDC) built-in in the EM78M611 can interpret the USB Standard Command and response automatically without involving firmware. The embedded Series Interface Engine (SIE) handles the serialization and deserialization of actual USB transmission. Thus, a developer can concentrate his efforts more in perfecting the device actual functions and spend less energy in dealing with USB transaction.

The UDC handles and decodes most Standard USB commands defined in the USB Specification Rev1.1. If UDC receives an unsupported command, it will set a flag to notify MCU the receipt of such command. The Standard Commands that EM78M611 supports includes; **Clear Feature**, **Get Configuration**, **Get Interface**, **Get Status**, **Set Address**, **Set Configuration**, **Set Feature, and Set Interface**.

Each time UDC receives a USB command, it writes the command into EP0’s FIFO. Only when it receives unsupported command that the UDC will notify the MCU through interrupt.

Therefore, EM78M611 is very flexible under USB application because the developer can freely choose the method of decoding the USB command as dictated by different situation.

8.3.3 Device Address and Endpoints

EM78M611 supports one device address and three endpoints, EP0 for control endpoint, EP1 and EP2 for interrupt endpoint. Sending data to USB host in EM78M611 is very easy. Just write data into EP’s FIFO, then set flag, and the UDC will handle the rest. It will then confirm that the USB host has received the correct data from EM78M611.

8.4 Reset

The EM78M611 provides three types of reset**:** (1) Power-on Reset, (2) WatchDog Reset, and (3) USB Reset.

8.4.1 Power-On Reset

Power-on Reset occurs when the device is attached to power and a reset signal is initiated. The signal will last until the MCU becomes stable. After a Power-on Reset, the MCU enters into following predetermined states (see below), and then, it is ready to execute the program.

a. The program counter is cleared.

b. The TCC timer and WatchDog timer are cleared.

c. Special registers and Special Control registers are all set to initial value.

The MCU also has a low voltage detector that detects low output power condition. Whenever the output voltage of the 3.3V regulator decreases to below 2.2V, a reset signal is set off.

8.4.2 WatchDog Reset

When the WatchDog timer overflows, it causes the WatchDog to reset. After it resets, the program is executed from the beginning and some registers will be reset. The UDC however, remains unaffected.

8.4.3 USB Reset

When UDC detects a USB Reset signal on USB Bus, it interrupts the MCU, then proceed to perform the specified process that follows. After a USB device is attached to the USB port, it cannot respond to any bus transactions until it receives a USB Reset signal from the bus.

8.5 Saving Power Mode

The EM78M611 provides two options of power-saving modes for energy conservation, i.e., Power Down mode and Dual clock mode.

8.5.1 Power Down Mode

The EM78M611 enters into Power Down mode by clearing the RUN register (IOCE[4]). During this mode, the oscillator is turned off and the MCU goes to sleep. It will wake up when signal from USB host is resumed, or when the WatchDog reset or the input port state changes.

If the MCU wakes up when I/O port status changes, the direction of I/O port should be set at input direction, then read the state of port. For example**:**

```
:
// Set the Port 6 to input port
MOV     A , 0XFF
IOW      PORT6
// Read the state of Port 6
MOV     PORT6, PORT6
// Clear the RUN bit
IOR      0XE
AND     A , 0B11101111
IOW     0XE
:
:
```

If the MCU is awaken by a USB Resume signal, the next instruction will be executed and one flag, RC[3] will be set to 1.

8.5.2 Dual Clock Mode

The EM78M611 has one internal oscillator for power saving application. Clearing the Bit IOCE [7] will enable the low frequency oscillator. At the same time, the external oscillator will be turned off. Then the MCU will run under very low frequency to conserve power. Four types of frequency are available for selection in setting Bits IOCA [6, 7].

The USB Host Resume Interrupt can only be used in this mode. If this interrupt is enabled, the MCU will be interrupted when the USB Suspend signal is detected on USB Bus.

8.6 Interrupt

The EM78611 has one interrupt vectors in 0x0001. When an interrupt occurs during the MCU running program, it will jump to the interrupt vector (0x0001) and execute the instructions sequentially from interrupt vector. RF is the interrupt status register, which records the interrupt status in the relative flags/bits.

The interrupt condition could be one of the following**:**

1. TCC Overflow**:** When the Timer Clock / Counter Register (R1) overflows, the status flag RF[0] will be set to 1. Its interrupt vector is 0X0001.
2. Port7 State Change**:** When the input signals in Port 7 changes, the status flag RF[4] will be set to 1. Its interrupt vector is 0X0001.
3. SE1 Pattern Detection Interrupt Conditions**:** If the Pattern Detection Application function is enabled, there will be four conditions with which interruption is generated, and the status flag RF[5] is set to 1 (interrupt vector is 0X0001).
   a) Signal from P.92 changes to low, and Pattern Counter value is bigger than R11 register value.
   b) Signal from P.92 changes to high, and Pattern Counter value bigger than R10 register value.
   c) P.92 stays high, and Pattern Counter value equal 0XFF.
   d) P.92 stays low, and Pattern Counter value equal 0XFF.
4. SE2 Pattern Counter Interrupt Conditions**:** If the Pattern Detection Application function is enabled, there will be three conditions with which interruption is generated and the status flag RF[6] is set to 1(interrupt vector is 0X0001).
   a) Signal from P.93 changes to low, and Pattern Counter value is bigger than R13 register value.
   b) Signal from P.93 changes to high, and Pattern Counter value is bigger than R12 register value.
   c) P.93 stays high, and Pattern Counter value equal 0XFF.
   d) P.93 stays low, and Pattern Counter value equal 0XFF.

5. EP0 interrupt**:** When the UDC successfully accepts a setup transaction from host to EndPoint0, the status flag RF[1] is set to 1. Its interrupt vector is 0X0001

6. USB suspend**:** When UDC detects a USB Suspend signal on USB bus, the status flag RF[2] is set to 1. Its interrupt vector is 0X0001.

7. USB Reset**:** When the UDC detects a USB Reset signal on USB bus, the status flag R[3] is set to 1. Its interrupt vector is 0X0001.

8. USB Host Resume**:** When UDC detects that the USB bus is no longer in Suspend condition and without Device Resume signal, the status flag R[7] is set to 1. Its interrupt vector is 0X0001.

IOCF is an interrupt mask register which can be set bit by bit. While their respective bit is written to 0, the hardware interrupt will inhibit, that is, the EM78M611 will not jump to the interrupt vector to execute instructions. But the interrupt status flags still records the conditions no matter whether the interrupt is masked or not. The interrupt status flags must be cleared by firmware before leaving the interrupt service routine and enabling interrupt.

The global interrupt is enabled by the ENI (RETI) instruction and is disabled by the DISI instruction.

8.7 Pattern Detect Application (PDA)

8.7.1 Function Description

This function is designed for the serial signal transmission, e.g., the transmission between a wireless device and its receiver box. The EM78M611 has two sets of built-in Pattern Detect Application block that ensures the EM78M611 is equipped with a compound device, such as the receiver box controller for a wireless keyboard paired with a wireless mouse.

Pattern Detect Application (PDA) can calculate the length of one pattern and interrupt the MCU while the serial signal is transiting from high to low (or vise-versa). Then the MCU reads the length value from a specified register.

8.7.2 Control Register

The PDA includes an enable control bit, one control register and four length counter registers in 0x10 ~0x13.

IOCA [2] PDA Enable Control Bit. When this bit is set, the PDA function starts and the P92 and P93 become input pin automatically to sample the serial signal.

1 : enable PDA function.

0 : disable PDA function.

RB (PDA Control Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
SE2.F	SE1.F	SR.2	SR.1	SR.0	DB2	DB1	DB0

This register is used to define two parameters of PDA function; signal sampling rate and debounce length. When a pattern ends, the value in the counter is loaded into its respective register and the RB[6] or RB[7] is set to indicate which type of pattern (high or low) is at its end or which type of pattern counter is on overflow.

0: low pattern.

1: high pattern.

R10 (P.92 Low Pattern Counter)

This register records the length of P.92 in low status.

R11 (P.92 High Pattern Counter)

This register records the length of P.92 in high status.

R12 (P.93 Low Pattern Counter)

This register record the length of P.93 in low status.

R13 (P.93 High Pattern Counter)

This register records the length of P.93 in high status.

R10~R13 function as general registers if this function is not enabled. Once the enabled bit is set, these four registers will be loaded with the value of pattern counter.

8.7.3 Sampling Rate and Debounce Length

Although the two pattern detect pins are separate, and each pin has its own pattern counter. Both pins use the same Sampling Rate and Debounce Length parameters.

The PDA samples the serial signal every fixed interval. The pattern counter will increase by one at sampling time if the signal remains unchanged. If the signal is at high state, then the “high pattern counter“ will increase; otherwise the “low pattern counter” increases. As long as the signal state changes, the PDA will debounce signal and load the value of pattern counter into the respectively register for the firmware to read. For example, if the signal in P.92 is in “low” state, the low counter of P.92 will counts continuously until the state of the input signal in P.92 changes. When the state of change occurs (in this case, the signal changes from “low” to “high” state), the PDA will take for a time break (which is equal the result of sampling interval multiplied by the debounce length), to avoid possible noise. After the debounce length time, if the signal remains in high state, the high pattern counter will start to count and

load the low pattern counter's value into R10. At the same time, RB[6] is cleared to indicate the low pattern is over.

The correlation between the value of control register and debounce time are as follows:

DB.2	DB.1	DB.0	Debounce Time
0	0	0	No Sampling clock.
0	0	1	1 Sampling clock
0	1	0	2 Sampling clock
0	1	1	3 Sampling clock.
1	0	0	4 Sampling clock
1	0	1	5 Sampling clock
1	1	0	6 Sampling clock
1	1	1	7 Sampling clock

Now consider another situation of this case, where the signal of P92 always stays "low". The low pattern counter of P92 will eventually overflow. Once the counter overflows, the content of the counter will also be loaded into R10, that is, the register is written to 0xFF, then the counter is reset to count from zero again.

If the hardware interrupt of PDA function is enabled, (IOCF[5] is equal to "1"), then the program will go to 0x0001 to execute interrupt routine while the content of a pattern counter is loaded into the register.

The correlation between the value of control register and actual sampling rate are as shown below:

SR.2	SR.1	SR.0	Sampling Rate (External oscillator frequency = 6MHz)	Sampling Rate (External oscillator frequency = 12MHz)
0	0	0	N.A.	N.A.
0	0	1	N.A.	N.A.
0	1	0	1500 (Count / mSec)	N.A.
0	1	1	750 (Count / mSec)	1500 (Count/ mSec)
1	0	0	375 (Count / mSec)	750 (Count / mSec)
1	0	1	188 (Count / mSec)	375 (Count / mSec)
1	1	0	94 (Count / mSec)	188 (Count / mSec)
1	1	1	47 (Count / mSec)	94 (Count / mSec)

After the PDA function is enabled (by setting IOCA[2] to 1), user can write a default value to the High Pattern counter register and Low Pattern counter register. Then set the corresponding interrupt enable bit (IOCF[5]). When the counting value of one "H" pattern is bigger than the default value of R11, the Pattern Detecting interrupt will be generated. Similarly, if the counting value of one "L" pattern is bigger than the default value of R10, the Low Pattern Detecting interrupt will occur. Thus, the EM78M611 is notified and aware that one effective pattern is received from P.92.

If user has no need of these two interrupts, they can be masked. The new value of counting

a pattern still will be loaded to the R10 and R11. The firmware must poll and determine whether the value of these two registers had changed or not.

8.7.4 Example

Initial Setting :

IOCA[5:3] = 5 : Setting Prescaler. Setting 1:32.

```
IOR IOCA
AND A,@0XC7        ;11 00_0 111
OR A,@0X28         ;00 10_1 000
IOW IOCA
```

RB[3:0] = 3 : Setting Debonce Times.

```
MOV A,@0X03
MOV RB,A
```

R10~R13 = 150(800uS) : Setting compare value.

```
MOV A,@150
MOV R10~13,A
```

IOCA[2] : Enabling RF function :

```
IOR IOCA
OR A,@0X04         ;0000_0 1 00
IOW IOCA
```

- The active of the RF timing counter : After setting.
- Assume that the T1 is the High pattern counter and the T2 is the Low pattern counter.

  The PDA function will compare R11 or R13 with T1 or compare R10 or R12 with T2.

  If T1 >= R11 , then setting RB[4] = 1 and making RF1 interrupting.

  If T1 >= R13 , then setting RB[5] = 1 and making RF2 interrupting.

  If T2 >= R10 , then setting RB[4] = 0 and making RF1 interrupting.

  If T2 >= R12 , then setting RB[5] = 0 and making RF2 interrupting.
- After interrupting. The program will check Timing Count & save state.

  R10 : The low signal counter of the 1st RF module that inputted from P92.

  R11 : The high signal counter of the 1st RF module that inputted from P92.

  R12 : The low signal counter of the 2nd RF module that inputted from P93.

  R13 : The high signal counter of the 2nd RF module that inputted from P93.

8.8 Pulse Width Modulation (PWM)

8.8.1 Function Description

In PWM mode, both of PWM1 (P.92) and PWM2 (P.93) produce plus programmable signal of up to 8-bits resolution.

The PWM Period is defined as *0xFF * Timer Counter Clock*. The Timer Counter clock source is controlled by an extra control register, ERE. For example; if the Clock source is 1MHz, then the Period will be 255u seconds.

Period = 255 * (1/Timer Counter Clock)

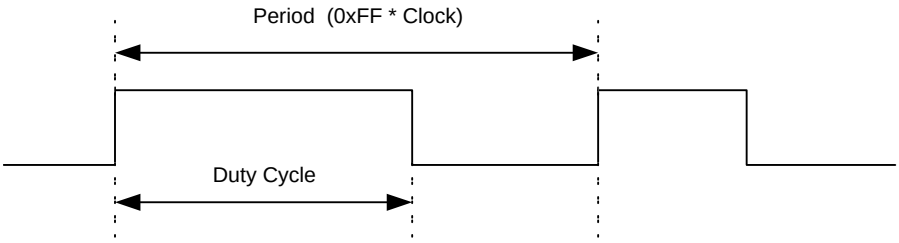


Fig.8.9.2 The PWM Output Timing

8.8.2 Duty Cycle

The PWM duty cycle is defined by writing to the R10/R11 Register for PWM1/PWM2.

Duty Cycle = (R10 / 255) * 100% for PWM1
(R11 / 255) * 100% for PWM2

8.8.3 Control Register

R10 (PWM1 Duty Cycle Register)

A specified value keeps the output of PWM1 to remain at high in a Period.

R11 (PWM2 Duty Cycle Register)

A specified value keeps the output of PWM2 to remain at high in a Period.

ERE(PWM Control Register) *Default Value: (0B_0000_0001)*

7	6	5	4	3	2	1	0
PEN2	PEN1	-	-	-	PS2	PS1	PS0

ERE [0~2] PWM Clock Prescaler.

PS2	PS1	PS0	Clock(Hz)	Period/255 (s)
0	0	0	Fosc/3	0.5u
0	0	1	Fosc/6	1u
0	1	0	Fosc/12	2u
0	1	1	Fosc/24	4u
1	0	0	Fosc/48	8u
1	0	1	Fosc/96	16u
1	1	0	Fosc/192	32u
1	1	1	Fosc/384	64u

ERE [6,7] PWM1/PWM2 Enable Bit

0:Disable

1:Enable

8.9 Analog-To-Digital Converter (ADC)

8.9.1 Function Description

The Analog to Digital converter consists of a 5-bit analog multiplexer, one Control Register (ERA), and two data registers (RBS & RCS) for 10-bit resolution.

The ADC module utilizes successive approximation to convert the unknown analog signal to a digital value. The result is fed to the ADDATA. Input channels are selected by the analog input multiplexer via the ADCS/RAS bits AD0~AD4.

- 10-bit resolution**:** 0x00-00~0xC0-FF (0b11000000-11111111)
- Start (0x00-00)**:** 0 Vref~(1/1024)*Vref
- Full (0xC0-FF)**:** (1023/1024)*Vref~Vref
- Converting Time**:** 12 clock time of internal clock source

8.9.2 Control Register

ERA (AD Channel Select Register) *Default Value: (0B_0001_1111)*

7	6	5	4	3	2	1	0
ADC	0	0	AD4	AD3	AD2	AD1	AD0

ERA [0~4]:AD Channel Selector

AD4	AD3	AD2	AD1	AD0	Channel	I/O Port
0	0	0	0	0	0	P50
0	0	0	0	1	1	P51
0	0	0	1	0	2	P52
0	0	0	1	1	3	P53
0	0	1	0	0	4	P54
0	0	1	0	1	5	P55
0	0	1	1	0	6	P56
0	0	1	1	1	7	P57
0	1	0	0	0	8	P80
0	1	0	0	1	9	P81
0	1	0	1	0	10	P82
0	1	0	1	1	11	P83
0	1	1	0	0	12	P84
0	1	1	0	1	13	P85
0	1	1	1	0	14	P86
0	1	1	1	1	15	P87
1	0	0	0	0	16	P60
1	0	0	0	1	17	P61
1	0	0	1	0	18	P62
1	0	0	1	1	19	P63
1	0	1	0	0	20	P64
1	0	1	0	1	21	P65
1	0	1	1	0	22	P66
1	0	1	1	1	23	P67

ERA [7] AD Converter ready flag.

0 → 1: Start AD Converting (set by firmware).

1 → 0: When AD finishes converting and has moved digital data into AD Data Register, this bit will be set by hardware.

[NOTE] *Hardware can enable this function only at AD Channel Selector of the functional I/O port. After Power-on reset, the initial value of this register is 0b0001 1111.*

ERB (AD LSB Data Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
Bit 1	Bit 0	0	0	0	0	0	0

AD Digital Data LSB 8 bits.

ERC (AD MSB Data Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2

AD Digital Data MSB 2 bits.

ERD (AD Control Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
0	0	0	0	0	-	ADPS1	ADPS0

ERD [0 1]:The clock source of AD converting time.

00: 256kHz

01: 128kHz

10: 64kHz

11: 32kHz

9. Absolute Maximum Ratings

Symbol	Min	Max	Unit
Temperature under bias	0	70	ºC
Storage temperature	-65	150	ºC
Input voltage	-0.5	6.0	V
Output voltage	-0.5	6.0	V

10. DC Electrical Characteristic

($T = 25^oC$, V_{DD}=5V, V_{SS}=0V)

Symble	Parameter	Condition	Min	Type	Max	Unit
3.3V Regulator						
V_{Rag}	Output voltage of 3.3v Regulator	V_{DD} = 4.4V ~ 5.25V	3.0	3.3	3.6	V
V_{ResetL}	Low Power Reset detecting low Voltage			-	2.2	V
V_{ResetH}	Low Power Reset detecting high Voltage		3.0	-		V
MCU operating						
I_{IL}	Input Leakage Current for input pins	VIN=VDD,VSS	-	-	±1	μA
V_{IHX}	Clock Input High Voltage	OSCI	2.5	-	-	V
V_{ILX}	Clock Input Low Voltage	OSCI	-	-	1.0	V
I_{CC1}	VDD operating supply current – Normal frequency operation mode	Crystal type Freq. = 6MHz Output pins floating	-	-	10	mA
I_{CC2}	VDD operating supply current – Normal frequency operation mode	Crystal type Freq. = 12MHz Output pins floating	-	-	20	mA
I_{CC3}	VDD operating supply current – Dual clock mode	RC oscillation type Freq. = 256kHz Ouput pins floating	-	-	250	μA
I_{SB1}	Operating supply current 1 – Power down mode	All input and I/O pins at VDD Output pins floating WDT disabled	-	-	80	μA
I_{SB2}	Operating supply current 2 – Power down mode	All input and I/O pins at VDD Output pins floating WDT enable	-	-	100	μA
GPIO Pins						
V_{IH}	Input High Voltage	Port 5 & Port 6 & Port 7 & Port 8 & Port 9	2.0	-	-	V
V_{IL}	Input Low Voltage	Port 5 & Port 6 & Port 7 & Port8 & Port 9	-	-	0.8	V
V_{OH1}	Output High Voltage (P70~P73,P76 and P77)	I_{Sink} = 10.0mA V_{DD} = 5V		2.4		V
V_{OH2}	Output High Voltage (P74, P75)	I_{Sink} = 5.0mA V_{DD} = 5V		2.4		V
V_{OH3}	Output High Voltage (Port5 & Port6 & Port8 and P90~P93, P95, P96)	I_{Sink} = 10.0mA V_{REG} = 3.3V		2.4		V
V_{OL1}	Output Low Voltage (P76 and P77 normal mode)	I_{Sink} = 10.0mA V_{DD} = 5V		0.4		V
V_{OL2}	Output Low Voltage (P74, P75)	I_{Sink} = 5.0mA V_{DD} = 5V		0.4		V
V_{OL3}	Output Low Voltage (P70~P73,P76 and P77 sink LED)	I_{Sink} = 10.0mA V_{DD} = 5V		3		V

V_{OL4}	Output Low Voltage (P90 ~ P96 normal mode)	I_{Sink} = 10.0mA V_{REG} = 3.3V		0.4		V
V_{OL5}	Output Low Voltage (P90 ~ P96 sink LED)	I_{Sink} = 10.0mA V_{REG} = 3.3V		1		V
I_{PH1}	Input current with pull-high resister (Port 5, 6, 8, P.90 ~ P.93, P.95 ~ P.96)	Input pin with pull-high resistor (25kOhm) V_{IN} = V_{SS}		125		µA
I_{PH2}	Input current with pull-high resister (P.74 ~ P.77)	Input pin with pull-high resistor (2.2kOhm) V_{IN} = V_{SS}		2.27		mA
USB Interface						
V_{OH}	Static Output High	USB operation Mode	2.8	-	3.6	V
V_{OL}	Static Output Low		-	-	0.3	V
V_{DI}	Differential Input Sensitivity		0.2	-	-	V
V_{CM}	Differential Input Command Mode Range		0.8	-	2.5	V
V_{SE}	Single Ended Receiver Threshold	USB operation Mode	0.8	-	2.0	V
C_{IN}	Transceiver Capacitance		-	-	20	pF
V_{RG}	Output Voltage of Internal Regulator		3.0	-	3.6	V

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