SONY

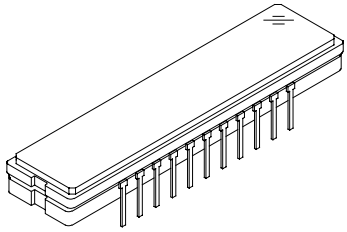
ILX551A

2048-pixel CCD Linear Sensor (B/W)

Description

The ILX551A is a reduction type CCD linear sensor designed for facsimile, image scanner and OCR use. This sensor reads B4 size documents at a density of 200DPI (Dot Per Inch). A built-in timing generator and clock-drivers ensure direct drive at 5V logic for easy use.

22 pin DIP (Cer-DIP)



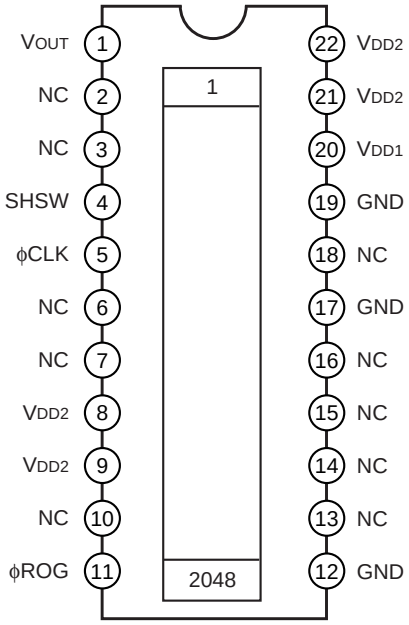
Features

- Number of effective pixels: 2048 pixels
- Pixel size: 14µm × 14µm (14µm pitch)
- Built-in timing generator and clock-drivers
- Ultra low lag
- Maximum clock frequency: 5MHz

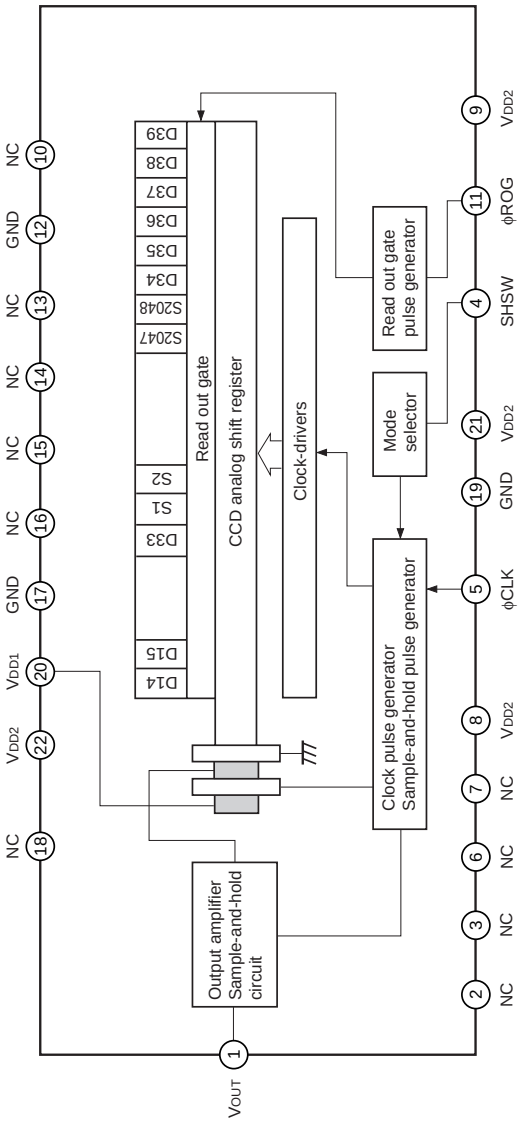
Absolute Maximum Ratings

• Supply voltage	V_{DD1}	11	V
	V_{DD2}	6	V
• Operating temperature		–10 to +55	°C
• Storage temperature		–30 to +80	°C

Pin Configuration (Top View)



Block Diagram



E00439-PS

Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	V_{OUT}	Signal output	12	GND	GND
2	NC	NC	13	NC	NC
3	NC	NC	14	NC	NC
4	SHSW	Switch { with S/H → GND; without S/H → $V_{DD}2$	15	NC	NC
5	ϕCLK	Clock pulse	16	NC	NC
6	NC	NC	17	GND	GND
7	NC	NC	18	NC	NC
8	V_{DD2}	5V power supply	19	GND	GND
9	V_{DD2}	5V power supply	20	V_{DD1}	9V power supply
10	NC	NC	21	V_{DD2}	5V power supply
11	ϕROG	Clock pulse	22	V_{DD2}	5V power supply

Recommended Supply Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD1}	8.5	9.0	9.5	V
V_{DD2}	4.75	5.0	5.25	V

Note) Rules for raising and lowering power supply voltage
To raise power supply voltage, first raise V_{DD1} (9V) and then V_{DD2} (5V).
To lower voltage, first lower V_{DD2} (5V) and then V_{DD1} (9V).

Mode Description

Mode in use	Pin condition
S/H	Pin 4 SHSW
Yes	GND
No	V_{DD2}

Input Capacity of Pins

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of ϕCLK pin	$C_{\phi CLK}$	—	10	—	pF
Input capacity of ϕROG pin	$C_{\phi ROG}$	—	10	—	pF

Recommended Input Pulse Voltage

Item	Min.	Typ.	Max.	Unit
Input clock high level	4.5	5.0	5.5	V
Input clock low level	0.0	—	0.5	V

Electrooptical Characteristics

(Ta = 25°C, V_{DD1} = 9V, V_{DD2} = 5V, Clock frequency = 1MHz, Light source = 3200K, IR cut filter: CM-500S (t = 1.0mm))

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Secsitivity	R	30	40	50	V/(lx · s)	Note 1
Sensitivity nonuniformity	PRNU	—	2.0	8.0	%	Note 2
Saturation output voltage	V_{SAT}	1.5	1.8	—	V	—
Dark voltage average	V_{DRK}	—	0.3	2.0	mV	Note 3
Dark signal nonuniformity	DSNU	—	0.5	3.0	mV	Note 3
Image lag	IL	—	0.02	—	%	Note 4
Dynamic range	DR	—	6000	—	—	Note 5
Saturation exposure	SE	—	0.045	—	lx · s	Note 6
9V supply current	I_{VDD1}	—	4.0	8.0	mA	—
5V supply current	I_{VDD2}	—	1.8	5.0	mA	—
Total transfer efficiency	TTE	92.0	97.0	—	%	—
Output impedance	Z_O	—	600	—	Ω	—
Offset level	V_{OS}	—	4.0	—	V	Note 7

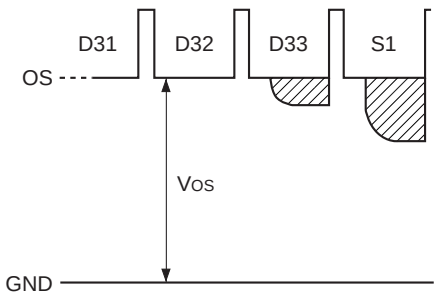
Notes)

1. For the sensitivity test light is applied with a uniform intensity of illumination.
2. PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 1.

$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100\ [\%]$$

   The maximum output is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.
3. Integration time is 10ms.
4. V_{OUT} = 500mV
5. $DR = \frac{V_{SAT}}{V_{DRK}}$

   When optical accumulated time is shorter, the dynamic range gets wider because dark voltage is in proportion to optical accumulated time.
6. $SE = \frac{V_{SAT}}{R}$
7. Vos is defined as indicated below.



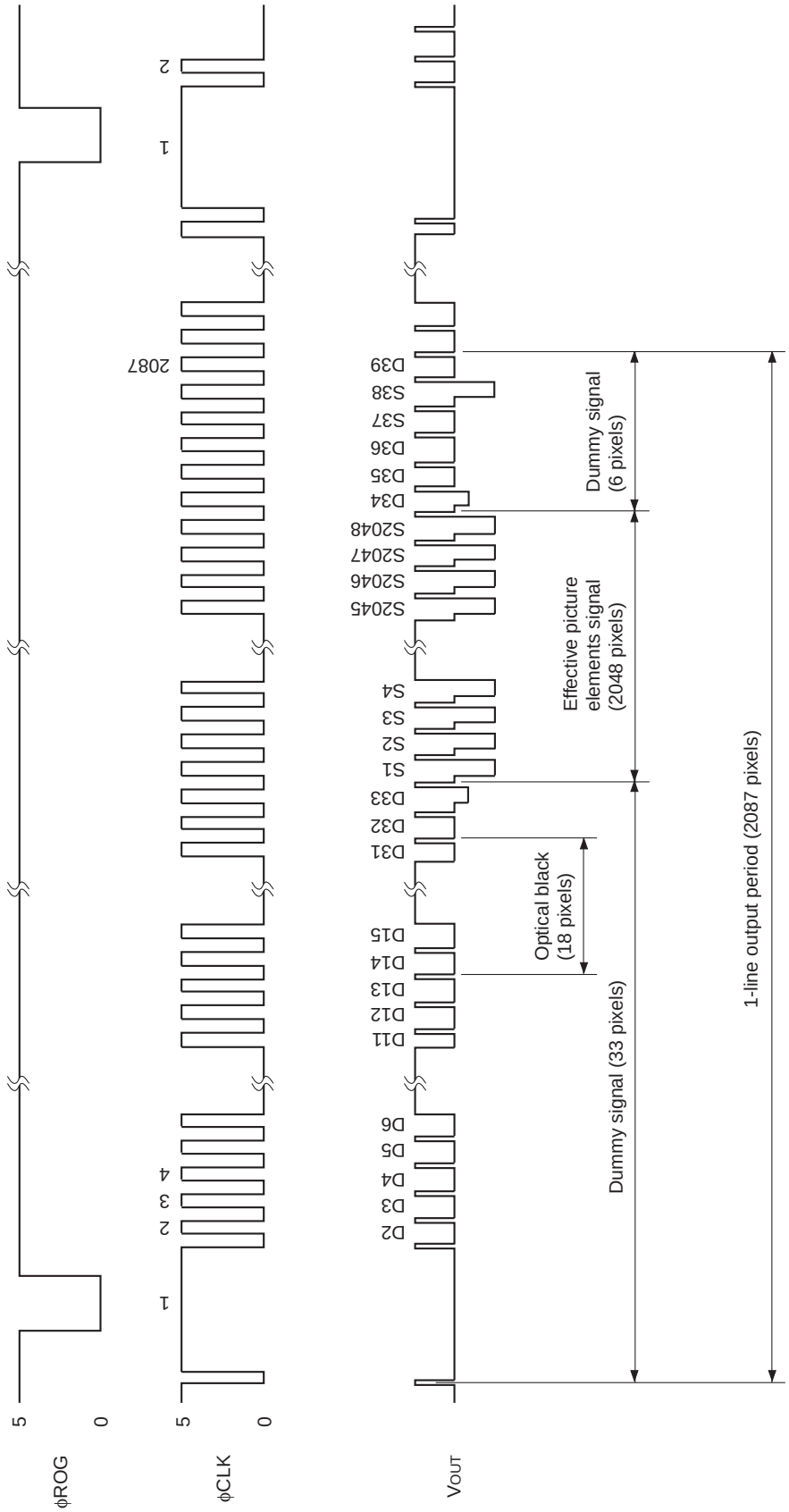
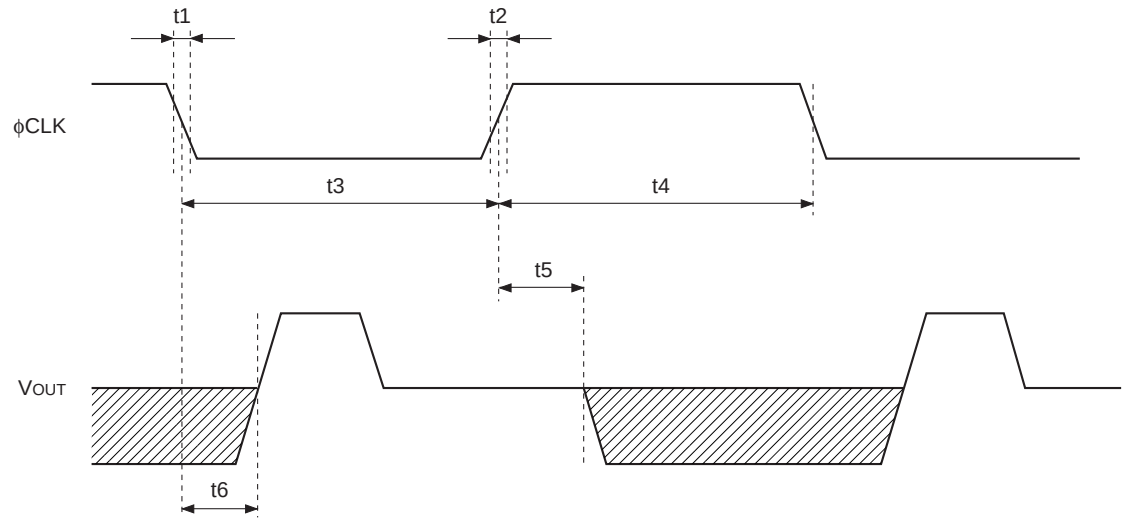


Fig. 1. Clock Timing Diagram (without S/H mode)

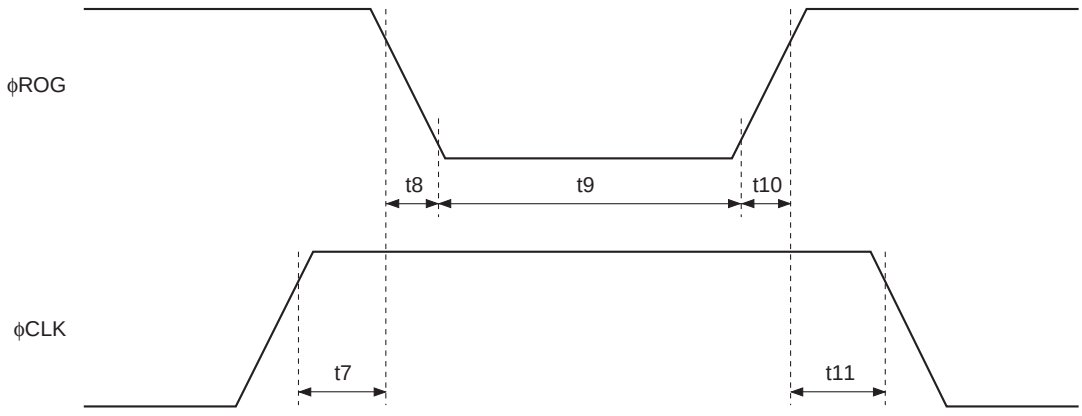
Fig. 2. φCLK, VOUT Timing



Item	Symbol	Min.	Typ.	Max.	Unit
φCLK pulse rise/fall time	t1, t2	0	10	—	ns
φCLK pulse duty *1	—	40	50	60	%
φCLK – VOUT 1	t5	50	80	110	ns
φCLK – VOUT 2	t6	30	75	120	ns

*1 $100 \times t3/(t3 + t4)$

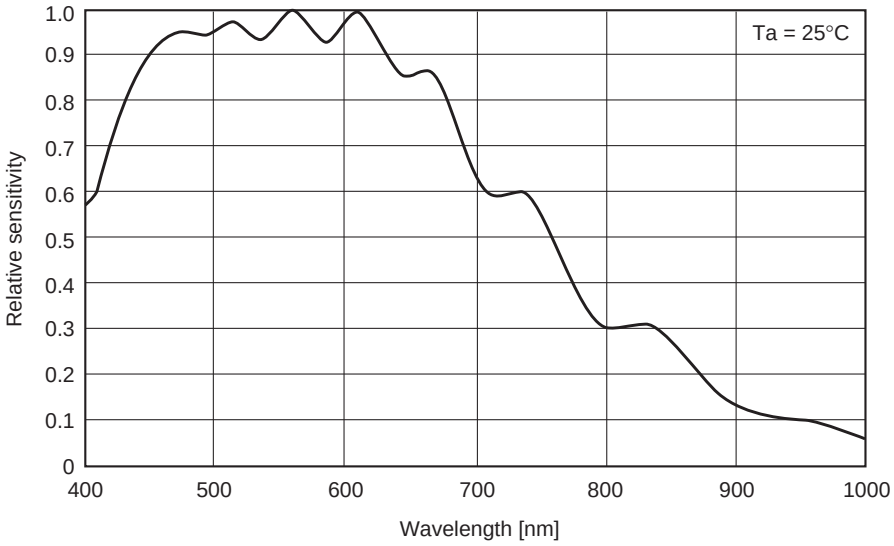
Fig. 3. φROG, φCLK Timing



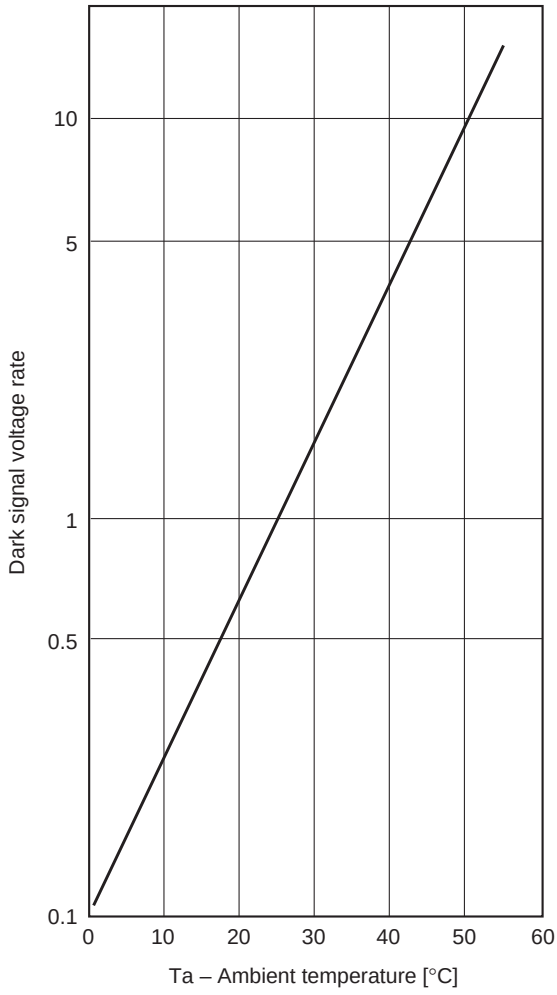
Item	Symbol	Min.	Typ.	Max.	Unit
φROG, φCLK pulse timing	t7, t11	500	1000	—	ns
φROG pulse rise/fall time	t8, t10	0	10	—	ns
φROG pulse period	t9	500	1000	—	ns

Example of Representative Characteristics

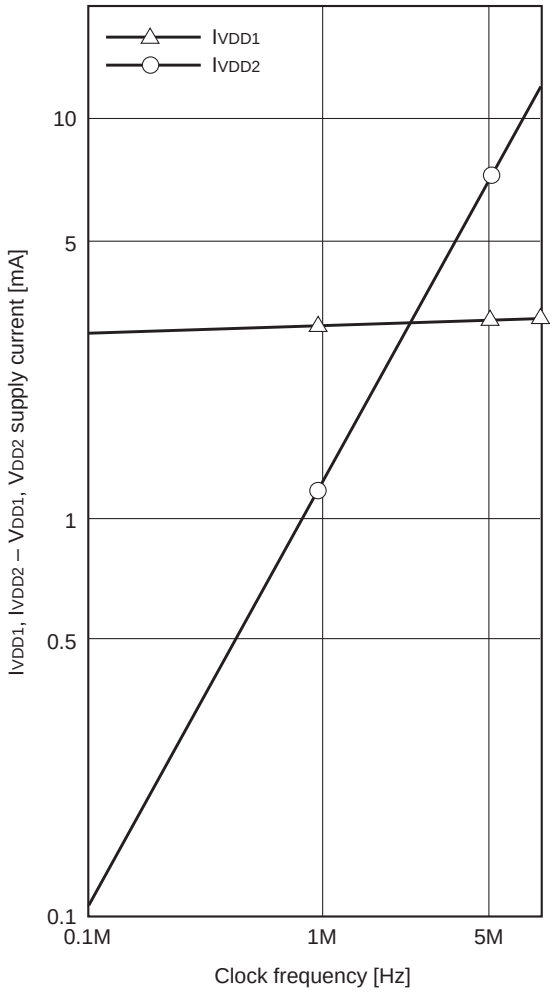
Spectral sensitivity characteristics (Standard characteristics)



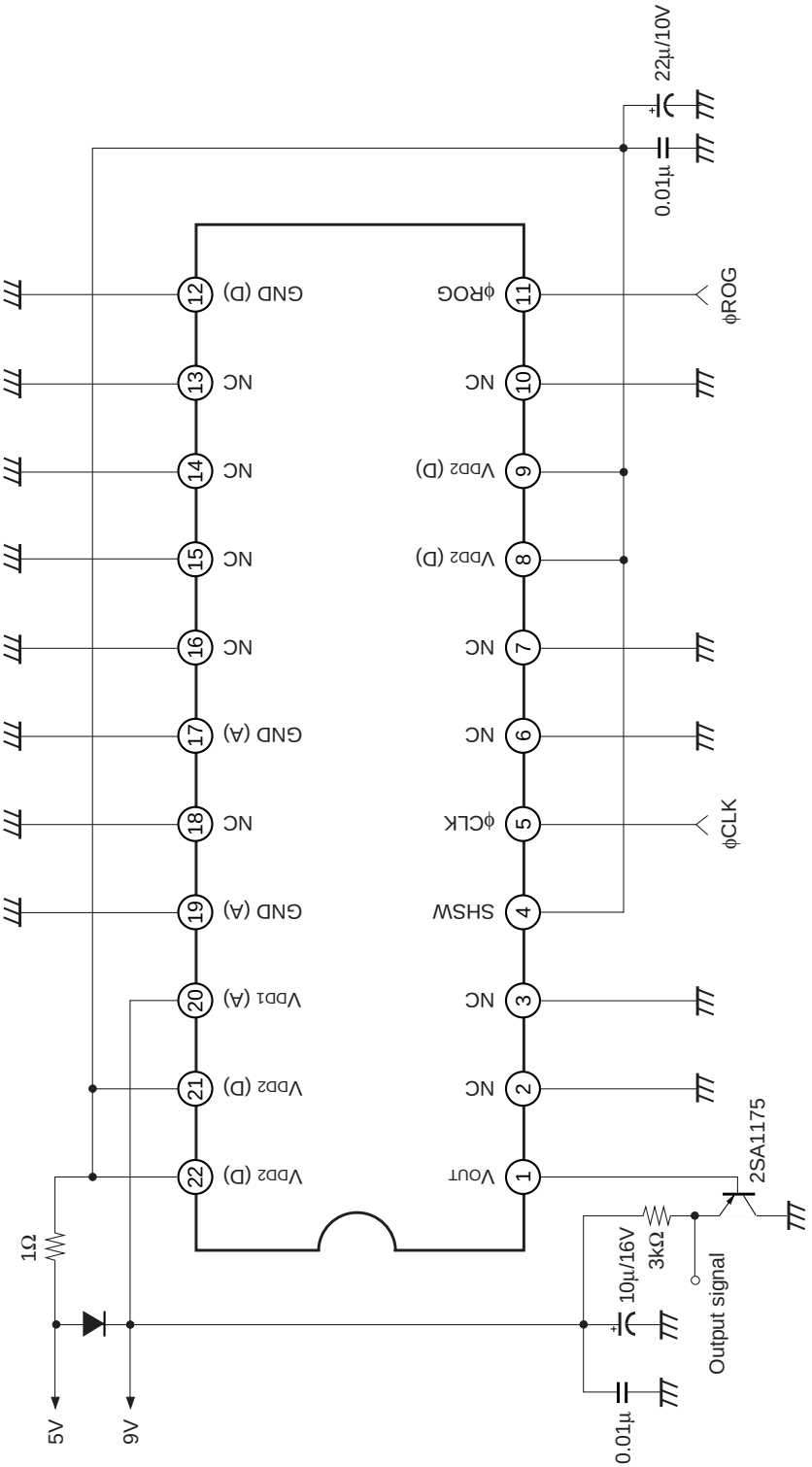
Dark signal voltage rate vs. Ambient temperature (Standard characteristics)



V_{DD1}, V_{DD2} supply current vs. Clock frequency (Standard characteristics)



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes of Handling

1) Static charge prevention

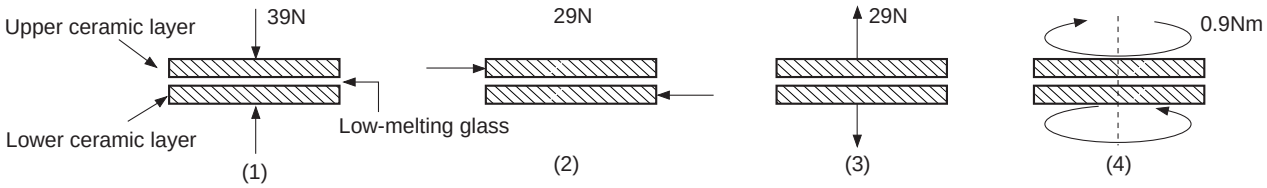
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

2) Notes on Handling CCD Cer-DIP Packages

The following points should be observed when handling and installing cer DIP packages.

a) Remain within the following limits when applying static load to the ceramic portion of the package:
   (1) Compressive strength: 39N/surface
   (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)
   (2) Shearing strength: 29N/surface
   (3) Tensile strength: 29N/surface
   (4) Torsional strength: 0.9Nm



b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.
c) Be aware that any of the following can cause the glass to crack: because the upper and lower ceramic layers are shielded by low-melting glass,
   (1) Applying repetitive bending stress to the external leads.
   (2) Applying heat to the external leads for an extended period of time with soldering iron.
   (3) Rapid cooling or heating.
   (4) Rapid cooling or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.
   (5) Prying the upper or lower ceramic layers away at a support point of the low-melting glass.

   Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

3) Soldering

a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less then 2 seconds. For repairs and remount, cool sufficiently.
c) To dismount an imaging device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

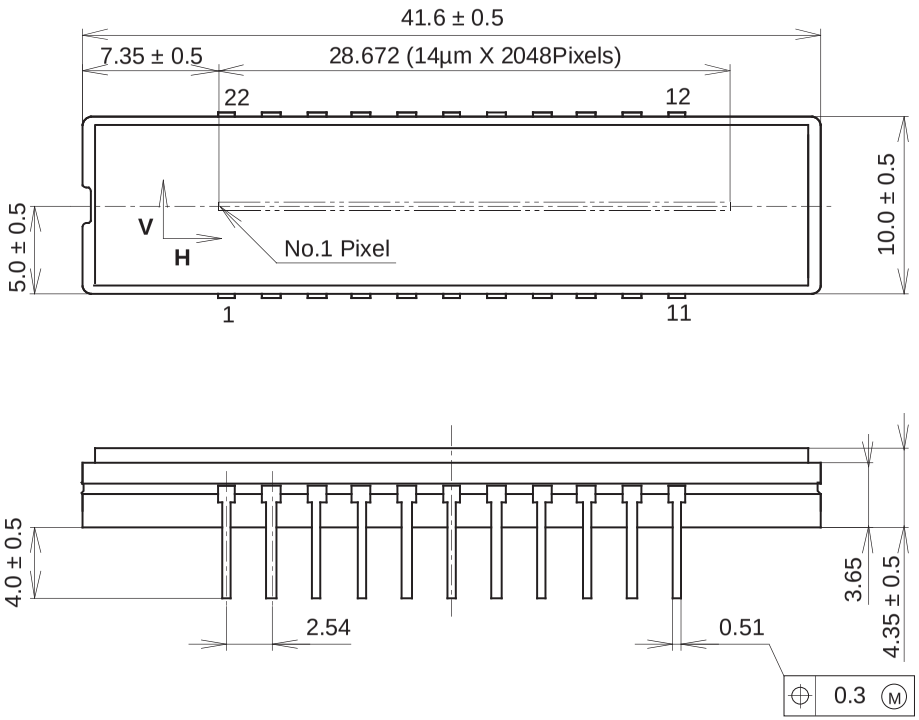
4) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

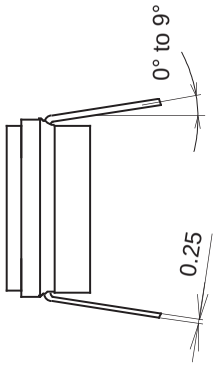
5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

Package Outline Unit: mm

22pin DIP (400mil)





1. The height from the bottom to the sensor surface is 2.45 ± 0.3mm.
2. The thickness of the cover glass is 0.7mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	5.20g
DRAWING NUMBER	LS-A18-01(E)