MN838896

1. Type

CMOS LSI source driver for color TFT LCD panels

2. Overview

This LSI converts the digital display data from a personal computer, portable device, or other source into analog signals for driving a color TFT LCD panel.

3. Features

(1) Power saving driver
(2) Built in DA converter accepting 6-bit digital input (for 262,144 colors)
(3) Choice of 408, 396, 372, and 360 drive outputs
(4) Input data bus at pixel level
(5) Choice of output data format: gray scale or binary
(6) Thirteen reference voltage inputs for producing 10 segment gamma adjustment graph.
(7) Set output voltage inflection points at data values 00, 01, 07, 0F, 17, 1F, 27, 2F, 37, 3E, and 3F.
(8) Prechargeless drive circuits
(9) Support for serial cascade connections
(10) Automatic internal clock stop after fixed number of data inputs
(11) Choice of shift register shift direction: right or left
(12) Gray scale data inversion available every clock cycle
(13) Low voltage operation: 1.8 V (typ.) for logic circuits; 3.5 V (typ.) for analog circuits
(14) Maximum operating clock frequency: 10 MHz
(15) Power save function for cutting off current to outputs, fixing them at high impedance
(16) Switching of gamma adjustment resistors for binary output, high impedance output, etc.

4. Internal Block Diagram

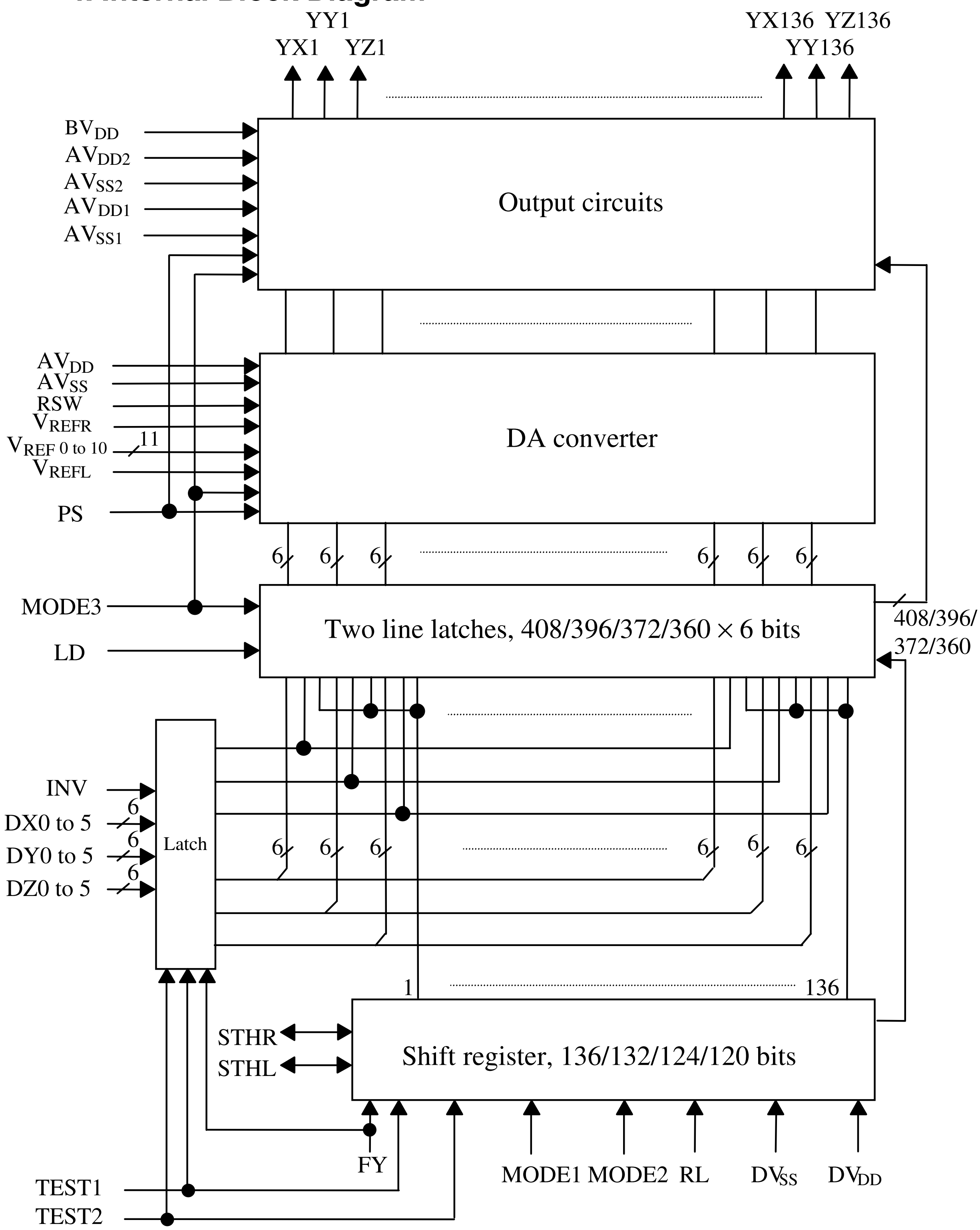


Figure 4.1 Block Diagram

5. Pin Descriptions

Table 5.1 Pin Descriptions

<table>
<tr><th>Pin Name</th><th>I/O Direction</th><th>Pin Function</th><th>Description</th></tr>
<tr><td>DX0 to 5,
DY0 to 5,
DZ0 to 5</td><td>Input</td><td>Digital data input pins, gray scale or binary format (DX5, DY5, DZ5)</td><td>The MODE3 input level specifies the format:
Low level for gray scale (RGB);
High level for binary.
For gray scale input, DX5, DY5, and DZ5 represent the MSB; DX0, DY0, and DZ0, the LSB.
Binary input uses only DX5, DY5, and DZ5.
Always drive the unused pins (DX4 to DX0, DY4 to DY0, and DZ4 to DZ0) at either High or Low level, however.
The data logic when the INV input is at Low level is AVDD for Low level and AVSS for High level.
Driving INV at High level reverses the data logic.</td></tr>
<tr><td>YX1 to 136,
YY1 to 136,
YZ1 to 136</td><td>Output</td><td>Analog image output pins</td><td>These signals drive the LCD panel.</td></tr>
<tr><td>STH R, STHL</td><td>I/O</td><td>Start pulse I/O pins</td><td>These I/O pins are for the internal shift register's start pulses.
The following table indicates data shift direction by start pulses during face up.
<table>
<tr><th></th><th>RL = H</th><th>RL = L</th></tr>
<tr><td>STHR</td><td>Right shift input</td><td>Left shift output</td></tr>
<tr><td>STHL</td><td>Right shift output</td><td>Left shift input</td></tr>
</table></td></tr>
<tr><td>RL</td><td>Input</td><td>Shift direction input pin</td><td>This specifies the shift direction: High level for right; Low level for left.
H: Right shift input (YX,YY,YZ1 → 136)
L: Left shift input (YX,YY,YZ136 → 1)</td></tr>
<tr><td>FY</td><td>Input</td><td>Shift clock input pin</td><td>This accepts the transfer clock for the shift register</td></tr>
<tr><td>LD</td><td>Input</td><td>Data load input pin</td><td>High level input enables transfer, synchronized with rising edges in the FY signal, of the LCD drive data from the built-in DA converter.</td></tr>
<tr><td>INV</td><td>Input</td><td>Data inversion control input pin</td><td>High level input reverses the logic for data input. This signal can be switched anywhere except the latch signal, rising edges in the FY signal.</td></tr>
<tr><td>MODE1, 2</td><td>Input</td><td>Number of drive outputs select pin</td><td>These specify the number of LCD panel drive outputs.
<table>
<tr><th>MODE1</th><th>MODE2</th><th>Number of drive outputs</th><th>Unused pins</th></tr>
<tr><td>High</td><td>High</td><td>408</td><td>None</td></tr>
<tr><td>High</td><td>Low</td><td>396</td><td>YX67 to YX70
YY67 to YY70
YZ67 to YZ70</td></tr>
<tr><td>Low</td><td>High</td><td>372</td><td>YX63 to YX74
YY63 to YY74
YZ63 to YZ74</td></tr>
<tr><td>Low</td><td>Low</td><td>360</td><td>YX61 to YX76
YY61 to YY76
YZ61 to YZ76</td></tr>
</table>
*Unused pins have high-impedance output</td></tr>
<tr><td>MODE3</td><td>Input</td><td>Input format select pin</td><td>This specifies the data input format: gray scale or binary.
High level: Binary. DX5, DY5, and DZ5 only. The DA converter is off.
Low level: Gray scale. DX5 to DX0, DY5 to DY0, and DZ5 to DZ0. The DA converter is on.</td></tr>
</table>

Pin Name	I/O Direction	Pin Function	Description
RSW	Input	Gamma adjustment resistor select control	This controls the use of gamma adjustment resistors. Note that switching need not be synchronized with the FY signal. Low level: Enable (gray scale output) High level: Disable (binary output, , high-impedance output, etc.) Enable the use of these resistors at least five H clock cycles before switching to gray scale output.
PS	Input	Power save function select pin	High level input at a rising edge in the FY signal cuts off current to outputs, fixing them at high-impedance. High level: High-impedance outputs. No current to operational amplifier or other components. Low level: Normal operation
TEST1 TEST2	Input	TEST input pins	Normally fix these inputs both at Low level. Low level: Normal operation High level: Test mode TEST1 / TEST2 / Operating Mode: Low / Low / Normal operation Low / High / Switch gamma adjustment resistors OFF when the PS pin input is at High level High / X / Boost image output drive power
$V_{REF0 \text{ to } 10, R, L}$	Input	Gamma adjustment potential input pin	This input is the gamma adjustment potential input pin for the DA converter.
AV_{DD}	Input	Analog power supply	This is the power supply for the DA converter's analog circuits.
AV_{SS}	Input	Analog ground	
AV_{DD1}	Input	Analog power supply	This is the power supply for the output analog circuits.
AV_{SS1}	Input	Analog ground Ground for analog circuits and binary drive signals	This is the ground for the output analog circuits and the binary drive circuits.
AV_{DD2}	Input	Analog power supply	This is the power supply for the circuits protecting the output circuits.
AV_{SS2}	Input	Analog ground	
BV_{DD}	Input	Binary drive power supply	This is the power supply for the binary drive output signals.
DV_{DD}	Input	Digital power supply	This is the power supply for the digital circuits.
DV_{SS}	Input	Digital ground	
COM1 to 4	—	Through connections	These provide straight connections to the corresponding output pins. They are not connected to other circuits.
DUMMY	—	Dummy pins	These are dummies. They are not connected to other circuits.

6. Description of Operation

6.1 Functional Description

The MODE3 pin offers a choice of 6-bit gray scale data or 1-bit binary data. The MODE1 and MODE2 pins specify the number of outputs.
The following Table summarizes the effects of MODE3 and RL input levels on I/O pins when both MODE1 and MODE2 are at High level (408 outputs).

Table 6.1 MODE3 and RL Settings (MODE1 = MODE2 = High Level)

MODE3	RL	Input pins	Data transfer direction	Data Output format
			FX : 1 - 2 - 3 - ··· - 68 - 69 - ··· - 134 - 135 - 136	
Low level (gray scale input)	H	DX0 - 5	YX1 - YX2 - YX3 - ··· - YX68 - YX69 - ··· - YX134 - YX135 - YX136	64-level analog outputs
		DY0 - 5	YY1 - YY2 - YY3 - ··· - YY68 - YY69 - ··· - YY134 - YY135 - YY136	
		DZ0 - 5	YZ1 - YZ2 - YZ3 - ··· - YZ68 - YZ69 - ··· - YZ134 - YZ135 - YZ136	
	L	DX0 - 5	YX136 - YX135 - YX134 - ··· - YX69 - YX68 - ··· - YX3 - YX2 - YX1	
		DY0 - 5	YY136 - YY135 - YY134 - ··· - YY69 - YY68 - ··· - YY3 - YY2 - YY1	
		DZ0 - 5	YZ136 - YZ135 - YX134 - ··· - YZ69 - YZ68 - ··· - YZ3 - YZ2 - YZ1	
High level (binary input)	H	DX5	YX1 - YX2 - YX3 - ··· - YX68 - YX69 - ··· - YX134 - YX135 - YX136	Binary digital outputs
		DY5	YY1 - YY2 - YY3 - ··· - YY68 - YY69 - ··· - YY134 - YY135 - YY136	
		DZ5	YZ1 - YZ2 - YZ3 - ··· - YZ68 - YZ69 - ··· - YZ134 - YZ135 - YZ136	
	L	DX5	YX136 - YX135 - YX134 - ··· - YX69 - YX68 - ··· - YX3 - YX2 - YX1	
		DY5	YY136 - YY135 - YY134 - ··· - YY69 - YY68 - ··· - YY3 - YY2 - YY1	
		DZ5	YZ136 - YZ135 - YX134 - ··· - YZ69 - YZ68 - ··· - YZ3 - YZ2 - YZ1	

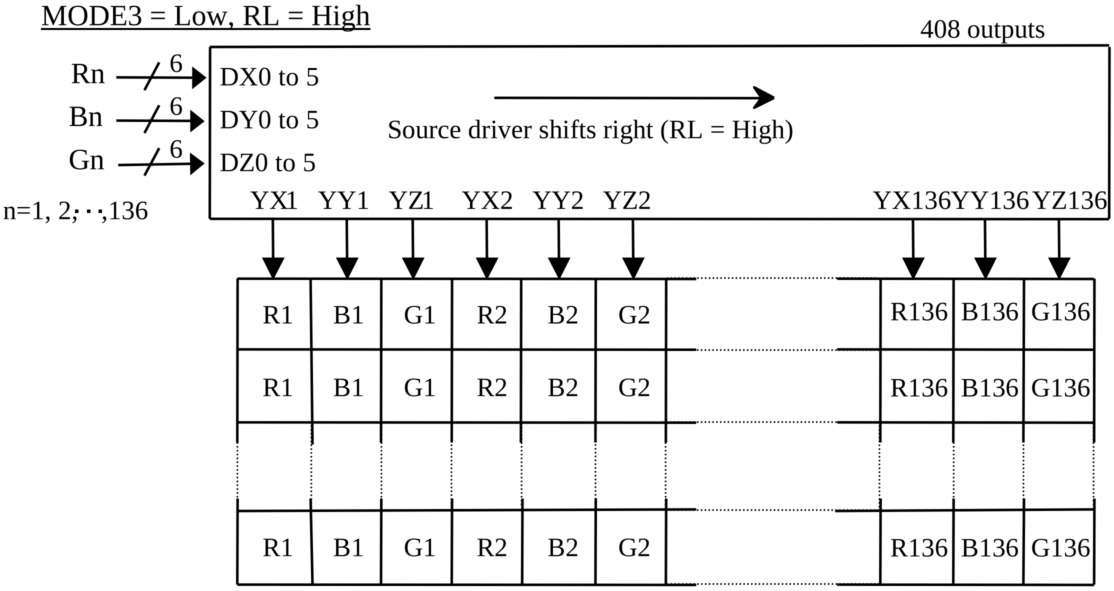
The following unused pins have high-impedance output.
396 outputs: YX67 - YX70, YY67 - YY70, and YZ67 - YZ70
372 outputs: YX63 - YX74, YY63 - YY74, and YZ63 - YZ74
360 outputs: YX61 - YX76, YY61 - YY76, and YZ61 - YZ76

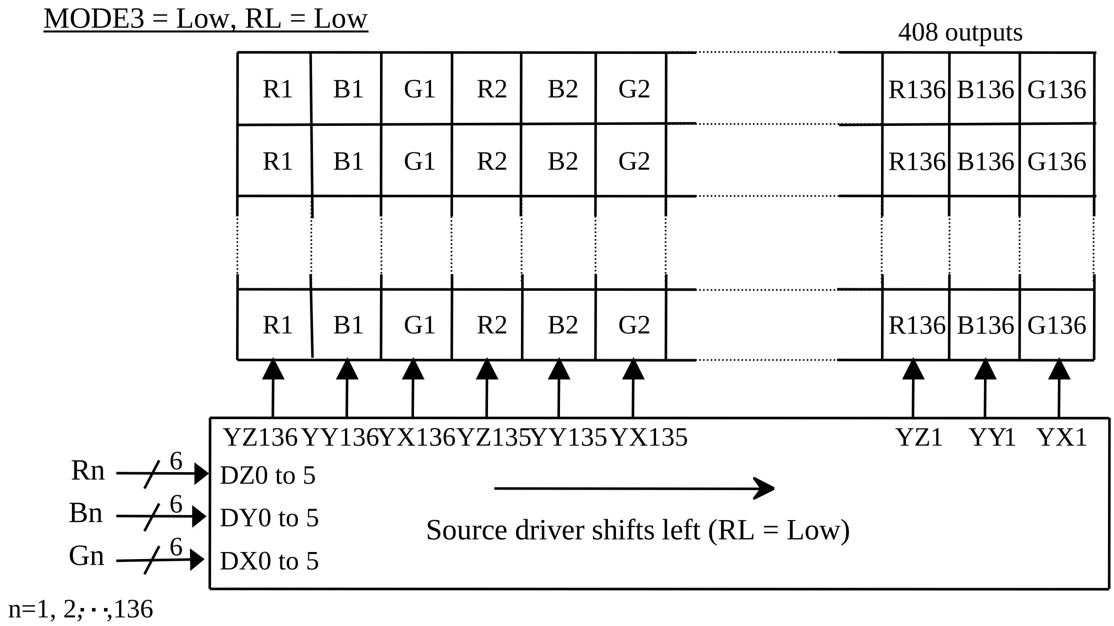
6.2 Relationships Between Data Input and Output Pins

(1) Gray scale data input (MODE3 = Low)

The following summarizes the relationships between data input and output pins for gray scale data input (MODE3 = Low).

So, binary data input is naturally ignored during gray scale data input.





(2) Binary input (MODE3 = High)

Binary input uses only the pins DX5, DY5, and DZ5. The relationships between data input and output pins are otherwise the same.

So, binary data input is naturally ignored during gray scale data input.

6.3 Power Save Function

High level PS pin input at a rising edge in the FY signal cuts off current to outputs, fixing them at high-impedance.

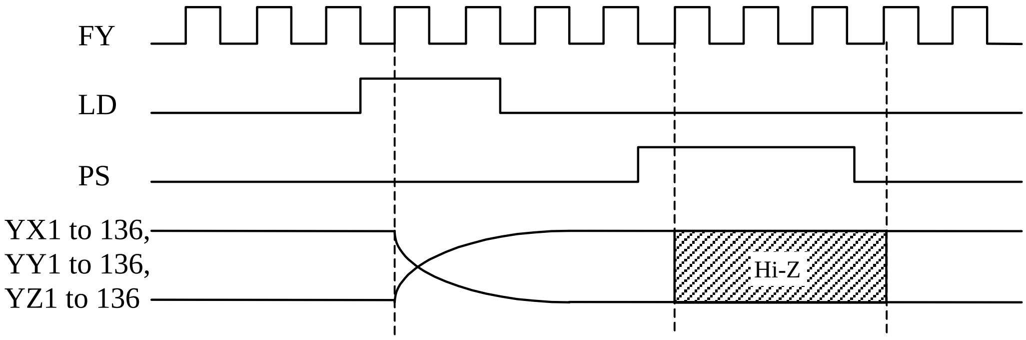


Figure 6.3 High-Impedance Output Interval

6.4 Blanking Interval

The following timing chart summarizes the relationships between the load data (LD) and start pulse (STHR and STHL) inputs and the blanking interval.

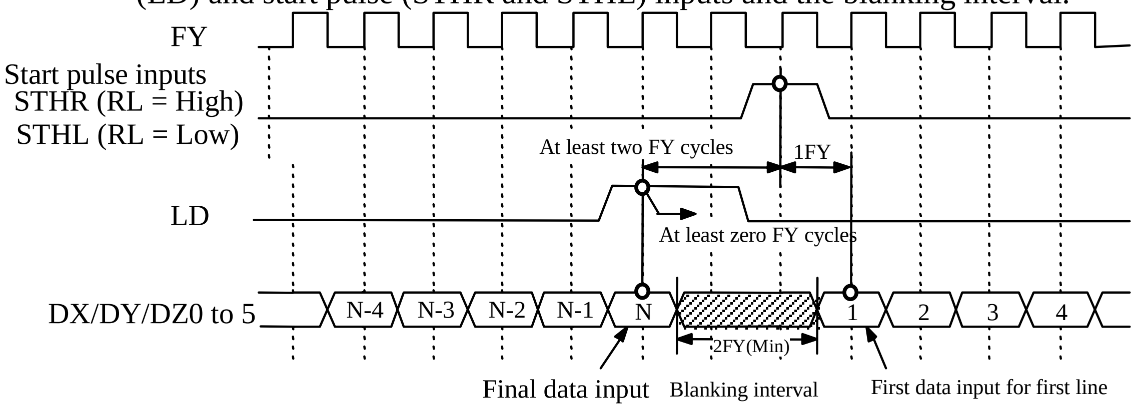


Figure 6.4 Blanking Interval

6.5 Data Inverse Function

Driving the INV input at High level inverts all bits in the data input.

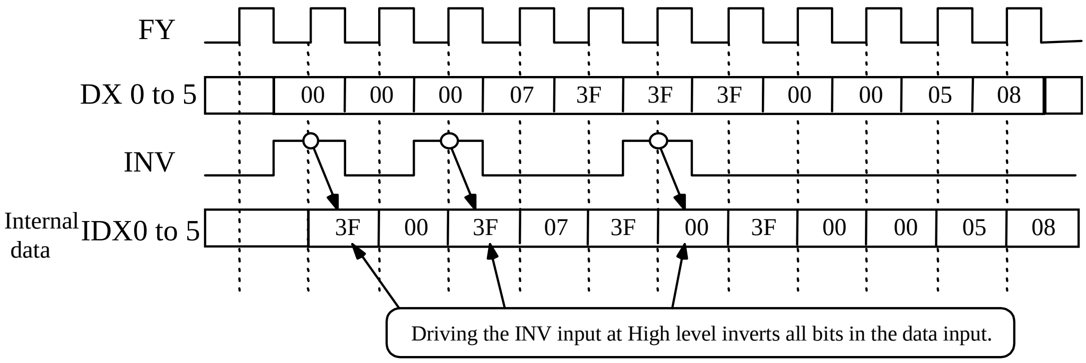


Figure 6.5 Data Inverse Function

6.6 Switching Input Formats

The following timing chart summarizes the relationships between changes in input format and the subsequent changes in output.

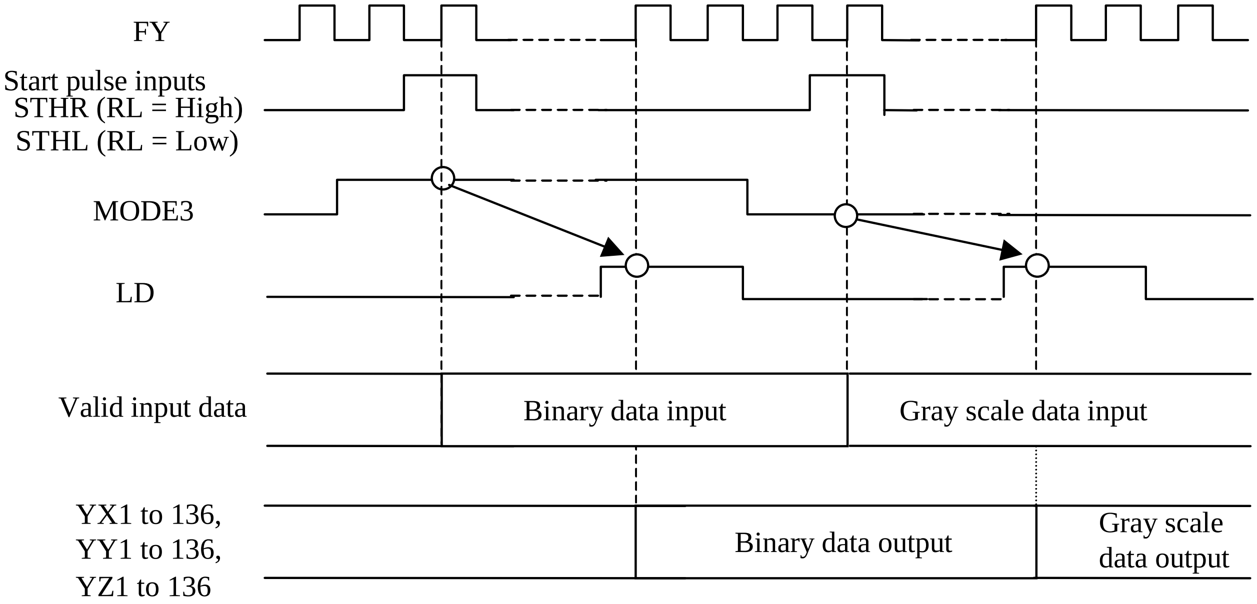


Figure 6.6.1 Switching Formats (1/2)

The LSI drives the output pins at high-impedance for one FY cycle when changing output formats.

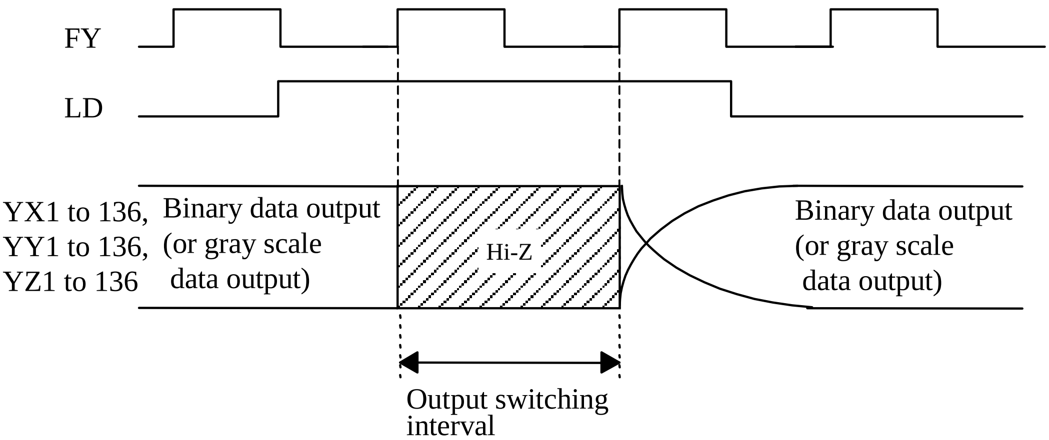


Figure 6.6.2 Switching Formats (2/2)

6.7 Cascade Connection

(1) RL = High

Driver A starts latching data one FY cycle after receiving a start pulse (STHR).
It asserts the carry signal (STHL) one FY cycle before latching the last data and then stopping.

MODE1 = MODE2 = High (408 outputs): 135 FY cycles
MODE1 = High, MODE2 = Low (396 outputs): 131 FY cycles
MODE1 = Low, MODE2 = High (372 outputs): 123 FY cycles
MODE1 = MODE2 = High (360 outputs): 119 FY cycles

Cascade Connection

Driver B starts latching data one FY cycle after receiving the carry signal (STHL) from driver A.

Note: Although the carry signal (STHL) pulses are two FY cycles long, only the first cycle counts.
The next driver treats the two cycles as a single pulse.

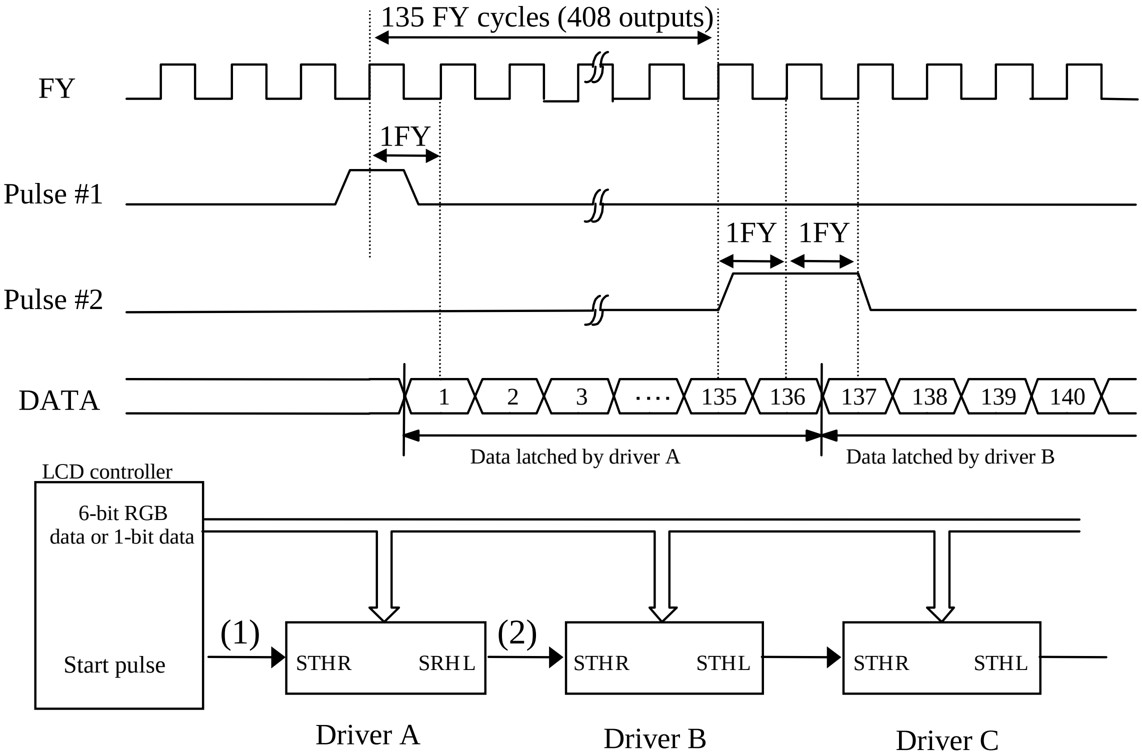


Figure 6.7 Serial Cascade Connection

(2) RL = Low

The start pulse input is from STHL; the carry output, from STHR. Apart from that, operation is the same as for RL = High.

6.8 Relationship between Input Data and Output Voltage

6.8.1 Built-In Gamma Adjustment Resistors

The output voltage depends on the input data and thirteen gamma adjustment voltages ($V_{REF\ x}$, x = H, 0 to 10, L). See graph and conversion table on the next two pages.

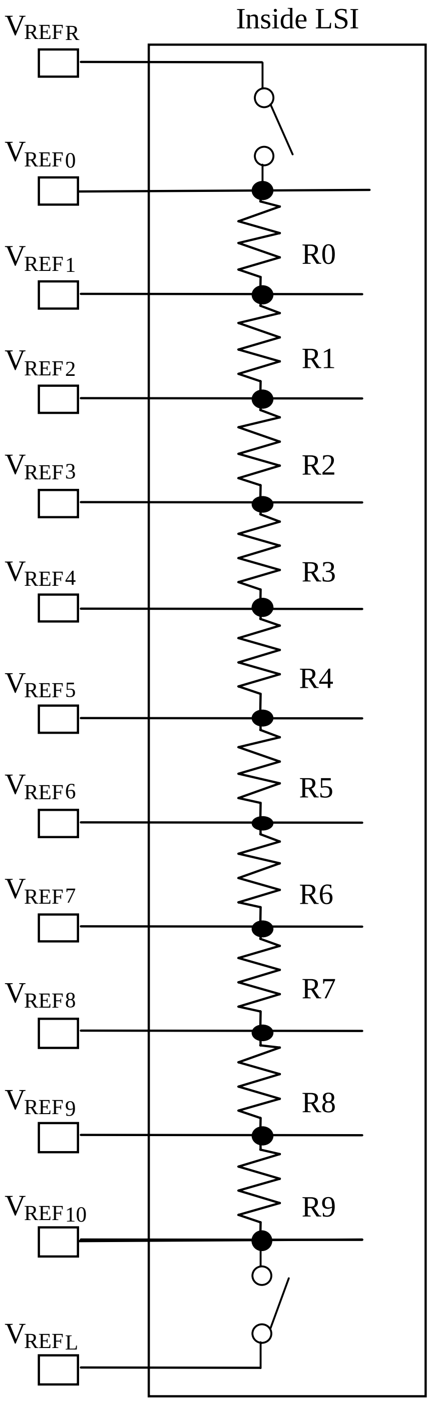


Figure 6.8.1
Built-In Gamma Adjustment Resistors

The LSI contains ten divider resistances and two switches between $V_{REG\ H}$ and $V_{REG\ L}$. Table 6.8 summarizes the formulas for calculating the output voltages from the voltages applied to pins $V_{REF\ x}$, x = 0 to 10. Applying voltages only to $V_{REG\ H}$ and $V_{REG\ L}$ produces the default graph shown in Figure 6.8.2.
Note that we recommend the use of an operational amplifier or similar means to guarantee low-impedance input to the V_{REG} pins.
The RSW pin input controls the two switches between $V_{REG\ H}$ and $V_{REG\ L}$, allowing the user application system to conserve power by cutting the current flowing between the two pins.

(Note 1)

The adjustment voltages ($V_{REF\ x}$, x = H, 0 to 10, L) must satisfy one of the following two relationships.

$$AV_{DD} > V_{REFR} \geq V_{REF0} \geq V_{REF1} \geq \cdots\cdots \geq V_{REF10} \geq V_{REFL} > AV_{SS}$$

or

$$AV_{DD} > V_{REFL} \geq V_{REF10} \geq V_{REF9} \geq \cdots\cdots \geq V_{REF0} \geq V_{REFR} > AV_{SS}$$

Do not change these voltages while the chip is in operation.

The following are the values for the internal resistances R0 to R9.

Gamma Adjustment Resistances

R0	0.00
R1	1.02
R2	0.83
R3	0.66
R4	0.51
R5	0.51
R6	0.64
R7	0.80
R8	1.00
R9	0.14

6.8.2 Relationship between Input Data and Output Voltage

The following Figure gives the gamma adjustment curve for INV = Low.

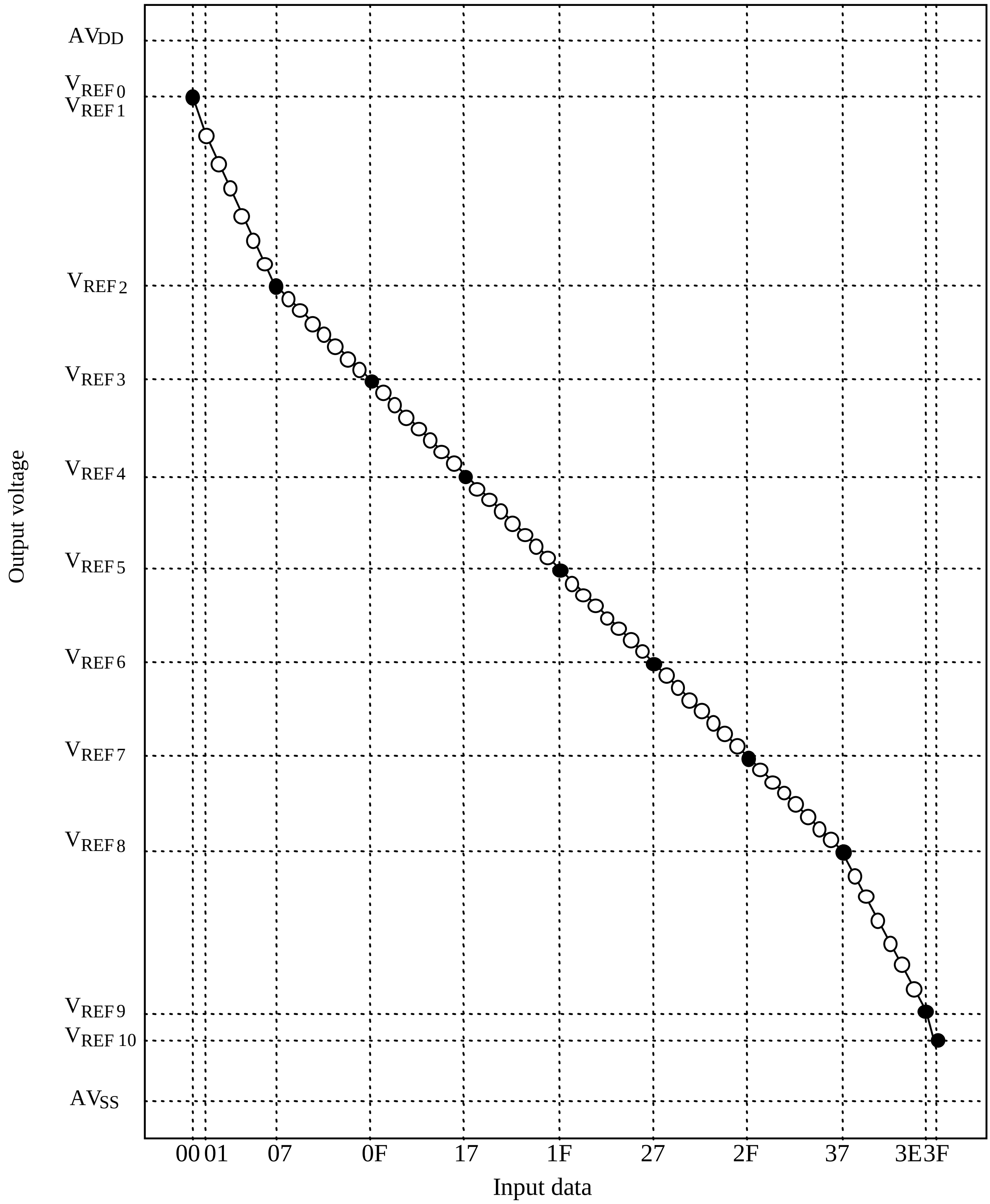


Figure 6.8.2 Relationship between Input Data and Output Voltage

($AV_{DD} > V_{REFR} \geq V_{REF0} \geq V_{REF1} \geq \ldots \ldots \geq V_{REF10} \geq V_{REFL} > AV_{SS}$)

6.8.3 Relationship between Reference Voltages and Output Voltages

The following Table gives the formulas for converting input data for INV = Low.

Table 6.8 Relationship between Reference Voltages and Output Voltages

($AV_{DD} > V_{REFR} \geq V_{REF0} \geq V_{REF1} \geq \ldots \ldots \geq V_{REF10} \geq V_{REFL} > AV_{SS}$)

Input data	Formula for calculating output voltage	Input data	Formula for calculating output voltage
00h	V_{REF0}	20h	V_{REF6} + (V_{REF5} to V_{REF6}) × 7/8
01h	V_{REF2} + (V_{REF1} to V_{REF2}) × 6/7	21h	V_{REF6} + (V_{REF5} to V_{REF6}) × 6/8
02h	V_{REF2} + (V_{REF1} to V_{REF2}) × 5/7	22h	V_{REF6} + (V_{REF5} to V_{REF6}) × 5/8
03h	V_{REF2} + (V_{REF1} to V_{REF2}) × 4/7	23h	V_{REF6} + (V_{REF5} to V_{REF6}) × 4/8
04h	V_{REF2} + (V_{REF1} to V_{REF2}) × 3/7	24h	V_{REF6} + (V_{REF5} to V_{REF6}) × 3/8
05h	V_{REF2} + (V_{REF1} to V_{REF2}) × 2/7	25h	V_{REF6} + (V_{REF5} to V_{REF6}) × 2/8
06h	V_{REF2} + (V_{REF1} to V_{REF2}) × 1/7	26h	V_{REF6} + (V_{REF5} to V_{REF6}) × 1/8
07h	V_{REF2}	27h	V_{REF6}
08h	V_{REF3} + (V_{REF2} to V_{REF3}) × 7/8	28h	V_{REF7} + (V_{REF6} to V_{REF7}) × 7/8
09h	V_{REF3} + (V_{REF2} to V_{REF3}) × 6/8	29h	V_{REF7} + (V_{REF6} to V_{REF7}) × 6/8
0Ah	V_{REF3} + (V_{REF2} to V_{REF3}) × 5/8	2Ah	V_{REF7} + (V_{REF6} to V_{REF7}) × 5/8
0Bh	V_{REF3} + (V_{REF2} to V_{REF3}) × 4/8	2Bh	V_{REF7} + (V_{REF6} to V_{REF7}) × 4/8
0Ch	V_{REF3} + (V_{REF2} to V_{REF3}) × 3/8	2Ch	V_{REF7} + (V_{REF6} to V_{REF7}) × 3/8
0Dh	V_{REF3} + (V_{REF2} to V_{REF3}) × 2/8	2Dh	V_{REF7} + (V_{REF6} to V_{REF7}) × 2/8
0Eh	V_{REF3} + (V_{REF2} to V_{REF3}) × 1/8	2Eh	V_{REF7} + (V_{REF6} to V_{REF7}) × 1/8
0Fh	V_{REF3}	2Fh	V_{REF7}
10h	V_{REF4} + (V_{REF3} to V_{REF4}) × 7/8	30h	V_{REF8} + (V_{REF7} to V_{REF8}) × 7/8
11h	V_{REF4} + (V_{REF3} to V_{REF4}) × 6/8	31h	V_{REF8} + (V_{REF7} to V_{REF8}) × 6/8
12h	V_{REF4} + (V_{REF3} to V_{REF4}) × 5/8	32h	V_{REF8} + (V_{REF7} to V_{REF8}) × 5/8
13h	V_{REF4} + (V_{REF3} to V_{REF4}) × 4/8	33h	V_{REF8} + (V_{REF7} to V_{REF8}) × 4/8
14h	V_{REF4} + (V_{REF3} to V_{REF4}) × 3/8	34h	V_{REF8} + (V_{REF7} to V_{REF8}) × 3/8
15h	V_{REF4} + (V_{REF3} to V_{REF4}) × 2/8	35h	V_{REF8} + (V_{REF7} to V_{REF8}) × 2/8
16h	V_{REF4} + (V_{REF3} to V_{REF4}) × 1/8	36h	V_{REF8} + (V_{REF7} to V_{REF8}) × 1/8
17h	V_{REF4}	37h	V_{REF8}
18h	V_{REF5} + (V_{REF4} to V_{REF5}) × 7/8	38h	V_{REF9} + (V_{REF8} to V_{REF9}) × 6/7
19h	V_{REF5} + (V_{REF4} to V_{REF5}) × 6/8	39h	V_{REF9} + (V_{REF8} to V_{REF9}) × 5/7
1Ah	V_{REF5} + (V_{REF4} to V_{REF5}) × 5/8	3Ah	V_{REF9} + (V_{REF8} to V_{REF9}) × 4/7
1Bh	V_{REF5} + (V_{REF4} to V_{REF5}) × 4/8	3Bh	V_{REF9} + (V_{REF8} to V_{REF9}) × 3/7
1Ch	V_{REF5} + (V_{REF4} to V_{REF5}) × 3/8	3Ch	V_{REF9} + (V_{REF8} to V_{REF9}) × 2/7
1Dh	V_{REF5} + (V_{REF4} to V_{REF5}) × 2/8	3Dh	V_{REF9} + (V_{REF8} to V_{REF9}) × 1/7
1Eh	V_{REF5} + (V_{REF4} to V_{REF5}) × 1/8	3Eh	V_{REF9}
1Fh	V_{REF5}	3Fh	V_{REF10}

7. Product Standards

A. Absolute Maximum Ratings

$AV_{SS} = DV_{SS} = 0V$

	Item	Symbol	Rating	Unit
A1	Digital power supply voltage	DV_{DD}	- 0.3 to 6.5	V
A2	Analog power supply voltage	AV_{DD}	- 0.3 to 6.5	V
A3	Binary drive power supply voltage	BV_{DD}	- 0.3 to AV_{DD}	V
A4	Digital input voltage	V_{I1}	- 0.3 to DV_{DD} +0.3	V
A5	Analog input voltage	V_{I2}	- 0.3 to AV_{DD} +0.3	V
A6	Digital output voltage	V_{O1}	- 0.3 to DV_{DD} +0.3	V
A7	Analog output voltage	V_{O2}	- 0.3 to AV_{DD} +0.3	V
A8	Operating storage temperature	T_{opr}	- 30 to +85	°C
A9	Operating ambient temperature	T_a	- 20 to +75	°C
A10	Storage temperature	T_{stg}	- 40 to +125	°C

Note: The above absolute maximum ratings represent limits for avoiding damage to the product. They do not guarantee operation.

· The above standards apply only to our standard package for the product.

B. Operating Conditions

Ta = - 20 °C to +75 °C $AV_{SS} = DV_{SS} = 0V$

	Item	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
B1	Digital power supply voltage	DV_{DD}		1.65	1.8	3.6	V
B2	Analog power supply voltage	AV_{DD}		3.0	3.5	5.5	V
B3	Binary drive power supply voltage	BV_{DD}		2.6	3.5	AV_{DD}	V
B4	Gamma adjustment reference voltages	$V_{REFR, L, 0 \text{ to } 10}$		0.1		AV_{DD} - 0.1	V
B5	Operating frequency	f_{FY}				10	MHz
B6	Drive load capacity	C_Y				50	pF
B7	Digital signal input capacity	C_{IN}	1 MHz		7	15	pF

Notes

(1) Use only direct connections to power supply pins sharing the same symbol (AV_{DD}, DV_{DD}, and BV_{DD}).

(2) Use only direct connections to ground pins sharing the same symbol (AV_{SS} and DV_{SS}).

(3) Apply voltages in the following order: DV_{DD} pins, logic input pins, AV_{DD} pins, BV_{DD} pins, and $V_{REF\ x}$. Remove them in the reverse order.

(4) Make sure that the following relationship applies at all times.

· The above standards apply only to our standard package for the product.

C. Electrical Characteristics

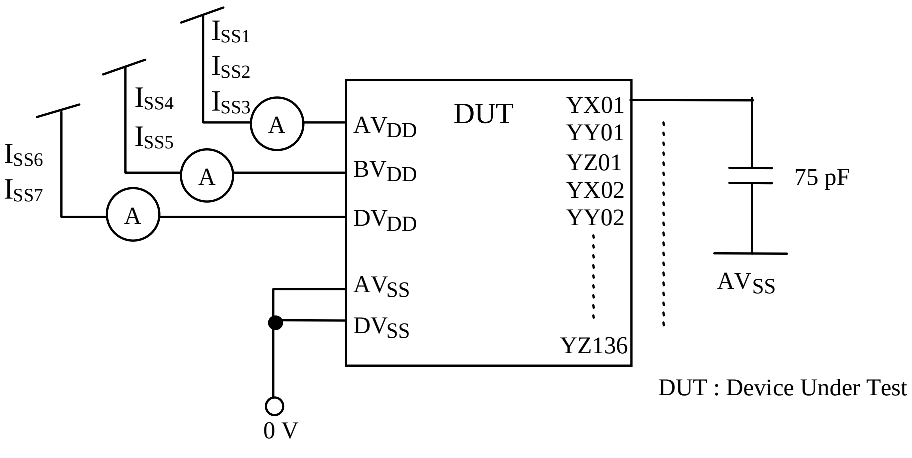
(1) DC Characteristics

DV_{DD} = 1.8V, AV_{DD} = BV_{DD} = 3.5V, AV_{SS} = DV_{SS} = 0 V, Ta = 25 °C

	Item	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C1	Analog operation power supply current (1)	I_{SS1}	Notes 6 and 7		1.8	4.5	mA
C2	Analog operation power supply current (2)	I_{SS2}	The above, without loads Notes 9		0.8		mA
C3	Analog standby power supply current	I_{SS3}	PS = High			5	µA
C4	Binary drive operation power supply voltage	I_{SS4}	Notes 6 and 7		1.1	3.0	mA
C5	Binary drive standby power supply current	I_{SS5}	Clock signal off			5	µA
C6	Digital operation power supply voltage	I_{SS6}	Notes 5 and 6		0.1	1.0	mA
C7	Digital standby power supply current	I_{SS7}	Clock signal off			5	µA

(5) Typical conditions
FY frequency of 10 MHz, raster period of 50 µs, data pattern alternating between 00 and 3F every raster period, fixed $V_{REF\ x}$

(6) Maximum conditions
FY frequency of 10 MHz, raster period of 50 µs, data pattern alternating between 00 and 3F every raster period, fixed $V_{REF\ x}$



(7) The loads on the analog output pins are as shown. Note that the numbers for those load circuits sometimes change.

(8) The following is the formula for calculating the power consumption with the loads described in note 6 above.
$I_{SS1} \times AV_{DD} + I_{SS6} \times DV_{DD}$ (consumption by gamma adjustment resistors not included)

(9) This value is for reference only. It is not guaranteed.
The above standards apply only to our standard package for the product.

· The above standards apply only to our standard package for the product.

DV_{DD} = 1.8V, AV_{DD} = BV_{DD} = 3.5V, AV_{SS} = DV_{SS} = 0 V, Ta = 25 °C

Item		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1) Input pins (RL, LD, DX0 to 5, DY0 to 5, DZ0 to 5, FY, INV, PS, MODE1 to 3, RSW)							
C6	High level input	V_{IH1}		0.8 × DV_{DD}		DV_{DD}	V
C7	Low level input	V_{IL1}		0		0.2 × DV_{DD}	V
C8	Input leak current	I_{LI1}		- 2		2	μA
2) I/O pins (STHR, STHL)							
C9	High level input	V_{IH2}		0.8 × DV_{DD}		DV_{DD}	V
C10	Low level input	V_{IL2}		0		0.2 × DV_{DD}	V
C11	High level output	V_{OH1}	I_O = - 1.0 mA	DV_{DD} - 0.5			V
C12	Low level output	V_{OL1}	I_O = 1.0 mA			0.5	V
C13	Input leak current	I_{LI2}		- 2		2	μA
3) Pull down pins (TEST1, TEST2)							
C14	High level input	V_{IH3}		0.8 × DV_{DD}		DV_{DD}	V
C15	Low level input	V_{IL3}		0		0.2 × DV_{DD}	V
C16	Pull down resistances	R_{PD}		140	280	560	k Ω

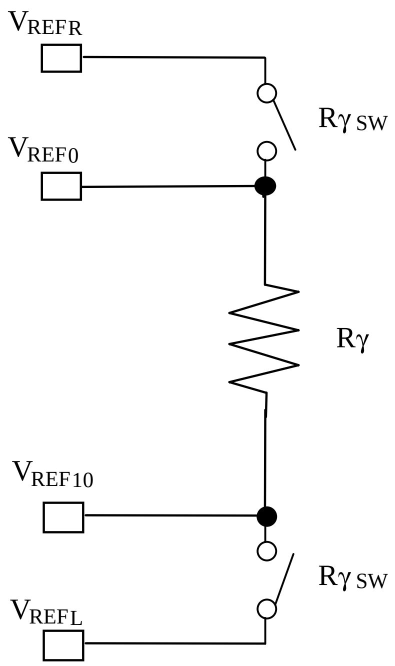
· The above standards apply only to our standard package for the product.

DV_{DD} = 1.8V, AV_{DD} = BV_{DD} = 3.5V, AV_{SS} = DV_{SS} = 0 V, Ta = 25 °C

	Item	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
(3) Gamma adjustment resistances							
C17	Total resistance	Rγ	Between $V_{REF\ 0}$ and $V_{REF\ 10}$	25	40	55	kΩ
C18	Switch resistance	$R\gamma_{SW}$	Between $V_{REF\ R}$ and $V_{REF\ 0}$, Between $V_{REF\ L}$ and $V_{REF\ 10}$	25	50	100	Ω

10) Conditions

$V_{REF\ R}$ ($V_{REF\ L}$) = 3.400 V, $V_{REF\ 0}$ ($V_{REF\ 10}$) = 3.395 V
And
$V_{REF\ R}$ ($V_{REF\ L}$) = 0.100 V, $V_{REF\ 0}$ ($V_{REF\ 10}$) = 0.105 V



· The above standards apply only to our standard package for the product.

DV_{DD} = 1.8V, AV_{DD} = BV_{DD} = 3.5V, AV_{SS} = DV_{SS} = 0 V, Ta = 25 °C

	Item	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
(4) Analog output pins (YX1 to 136, YY1 to 136, YZ1 to 136)							
C19	High level output current (gray scale output)	I_{OH1}	V_x = 3.4 V V_{OUT} = 2.4V Note 11			- 0.05	mA
C20		I_{OL1}	V_x = 0.1 V V_{OUT} = 1.1 V Note 11	0.05			mA
C21	Average output voltage deviation	ΔV_O	2.7 V ≤ V_x		± 20	± 25	mV
			0.8 V < V_x < 2.7V		± 10	± 20	
			V_x ≤ 0.8 V		± 20	± 25	
C22	Output voltage range	V_O		AV_{SS} +0.1		AV_{DD} - 0.1	V
C23	High level output current (binary output)	I_{OH2}	V_x = 3.5 V V_{OUT} = 2.5V Note 11			- 0.1	mA
C24	Low level output current (binary output)	I_{OL2}	V_x = 0.0 V V_{OUT} = 1.0 V Note 11	0.1			mA
(5) Through connection pins (COM1 to 4)							
C25	Wiring resistance	R_{COM}			7		Ω

Note: For further details on through connection pin wiring resistance, refer to the reference data attached to the delivery specifications.

11) V_X is the output voltage for the analog output pin;
V_{OUT}, the voltage applied to the pin.

· The above standards apply only to our standard package for the product.

(2) AC Characteristics

DV_{DD} = 1.8V, AV_{DD} = BV_{DD} = 3.5V, AV_{SS} = DV_{SS} = 0 V, Ta = 25 °C

	Item	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C26	FY period	t_p	Duty = 50 %	100			ns
C27	FY High level pulse width	t_{wcH}		45			ns
C28	FY Low level pulse width	t_{wcL}		45			ns
C29	Data/INV setup time	t_{st1}		20			ns
C30	Data/INV hold time	t_{hd1}		20			ns
C31	Start pulse setup time	t_{st2}		20			ns
C32	Start pulse hold time	t_{hd2}		20			ns
C33	Start pulse Low level pulse width	t_{wsL}		2			FY period
C34	Carry output delay time	t_{d1}	C_L = 15 pF			50	ns
C35	LD signal High level pulse width	wldH		2			FY period
C36	LD signal Low level pulse width	t_{wldL}		2			FY period
C37	LD signal-start pulse setup time	t_{st3}		2			FY period
C38	LD-FY setup time	t_{st4}		20			ns
C39	LD-FY hold time	t_{hd4}		20			ns
C40	MODE3 setup time	t_{st5}	Note 12)	20			ns
C41	MODE3 hold time	t_{hd5}	Note 12)	20			ns
C42	PS setup time	t_{st6}		20			ns
C43	PS hold time	t_{hd6}		20			ns
C44	Data input invalid interval	t_{ng1}		1			FY period
C45	Final data timing	t_{ng2}				1	FY period
C46	LCD drive signal delay 1	t_{d2}	C_L = 15 pF Note 13)			20	µs
C47	LCD drive signal delay 2	t_{d3}	C_L = 15 pF Note 13), Note 14)			30	µs
C48	LCD drive signal stop time	t_{d4}	C_L = 15 pF			5	µs
C49	RSW setup time	t_{st7}				280	µs

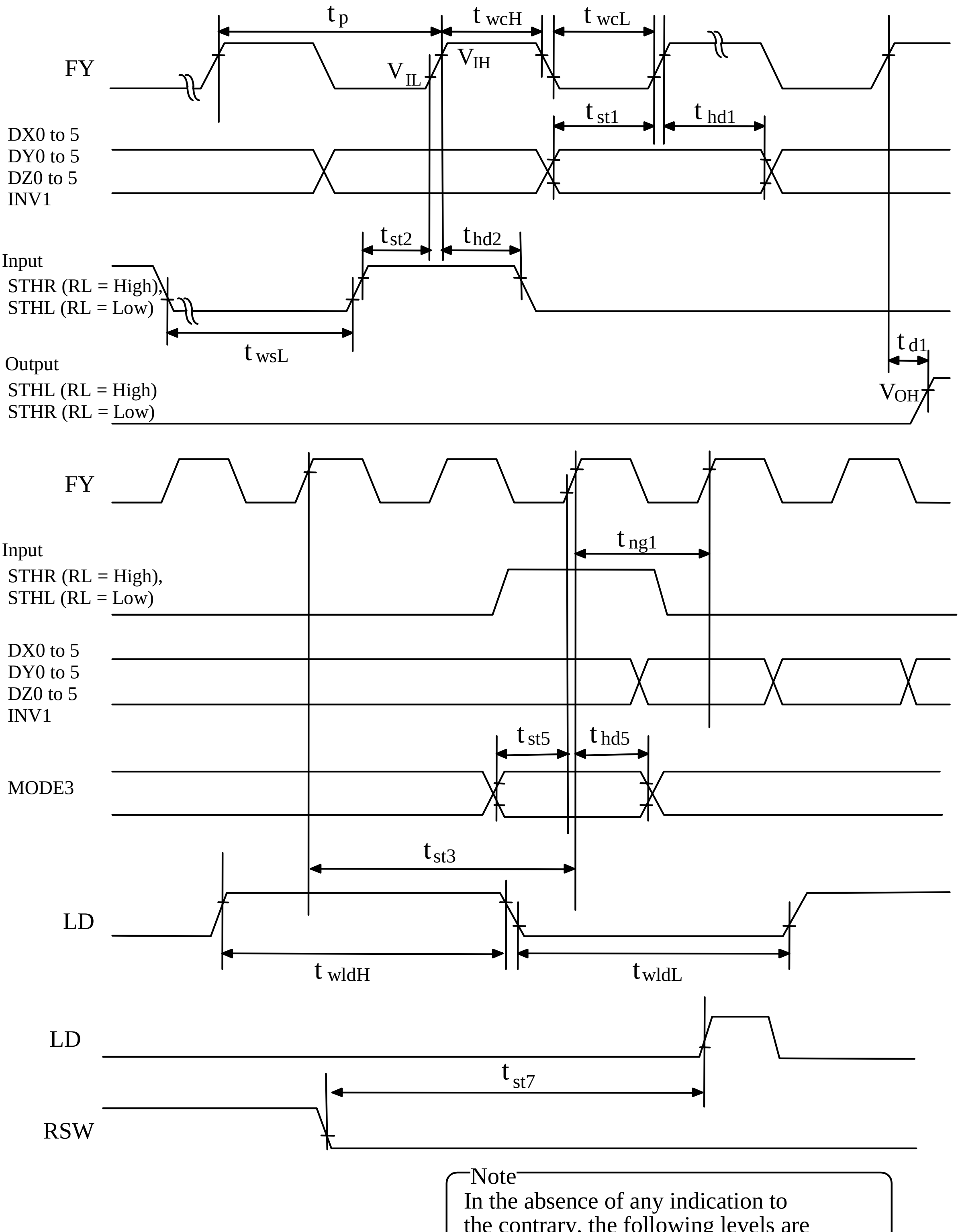
12) The reference point is the first FY rising edge after the rising edge in the start signal (STHR or STHL).

13) This time is defined as that taken for the driver output voltage to reach, within 6-bit precision, the target voltage.

14) The target output voltage shall be the output voltage just before the power save function takes effect--that is, the latter shall be assumed to have reached the target.

· The above standards apply only to our standard package for the product.

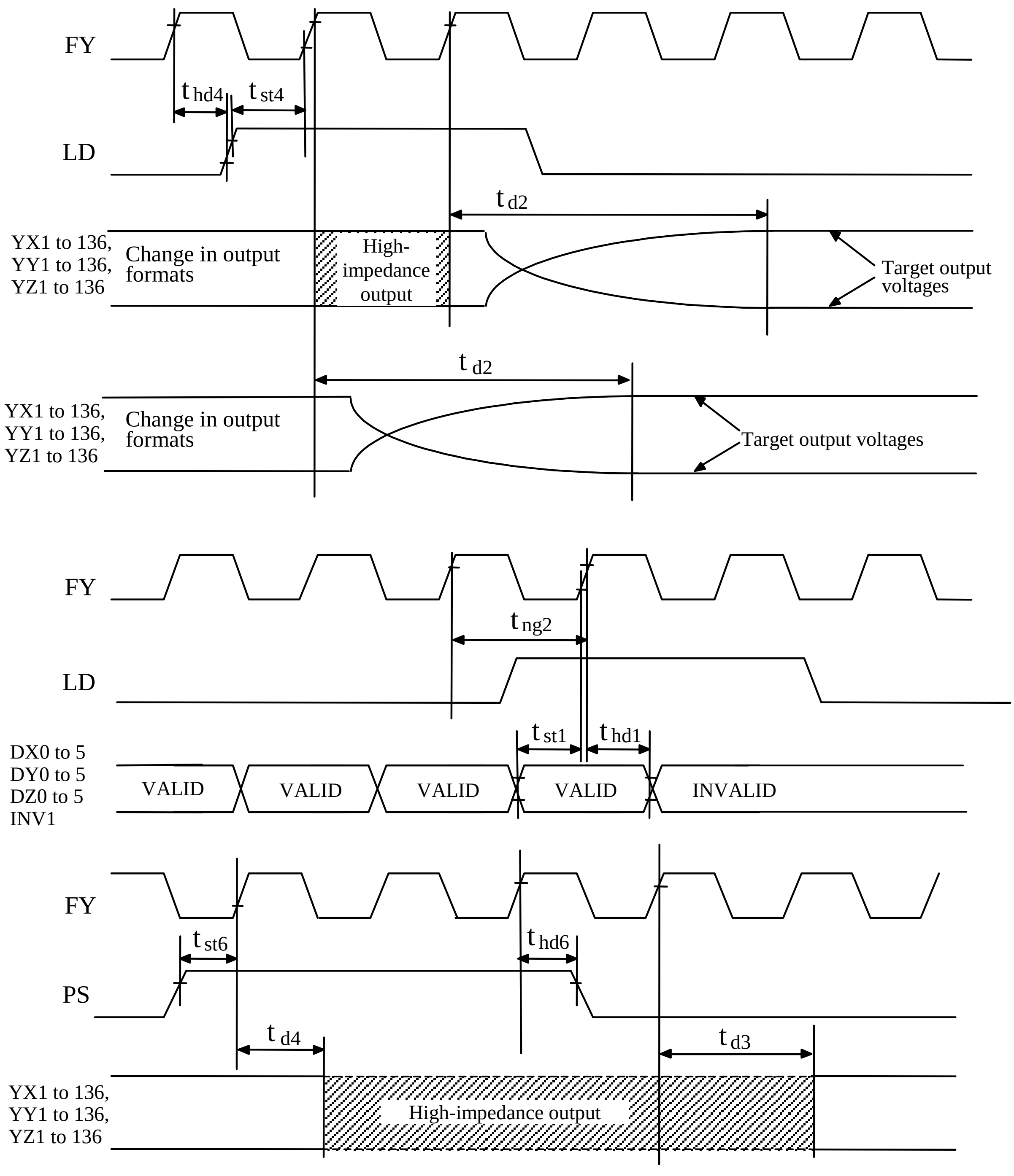
AC Characteristics Timing Chart 1



Note
In the absence of any indication to the contrary, the following levels are assumed.

$V_{IH} = V_{OH} = 0.8 \times DV_{DD}$
$V_{IL} = V_{OL} = 0.2 \times DV_{DD}$

AC Characteristics Timing Chart 2



Note
In the absence of any indication to the contrary, the following levels are assumed.

$V_{IH} = V_{OH} = 0.8 \times DV_{DD}$

$V_{IL} = V_{OL} = 0.2 \times DV_{DD}$

Request for your special attention and precautions in using the technical information and semiconductors described in this material

(1) An export permit needs to be obtained from the competent authorities of the Japanese Government if any of the products or technologies described in this material and controlled under the "Foreign Exchange and Foreign Trade Law" is to be exported or taken out of Japan.

(2) The technical information described in this material is limited to showing representative characteristics and applied circuit examples of the products. It does not constitute the warranting of industrial property, the granting of relative rights, or the granting of any license.

(3) The products described in this material are intended to be used for standard applications or general electronic equipment (such as office equipment, communications equipment, measuring instruments and household appliances).
Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automobiles, traffic control equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
- Any applications other than the standard applications intended.

(4) The products and product specifications described in this material are subject to change without notice for reasons of modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the guaranteed values, in particular those of maximum rating, the range of operating power supply voltage and heat radiation characteristics. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, redundant design is recommended, so that such equipment may not violate relevant laws or regulations because of the function of our products.

(6) When using products for which dry packing is required, observe the conditions (including shelf life and after-unpacking standby time) agreed upon when specification sheets are individually exchanged.

(7) No part of this material may be reprinted or reproduced by any means without written permission from our company.

Please read the following notes before using the datasheets

A. These materials are intended as a reference to assist customers with the selection of Panasonic semiconductor products best suited to their applications.
Due to modification or other reasons, any information contained in this material, such as available product types, technical data, and so on, is subject to change without notice.
Customers are advised to contact our semiconductor sales office and obtain the latest information before starting precise technical research and/or purchasing activities.

B. Panasonic is endeavoring to continually improve the quality and reliability of these materials but there is always the possibility that further rectifications will be required in the future. Therefore, Panasonic will not assume any liability for any damages arising from any errors etc. that may appear in this material.

C. These materials are solely intended for a customer's individual use.
Therefore, without the prior written approval of Panasonic, any other use such as reproducing, selling, or distributing this material to a third party, via the Internet or in any other way, is prohibited.