

DATA SHEET

SA56613-XX

5 V, 150 mA LDO and independent
delayed $\overline{\text{RESET}}$

Product data

2002 Mar 25

5 V, 150 mA LDO and independent delayed $\overline{\text{RESET}}$

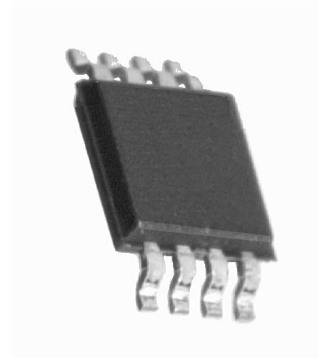
SA56613-XX

DESCRIPTION

The SA56613-XX has a precise fixed 5 V output with a typical accuracy of $\pm 2\%$ to provide very low dropout and low noise in CD-ROM drives, battery-operated systems, and portable computers applications. This regulator consists of an internal voltage reference, an error amplifier, a driver with current limiter and a thermal shutdown.

An Active-LOW $\overline{\text{RESET}}$ is asserted when the regulator output voltage (V_{OUT}) falls below the reset detection voltage threshold. The SA56613-XX is available with fixed detection threshold voltages of 4.2, 4.5, and 4.7 V. The $\overline{\text{RESET}}$ output remains low for 1 ms (typical) when a 10 nF capacitor is connected to C_{D} pin. The reset time delay can be adjusted by replacing capacitance values from C_{D} pin to Ground.

The device is available in the small SO8 package.



FEATURES

- Very low dropout voltage: 250 mV typ. ($I_{\text{OUT}} = 30 \text{ mA}$)
- High precision output voltage: $\pm 2\%$
- Output current capacity: 150 mA
- Low Noise: 200 μV_{rms} typ. @ 20 Hz to 80 kHz and for $I_{\text{OUT}} = 30 \text{ mA}$
- Extremely good line regulation: 10 mV typical
- Very good load regulation: 40 mV typical
- Low temperature drift co-efficient to V_{OUT} : $\pm 100 \text{ ppm}/^\circ\text{C}$
- Internal current limit and thermal shut-down circuits
- Adjustment-free reset detection voltages: 4.2 V typ., 4.5 V typ. and 4.7 V typ.
- Delay time can be adjusted by external capacitor.
- Wide operating temperature range: -40°C to $+85^\circ\text{C}$

APPLICATIONS

- TV and monitors
- Electronic notebooks, PDAs and Palmtop computers
- Cameras, VCRs and camcorders
- PCMCIA cards and CD-ROM drives
- Modems
- Battery-powered or hand-held instruments

SIMPLIFIED SYSTEM DIAGRAM

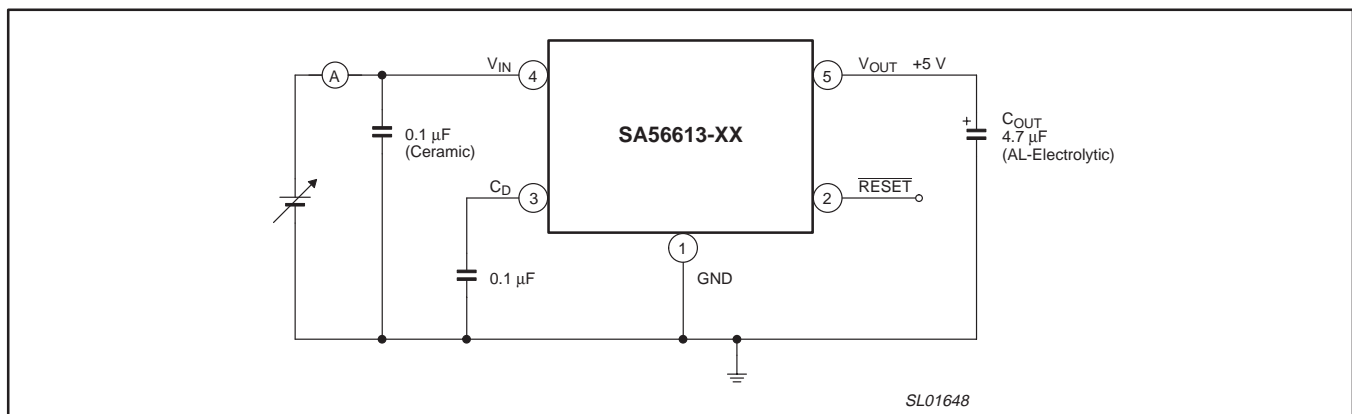


Figure 1. Simplified system diagram.

5 V, 150 mA LDO and independent delayed RESET

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		TEMPERATURE RANGE
	NAME	DESCRIPTION	
SA56613-XXD	SO8	plastic small outline package; 8 leads; body width 3.9 mm	-40 to +85 °C

NOTE:

The device has 3 voltage options, indicated by the XX on the 'Type number'.

XX	OUTPUT VOLTAGE (Typical)	RESET THRESHOLD (Typical)
42	5.0 V	4.2 V
45	5.0 V	4.5 V
47	5.0 V	4.7 V

PIN CONFIGURATION

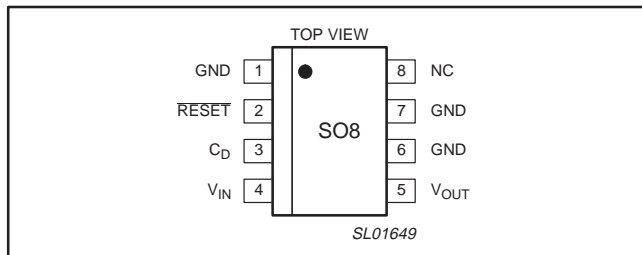


Figure 2. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	GND	Ground
2	RESET	Active-LOW reset signal output pin. The output remains LOW while V_{OUT} is below V_{SH} , the reset threshold, and for an external set time delay C_D pin after V_{OUT} rises above reset threshold.
3	C_D	Reset delay time capacitor pin. RESET pin output delay time can be set by the capacitance connected to the C_D pin. $t_{PLH} = 10^5 \times C$ where: t_{PLH} = transmission delay time (s) C = capacitor value (F)
4	V_{IN}	Supply voltage input pin
5	V_{OUT}	Regulated output voltage pin
6	GND	Ground pin and heat sink
7	GND	Ground pin and heat sink
8	N/C	No connection

MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{IN}	Input supply voltage	-0.3	+18	V
I_{OUT}	Output current	-	200	mA
T_{opr}	Operating ambient temperature	-40	+85	°C
T_{stg}	Storage temperature	-40	+150	°C
$T_{j(max)}$	Maximum junction temperature	-	+125	°C
P_D	Power dissipation (Note 1)	Derate 6.5 mW/°C above T_{amb} 25 °C		mW

NOTE:

1. When mounted on a 55 × 20 mm paper phenol board.

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ELECTRICAL CHARACTERISTICS $T_{amb} = 25\text{ }^{\circ}\text{C}$, Figure 13 "Test circuit", unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CCq1}	No-load input current 1	$V_{IN} = 6\text{ V}; I_{OUT} = 0\text{ mA}$	–	400	800	μA
I_{CCq2}	No-load input current 2	$V_{IN} = 4\text{ V}; I_{OUT} = 0\text{ mA}$	–	2.5	–	μA
Regulator						
V_{OUT}	Output voltage	$V_{IN} = 6\text{ V}; I_{OUT} = 30\text{ mA}$	4.90	5.00	5.10	V
$V_{I/O(dif)}$	Input/output differential voltage	$V_{IN} = 4.8\text{ V}; I_{OUT} = 150\text{ mA}$	–	0.25	0.5	V
ΔV_1	Line regulation	$V_{IN} = 6\text{ V} \rightarrow 10\text{ V}; I_{OUT} = 30\text{ mA}$	–	10	30	mV
ΔV_2	Load regulation	$V_{IN} = 6\text{ V}; I_{OUT} = 0\text{ mA} \rightarrow 150\text{ mA}$	–	40	80	mV
$\Delta V_{OUT}/\Delta T$	V_{OUT} temperature coefficient (Note 1)	$T_j = -20\text{ }^{\circ}\text{C} \rightarrow +85\text{ }^{\circ}\text{C};$ $V_{IN} = 6\text{ V}; I_{OUT} = 30\text{ mA}$	–	100	–	ppm/ $^{\circ}\text{C}$
RR	Ripple rejection (Note 1)	$V_{IN} = 6\text{ V}; f = 120\text{ Hz};$ $V_{RIPPLE} = 1\text{ V}_{p-p}; I_{OUT} = 30\text{ mA}$	50	60	–	dB
$V_{n(o)}$	Noise output voltage (Note 1)	$V_{IN} = 6\text{ V}; f = 20 \sim 80\text{ kHz};$ $I_{OUT} = 30\text{ mA}$	–	200	400	μV_{rms}
Reset						
V_S	Detection voltage	$V_{IN} = H \rightarrow L$ SA56613–42 SA56613–45 SA56613–47	4.03 4.31 4.51	4.20 4.50 4.70	4.37 4.69 4.89	V V V
$\Delta V_S/\Delta T$	V_S temperature coefficient (Note 1)	$T_j = -20\text{ }^{\circ}\text{C} \rightarrow +85\text{ }^{\circ}\text{C}$	–	100	–	ppm/ $^{\circ}\text{C}$
ΔV_S	Hysteresis voltage	$V_{IN} = H \rightarrow L \rightarrow H$	25	50	100	mV
V_{OL}	LOW-level output voltage	$V_{IN} = 3.9\text{ V}; R_L = 4.7\text{ k}\Omega$	–	100	200	mV
t_{PLH1}	Reset delay time	$V_{IN} = 4\text{ V} \rightarrow 5\text{ V}; C_D = 0.1\text{ }\mu\text{F}$	5	10	15	ms
t_{PHL}	'L' transmission delay time (Note 1)	$V_{IN} = 5\text{ V} \rightarrow 4\text{ V}; C_D = 0.1\text{ }\mu\text{F}$	–	30	90	μs
V_{OPL}	Threshold operating voltage	$V_{OL} = 0.4\text{ V}$	–	0.65	0.85	V

NOTE:

1. This parameter is guaranteed by design.

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TYPICAL PERFORMANCE CURVES (SA56613-42D)

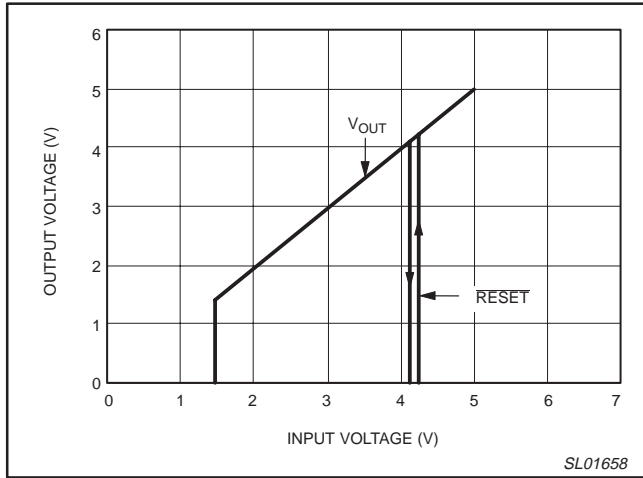


Figure 3. Detection voltage ($I_{OUT} = 0$ mA).

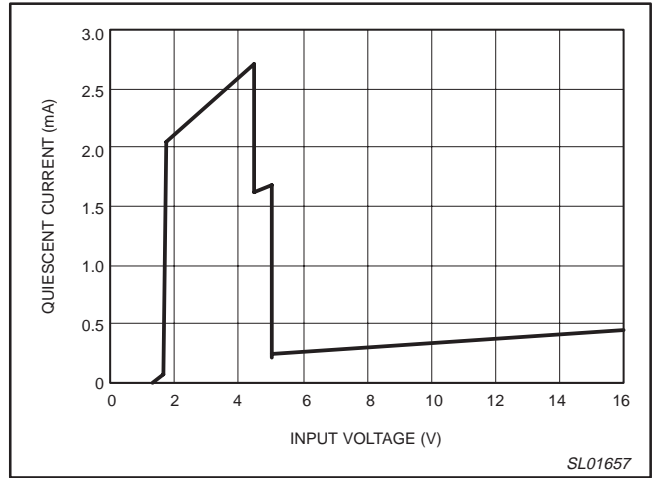


Figure 4. Quiescent current ($I_{OUT} = 0$ mA).

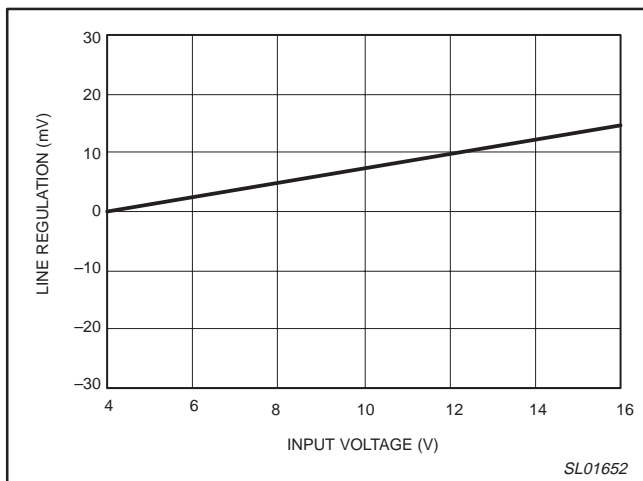


Figure 5. Line regulation.

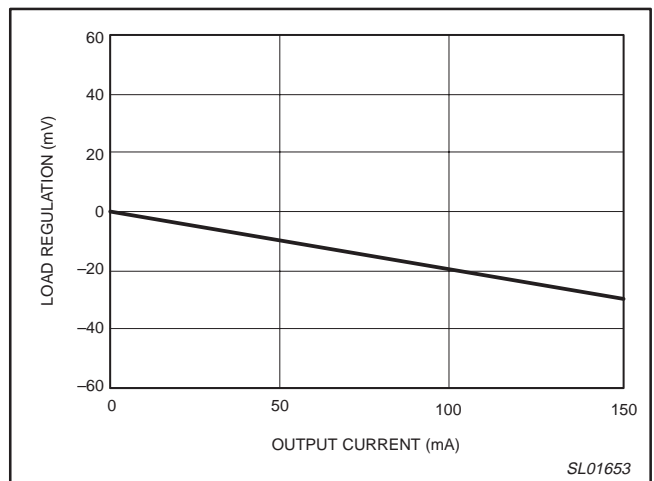


Figure 6. Load regulation.

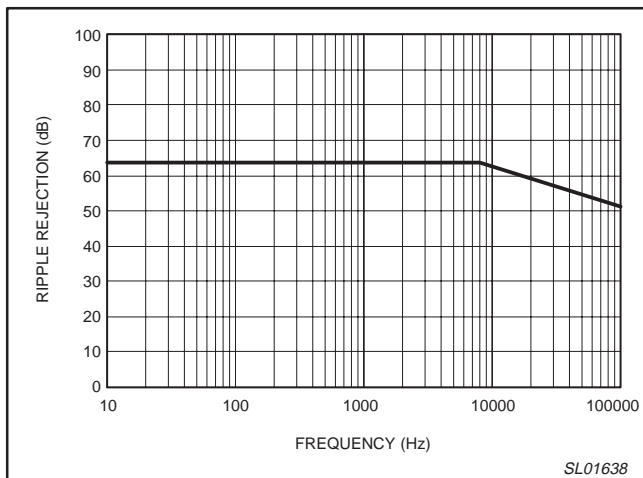


Figure 7. Ripple rejection.

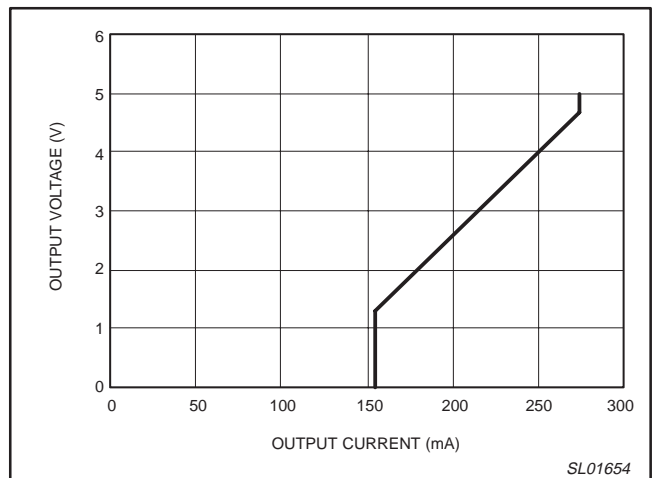


Figure 8. Current limit.

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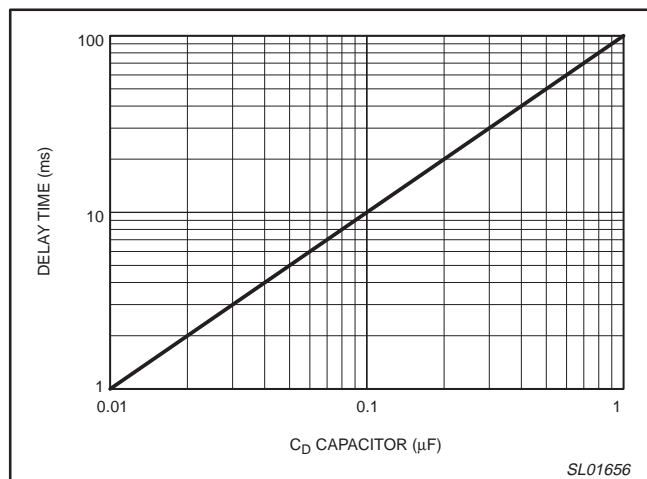


Figure 9. Reset delay time.

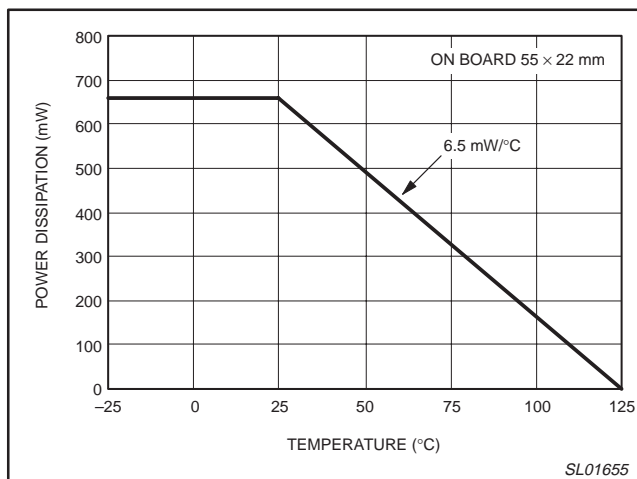


Figure 10. Power dissipation.

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TIMING DIAGRAM

The Timing Diagram in Figure 11 depicts the operation of the device. Letters A-I on the Time axis indicates specific events.

A: At "A", V_{OUT} abruptly begins to increase. Also the $\overline{\text{RESET}}$ voltage initially increases but abruptly decreases when V_{OUT} reaches the threshold operating level (typically 0.65 V) that activates the internal bias circuitry and $\overline{\text{RESET}}$ is asserted.

B: At "B", V_{OUT} reaches the threshold level of V_{SH} . At this point the delay time, t_{PLH} is initiated while V_{OUT} rises above V_{SH} to its normal operating level of 5 V. The $\overline{\text{RESET}}$ voltage remains LOW.

C: At "C", V_{OUT} is above V_{SL} and the delay time, t_{PLH} elapses. At this instant, the device releases the hold on the $\overline{\text{RESET}}$. The reset output then goes HIGH. In a microprocessor based system these events release the reset from the microprocessor, allowing the microprocessor to function normally.

D-E: At "D", V_{IN} falls below 5 V, causing V_{OUT} to follow. V_{OUT} continues to fall until the V_{SL} undervoltage detection threshold is reached at "E". This causes a reset signal to be generated ($\overline{\text{RESET}}$ goes LOW).

E-F: Between "E" and "F", V_{OUT} continues to fall and then starts rising.

F: At "F", V_{OUT} rises to the V_{SH} level. Once again, the device initiates the delay timer.

F-G: V_{OUT} rises above V_{SH} and returns to normal 5 V output. At "G", the delay (t_{PLH}) times out and once again, then it releases the hold on the $\overline{\text{RESET}}$ and it goes HIGH.

G-H: At "G", V_{OUT} is above the upper threshold and begins to fall, causing $\overline{\text{RESET}}$ to follow it. As long as V_{OUT} remains above the V_{SL} , no reset signal will be generated.

H: At event "H", V_{OUT} falls until the V_{SL} undervoltage detection threshold is reached. At this level, a $\overline{\text{RESET}}$ signal is generated and $\overline{\text{RESET}}$ goes LOW.

I: At event "I", V_{OUT} has decreased until normal internal circuit bias is unable to maintain a $\overline{\text{RESET}}$. As a result, V_{CC} may rise to less than 0.65 V. As V_{CC} decreases further, the V_{OUT} reset also decreases to zero.

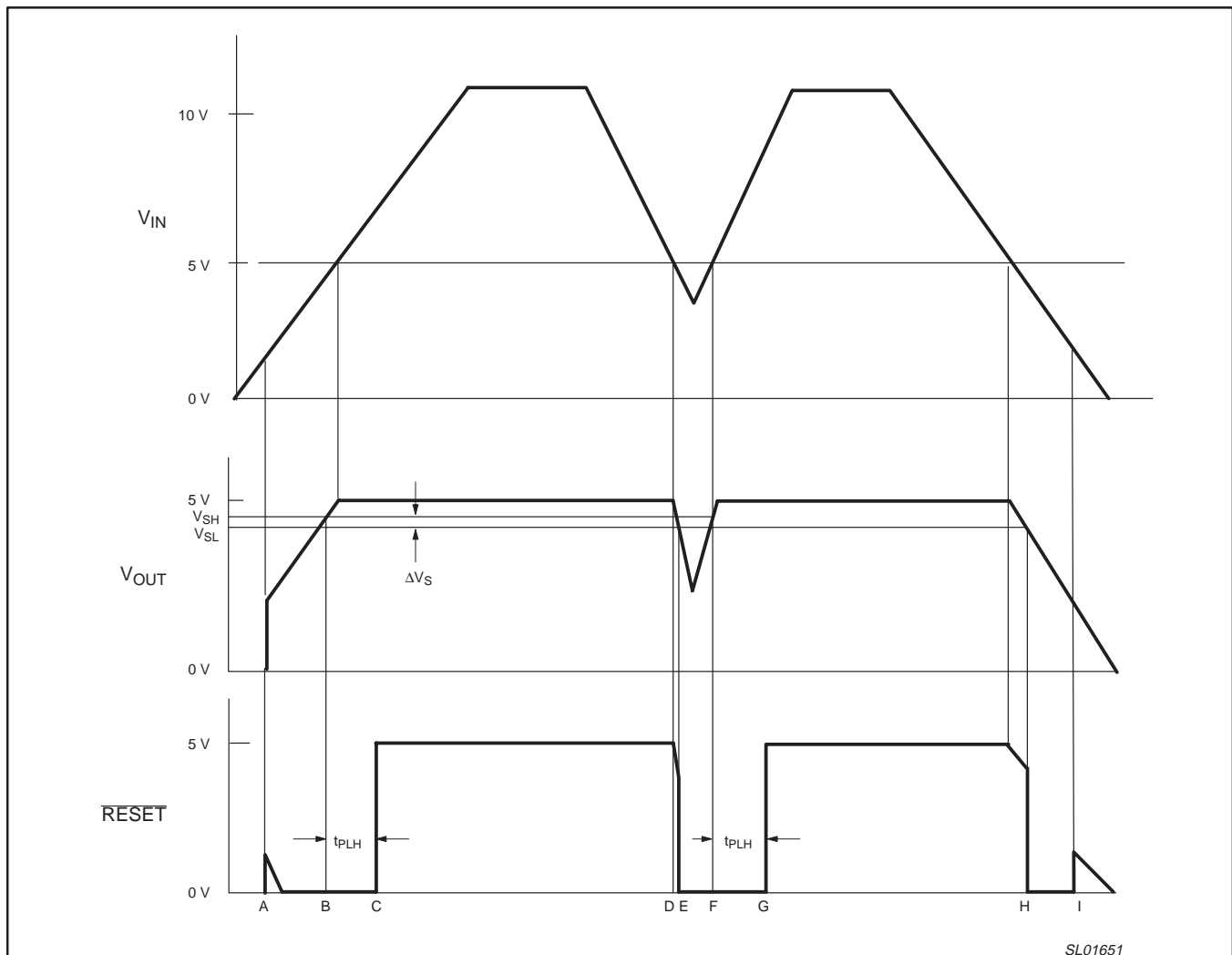


Figure 11. Timing diagram.

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APPLICATION INFORMATION

Input capacitor

An input capacitor of $\geq 1 \mu\text{F}$ is required to eliminate the AC coupling noise. This capacitor must be located as close as possible to V_{IN} or GND pin (not more than 1 cm) and returned to a clean analog ground. Any good quality ceramic, tantalum or film capacitor will work.

Output capacitor

Phase compensation is made for securing stable operation even if the load current varies. For this reason, an output capacitor with good frequency characteristics is needed. Set it as close to the circuit as possible and make the wiring as short as possible.

The value of the output capacitance has to be at least $47 \mu\text{F}$ connected from V_{OUT} to GND. When operating from sources other than batteries, supply-noise rejection and transient response can be improved by increasing the value of the input and output capacitors and employing passive filtering techniques.

RESET output

The SA56613-XX has an Active-LOW $\overline{\text{RESET}}$ output. When V_{OUT} of the regulator rises above V_{SH} , the upper detection threshold voltage, the reset delay time is initiated. After the programmed delay time elapses, $\overline{\text{RESET}}$ is released and goes HIGH. The time delay can be set typically from 1 ms to 100 ms by connecting a time delay capacitor from C_{D} (pin 3) to ground (see Figure 9: $\overline{\text{RESET}}$ Delay time versus C_{D} , Delay Capacitor).

The $\overline{\text{RESET}}$ delay time (t_{PLH}) can be approximated by the following equation:

$$t_{\text{PLH}} = 10^5 \times C \quad \text{Eqn. (1)}$$

(Time is expressed in seconds, Capacitance in Farads.)

For example, for a delay capacitor, C_{D} of $0.1 \mu\text{F}$ (100 nF), t_{PLH} is approximately 10 ms.

When the regulator output Voltage falls to or below V_{SL} , the lower detection threshold voltage, the $\overline{\text{RESET}}$ output is asserted and it goes to an Active-LOW state. This "LOW" transmission delay time is typically $30 \mu\text{s}$ with C_{D} at 100 nF.

Reset hysteresis voltage

The reset hysteresis voltage, ΔV_{S} is defined in the following equation:

$$\Delta V_{\text{S}} = V_{\text{SH}} - V_{\text{SL}} \quad \text{Eqn. (2)}$$

Hysteresis voltage is typically 50 mV. This small level of hysteresis ensures that the reset will not dither when the regulator V_{OUT} is noisy.

PCB layout

The component placement around the LDO should be done carefully to achieve good dynamic line and load response. The input and noise capacitors should be kept close to the LDO.

The rise in junction temperature depends on how efficiently the heat is carried away from the junction to ambient. The junction to lead thermal impedance is a characteristic of the package and fixed. The thermal impedance between lead to ambient can be reduced by increasing the copper area on the PCB. Increase the input, output and ground trace area to reduce the junction-to-ambient impedance.

Power dissipation

The SA56613-XX maximum power dissipation depends on the thermal resistance from the die junction to the ambient air. The maximum power dissipation shown in Figure 10 is 650 mW at ambient temperature of 25°C . It is derated at $6.5 \text{ mW}/^\circ\text{C}$ above 25°C .

Power dissipation of the device is $P_{\text{D}} = I_{\text{OUT}} (V_{\text{IN}} - V_{\text{OUT}})$. The maximum power dissipation is:

$$P_{\text{max}} = \frac{(T_{\text{j}} - T_{\text{amb}})}{(\theta_{\text{JA}})} \quad \text{Eqn. (3)}$$

where

θ_{JA} = $\theta_{\text{JB}} + \theta_{\text{BA}}$, the junction-to-ambient thermal resistance, θ_{JA} calculated from Figure 10 is $154^\circ\text{C}/\text{W}$;

θ_{JB} is the thermal resistance from the die junction to PCB material and copper traces;

θ_{BA} is the thermal resistance from the PCB material and copper traces to the surrounding air.

The GND pin provides an electrical connection to ground and a path for heat transfer from the device to the PCB and to the surrounding air. To maximize heat transfer, connect the GND pin to a large ground pad or ground plane.

The following example determines the maximum I_{OUT} at $T_{\text{amb}} = 25^\circ\text{C}$ for $V_{\text{IN}} = 1 \text{ V}$.

$$I_{\text{OUT}} = \frac{P_{\text{D}}}{(V_{\text{IN}} - V_{\text{OUT}})} = \frac{650 \text{ mW}}{(12 - 5)} = 92.8 \text{ mA} \quad \text{Eqn. (4)}$$

The maximum output current of the SA56613-XX is reduced as the input voltage, V_{IN} and the ambient temperature, T_{amb} increase.

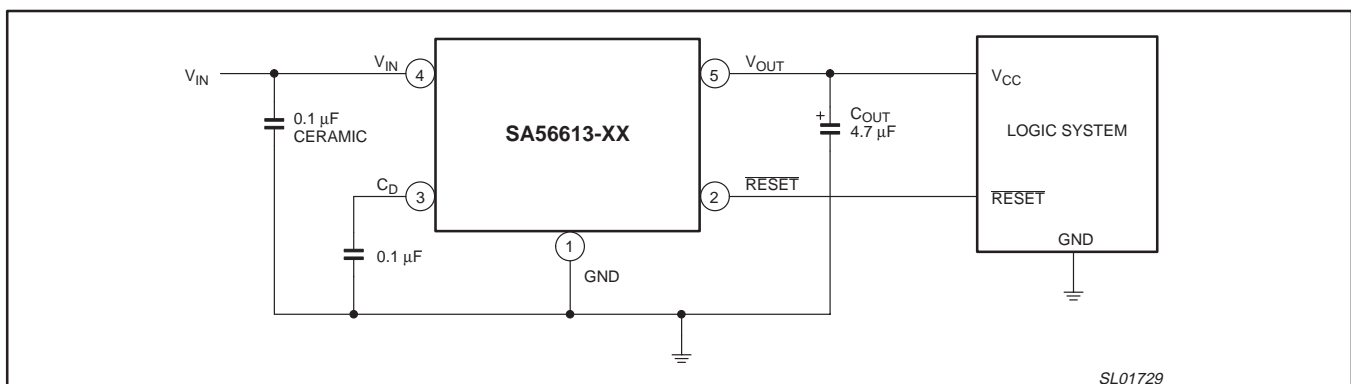


Figure 12. Typical application circuit.

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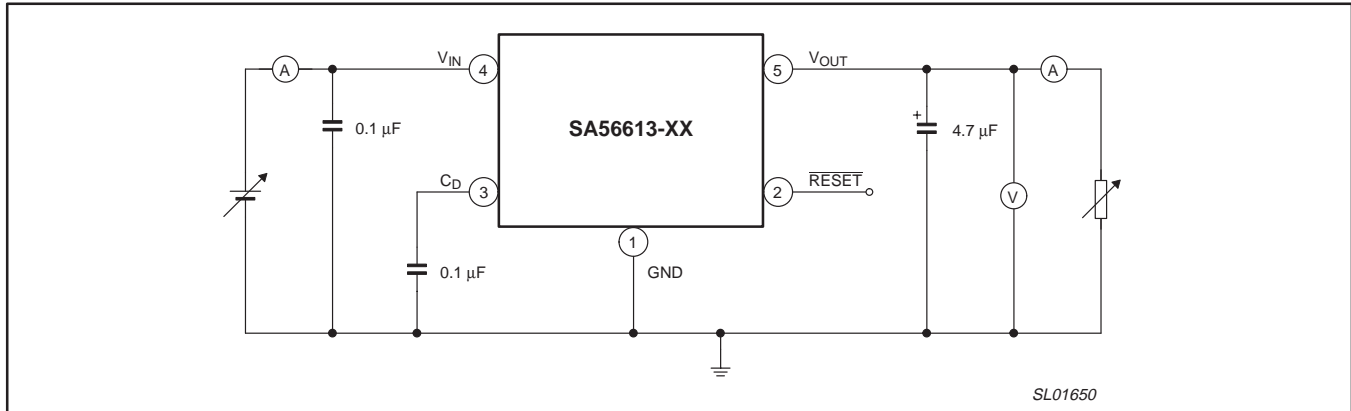


Figure 13. Test circuit.

PACKING METHOD

The SA56613-XX is packed in reels, as shown in Figure 14.

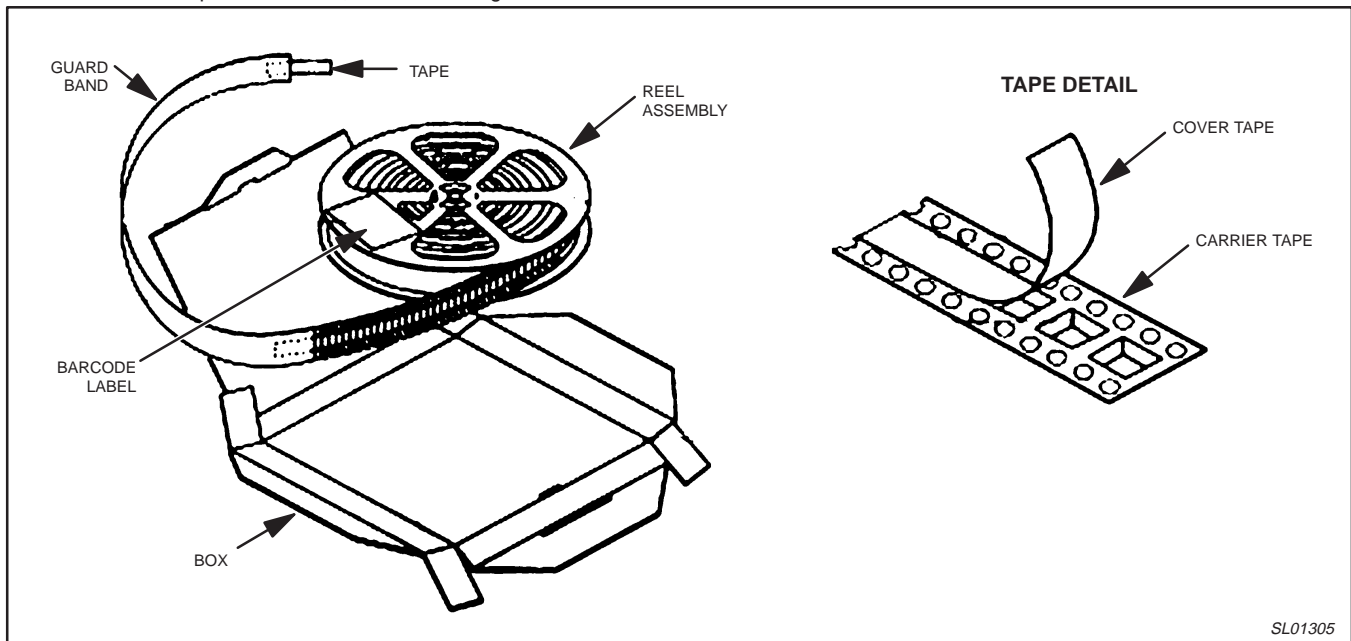
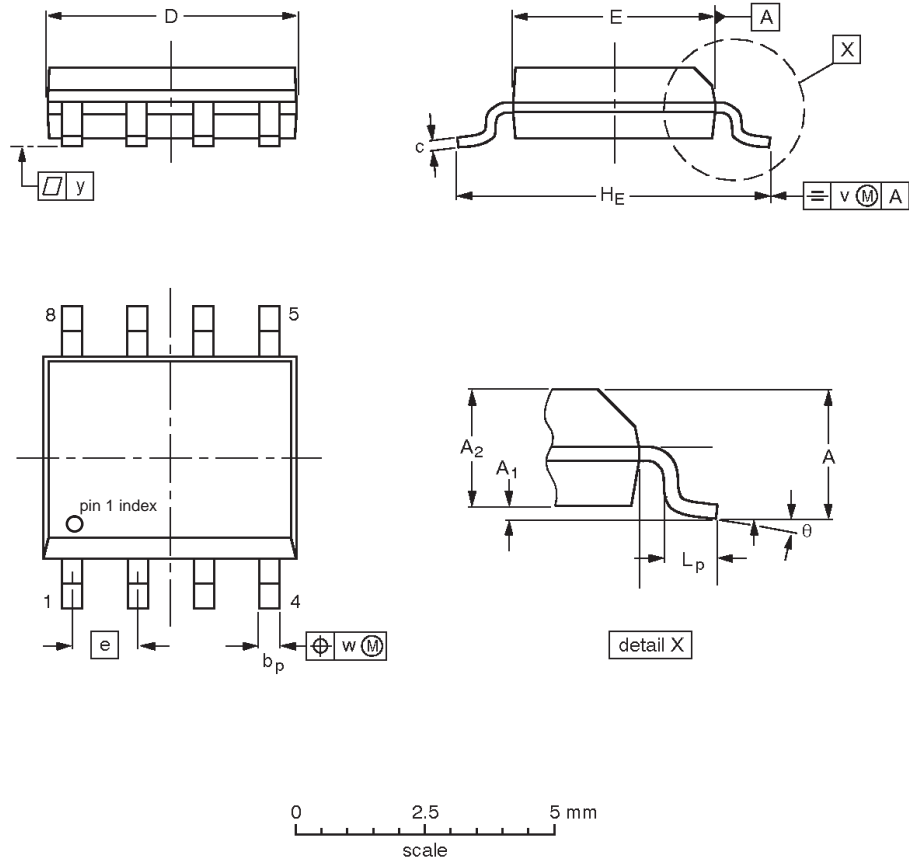


Figure 14. Tape and reel packing method.

5 V, 150 mA LDO and independent delayed RESET

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SO8: plastic small outline package; 8 leads; body width 3.9 mm



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	B ₂	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L _p	y	θ
mm	1.73	0.25 0.10	1.45 1.25	4.95 4.80	0.51 0.33	0.25 0.19	4.95 4.80	4.0 3.8	1.27	6.2 5.8	1.27 0.38	0.076	8° 0°
inches	0.068	0.010 0.004	0.057 0.049	0.189 0.195	0.013 0.020	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.050 0.015	0.003	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES		
	IEC	JEDEC	EIAJ
SO8	076E03	MS-012	

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NOTES

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Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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