

## 480-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 256-GRAY SCALES)

### DESCRIPTION

The  $\mu$ PD160083 is a source driver for TFT-LCDs capable of dealing with displays with 256-gray scales. Data input is based on digital input configured as 8 bits by 3 dots (1 pixel) with double clock edge, which can realize a full-color display of 16,777,216 colors by output of 256 values  $\gamma$ -corrected by an internal D/A converter and 9-by-2 external power modules. Because the output dynamic range is as large as  $V_{SS2} + 0.1$  V to  $V_{DD2} - 0.1$  V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 8-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a clock frequency of 85 MHz when driving at 3.0 V, this driver is applicable to UXGA-standard (1600 × 1200), SXGA-standard (1280 × 1024) TFT-LCD panels.

### FEATURES

- RSDS™ (Reduced Swing Differential Signaling) interface
- 480 outputs
- Input of 8 bits (gradation data) by 3 dots with double clock edge sampling
- Capable of outputting 256 values by means of 9-by-2 external power modules (18 units) and a D/A converter
- Logic power supply voltage ( $V_{DD1}$ ): 2.7 to 3.6 V
- Driver power supply voltage ( $V_{DD2}$ ): 10.5 to 13.5 V
- Output dynamic range:  $V_{SS2} + 0.1$  V to  $V_{DD2} - 0.1$  V
- High-speed data transfer:  $f_{CLK} = 85\text{MHz MAX.}$  (Internal data transfer speed when operating at  $V_{DD1} = 3.0$  V)
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output Voltage polarity inversion function (POL)
- Input data inversion function (INV)
- Controlable output short function (MODE1 to MODE3)

**Remark** RSDS™ is a trademark of National Semiconductor Corporation.

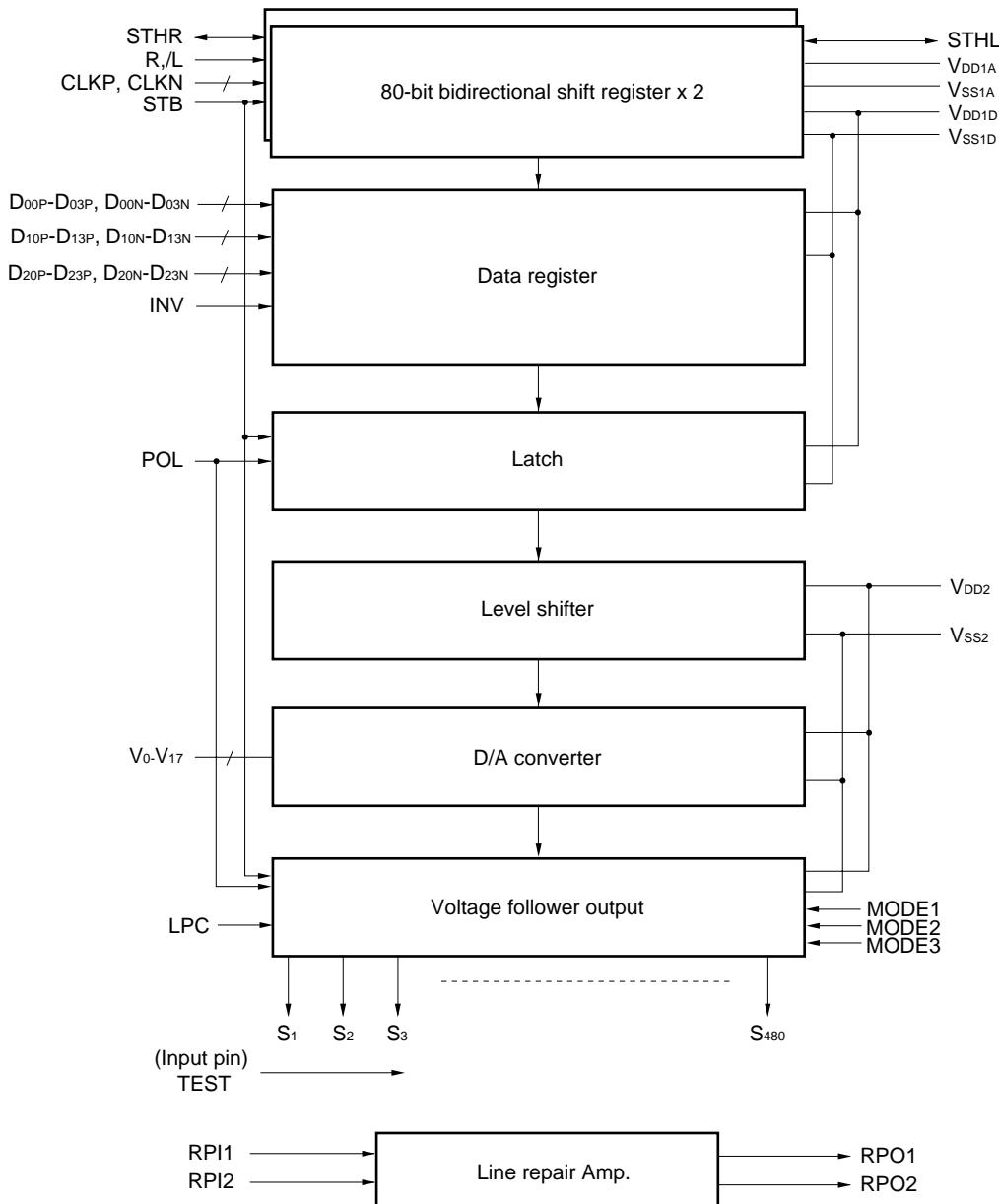
### ORDERING INFORMATION

| Part Number          | Package           |
|----------------------|-------------------|
| $\mu$ PD160083N-xxx  | TCP (TAB package) |
| $\mu$ PD160083NL-xxx | COF (COF package) |

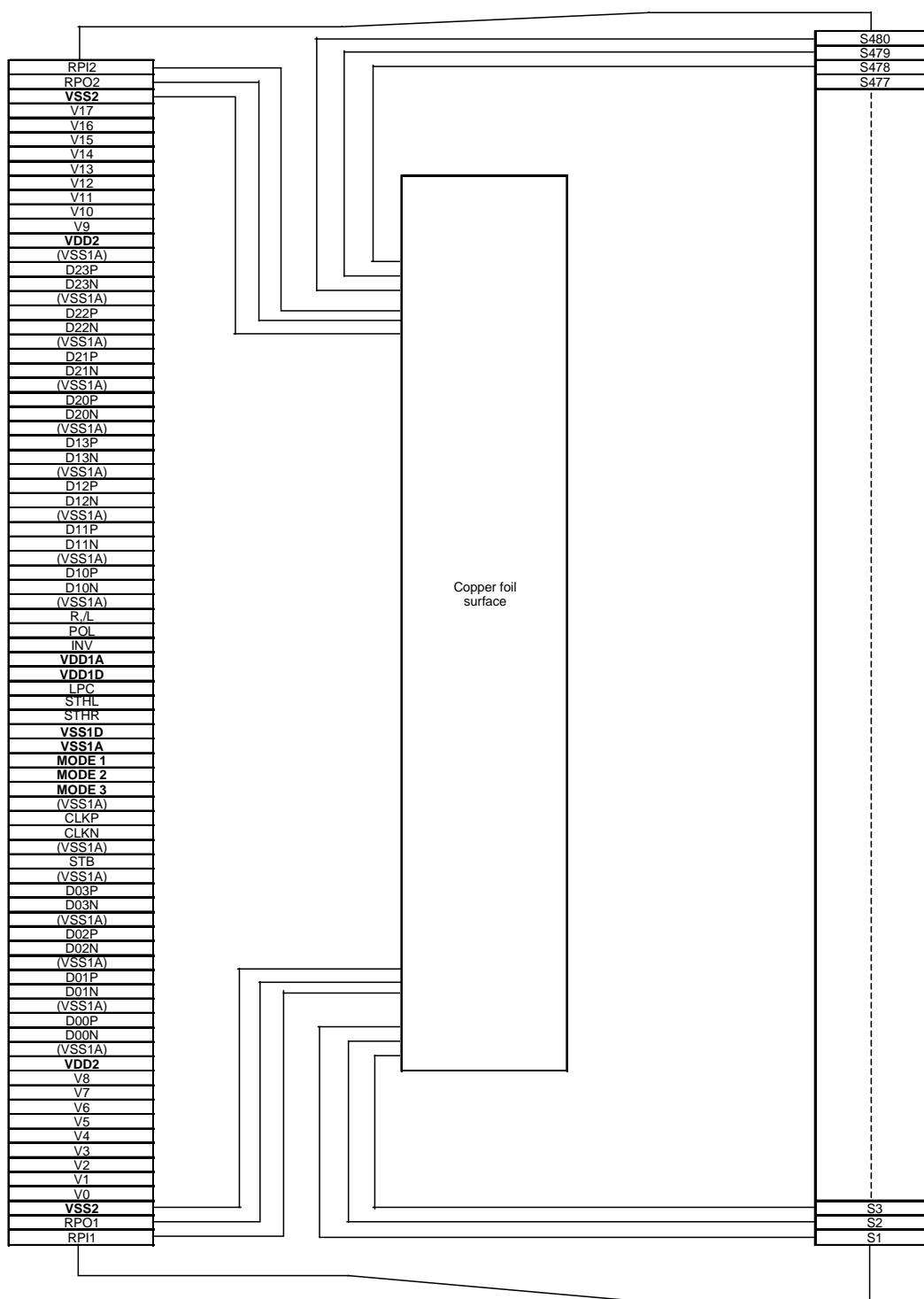
**Remark** The TCP/COF's external shape is customized. To order the required shape, so please contact one of our sales representatives

The information contained in this document is being issued in advance of the production cycle for the product. The parameters for the product may change before final production or NEC Electronics Corporation, at its own discretion, may withdraw the product prior to its production. Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

## 1. BLOCK DIAGRAM



**Remark** /xxx indicates active low signal.

2. PIN CONFIGURATION ( $\mu$ PD160083N-xxx: TCP) (Copper foil surface, face-up)

**Remark 1.** This figure does not specify the TCP package.

2. (VSS1A) is recommended to connect to analog GND on PCB for the return current of transmission line.  
And please don't use these pins for power supply terminal with dynamic current.

### 3. PIN FUNCTIONS

(1/2)

| Pin Symbol   | Pin Name                | I/O       | Description  |                                 |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
|--|-------------------------|-----------|--|---------------------------------|-------|-------|-------|--------------|--------|-----------|---|---|------------|--------------------------|---|-----------|---|--------|----------------|---|-----------|-----------|---------------------------------|---|---|---|---------------------------------|
| S <sub>1</sub> to S <sub>480</sub>   | Driver                  | Output    | The D/A converted 256-gray-scale analog voltage is output.   |                                 |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
| D <sub>00P</sub> to D <sub>03P</sub> ,<br>D <sub>00N</sub> to D <sub>03N</sub> | Display data<br>(RSDS)  | Input     | The display data is input with a width of 12 bits by double edge, viz., the gray scale data (8 bits) by 3 dots (1 pixel).  |                                 |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
| D <sub>10P</sub> to D <sub>13P</sub> ,<br>D <sub>10N</sub> to D <sub>13N</sub> |                         |           |  |                                 |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
| D <sub>20P</sub> to D <sub>23P</sub> ,<br>D <sub>20N</sub> to D <sub>23N</sub> |                         |           |  |                                 |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
| R/L<br>(CMOS)  | Shift direction control | Input     | These refer to the start pulse input/output pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows.<br>R/L = H (V <sub>DD1</sub> level): STHR input, S <sub>1</sub> → S <sub>480</sub> , STHL output<br>R/L = L (V <sub>SS1</sub> level): STHL input, S <sub>480</sub> → S <sub>1</sub> , STHR output   |                                 |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
| STHR<br>(CMOS)   | Right shift start pulse | I/O       | R/L = H (V <sub>DD1</sub> level): Becomes the start pulse input pin.<br>R/L = L (V <sub>SS1</sub> level): Becomes the start pulse output pin.  |                                 |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
| STHL<br>(CMOS)   | Left shift start        | I/O       | R/L = H (V <sub>DD1</sub> level): Becomes the start pulse output pin.<br>R/L = L (V <sub>SS1</sub> level): Becomes the start pulse input pin.  |                                 |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
| CLKP,<br>CLKN<br>(RSDS)  | Shift clock             | Input     | Refers to the shift register's shift clock input. The display data is incorporated into the data register at both of rising and falling edge.<br>At the falling edge of the 160th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver.  |                                 |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
| STB<br>(CMOS)  | Latch                   | Input     | The contents of the data register are transferred to the latch circuit at the rising edge. And the output timing and output short function are controlled by MODE1 to MODE3. Please refer to <b>8. RELATIONSHIP BETWEEN STB, POL, MODE1 to MODE3 AND OUTPUT WAVEFORM</b> for more detail. It is necessary to ensure input of one pulse per horizontal period.  |                                 |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
| POL<br>(CMOS)  | Polarity                | Input     | POL = H (V <sub>DD1</sub> level): The S <sub>2n-1</sub> output uses V <sub>0</sub> -V <sub>8</sub> as the reference supply.<br>The S <sub>2n</sub> output uses V <sub>9</sub> -V <sub>17</sub> as the reference supply.<br>POL = L (V <sub>SS1</sub> level): The S <sub>2n-1</sub> output uses V <sub>9</sub> -V <sub>17</sub> as the reference supply.<br>The S <sub>2n</sub> output uses V <sub>0</sub> -V <sub>8</sub> as the reference supply.<br>S <sub>2n-1</sub> indicates the odd output; and S <sub>2n</sub> indicates the even output. Input of the POL signal is allowed the setup time (t <sub>POL-STB</sub> ) with respect to STB's rising edge.  |                                 |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
| INV<br>(CMOS)  | Data inversion          | Input     | Data inversion can invert when display data is loaded.<br>INV = H (V <sub>DD1</sub> level): Data inversion loads display data after inverting it.<br>INV = L (V <sub>SS1</sub> level): Data inversion does not invert input data.<br>Please input DC signal. For details, refer to <b>6. DATA INVERSION</b> .  |                                 |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
| LPC  | Low power control       | Input     | LPC = L or open: Normal mode (default)<br>LPC = H: Low power mode (35% lower than noamal mode)<br>This pin is pulled down to the V <sub>SS1D</sub> inside the IC.  |                                 |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
| MODE1 to<br>MODE3  | Output short control    | Input     | This pin controls the output short function.<br><table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>MODE1</th><th>MODE2</th><th>MODE3</th><th>Output Short</th><th>Remark</th></tr> <tr> <td>H or open</td><td>X</td><td>X</td><td>Non-active</td><td>Output short circuit OFF</td></tr> <tr> <td rowspan="2">L</td><td>H or open</td><td>X</td><td>Active</td><td>During STB = H</td></tr> <tr> <td rowspan="2">L</td><td>H or open</td><td>H or open</td><td>During 34 CLK after STB falling</td></tr> <tr> <td rowspan="2">L</td><td>L</td><td>L</td><td>During 68 CLK after STB falling</td></tr> </table> <p><b>Remark</b> X: H or L</p> <p>Output short function works only when POL signal is changed from previous line.<br/>This pin is pulled up to V<sub>DD1D</sub> inside the IC.</p> |                                 | MODE1 | MODE2 | MODE3 | Output Short | Remark | H or open | X | X | Non-active | Output short circuit OFF | L | H or open | X | Active | During STB = H | L | H or open | H or open | During 34 CLK after STB falling | L | L | L | During 68 CLK after STB falling |
| MODE1  | MODE2                   | MODE3     | Output Short   | Remark                          |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
| H or open  | X                       | X         | Non-active   | Output short circuit OFF        |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
| L  | H or open               | X         | Active   | During STB = H                  |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
|  | L                       | H or open | H or open  | During 34 CLK after STB falling |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |
| L  |                         | L         | L  | During 68 CLK after STB falling |       |       |       |              |        |           |   |   |            |                          |   |           |   |        |                |   |           |           |                                 |   |   |   |                                 |

(2/2)

| Pin Symbol                      | Pin Name                           | I/O    | Description  |
|---------------------------------|------------------------------------|--------|--|
| RPI1, RPI2                      | Line-repair Amp.                   | Input  | The driver-ability of the line-repair amp is around twice of the normal analog output S1 to S480.  |
| RPO1, RPO2                      |                                    | Output | And these outputs are changed at the rising edge of STB and don't have Hi-Z (High impedance) period.<br>RPI1 (RPI2) → impedance changed → RPO1 (RPO2)  |
| TEST                            | Test                               | Input  | TEST = H or open: Normal operation mode<br>TEST = L: Test mode   |
| V <sub>0</sub> -V <sub>17</sub> | $\gamma$ -corrected power supplies | –      | Input the $\gamma$ -corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level.<br>$V_{DD2} - 0.1 \text{ V} \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 \geq 0.5 \text{ V}_{DD2}$<br>$0.5 \text{ V}_{DD2} \geq V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_5 > V_{16} > V_{17} \geq V_{SS2} + 0.1 \text{ V}$ |
| V <sub>DD1D/A</sub>             | Logic power supply                 | –      | 2.7 to 3.6 V   |
| V <sub>DD2</sub>                | Driver power supply                | –      | 10.5 to 13.5 V   |
| V <sub>SS1D/A</sub>             | Logic ground                       | –      | Grounding  |
| V <sub>SS2</sub>                | Driver ground                      | –      | Grounding  |

**Cautions 1. The power on sequence must be V<sub>DD1D</sub>, V<sub>DD1A</sub>, logic input, and V<sub>DD2</sub> and V<sub>0</sub>-V<sub>17</sub> in that order.**

Reverse this sequence to shut down (Simultaneous power application to V<sub>DD2</sub> and V<sub>0</sub>-V<sub>17</sub> is possible.).

2. To stabilize the supply voltage, please be sure to insert a 0.1  $\mu\text{F}$  bypass capacitor between V<sub>DD1D</sub>, V<sub>DD1A</sub>-V<sub>SS1D</sub>, V<sub>DD1A</sub> and V<sub>DD2</sub>-V<sub>SS2</sub>. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01  $\mu\text{F}$  is also advised between the  $\gamma$ -corrected power supply pins (V<sub>0</sub>, V<sub>1</sub>, V<sub>2</sub>, ..., V<sub>17</sub>) and V<sub>SS2</sub>.
3. Because of the large power consumption of this driver IC, it is necessary to pay attention to the driver IC's temperature for the Junction Temperature. So, it should be considered to use the suitable mechanical design for the heat spreading and use the LPC function and the output reset function for the power reduction. Especially, it is recommended to measure the temperature of the driver IC surface.

#### 4. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The  $\mu$ PD160083 incorporates a 8-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches. The ladder resistors ( $r_0$  to  $r_{255}$ ) are designed so that the ratio of LCD panel  $\gamma$ -compensated voltages to  $V_0'$ - $V_{255}'$  and  $V_0''$ - $V_{255}''$  is almost equivalent, therefore, each resistance value indicates figure 4-2. For the 2 sets of 9  $\gamma$ -compensated power supplies,  $V_0$ - $V_8$  and  $V_9$ - $V_{17}$ , respectively, input gray scale voltages of the same polarity with respect to the common voltage

Figure 4-1 shows the relationship between the driving voltages such as liquid-crystal driving voltages  $V_{DD2}$ ,  $V_{SS2}$  and 0.5  $V_{DD2}$ , and  $\gamma$ -corrected voltages  $V_0$ - $V_{17}$  and the input data. Be sure to maintain the voltage relationships below.

$$V_{DD2} - 0.1 \text{ V} \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 \geq 0.5 V_{DD2}$$

$$0.5 V_{DD2} \geq V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{16} > V_{17} \geq V_{SS2} + 0.1 \text{ V}$$

Figures 4-2 shows  $\gamma$ -corrected voltages and ladder resistors ratio and figure 4-3 shows relationship between the input data and the output voltage.

**Figure 4-1. Relationship Between Input Data and  $\gamma$ -corrected Power Supply**

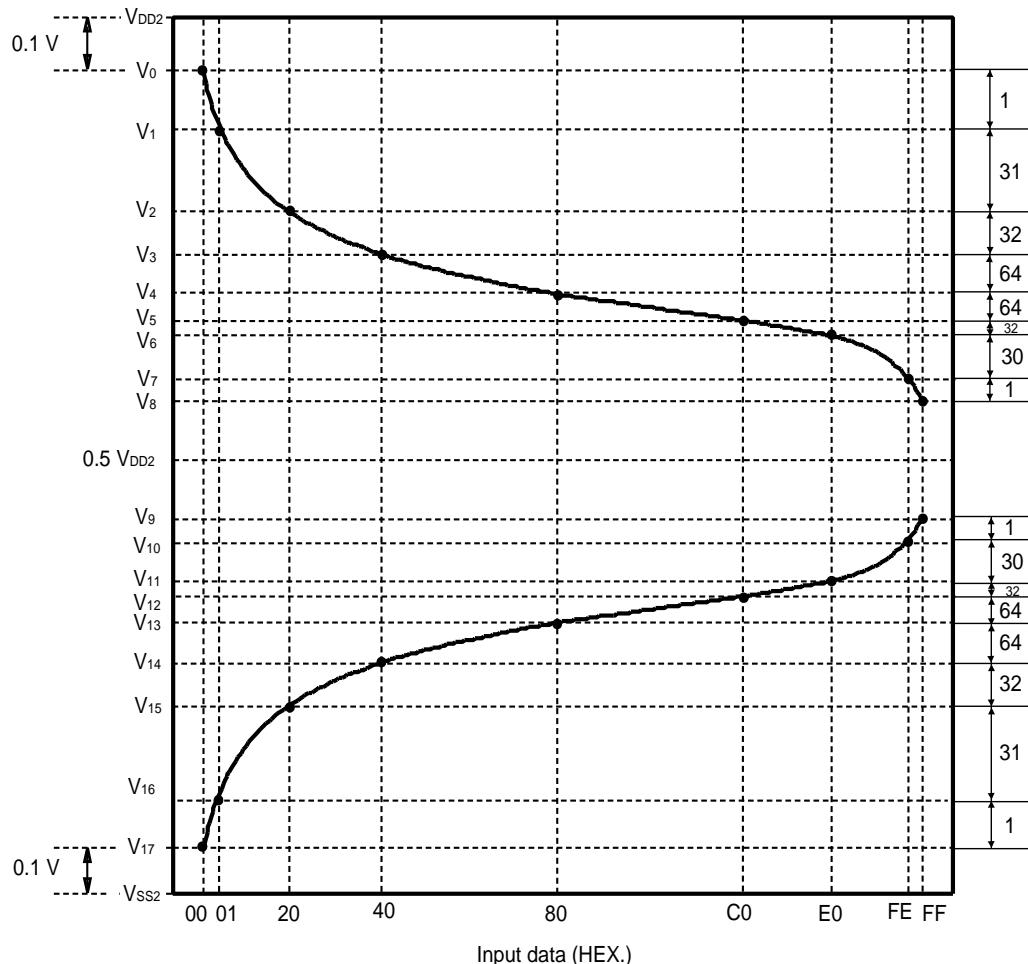
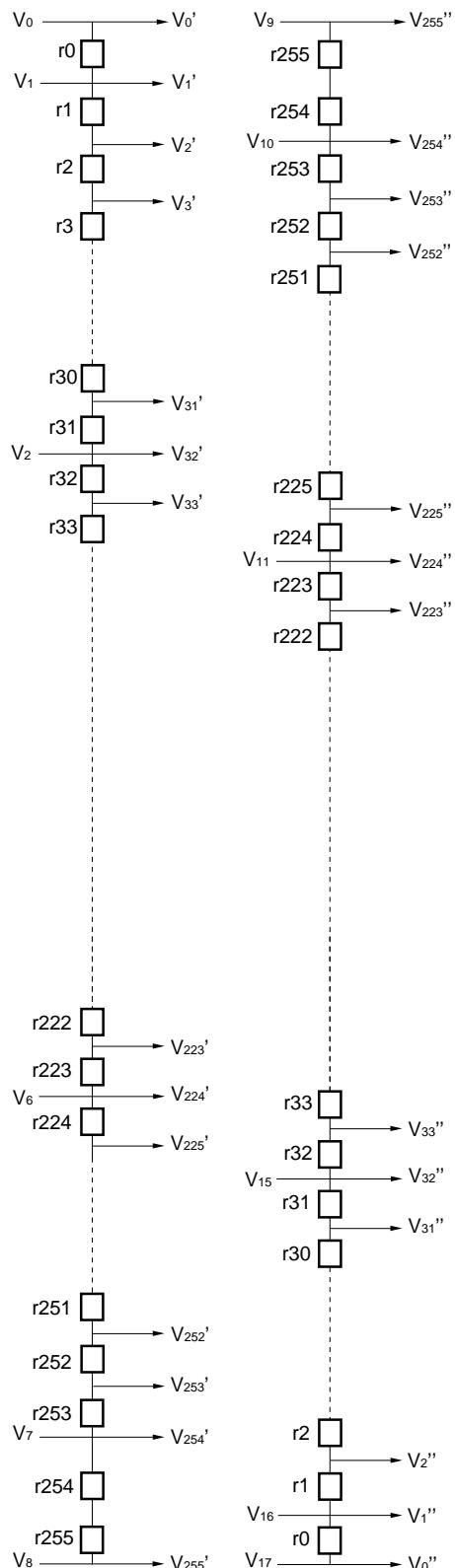


Figure 4-2.  $\gamma$ -corrected Voltages and Ladder Resistors Ratio

| r <sub>n</sub> | Ratio | Value |
|----------------|-------|-------|----------------|-------|-------|----------------|-------|-------|----------------|-------|-------|
| r0             | 31.50 | 630   | r64            | 2.25  | 45    | r128           | 1.00  | 20    | r192           | 1.00  | 20    |
| r1             | 27.50 | 550   | r65            | 2.25  | 45    | r129           | 1.00  | 20    | r193           | 1.00  | 20    |
| r2             | 24.00 | 480   | r66            | 2.25  | 45    | r130           | 1.00  | 20    | r194           | 1.00  | 20    |
| r3             | 21.50 | 430   | r67            | 2.25  | 45    | r131           | 1.00  | 20    | r195           | 1.00  | 20    |
| r4             | 19.00 | 380   | r68            | 2.00  | 40    | r132           | 1.00  | 20    | r196           | 1.25  | 25    |
| r5             | 17.50 | 350   | r69            | 2.00  | 40    | r133           | 1.00  | 20    | r197           | 1.25  | 25    |
| r6             | 16.50 | 330   | r70            | 2.00  | 40    | r134           | 1.00  | 20    | r198           | 1.25  | 25    |
| r7             | 15.00 | 300   | r71            | 2.00  | 40    | r135           | 1.00  | 20    | r199           | 1.25  | 25    |
| r8             | 14.00 | 280   | r72            | 2.00  | 40    | r136           | 1.00  | 20    | r200           | 1.25  | 25    |
| r9             | 13.00 | 260   | r73            | 2.00  | 40    | r137           | 1.00  | 20    | r201           | 1.25  | 25    |
| r10            | 12.00 | 240   | r74            | 2.00  | 40    | r138           | 1.00  | 20    | r202           | 1.25  | 25    |
| r11            | 11.00 | 220   | r75            | 2.00  | 40    | r139           | 1.00  | 20    | r203           | 1.25  | 25    |
| r12            | 10.00 | 200   | r76            | 1.75  | 35    | r140           | 1.00  | 20    | r204           | 1.25  | 25    |
| r13            | 9.50  | 190   | r77            | 1.75  | 35    | r141           | 1.00  | 20    | r205           | 1.25  | 25    |
| r14            | 9.50  | 190   | r78            | 1.75  | 35    | r142           | 1.00  | 20    | r206           | 1.25  | 25    |
| r15            | 9.00  | 180   | r79            | 1.75  | 35    | r143           | 1.00  | 20    | r207           | 1.25  | 25    |
| r16            | 8.50  | 170   | r80            | 1.75  | 35    | r144           | 1.00  | 20    | r208           | 1.25  | 25    |
| r17            | 8.00  | 160   | r81            | 1.75  | 35    | r145           | 1.00  | 20    | r209           | 1.25  | 25    |
| r18            | 7.50  | 150   | r82            | 1.75  | 35    | r146           | 1.00  | 20    | r210           | 1.25  | 25    |
| r19            | 7.50  | 150   | r83            | 1.75  | 35    | r147           | 1.00  | 20    | r211           | 1.25  | 25    |
| r20            | 7.00  | 140   | r84            | 1.75  | 35    | r148           | 1.00  | 20    | r212           | 1.25  | 25    |
| r21            | 6.50  | 130   | r85            | 1.75  | 35    | r149           | 1.00  | 20    | r213           | 1.25  | 25    |
| r22            | 6.50  | 130   | r86            | 1.50  | 30    | r150           | 1.00  | 20    | r214           | 1.25  | 25    |
| r23            | 6.00  | 120   | r87            | 1.50  | 30    | r151           | 1.00  | 20    | r215           | 1.25  | 25    |
| r24            | 6.00  | 120   | r88            | 1.50  | 30    | r152           | 1.00  | 20    | r216           | 1.25  | 25    |
| r25            | 5.50  | 110   | r89            | 1.50  | 30    | r153           | 1.00  | 20    | r217           | 1.25  | 25    |
| r26            | 5.50  | 110   | r90            | 1.50  | 30    | r154           | 1.00  | 20    | r218           | 1.50  | 30    |
| r27            | 5.50  | 110   | r91            | 1.50  | 30    | r155           | 1.00  | 20    | r219           | 1.50  | 30    |
| r28            | 5.00  | 100   | r92            | 1.50  | 30    | r156           | 1.00  | 20    | r220           | 1.50  | 30    |
| r29            | 5.00  | 100   | r93            | 1.50  | 30    | r157           | 1.00  | 20    | r221           | 1.50  | 30    |
| r30            | 5.00  | 100   | r94            | 1.50  | 30    | r158           | 1.00  | 20    | r222           | 1.50  | 30    |
| r31            | 4.50  | 90    | r95            | 1.50  | 30    | r159           | 1.00  | 20    | r223           | 1.50  | 30    |
| r32            | 4.50  | 90    | r96            | 1.50  | 30    | r160           | 1.00  | 20    | r224           | 1.50  | 30    |
| r33            | 4.50  | 90    | r97            | 1.50  | 30    | r161           | 1.00  | 20    | r225           | 2.00  | 40    |
| r34            | 4.00  | 80    | r98            | 1.50  | 30    | r162           | 1.00  | 20    | r226           | 2.00  | 40    |
| r35            | 4.00  | 80    | r99            | 1.50  | 30    | r163           | 1.00  | 20    | r227           | 2.00  | 40    |
| r36            | 4.00  | 80    | r100           | 1.50  | 30    | r164           | 1.00  | 20    | r228           | 2.00  | 40    |
| r37            | 4.00  | 80    | r101           | 1.50  | 30    | r165           | 1.00  | 20    | r229           | 2.00  | 40    |
| r38            | 3.75  | 75    | r102           | 1.50  | 30    | r166           | 1.00  | 20    | r230           | 2.50  | 50    |
| r39            | 3.75  | 75    | r103           | 1.50  | 30    | r167           | 1.00  | 20    | r231           | 2.50  | 50    |
| r40            | 3.50  | 70    | r104           | 1.50  | 30    | r168           | 1.00  | 20    | r232           | 2.50  | 50    |
| r41            | 3.50  | 70    | r105           | 1.50  | 30    | r169           | 1.00  | 20    | r233           | 3.00  | 60    |
| r42            | 3.50  | 70    | r106           | 1.50  | 30    | r170           | 1.00  | 20    | r234           | 3.00  | 60    |
| r43            | 3.50  | 70    | r107           | 1.50  | 30    | r171           | 1.00  | 20    | r235           | 3.00  | 60    |
| r44            | 3.25  | 65    | r108           | 1.50  | 30    | r172           | 1.00  | 20    | r236           | 3.50  | 70    |
| r45            | 3.25  | 65    | r109           | 1.50  | 30    | r173           | 1.00  | 20    | r237           | 3.50  | 70    |
| r46            | 3.00  | 60    | r110           | 1.25  | 25    | r174           | 1.00  | 20    | r238           | 4.00  | 80    |
| r47            | 3.00  | 60    | r111           | 1.25  | 25    | r175           | 1.00  | 20    | r239           | 4.00  | 80    |
| r48            | 3.00  | 60    | r112           | 1.25  | 25    | r176           | 1.00  | 20    | r240           | 4.50  | 90    |
| r49            | 3.00  | 60    | r113           | 1.25  | 25    | r177           | 1.00  | 20    | r241           | 5.00  | 100   |
| r50            | 3.00  | 60    | r114           | 1.25  | 25    | r178           | 1.00  | 20    | r242           | 5.00  | 100   |
| r51            | 3.00  | 60    | r115           | 1.25  | 25    | r179           | 1.00  | 20    | r243           | 5.50  | 110   |
| r52            | 2.75  | 55    | r116           | 1.25  | 25    | r180           | 1.00  | 20    | r244           | 6.00  | 120   |
| r53            | 2.75  | 55    | r117           | 1.25  | 25    | r181           | 1.00  | 20    | r245           | 6.50  | 130   |
| r54            | 2.75  | 55    | r118           | 1.25  | 25    | r182           | 1.00  | 20    | r246           | 7.00  | 140   |
| r55            | 2.75  | 55    | r119           | 1.25  | 25    | r183           | 1.00  | 20    | r247           | 7.50  | 150   |
| r56            | 2.50  | 50    | r120           | 1.25  | 25    | r184           | 1.00  | 20    | r248           | 8.00  | 160   |
| r57            | 2.50  | 50    | r121           | 1.25  | 25    | r185           | 1.00  | 20    | r249           | 8.50  | 170   |
| r58            | 2.50  | 50    | r122           | 1.25  | 25    | r186           | 1.00  | 20    | r250           | 9.00  | 180   |
| r59            | 2.50  | 50    | r123           | 1.25  | 25    | r187           | 1.00  | 20    | r251           | 9.50  | 190   |
| r60            | 2.50  | 50    | r124           | 1.25  | 25    | r188           | 1.00  | 20    | r252           | 10.50 | 210   |
| r61            | 2.50  | 50    | r125           | 1.25  | 25    | r189           | 1.00  | 20    | r253           | 11.50 | 230   |
| r62            | 2.25  | 45    | r126           | 1.00  | 20    | r190           | 1.00  | 20    | r254           | 12.50 | 250   |
| r63            | 2.25  | 45    | r127           | 1.00  | 20    | r191           | 1.00  | 20    | r255           | 25.00 | 500   |

**Caution There is no connection between V<sub>8</sub> and V<sub>9</sub> pin inside the IC.**





## 5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 8 bits  $\times$  1 RGB (3 dots)

Input width: 12 bits  $\times$  double edge (1-pixel data)

### (1) R/L = H (Right shift)

| Output | S <sub>1</sub>   | S <sub>2</sub>   | S <sub>3</sub>   | S <sub>4</sub>   | ... | S <sub>479</sub>   | S <sub>480</sub>   |
|--------|--|--|--|--|-----|--|--|
| Data   | D <sub>00P</sub> -D <sub>03P</sub> ,<br>D <sub>00N</sub> -D <sub>03N</sub> | D <sub>10P</sub> -D <sub>13P</sub> ,<br>D <sub>10N</sub> -D <sub>13N</sub> | D <sub>20P</sub> -D <sub>23P</sub> ,<br>D <sub>20N</sub> -D <sub>23N</sub> | D <sub>00P</sub> -D <sub>03P</sub> ,<br>D <sub>00N</sub> -D <sub>03N</sub> | ... | D <sub>10P</sub> -D <sub>13P</sub> ,<br>D <sub>10N</sub> -D <sub>13N</sub> | D <sub>20P</sub> -D <sub>23P</sub> ,<br>D <sub>20N</sub> -D <sub>23N</sub> |

### (2) R/L = L (Left shift)

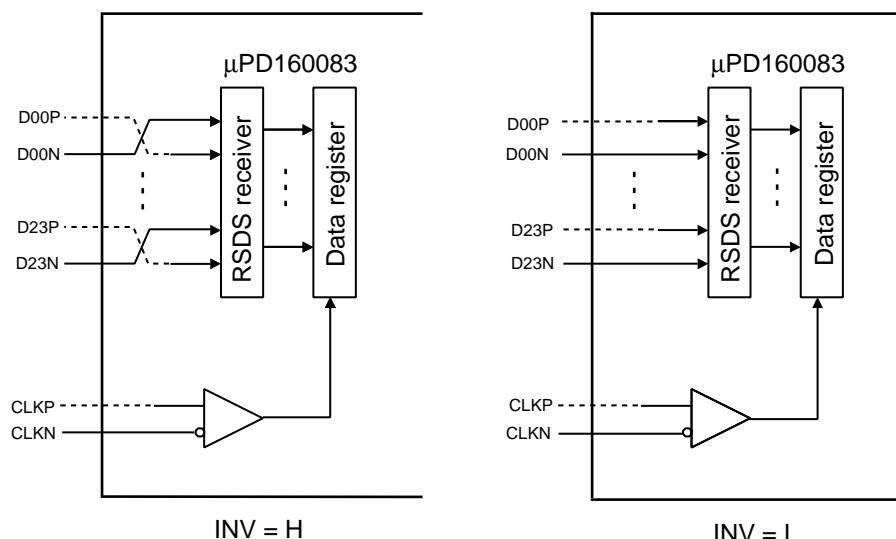
| Output | S <sub>1</sub>   | S <sub>2</sub>   | S <sub>3</sub>   | S <sub>4</sub>   | ... | S <sub>479</sub>   | S <sub>480</sub>   |
|--------|--|--|--|--|-----|--|--|
| Data   | D <sub>00P</sub> -D <sub>03P</sub> ,<br>D <sub>00N</sub> -D <sub>03N</sub> | D <sub>10P</sub> -D <sub>13P</sub> ,<br>D <sub>10N</sub> -D <sub>13N</sub> | D <sub>20P</sub> -D <sub>23P</sub> ,<br>D <sub>20N</sub> -D <sub>23N</sub> | D <sub>00P</sub> -D <sub>03P</sub> ,<br>D <sub>00N</sub> -D <sub>03N</sub> | ... | D <sub>10P</sub> -D <sub>13P</sub> ,<br>D <sub>10N</sub> -D <sub>13N</sub> | D <sub>20P</sub> -D <sub>23P</sub> ,<br>D <sub>20N</sub> -D <sub>23N</sub> |

| POL | S <sub>2n-1</sub> <sup>Note</sup> | S <sub>2n</sub> <sup>Note</sup> |
|-----|-----------------------------------|---------------------------------|
| H   | V <sub>0</sub> -V <sub>8</sub>    | V <sub>9</sub> -V <sub>17</sub> |
| L   | V <sub>9</sub> -V <sub>17</sub>   | V <sub>0</sub> -V <sub>8</sub>  |

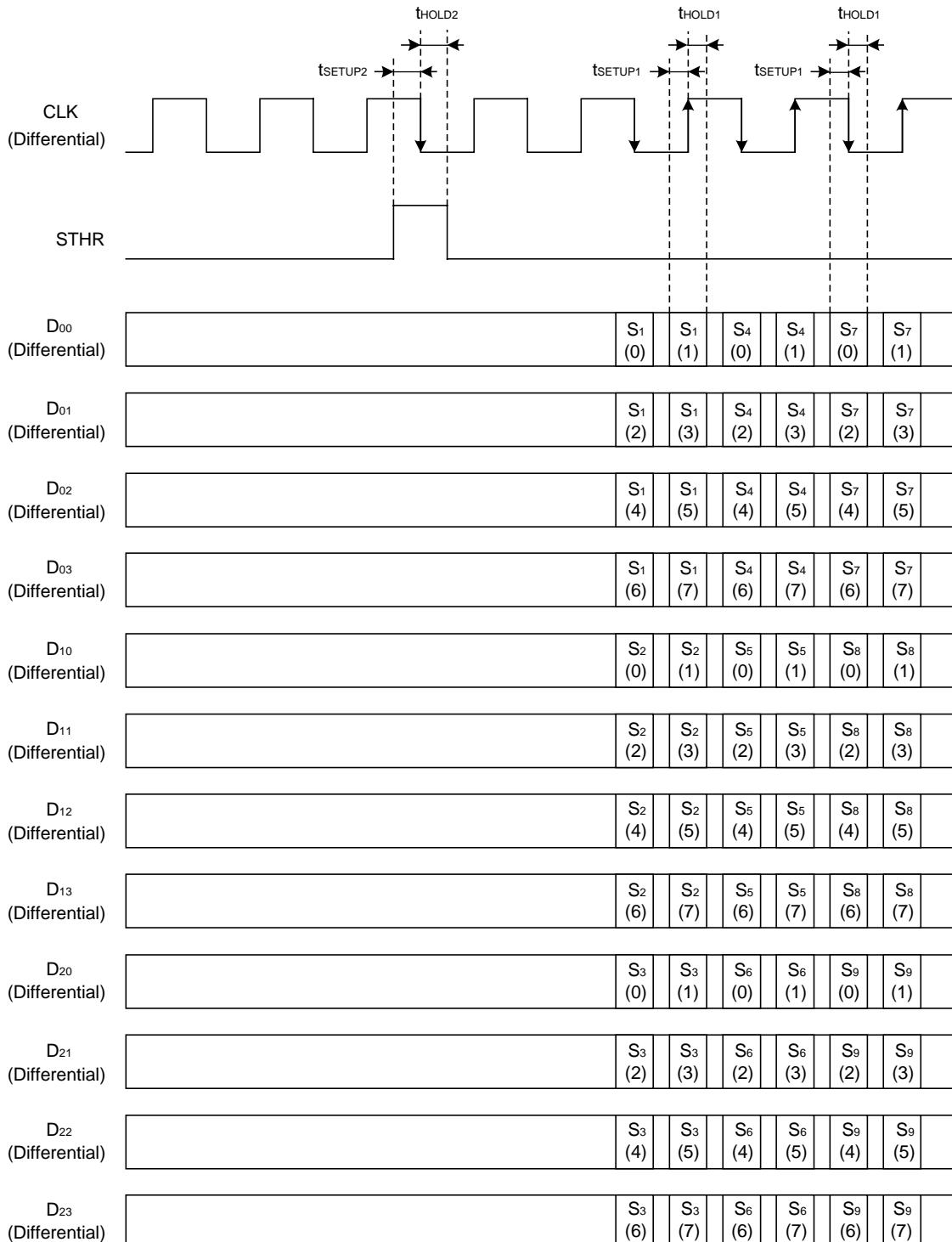
Note S<sub>2n-1</sub> (Odd output), S<sub>2n</sub> (Even output), n = 1, 2, ... 240

## 6. DATA INVERSION (INV)

INV controls the internal data inversion. When INV = H, the internal data is inverted and CLK is not inverted (See the figure as below). Using the INV pin, the RSDS data bus interface can be changed.



## 7. TIMING CHART AND RELATIONSHIP BETWEEN 8-BIT DATA AND DATA BUS LINE



**Remark** S<sub>n(0)</sub>: LSB, S<sub>n(7)</sub>: MSB

## 8. RELATIONSHIP BETWEEN MODE, STB, POL, MODE1 to MODE3 AND OUTPUT WAVEFORM

The  $\mu$ PD160083 has a various kind of output short function that can be controlled by MODE1 to MODE3. Please refer to the following description of each function and decide MODE1 to MODE3 after considering the suitable driving method.

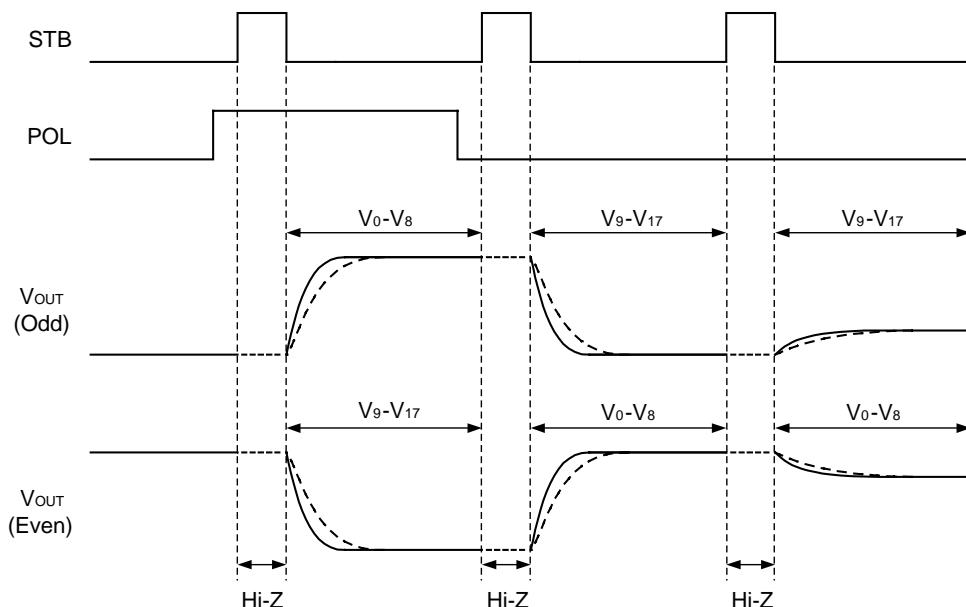
| MODE1     | MODE2     | MODE3     | Charge Sharing | Description of Output Short              |
|-----------|-----------|-----------|----------------|--|
| H or open | X         | X         | Non-active     | Output short doesn't work                |
| L         | H or open | X         | Active         | During STB = H                           |
|           | L         | H or open | Active         | During 34 CLKs after falling edge of STB |
|           | L         | Active    |                | During 68 CLKs after falling edge of STB |

**Remark** X: H or L

### (1) MODE1 = H or open

All outputs always become Hi-Z condition during STB = H at this mode. And output short function doesn't work and all output always start at the falling edge of STB (See figure 8-1).

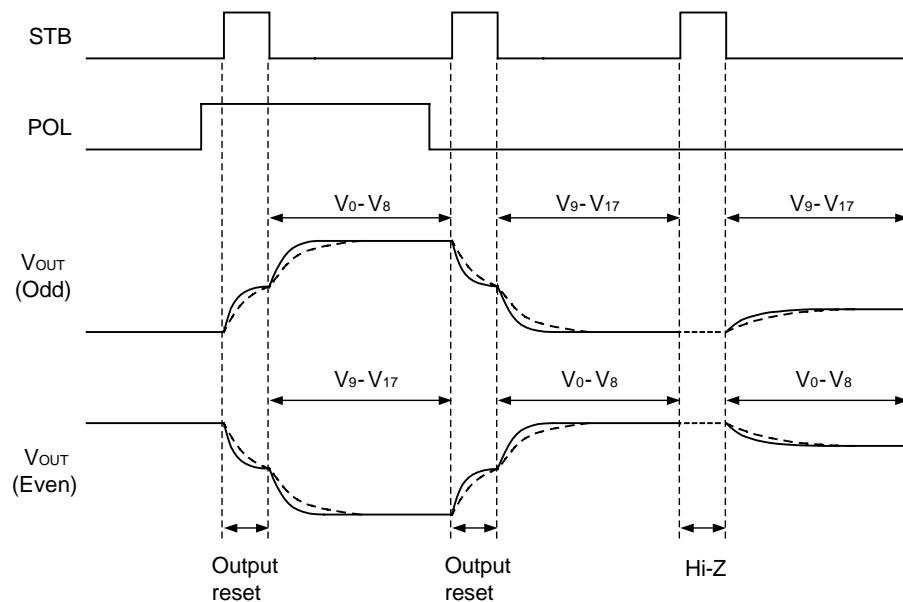
**Figure 8-1. MODE1 = H or open**



**Remark** --- : Repair Amp. output

**(2) MODE1 = L, MODE2 = H or open**

Output short function works during STB = H at this mode. So all outputs are started at the falling edge of STB (See figure 8-2). But output short function works only when POL signal is changed. So All output become Hi-Z condition during STB = H without any change of POL signal (See figure 8-2).

**Figure 8-2. MODE1 = L, MODE2 = H or open**

**Remark** --- : Repair Amp. output

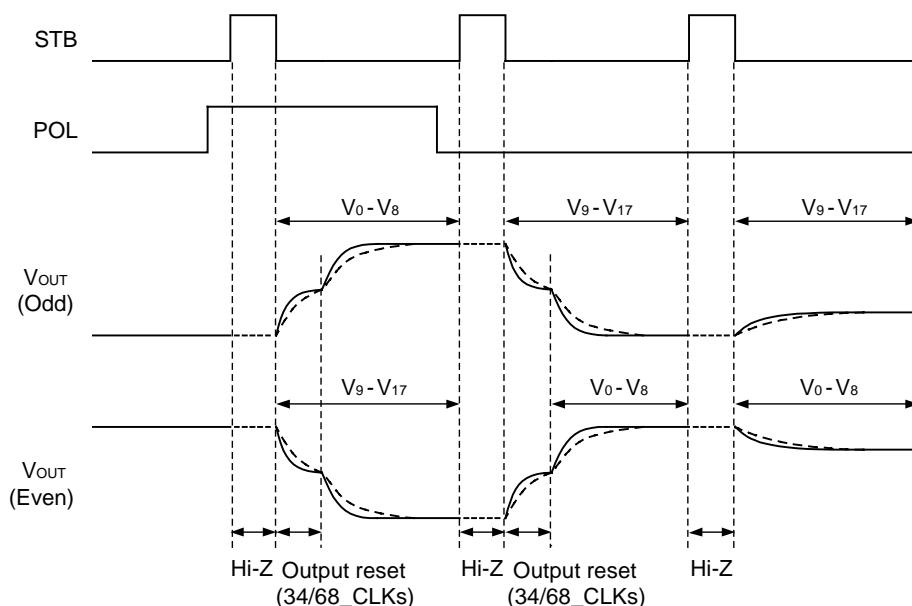
**(3) MODE1 = L, MODE2 = L**

All output always become Hi-Z condition during STB = H in this mode. And output short function works at the falling edge of STB during requested period by MODE3. At MODE3 = H, the driver IC counts 34 CLKs of output short period by itself, and count 68 CLKs at MODE = L. After finishing the output short period, the gray-scale voltage to the LCD panel is started. When POL signal is not changed, the gray-scale voltage to the LCD panel is started at the falling edge of STB without any change of POL signal (See figure 8-3).

| MODE3     | Output Short Period |
|-----------|---------------------|
| H or open | 34 CLKs             |
| L         | 68 CLKs             |

**Remark** MODE1 = L, MODE2 = L

**Figure 8-3. MODE1 = L, MODE2 = L**



**Remark** --- : Repair Amp. output

## 9. ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings ( $T_A = +25^\circ\text{C}$ , $V_{SS1D}, V_{SS1A} = V_{SS2} = 0 \text{ V}$ )

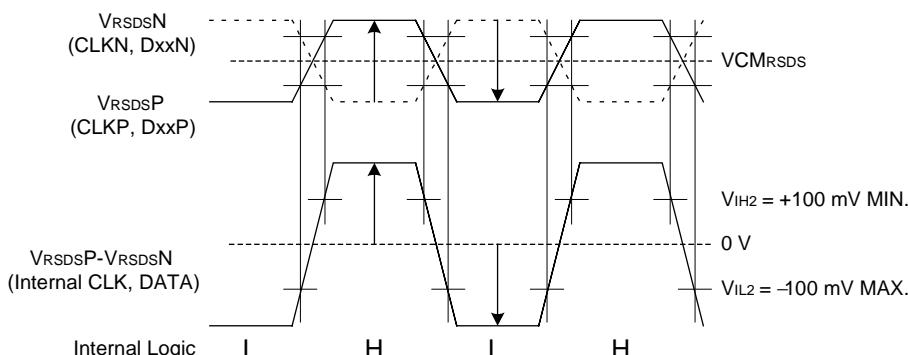
| Parameter                     | Symbol               | Ratings                 | Unit             |
|-------------------------------|----------------------|-------------------------|------------------|
| Logic Part Supply Voltage     | $V_{DD1D}, V_{DD1A}$ | -0.5 to +4.0            | V                |
| Driver Part Supply Voltage    | $V_{DD2}$            | -0.5 to +14.0           | V                |
| Logic Part Input Voltage      | $V_{I1}$             | -0.5 to $V_{DD1} + 0.5$ | V                |
| Driver Part Input Voltage     | $V_{I2}$             | -0.3 to $V_{DD2} + 0.3$ | V                |
| Logic Part Output Voltage     | $V_{O1}$             | -0.5 to $V_{DD1} + 0.5$ | V                |
| Driver Part Output Voltage    | $V_{O2}$             | -0.5 to $V_{DD2} + 0.5$ | V                |
| Operating Ambient Temperature | $T_A$                | -10 to +75              | $^\circ\text{C}$ |
| Storage Temperature           | $T_{stg}$            | -55 to +125             | $^\circ\text{C}$ |

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

### Recommended Operating Range ( $T_A = -10$ to $+75^\circ\text{C}$ , $V_{SS1D}, V_{SS1A} = V_{SS2} = 0 \text{ V}$ )

| Parameter   | Symbol               | Conditions                                      | MIN.   | TYP. | MAX.            | Unit |   |
|---|----------------------|---|--|------|-----------------|------|---|
| Logic Part Supply Voltage   | $V_{DD1D}, V_{DD1A}$ |   | 2.7  | 3.3  | 3.6             | V    |   |
| Driver Part Supply Voltage  | $V_{DD2}$            |   | 10.5   | 12.0 | 13.5            | V    |   |
| High-Level Input Voltage 1  | $V_{IH1}$            |   | 0.7 $V_{DD1}$                                |      | $V_{DD1}$       | V    |   |
| Low-Level Input Voltage 1   | $V_{IL1}$            |   | 0  |      | 0.3 $V_{DD1}$   | V    |   |
| High-Level Input Voltage 2<br>(Differential : $V_{RSDSN}-V_{RSDSN}$ ) | $V_{IH2}$            | CLK, $D_{xy}$<br>(x = 0 to 2)<br>(y = 0 to 3)   | $V_{CM} = 1.2 \text{ V}$ Note                | +100 | +200            | mV   |   |
| Low-Level Input Voltage 2<br>(Differential : $V_{RSDSN}-V_{RSDSN}$ )  | $V_{IL2}$            |   |  | -200 | -100            | mV   |   |
| Common Mode Input<br>Voltage  | $V_{CM}$             |   | $V_{OFF} = 200 \text{ mV}_{\text{p-p}}$ Note | 0.5  | 1.2             | 1.4  | V |
| Driver Part Output Voltage  | $V_O$                | S <sub>1</sub> to S <sub>480</sub> , RPO1, RPO2 | 0.1  |      | $V_{DD2} - 0.1$ | V    |   |
| $\gamma$ -Corrected Voltage   | $V_{NV}$             | $V_0-V_8$                                       | $0.5 V_{DD2}$                                |      | $V_{DD2} - 0.1$ | V    |   |
|   |                      | $V_9-V_{17}$                                    | 0.1  |      | 0.5 $V_{DD2}$   | V    |   |
| Clock Frequency   | $f_{CLK}$            | $V_{DD1} = 2.7 \text{ V}$                       |  |      | 70              | MHz  |   |
|   |                      | $V_{DD1} = 3.0 \text{ V}$                       |  |      | 85              | MHz  |   |

#### Note



**Remark**  $V_{CM} = (V_{CLKP} + V_{CLKN}) / 2$  or  $= (V_{DxxP} + V_{DxxN}) / 2$  (x = 0, 1, 2)  
 $V_{DIFF} = (V_{CLKP} - V_{CLKN}) / 2$  or  $= (V_{DxxP} - V_{DxxN}) / 2$  (x = 0, 1, 2)

Electrical Characteristics ( $T_A = -10$  to  $+75$  °C,  $V_{DD1} = 2.7$  to  $3.6$  V,  $V_{DD2} = 10.5$  to  $13.5$  V,  $V_{SS1} = V_{SS2} = 0$  V)

| Parameter  | Symbol            | Condition  | MIN.            | TYP.                      | MAX.                      | Unit       |
|--|-------------------|--|-----------------|---------------------------|---------------------------|------------|
| Input Leak Current   | $I_{IL}$          |  |                 |                           | $\pm 1.0$                 | $\mu$ A    |
| High-Level Output Voltage                                      | $V_{OH}$          | STHR (STHL), $I_{OH} = 0$ mA   | $V_{DD1} - 0.4$ |                           | $V_{DD1}$                 | V          |
| Low-Level Output Voltage                                       | $V_{OL}$          | STHR (STHL), $I_{OL} = 0$ mA   | $V_{SS1}$       |                           | $V_{SS1} + 0.4$           | V          |
| $\gamma$ -Corrected Resistance                                 | $R_\gamma$        | $V_{DD2} = 12.0$ V, $T_A = 25$ °C,<br>$V_0 - V_8 = V_9 - V_{17} = 5.0$ V | 11.91           | 17.02                     | 22.13                     | k $\Omega$ |
| Pull-up/pull-down Resistance                                   | $R_{PU}$          | $V_{DD1} = 3.3$ V, MODE1 to MODE3, LPC, TEST                             | 80              | 200                       | 500                       | k $\Omega$ |
| Driver Output Current  | $I_{VOH}$         | $S_1$ to $S_{480}$ , RPO1, RPO2,<br>$V_{DD2} = 12$ V                     |                 |                           | -70                       | $\mu$ A    |
|  | $I_{VOL}$         | $V_x = 1.0$ V,<br>$V_{OUT} = 1.5$ V <small>Note1</small>                 | 70              |                           |                           | $\mu$ A    |
| Output Voltage Deviation<br>( $DV_O$ )                         | $\Delta V_O$      | $V_O = 1.5$ V to $V_{DD2} - 1.5$ V.                                      |                 | $\pm 12$                  | $\pm 20$                  | mV         |
|  |                   | $V_O = 0.1$ to $1.5$ V,<br>$V_O = V_{DD2} - 1.5$ V to $V_{DD2} - 0.1$ V  |                 | $\pm 40$                  | $\pm 50$                  | mV         |
| Output Swing Voltage<br>Difference Deviation<br>( $DV_{RMS}$ ) | $\Delta V_{p-p1}$ | $V_O = 1.5$ V to $V_{DD2} - 1.5$ V                                       |                 | $\pm 6$                   | $\pm 10$                  | mV         |
|  | $\Delta V_{p-p2}$ | $V_O = 0.1$ to $1.5$ V,<br>$V_O = V_{DD2} - 1.5$ V to $V_{DD2} - 0.1$ V  |                 | $\pm 30$                  | $\pm 50$                  | mV         |
| Output Swing Voltage<br>Average Deviation                      | $AV_O$            | Input data: 80H  |                 | $\pm 1$                   | $\pm 7.5$                 | mV         |
| Logic Part Dynamic<br>Current Consumption 1                    | $I_{DD11}$        | $V_{DD1}$ <small>Note1 to note3</small>                                  |                 | 2.5 <small>Note2</small>  | 6.0 <small>Note3</small>  | mA         |
| Logic Part Dynamic<br>Current Consumption 2                    | $I_{DD12}$        | $V_{DD1}$ , <small>Note1 to note3</small>                                |                 | 2.0 <small>Note4</small>  | 6.0 <small>Note5</small>  | mA         |
| Driver Part Dynamic<br>Current Consumption                     | $I_{DD2}$         | $V_{DD2}$ , with no load,<br>RPI1, RPI2 are not floating                 |                 | 15.0 <small>Note6</small> | 45.0 <small>Note7</small> | mA         |

**Notes 1.**  $V_x$  refers to the output voltage of analog output pins  $S_1$  to  $S_{384}$ .

$V_{OUT}$  refers to the voltage applied to analog output pins  $S_1$  to  $S_{384}$ .

2.  $f_{CLKP}, f_{CLKN} = 67.5$  MHz,  $f_{STB} = 80.0$  kHz, test pattern = dot inversion,  $T_A = 25$  °C,  $V_{DD1} = 3.0$  V
3.  $f_{CLKP}, f_{CLKN} = 67.5$  MHz,  $f_{STB} = 80.0$  kHz, test pattern = dot inversion,  $V_{DD1} = 3.6$  V
4.  $f_{CLKP}, f_{CLKN} = 54.0$  MHz,  $f_{STB} = 64.9$  kHz, test pattern = dot inversion,  $T_A = 25$  °C,  $V_{DD1} = 3.0$  V
5.  $f_{CLKP}, f_{CLKN} = 54.0$  MHz,  $f_{STB} = 64.9$  kHz, test pattern = dot inversion,  $V_{DD1} = 3.6$  V
6.  $f_{CLKP}, f_{CLKN} = 67.5$  MHz,  $f_{STB} = 80.0$  kHz, test pattern = dot inversion,  $T_A = 25$  °C,  $V_{DD2} = 12.0$  V
7.  $f_{CLKP}, f_{CLKN} = 67.5$  MHz,  $f_{STB} = 80.0$  kHz, test pattern = dot inversion,  $V_{DD2} = 13.5$  V

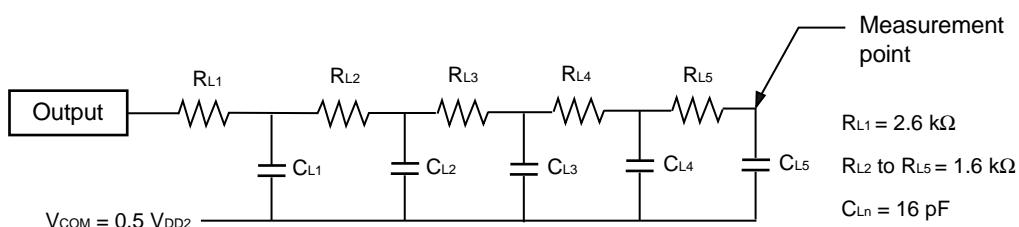
Switching Characteristics ( $T_A = -10$  to  $+75$  °C,  $V_{DD1} = 2.7$  to  $3.6$  V,  $V_{DD2} = 10.5$  to  $13.5$  V,  $V_{SS1} = V_{SS2} = 0$  V)

| Parameter                | Symbol                       | Condition   |                      | MIN. | TYP. | MAX. | Unit |
|--------------------------|------------------------------|---|----------------------|------|------|------|------|
| Start Pulse Delay Time   | $t_{PLH1}$                   | $C_L = 15$ pF   | $V_{DD1} < 3.0$ V    | 4    |      | 12.5 | ns   |
|                          |                              |   | $V_{DD1} \geq 3.0$ V | 4    |      | 10.0 | ns   |
| Driver Output Delay Time | $t_{PLH2}$ Note <sup>1</sup> | $V_{DD2} = 12.0$ V, RPO1, RPO2,<br>S <sub>1</sub> to S <sub>480</sub> , $R_L = 9$ kΩ, $C_L = 80$ pF |                      |      | 4    | 5    | μs   |
|                          | $t_{PLH3}$ Note <sup>2</sup> |   |                      |      | 5    | 8    | μs   |
|                          | $t_{PHL2}$ Note <sup>1</sup> |   |                      |      | 4    | 5    | μs   |
|                          | $t_{PHL3}$ Note <sup>2</sup> |   |                      |      | 5    | 8    | μs   |
|                          | $t_{PLH4}$ Note <sup>1</sup> |   |                      |      | 4    | 5    | μs   |
|                          | $t_{PLH5}$ Note <sup>2</sup> |   |                      |      | 5    | 8    | μs   |
|                          | $t_{PHL4}$ Note <sup>1</sup> |   |                      |      | 4    | 5    | μs   |
|                          | $t_{PHL5}$ Note <sup>2</sup> |   |                      |      | 5    | 8    | μs   |
| Input Capacitance        | $C_{I1}$                     | Logic input besides STHR (STHL),<br>$T_A = 25$ °C   |                      |      |      | 10   | pF   |
|                          | $C_{I2}$                     | STHR (STHL), $T_A = 25$ °C  |                      |      |      | 15   | pF   |

**Notes 1.** The value is specified when the drive voltage value reaches the target output voltage level of  $\pm 10\%$ .

**2.** The value is specified when the drive voltage value reaches the target output voltage level of  $\pm 0.02$  V  
(Condition:  $V_o = 3.0$  V  $\leftrightarrow$   $12.0$  V).

## &lt;Test condition&gt;



**Timing Requirement ( $T_A = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD1} = 2.7$  to  $3.6\text{V}$ ,  $V_{SS1} = 0\text{ V}$ ,  $t_r = t_f = 3.0\text{ ns (CMOS)}$ ,  
 $t_r = t_f = 1.0\text{ ns (RSDS)}$ )**

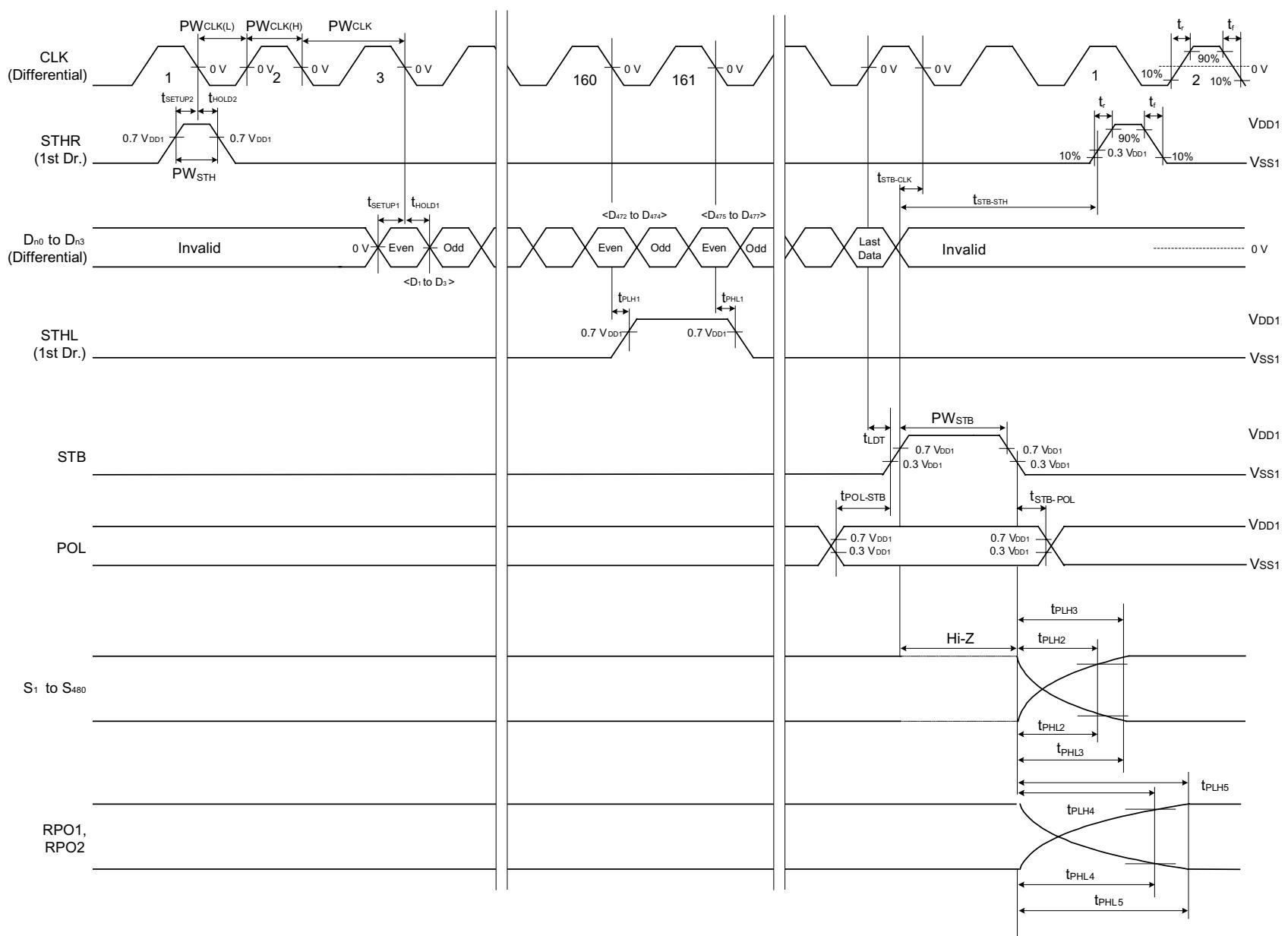
| Parameter                        | Symbol        | Condition  | MIN. | TYP. | MAX. | Unit |
|----------------------------------|---------------|--|------|------|------|------|
| Clock Period                     | $PW_{CLK}$    | $V_{DD1} = 2.7\text{ V}$   | 14.3 |      |      | ns   |
|                                  |               | $V_{DD1} = 3.0\text{ V}$   | 11.8 |      |      | ns   |
| Clock Pulse High Period          | $PW_{CLK(H)}$ |  | 5    |      |      | ns   |
| Clock Pulse Low Period           | $PW_{CLK(L)}$ |  | 5    |      |      | ns   |
| Data Setup Time                  | $t_{SETUP1}$  | $V_{DD1} = 2.7\text{ V}$   | 3    |      |      | ns   |
|                                  |               | $V_{DD1} = 3.0\text{ V}$   | 2    |      |      | ns   |
| Data Hold Time                   | $t_{HOLD1}$   | $V_{DD1} = 2.7\text{ V}$   | 1    |      |      | ns   |
|                                  |               | $V_{DD1} = 3.0\text{ V}$   | 0    |      |      | ns   |
| Start Pulse Setup Time           | $t_{SETUP2}$  |  | 1    |      |      | ns   |
| Start Pulse Hold Time            | $t_{HOLD2}$   |  | 3    |      |      | ns   |
| Start Pulse "H" Width            | $PW_{STH}$    |  | 1    |      | 2    | CLKP |
| STB Pulse "H" Width              | $PW_{STB}$    |  | 1    |      |      | us   |
| Last Data Timing                 | $t_{LDT}$     |  | 1    |      |      | CLKP |
| STB-CLK Time                     | $t_{STB-CLK}$ | $STB \uparrow \rightarrow CLKP, CLKN \downarrow$                 | 3    |      |      | ns   |
| Time Between STB and Start Pulse | $t_{STB-STH}$ | $STB \uparrow \rightarrow STHR (STHL) \uparrow$                  | 5    |      |      | CLKP |
| POL-STB Time                     | $t_{POL-STB}$ | $POL \uparrow \text{ or } \downarrow \rightarrow STB \uparrow$   | 14   |      |      | ns   |
| STB-POL Time                     | $t_{STB-POL}$ | $STB \downarrow \rightarrow POL \downarrow \text{ or } \uparrow$ | 10   |      |      | ns   |

**Remark**  $t_r, t_f$  are defined 10 to 90% of each signal amplitude.

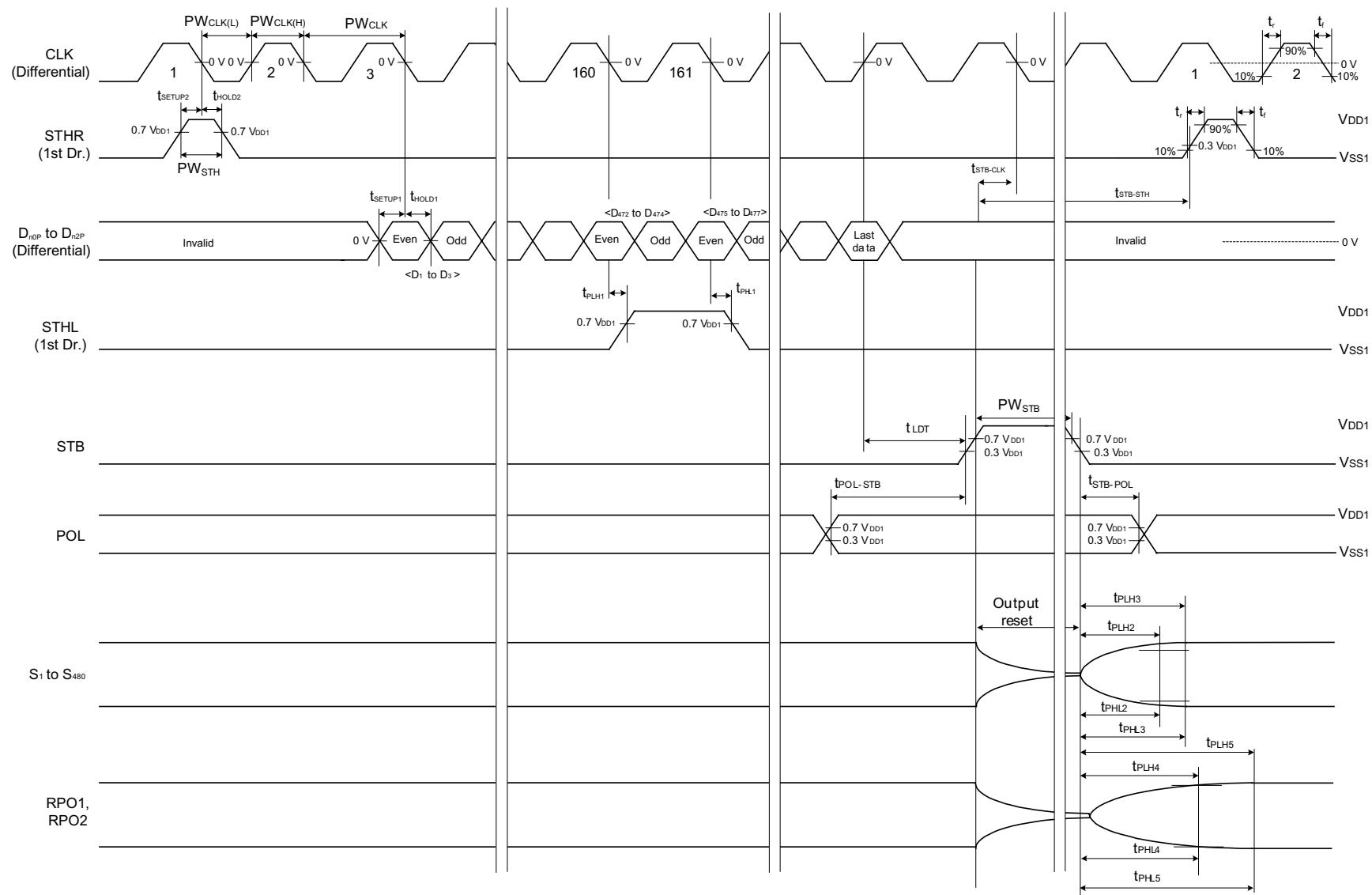
### Switching Characteristics Waveform (R/L = H)

Unless otherwise specified, the input level is defined to be  $V_H = 0.7 V_{DD1}$ ,  $V_L = 0.3 V_{DD1}$  at CMOS signal and 0 V at differential signal (RSDS).

**<MODE1 = H>**



&lt;MODE1 = L, MODE2 = H&gt;



## 10. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the  $\mu$ PD160010.

For more details, refer to the

[Semiconductor Device Mount Manual] (<http://www.necel.com/pkg/en/mount/index.html>)

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

$\mu$ PD160083N-xxx: TCP (TAB Package)

| Mounting Condition | Mounting Method                   | Condition   |
|--------------------|-----------------------------------|---|
| Thermocompression  | Soldering                         | Heating tool 300 to 350°C, heating for 2 to 3 sec, pressure 100g (per solder).  |
|                    | ACF<br>(Adhesive Conductive Film) | Temporary bonding 70 to 100°C, pressure 3 to 8 kg/cm <sup>2</sup> , time 3 to 5 sec.<br>Real bonding 165 to 180°C pressure 25 to 45 kg/cm <sup>2</sup> , time 30 to 40 sec.<br>(When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.) |

**Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.**

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V<sub>DD</sub> or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.