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Status	Product Specification
ECL Products	

100117

Triple 1–2–2 Input OR–AND/ OR–AND–INVERT Gate

FEATURES

- **Typical propagation delay: 1.4ns for the data inputs, 0.75ns for the Enable Inputs**
- **Typical supply current ($-I_{EE}$): 57mA**

DESCRIPTION

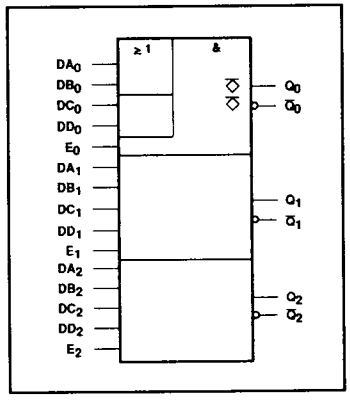
The 100117 has three OR/AND gates with True and Complementary outputs.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$DA_0 - DA_2$, $DB_0 - DB_2$, $DC_0 - DC_2$, $DD_0 - DD_2$	Data Inputs
$E_0 - E_2$	Enable Inputs
$Q_0 - Q_2$	True Data Outputs
$\overline{Q}_0 - \overline{Q}_2$	Complementary Data Outputs

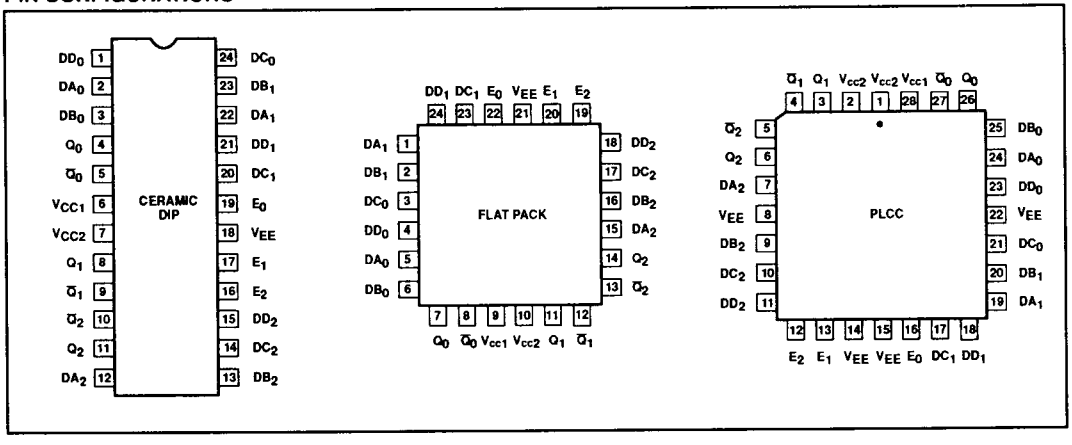
IEC/IEEE SYMBOL



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100117F
24–Pin Ceramic Flat Pack	100117Y
28–Pin PLCC	100117A

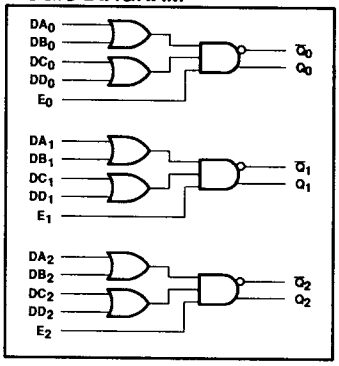
PIN CONFIGURATIONS



Gate

100117

LOGIC DIAGRAM

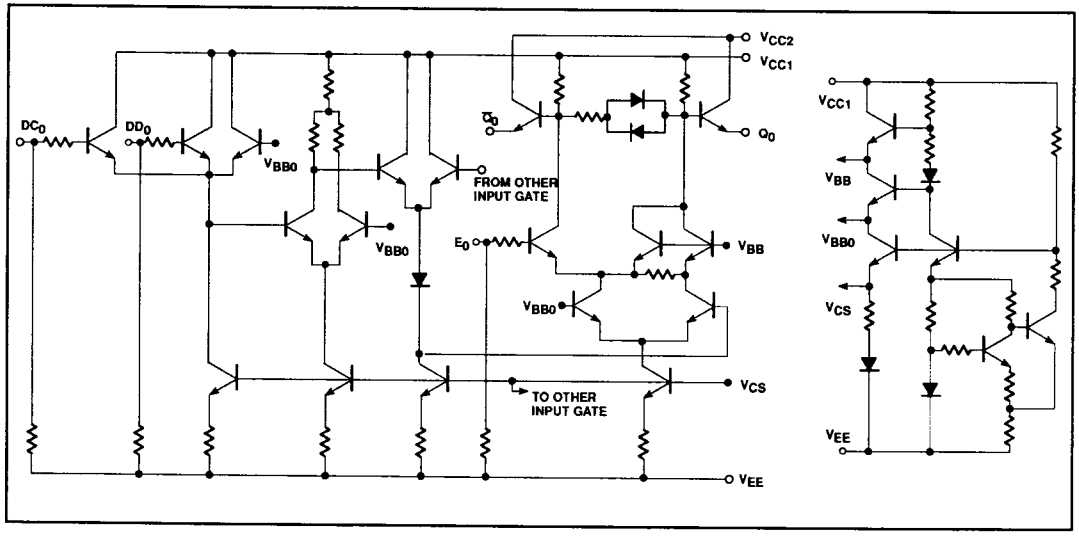


FUNCTION TABLE

INPUTS					OUTPUTS	
E_n	DA_n	DB_n	DC_n	DD_n	Q_n	$\overline{Q}_n$
L	X	X	X	X	L	H
X	X	X	L	L	L	H
X	L	L	X	X	L	H
H	H	X	H	X	H	L
H	X	H	X	H	H	L
H	X	H	H	X	H	L
H	H	X	X	H	H	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

$V_{CC1} = V_{CC2}$ = ground, $T_A = 0°C$ to $+85°C$ unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	−7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	−55	mA
T_S	Storage temperature range	−65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					260	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}.			37	57	79	mA

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n, DC_n, DD_n, to Q_n, $\overline{Q}_n$	Waveform 1	0.90 0.90	2.60 2.60	0.90 0.90	2.50 2.50	0.90 0.90	2.60 2.60	ns ns
t_{PLH} t_{PHL}	Propagation delay E_n to Q_n, $\overline{Q}_n$		0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.40 1.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.20 1.20	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n, DC_n, DD_n, to Q_n, $\overline{Q}_n$	Waveform 1	0.90 0.90	2.60 2.60	0.90 0.90	2.50 2.50	0.90 0.90	2.60 2.60	ns ns
t_{PLH} t_{PHL}	Propagation delay E_n to Q_n, $\overline{Q}_n$		0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.40 1.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.20 1.20	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n, DC_n, DD_n, to Q_n, $\overline{Q}_n$	Waveform 1	0.90 0.90	2.40 2.40	0.90 0.90	2.30 2.30	0.90 0.90	2.40 2.40	ns ns
t_{PLH} t_{PHL}	Propagation delay E_n to Q_n, $\overline{Q}_n$		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.20 1.20	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.20 1.20	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

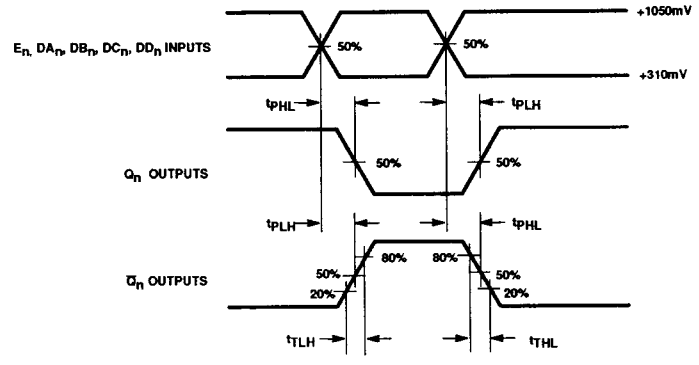
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} =$ ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n, DC_n, DD_n, to Q_n, $\overline{Q}_n$	Waveform 1	0.90 0.90	2.40 2.40	0.90 0.90	2.30 2.30	0.90 0.90	2.40 2.40	ns ns
t_{PLH} t_{PHL}	Propagation delay E_n to Q_n, $\overline{Q}_n$		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.20 1.20	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.20 1.20	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.