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ECL Products	

10116
Line Receiver

Triple Differential Line Receiver

FEATURES

- **Typical propagation delay: 2.4ns**
- **Typical supply current ($-I_{EE}$): 17mA**

DESCRIPTION

The 10116 is a Triple Differential Line Receiver with low-impedance emitter-follower complementary outputs.

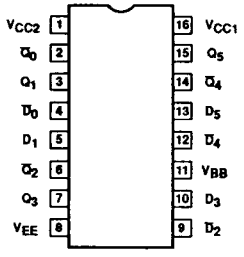
Intended primarily to receive data from twisted-pair lines, this device is also suitable for minicomputers, testing and instrumentation. It can also be used as a sense amplifier for MOS RAMs as a MOS-to-ECL interface circuit; as a high-speed comparator and having an internal reference supply voltage (V_{BB}) output, it can operate as a Schmitt Trigger.

One input from any unused amplifier in a package must be tied to V_{BB}.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10116N
16–Pin Ceramic DIP	10116F
16–Pin SO	10116D

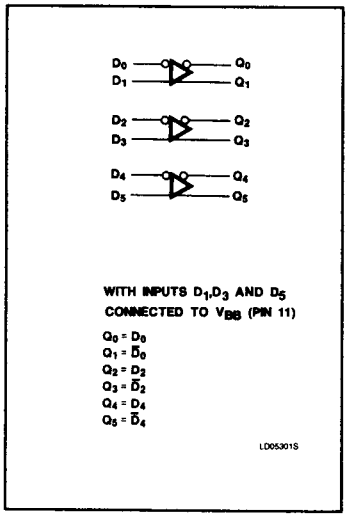
PIN CONFIGURATION



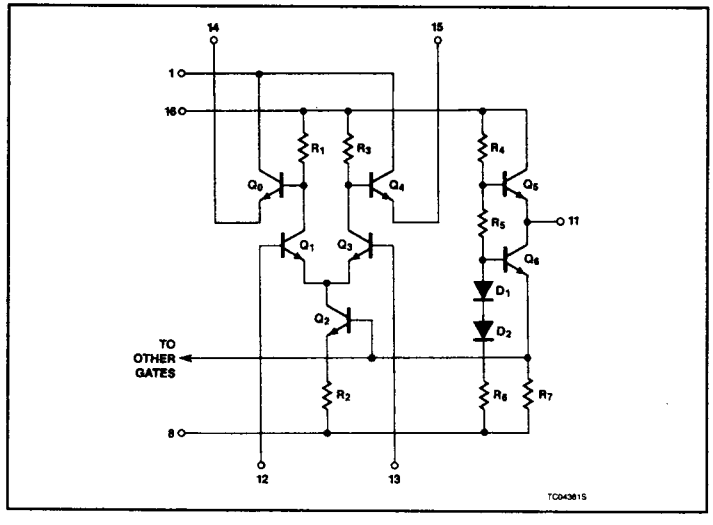
PIN DESCRIPTION

PINS	DESCRIPTION
$\overline{D}_0$, $\overline{D}_2$, $\overline{D}_4$; D_1, D_3, D_5	Data Inputs
V_{BB}	Reference Bias Voltage Output
Q_1, Q_3, Q_5	Data Outputs (OR)
$\overline{Q}_0$, $\overline{Q}_2$, $\overline{Q}_4$	Data Outputs (NOR)

LOGIC DIAGRAM



SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	For Q_n outputs, apply V_{ILMIN} to each inverting input, one at a time, w/ V_{IHMAX} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs. For $\overline{Q}_n$ outputs, apply V_{IHMAX} to each inverting input, one at a time, with V_{ILMIN} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs.[4]	–1060		–890	mV
		$T_A = +25°C$		–960		–810	mV
		$T_A = +85°C$		–890		–700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	For Q_n outputs, apply V_{ILT} to each inverting input, one at a time, w/ V_{IHMAX} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs. For $\overline{Q}_n$ outputs, apply V_{IHT} to each inverting input, one at a time, with V_{ILMIN} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs.[4]	–1080			mV
		$T_A = +25°C$		–980			mV
		$T_A = +85°C$		–910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to each inverting input, one at a time, w/ V_{ILMIN} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs. For $\overline{Q}_n$ outputs, apply V_{ILT} to each inverting input, one at a time, with V_{IHMAX} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs.[4]			–1655	mV
		$T_A = +25°C$				–1630	mV
		$T_A = +85°C$				–1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to each inverting input, one at a time, w/ V_{ILMIN} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs. For $\overline{Q}_n$ outputs, apply V_{ILMIN} to each inverting input, one at a time, with V_{IHMAX} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs.[4]	–1890		–1675	mV
		$T_A = +25°C$		–1850		–1650	mV
		$T_A = +85°C$		–1825		–1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each inverting input under test, one at a time, w/ V_{ILMIN} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs. Apply V_{IHMAX} to each non–inverting input under test, one at a time, with V_{ILMIN} applied to all other non–inverting inputs and V_{BB} applied to all inverting inputs.[4]			150	µA
		$T_A = +25°C$				95	µA
		$T_A = +85°C$				95	µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$	Apply V_{ILMIN} to all inverting inputs. Apply V_{BB} to all non–inverting inputs.			23	mA
		$T_A = +25°C$			17	21	mA
		$T_A = +85°C$				23	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation	$T_A = +25°C$			0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation	$T_A = +25°C$			0.148		V/V
V_{BB}	Reference voltage	$T_A = -30°C$	All inverting or all non–inverting input pins are tied to the V_{BB} pin during measurement.	–1420		–1280	mV
		$T_A = +25°C$		–1350	–1290	–1230	mV
		$T_A = +85°C$		–1295		–1150	mV
$-I_{CBO}$	Input leakage current	$T_A = -30°C$	Apply V_{EE} to each inverting input under test, one at a time, w/ V_{ILMIN} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs.[4]			1.5	µA
		$T_A = +25°C$				1.0	µA
		$T_A = +85°C$				1.0	µA

See notes on following page.

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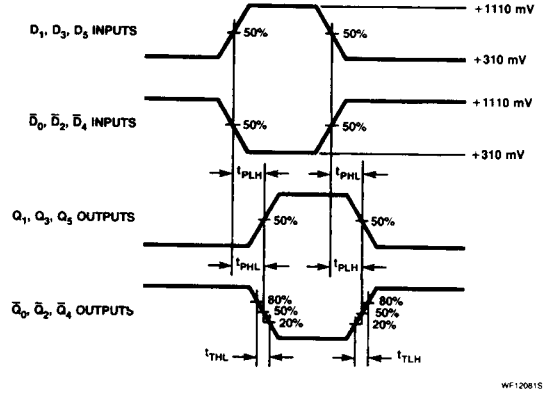
NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.
4. Refer to DC Test Circuit.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.00 1.00	3.10 3.10	1.00 1.00	2.00 2.00	2.90 2.90	1.00 1.00	3.30 3.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{D}_n$ to Q_n		1.00 1.00	3.10 3.10	1.00 1.00	2.00 2.00	2.90 2.90	1.00 1.00	3.30 3.30	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.10 1.10	3.60 3.60	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

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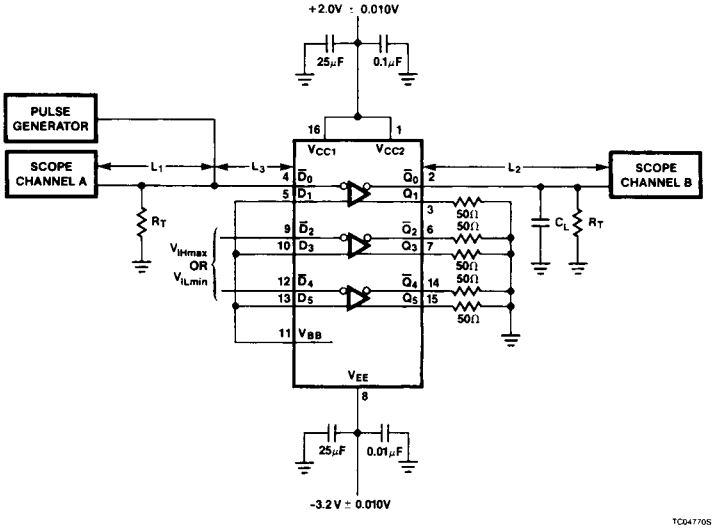
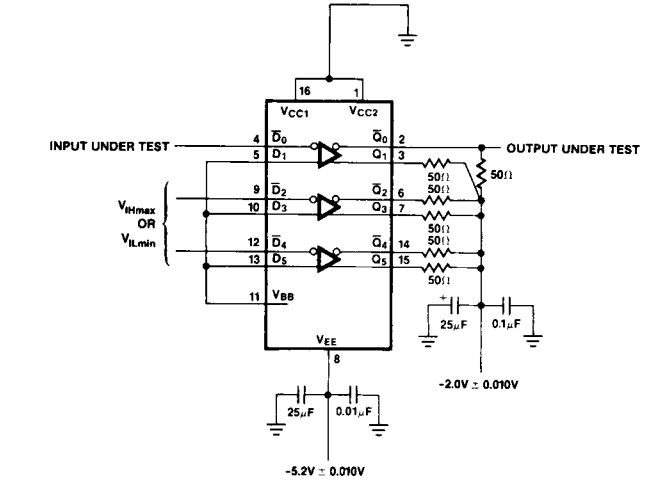
AC TEST CIRCUIT



NOTES:

1. $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to V_{CC}. 0.01μF and 25μF from GND to V_{EE} (0.01 and 0.1uF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lesd length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 are equal length 50Ω impedance lines. L_3, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance $\leq$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

DC TEST CIRCUIT



NOTES:

1. $V_{CC1} = V_{CC2} = 0V$ (GND), $V_{EE} = -5.2V \pm 0.010V$.
2. Decoupling 0.01μF and 25μF from GND to V_{EE}. 0.1μF and 25μF from GND to V_T (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to V_T.
5. All 50Ω resistors should have tolerance of ± 1% or better.