82595TX
ISA/PCMCIA HIGH INTEGRATION ETHERNET CONTROLLER

- **Optimal Integration for Lowest Cost Solution**
  - — Glueless 8-Bit/16-Bit ISA/PCMCIA 2.0 Bus Interface
  - — Provides Fully 802.3 Compliant AUI and TPE Serial Interface
  - — Local DRAM Support up to 64 Kbytes
  - — FLASH/EPROM Boot Support up to 1 Mbyte for Diskless Workstations
  - — Hardware and Software Portable between Motherboard, Adapter, and PCMCIA LAN Card Solution
- **High Performance Networking Functions**
  - — Concurrent Processing Functionality for Enhanced Performance
  - — 16-Bit/32-Bit IO Accesses to Local DRAM with Zero Added Wait-States
  - — Ring Buffer Structure for Continuous Frame Reception and Transmit Chaining
  - — Automatic Retransmission on Collision
  - — Automatically Corrects TPE Polarity Switching Problems
- **Low Power CHMOS IV Technology**
- **Ease of Use**
  - — Integrated Plug N' Play™ Hardware Functionality
  - — EEPROM Interface to Support Jumperless Designs
  - — Software Structures Optimized to Reduce Processing Steps
  - — Automatically Maps into Unused PC IO Locations to Help Eliminate LAN Setup Problems
  - — All Software Structures Contained in One 16-Byte IO Space
  - — JTAG Port for Reduced Board Testing Times
  - — Automatic or Manual Switching between TPE and AUI Ports
- **Power Management**
  - — SL Compatible SMOUT Power Down Input
  - — Software Power Down Command for Non-SL Systems
- **144-Lead tQFP Package Provides Smallest Available Form Factor**
- **100% Backwards Hardware/Software Compatible to 82595**

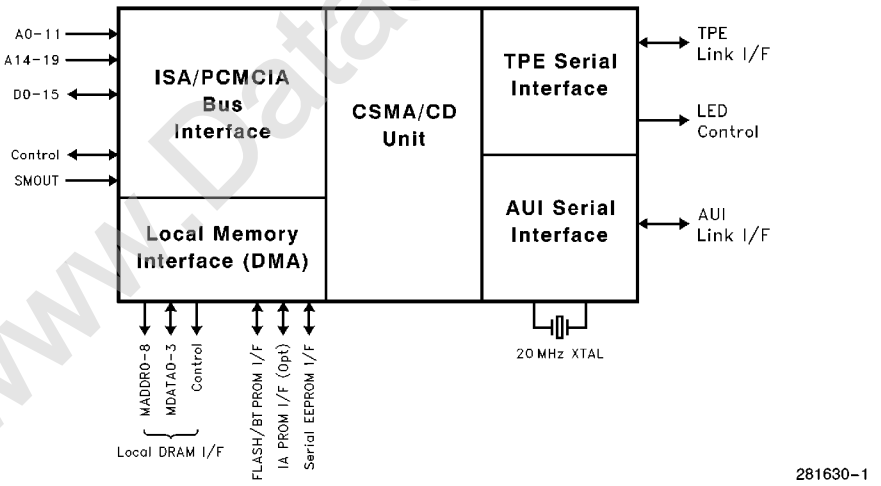

Figure 1. 82595TX Block Diagram

October 1995 Order Number: 281630-001

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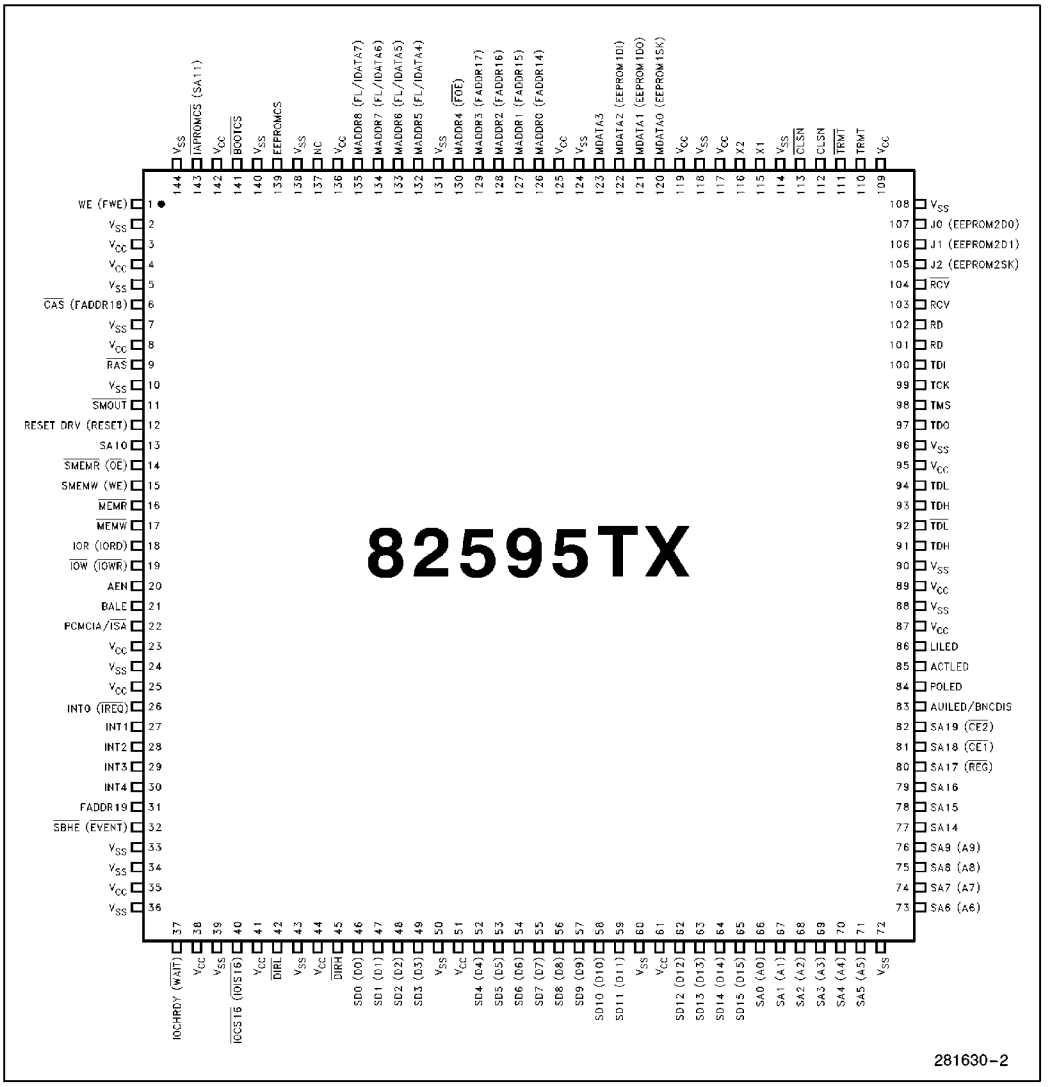


Figure 2. 82595TX Pinout

1.0 INTRODUCTION

1.1 82595TX Overview

The 82595TX is a highly integrated, high performance LAN controller which provides a cost effective LAN solution for ISA compatible Personal Computer (PC) motherboards (both desktop and portable), add-on ISA adapter boards, and PCMCIA cards. The 82595TX integrates all of the major functions of a buffered LAN solution into one chip with the exception of the local buffer memory, which is implemented by adding one DRAM component to the LAN solution. The 82595TX's new Concurrent Processing feature significantly enhances throughput performance. Both system bus and serial link activities occur concurrently, allowing the 82595TX to maximize network bandwidth by minimizing delays associated with transmit or receiving frames. The 82595TX's bus interface is a glueless attachment to either an ISA or PCMCIA version 2.0 bus. Its serial interface provides a Twisted Pair Ethernet (TPE) and an Attachment Unit Interface (AUI) connection. By integrating the majority of the LAN solution functions into one cost effective component, production cost saving can be achieved as well as significantly decreasing the design time for a solution. This level of integration also allows an 82595TX solution to be ported between different applications (PC motherboards, adapters, and PCMCIA IO cards), while maintaining a compatible hardware and software base. This results in further savings in both hardware and software development costs for manufacturers expanding into different applications i.e., an ISA adapter vendor producing PCMCIA IO cards, etc.

The 82595TX's software interface is optimized to reduce the number of processing steps that are required to interface to the 82595TX solution. The 82595TX's initialization and control registers are directly addressable within one 16-byte IO address block. The 82595TX can automatically resolve any conflicts to an IO block by moving its IO offset to an unused location in the case that a conflict occurs. The 82595TX's local memory is arranged in a simple ring buffer structure for efficient transfer of transmit and receive packets. The local memory, up to 64 Kbytes of DRAM, resides as either a 16-bit or 32-bit IO port in the host systems IO map programmable through configuration. The 82595TX provides direct control over the local DRAM, including refresh. The 82595TX performs a prefetch to the DRAM memory allowing CPU IO cycles to this data with no added wait-states. The 82595TX also provides an interface to up to 1 Mbyte of FLASH or EPROM memory. An interface to an EEPROM, which holds solution configuration values and can also contain the Node ID, allows for the implementation of a "jumperless" design. In addition, the 82595TX contains full hardware support for the implementation of the ISA Plug N' Play specification. Plug N' Play eliminates jumpers and complicated setup utilities by allowing peripheral functions to be added to a PC automatically (such as adapter cards) without the need to individually configure each parameter (e.g. Interrupt, IO Address, etc). This allows for configuration ease-of-use, which results in minimal time associated with installation.

The 82595TX's packaging and power management features are designed to consume minimal board real estate and system power. This is required for applications such as portable PC motherboard designs and PCMCIA cards which require a solution with very low real estate and power consumption. The 82595TX package is a 144-lead tQFP (thin Quad Flat Pack). Its dimensions are 20 mm by 20 mm, and 1.7 mm in height (roughly the same area as a US Nickel, and the same height as a US Dime). The 82595TX contains two power down modes; an SL compatible power down mode which utilizes the SL SMOUT input, and a POWER DOWN command for non-SL systems.

1.2 Enhancements to the 82595

The 82595TX is fully backwards compatible to the 82595, both in pinout and software. However, the 82595TX contains several advanced functions from the 82595 which increase performance and ease of use. The following is a list of the major enhancements to the 82595TX:

Concurrent Processing Functionality

32-Bit Local Memory IO Port

Integrated Plug N' Play support

Added EEPROM Interface for Plug N' Play

Flash addressing up to 1 Mbyte (versus 256K for 82595)

> For further information on these enhancements and a description of all the differences between the 82595 and 82595TX, please consult the 82595TX User's Manual, available through your local sales representative.

1.3 Compliance to Industry Standards

The 82595TX has two interfaces; the host system interface, which is an ISA or PCMCIA bus interface, and the serial, or network interface. Both interfaces have been standardized by the IEEE.

1.3.1 BUS INTERFACE— ISA IEEE P996/PCMCIA 2.0

The 82595TX implements the full ISA bus interface. It is compatible with the IEEE spec P996. The 82595TX also interfaces to ISA bus implementations that deviate from the IEEE spec by requiring early assertion of the IOCHRDY signal and alternate host address decode timing. This alternate timing can be configured in the 82595TX after a software test which is run at initialization time. The 82595TX can also be configured for a PCMCIA bus interface depending on the state of the PCMCIA/ISA input pin. In this case the 82595TX implements the complete PCMCIA interface, compatible to the PCMCIA revision 2.0 specification.

1.3.2 ETHERNET/TWISTED PAIR ETHERNET INTERFACE—IEEE 802.3 SPECIFICATION

The 82595TX's serial interface provides either an AUI port interface or a Twisted Pair Ethernet (TPE) interface. The AUI port can be connected to an Ethernet Transceiver cable drop, providing a fully compliant IEEE 802.3 AUI interface. The TPE port provides a fully compliant IEEE 10BASE-T interface. The 82595TX can automatically switch to whichever port (TPE or AUI) is active.

2.0 82595TX PIN DEFINITIONS

2.1 ISA Bus Interface

The ISA bus interface consists of three sections: an Address Bus, a Data Bus, and a Control section.

Symbol	Pin No.	Type	Name and Function
SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11	66 67 68 69 70 71 73 74 75 76 13 143	I	**ADDRESS BUS:** These pins provide address decoding for up to 1 Kbyte of address. These pins also provide 4 Kbytes of IO addressing to support the Plug N' Play Standard.
SA14 SA15 SA16 SA17 SA18 SA19	77 78 79 80 81 82	I	**ADDRESS BUS:** These pins provide address decoding between the 16 Kbyte and 1 Mbyte memory space. This allows for decoding of a Boot EPROM or a FLASH in 16K increments.

2.1 ISA Bus Interface (Continued)

Symbol	Pin No.	Type	Name and Function
SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7 SD8 SD9 SD10 SD11 SD12 SD13 SD14 SD15	46 47 48 49 52 53 54 55 56 57 58 59 62 63 64 65	I/O	**DATA BUS:** This is the data interface between the 82595TX and the host system. This data is buffered by one (8-bit design) or two (16-bit design) transceivers. The 82595TX's data lines should always be connected to the B side of the data bus transceiver.
AEN	20	I	**ADDRESS ENABLE:** Active high signal indicates a DMA cycle is active.
BALE	21	I	**BUFFERED ADDRESS LATCH ENABLE:** Falling edge used to latch a valid system address.
$\overline{\text{SMEMR}}$	14	I	**MEMORY READ** for system memory accesses below 1 Mbyte. Active low.
$\overline{\text{SMEMW}}$	15	I	**MEMORY WRITE** for system memory accesses below 1 Mbyte. Active low.
$\overline{\text{MEMR}}$/ 8/16 Detect	16	I	**MEMORY READ** for system memory accesses above or below 1 Mbyte. Active low. This pin also determines if the 82595TX is operating in an 8- or 16-bit system. For 16-bit systems, it should always be connected.
$\overline{\text{MEMW}}$	17	I	**MEMORY WRITE** for system memory accesses above or below 1 Mbyte. Active low.
$\overline{\text{IOR}}$	18	I	**IO READ:** Active low.
$\overline{\text{IOW}}$	19	I	**IO WRITE:** Active low.
$\overline{\text{IOCS16}}$	40	O	**IO CHIP SELECT 16:** Active low, open drain output which indicates that an IO cycle access to the 82595TX solution is 16-bit wide. Driven for IO cycles to the local memory or to the 82595TX.
IOCHRDY	37	O	**IO CHANNEL READY:** Active high, open drain output. When driven low, it extends host cycles to the 82595TX solution.
$\overline{\text{SBHE}}$	32	I	**SYSTEM BUS HIGH ENABLE:** Active low input indicates a data transfer on the high byte (D8–D15) of the system bus (a 16-bit transfer).
INT0 INT1 INT2 INT3 INT4	26 27 28 29 30	O	**82595TX INTERRUPT 0–4:** One of these five pins is selected to be active at a time (the other four are in Hi-Z state) by configuration. These active high outputs serve as interrupts to the host system.
RESET DRV	12	I	**RESET DRIVE:** Active high reset signal.

2.2 PCMCIA Bus Interface

The PCMCIA bus interface consists of three sections: an Address Bus, a Data Bus, and a Control section.

Symbol	Pin No.	Type	Name and Function
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9	66 67 68 69 70 71 73 74 75 76	I	**ADDRESS BUS:** These pins provide IO address decoding for up to 1 Kbyte.
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	46 47 48 49 52 53 54 55 56 57 58 59 62 63 64 65	I/O	**DATA BUS:** This is the data interface between the 82595TX and the host system.

2.2 PCMCIA Bus Interface (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{OE}$	14	I	**OUTPUT ENABLE (Memory Read):** Active low.
$\overline{WE}$	15	I	**WRITE ENABLE (Memory Write):** Active low.
$\overline{IORD}$	18	I	**IO READ:** Active low.
$\overline{IOWR}$	19	I	**IO WRITE:** Active low.
$\overline{IOIS16}$	40	O	**IO IS 16:** Active low output which indicates that an IO cycle access to the 82595TX solution is 16-bit wide. $\overline{IOIS16}$ should be asserted prior to Card Enable or CMD ($\overline{IORD}$ or $\overline{IOWR}$) assertion.
$\overline{WAIT}$	37	O	**WAIT:** Active low output when driven low, extends host cycles to the 82595TX.
$\overline{IREQ}$	26	O	**82595TX INTERRUPT:** Active low output.
RESET	12	I	**RESET:** Active high reset signal.
$\overline{CE1}$ $\overline{CE2}$	81 82	I	**Card Enable 1** and **Card Enable 2:** active low signals driven by the host. These signals provide a card select based on an address decode (decode done by the host) and also byte lane enables. When both $\overline{CE1}$ and $\overline{CE2}$ are high, no host accesses are made to the card. If $\overline{CE1}$ is low (active) and CE2 is high (inactive), the device operates in byte access mode with valid data being driven on D0–D7, and A0 determines the selection of an odd or even byte. When both $\overline{CE1}$ and $\overline{CE2}$ are low, a word access is taking place. In this case A0 is ignored, and the data is transferred on D0–D15. Odd-byte-only accesses can occur when $\overline{CE1}$ is high and $\overline{CE2}$ is low. In this case the data is driven on D8–D15 and A0 is ignored. See Section 4.9 for a summary of the PCMCIA decode functions.
$\overline{REG}$	80	I	**$\overline{REG}$:** is an active low input used to determine whether a host access is to Attribute memory (the 1st 1K of FLASH or CONF Regs) or to Common memory (FLASH above 1K). If $\overline{REG}$ is low the access is to Attribute memory, if $\overline{REG}$ is high the access is to Common memory. $\overline{REG}$ is also asserted low for all accesses to the 82595TX's IO Registers (including the access to the local DRAM via the 82595TX's Local Memory IO Port). See Section 4.9 for a summary of the PCMCIA decode functions.
$\overline{EVENT}$	32	O	**$\overline{EVENT}$:** is an active low output which, when enabled, will be asserted whenever a frame has been received by the 82595TX. This allows the 82595TX to "wake up" a system which has powered down (with the exception of powering down the LAN). This output will remain asserted until the 82595TX's RCV Interrupt (for the frame which woke up the system) has been acknowledged.

2.3 Local Memory Interface

Symbol	Pin No.	Type	Name and Function
MADDR0 MADDR1 MADDR2 MADDR3 MADDR4 MADDR5 MADDR6 MADDR7 MADDR8	126 127 128 129 130 132 133 134 135	O	**LOCAL MEMORY ADDRESS (MADDR0–MADDR8):** These outputs contain the multiplexed address for the local DRAM.

2.3 Local Memory Interface (Continued)

Symbol	Pin No.	Type	Name and Function
MDATA0 MDATA1 MDATA2 MDATA3	120 121 122 123	I/O	**LOCAL DATA BUS (MDATA0–MDATA3):** The four I/O signals, comprising the local data bus, are used to read or write data to or from the 4-bit wide DRAM. These signals also provide the lower 4 bits of data for accesses to an 8-bit FLASH/EPROM or IA PROM if these components are used. A 3.3K pull-up resistor connects to MDATA3 and enables EEPROM port 2.
$\overline{RAS}$	9	O	This active low output is the **Row Address Strobe** signal to the DRAM.
$\overline{CAS}$	6	O	This active low output is the **Column Address Strobe** signal to the DRAM.
$\overline{LWE}$	1	O	This active low output is the **Write Enable** to the DRAM.
FADDR14 FADDR15 FADDR16 FADDR17 FADDR18 FADDR19	126 127 128 129 6 31	O	**FLASH ADDRESS 14–17 :** These pins control the FLASH addressing from 16K to 1M to allow paging of the FLASH in 16K spaces. These addresses are under direct control of the FLASH PAGING configuration register. **NOTE:** ISA Bus I/F Only
$\overline{FOE}$	130	O	This output provides the active low **Output Enable** control to the **FLASH.**
$\overline{FWE}$	1	O	This output provides the active low **Write Enable** control to the **FLASH.**
$\overline{BOOTCS}$	141	O	**BOOT EPROM/FLASH $\overline{CS}$**
$\overline{IAPROMCS}$	143	O	**IA PROM $\overline{CS}$**
FL/IADATA4 FL/IADATA5 FL/IADATA6 FL/IADATA7	132 133 134 135	I/O	Provides the upper 4 bits of an 8 bit data path for both the Boot EPROM/FLASH and IA PROM, for CPU accesses. A 3.3K pull-down resistor connected to FL/IADATA4 and a 3.3K pull-up resistor connected to FL/IADATA7 enables AUTOFLASH/Boot EPROM detect.
EEPROMCS	139	I/O	**EEPROM CS:** Active high signal. If no EEPROM is connected, this pin should be connected to V_{CC}. In this case it will function as an input to the 82595TX to indicate no EEPROM is connected.
EEPROMSK Port 1 (EEPROM1SK) Port 2 (EEPROM2SK)	 120 105	O	**EEPROM SHIFT CLOCK:** This output is used to shift data into and out of the serial EEPROM. **NOTE:** Port 2 must be used for Plug N' Play
EEPROMDO Port 1 (EEPROM1DO) Port 2 (EEPROM2DO)	 121 107	I	**EEPROM DATA OUT** **NOTE:** Port 2 must be used for Plug N' Play
EEPROMDI Port 1 (EEPROM1DI) Port 2 (EEPROM1DI)	 122 106	O	**EEPROM DATA IN** **NOTE:** Port 2 must be used for Plug N' Play

2.4 Miscellaneous Control

Symbol	Pin No.	Type	Name and Function
$\overline{DIRL}$	42	O	**DIRECTION LOW:** Controls the direction of the low byte data bus transceiver. The direction defaults to always point in from the ISA bus to the 82595TX ($\overline{DIRL}$ = 1). This direction is turned around (82595TX out to ISA bus, $\overline{DIRL}$ = 0) only in the case of a read access to the 82595TX based solution.
$\overline{DIRH}$	45	O	**DIRECTION HIGH:** Controls the direction of the high byte data bus transceiver. The direction defaults to always point in from the ISA bus to the 82595TX ($\overline{DIRH}$ = 1). This direction is turned around (82595TX out to ISA bus, $\overline{DIRH}$ = 0) only in the case of a read access to the 82595TX based solution. This signal is active for 16-bit accesses only.
$\overline{SMOUT}$	11	I/O	This active LOW signal, when asserted, places the 82595TX into a Power Down mode. The 82595TX will remain in power down mode until $\overline{SMOUT}$ is unasserted. If this line is unconnected to $\overline{SMOUT}$ from the system bus, it can be used as an active low output which, when a POWER DOWN command is issued to the 82595TX, can be used to power down other external components (this output function is enabled by configuration).
PCMCIA/$\overline{ISA}$	22	I	This pin, when strapped low, selects an ISA bus interface. Strapped high selects PCMCIA.
J0 J1 J2	107 106 105	I I/O I/O	**JUMPER:** input for selecting between 7 ISA IO spaces (also selects whether the IO location should be read from the EEPROM). These pins should be connected to either V_{CC} or GND. The 82595TX reads the Jumper block during its initialization sequence.

J0	J1	J2	IO Address
GND	GND	GND	Address Contained in EEPROM
V_{CC}	GND	GND	2A0h
GND	V_{CC}	GND	280h
V_{CC}	V_{CC}	GND	340h
GND	GND	V_{CC}	300h
V_{CC}	GND	V_{CC}	360h
GND	V_{CC}	V_{CC}	350h
V_{CC}	V_{CC}	V_{CC}	330h

2.5 JTAG Control

Symbol	Pin No.	Type	Name and Function
TDO	97	O	**JTAG TEST DATA OUT**
TMS	98	I	**JTAG TEST MODE SELECT**
TCK	99	I	**JTAG TEST CLOCK**
TDI	100	I	**JTAG TEST DATA IN**

2.6 Serial Interface

Symbol	Pin No.	Type	Name and Function
TRMT	110	O	Positive side of the differential output driver pair that drives 10 Mb/s Manchester Encoded data on the TRMT pair of the AUI cable (Data Out A).
$\overline{\text{TRMT}}$	111	O	Negative side of the differential output driver pair that drives 10 Mb/s Manchester Encoded data on the TRMT pair of the AUI cable (Data Out B).
RCV	103	I	The positive input to a differential amplifier connected to the RCV pair of the AUI cable (Data In A). It is driven with 10 Mb/s Manchester Encoded data.
$\overline{\text{RCV}}$	104	I	The negative input to a differential amplifier connected to the RCV pair of the AUI cable (Data In B). It is driven with 10 Mb/s Manchester Encoded data.
CLSN	112	I	The positive input to a differential amplifier connected to the CLSN pair of the AUI cable (Collision In A).
$\overline{\text{CLSN}}$	113	I	The negative input to a differential amplifier connected to the CLSN pair of the AUI cable (Collision In B).
TDH	93	O	**TRANSMIT DATA HIGH:** Active high Manchester Encoded data to be transmitted onto the twisted pair. This signal is used in conjunction with TDL, $\overline{\text{TDH}}$, and $\overline{\text{TDL}}$ to generate the pre-conditioned twisted pair output waveform.
TDL	94	O	**TRANSMIT DATA LOW:** Twisted Pair Output Driver. Active high Manchester Encoded data with embedded pre-distortion information to be transmitted onto the twisted pair. This signal is used in conjunction with TDH, $\overline{\text{TDH}}$, and $\overline{\text{TDL}}$ to generate the pre-conditioned twisted pair output waveform.
$\overline{\text{TDH}}$	91	O	**TRANSMIT DATA HIGH INVERT:** Twisted Pair Output Driver. Active low Manchester Encoded data to be transmitted onto the twisted pair. This signal is used in conjunction with TDL, TDH, and $\overline{\text{TDL}}$ to generate the pre-conditioned twisted pair output waveform.
$\overline{\text{TDL}}$	92	O	**TRANSMIT DATA LOW INVERT:** Twisted Pair Output Driver. Active low Manchester Encoded data with embedded pre-distortion information to be transmitted onto the twisted pair. This signal is used in conjunction with TDL, TDH, and $\overline{\text{TDH}}$ to generate the pre-conditioned twisted pair output waveform.
RD	102	I	Active high Manchester Encoded data received from the twisted pair.
$\overline{\text{RD}}$	101	I	Active low Manchester Encoded data received from the twisted pair.
X1	115	I	**20 MHz CRYSTAL INPUT:** This pin can be driven with an external MOS level clock when X2 is left floating. This input provides the timing for all of the 82595TX functional blocks.
X2	116	O	**20 MHz CRYSTAL OUTPUT:** If X1 is driven with an external MOS level clock, X2 should be left floating.

2.6 Serial Interface (Continued)

Symbol	Pin No.	Type	Name and Function
AUI LED/BNC DIS	83	O	**AUI LED INDICATOR:** This output, when the 82595TX is used for as a TPE/AUI solution, will turn on an LED when the 82595TX is actively interfaced to its AUI serial port. When the 82595TX is used as a BNC/AUI solution, this output becomes the **BNC DIS** output, which can be used to power down the BNC Transceiver section (the Transceiver and the DC to DC Converter) of the solution when the BNC port is unconnected.
LILED	86	O	**LINK INTEGRITY LED:** Normally on (low) ouput which indicates a good link integrity status when the 82595TX is connected to an active TPE port. This output will remain on when the Link Integrity function has been disabled. It turns off (driven high) when Link Integrity fails, or when the 82595TX is actively interfaced to an AUI port. The minimum off time is 100 ms.
ACTLED	85	O	**LINK ACTIVITY LED:** Normally off (high) output turns on to indicate activity for transmission, reception, or collision. Flashes at a rate dependent on the level of activity on the link.
POLED	84	O	**POLARITY LED:** If the 82595TX detects that the receive TPE wires are reversed, POLED will turn on (low) to indicate the fault. POLED remains on even if automatic polarity correction is enabled, and the 82595TX has automatically corrected for the reversed wires.

2.7 Power and Ground

Symbol	Pin No.	Type	Name and Function
V_{CC}	3, 4, 8, 23, 25, 35, 38, 41, 44, 51, 61, 87, 89, 95, 109, 117, 119, 125, 136, 142	I	**POWER**: +5V ±5%.
V_{SS}	2, 5, 7, 10, 24, 33, 34, 36, 39, 43, 50 60, 72, 88, 90, 96, 108, 114, 118, 124, 131, 138, 140, 144	I	**GROUND**: 0V.

2.8 82595TX Pin Summary

ISA/PCMCIA Bus Interface

ISA Pin Name	MUXed PCMCIA Pin Name	Pin Type	P-Down State
SA0–SA11 (In)	A0–A9 (In)		Inactive
SA14–16 (In)			Inactive
SA17 (In)	REG (In)		Inactive/Act(1)
SA18 (In)	CE1 (In)		Inactive/Act(1)
SA19 (In)	CE2 (In)		Inactive
SD0–SD15 (I/O)	D0–D15 (I/O)	TS	TS
SMEMR (In)	OE (In)		Inactive
SMEMW (In)	WE (In)		Inactive
IOR (In)	IORD (In)		Inactive
IOW (In)	IOWR (In)		Inactive/Act(1)
INT0 (Out)	IREQ (Out)	TS	TS
INT1–4 (Out)		TS	TS
RESET DRV (In)	RESET (In)		Act
IOCS16 (Out)	IOIS16 (Out)	OD/TS	TS
BALE (In)			Inactive
IOCHRDY (Out)	WAIT (Out)	OD/2S	TS
SBHE (In)	EVENT (Out)	2S	Inactive/TS
AEN (In)			Inactive/Act(1)
MEMR (In)			Inactive
MEMW (In)			Inactive

NOTE:
1. For hardware powerdown using SMOUT, these pins will be inactive. For software powerdown, these pins remain active.

Local Memory Interface

Pin Name	MUXed Pin Name	Pin Type	P-Down State
MADDR0–3 (Out)	FADDR14–17 (Out)	2S	TS
MADDR4 (Out)	FOE (Out)	2S	TS
MADDR5–8 (Out)	FL/IADATA4–7 (In)	TS	TS
MDATA0 (I/O)	EEPROM1SK(Out)	TS	TS
MDATA1 (I/O)	EEPROM1DO(In)	TS	TS
MDATA2 (I/O)	EEPROM1DI(Out)	TS	TS
MDATA3 (I/O)		TS	TS
WE (Out)	FWE (Out)	2S	TS
RAS (Out)		2S	PU
CAS (Out)	FADDR18 (Out)	2S	PU
BOOTCS (Out)		2S	PU
IAPROMCS (Out)	SA11 (In) (Dual)	2S	PU
EEPROMCS (I/O)		TS	PD
FADDR19 (Out)		TS	TS

Miscellaneous Control

Pin Name	MUXed Pin Name	Pin Type	P-Down State	Dual Pin Name
DIRL (Out)		2S	PU	
DIRH (Out)		2S	PU	
J0(In)			ACT	EEPROM2D0 (In)
J1 (I/O)		TS	TS	EEPROM2DI (Out)
J2 (I/O)		TS	TS	EEPROM2SK (Out)
SMOUT (I/O)		TS	ACT/TS	
PCMCIA/ISA (In)			ACT	

JTAG Control

Pin Name	MUXed Pin Name	Pin Type	P-Down State
TMS (In)			In Act
TCK (In)			In Act
TDI (In)			In Act
TDO (Out)		2S	

Serial Interface

Pin Name	MUXed Pin Name	Pin Type	P-Down State
TRMT (Out)		Ana	TS
TRMT (Out)		Ana	TS
RCV (In)		Ana	In Act
RCV (In)		Ana	In Act
CLSN (In)		Ana	In Act
CLSN (In)		Ana	In Act
TDH (Out)		Ana	TS
TDL (Out)		Ana	TS
TDH (Out)		Ana	TS
TDL (Out)		Ana	TS
RD (In)		Ana	In Act
RD (In)		Ana	In Act
X1 (In)			In Act
X2 (Out)		2S	TS
LILED (Out)		2S	TS
POLED (Out)		2S	TS
ACTLED (Out)		2S	TS
AUILED (Out)	BNC DIS (Out)	2S	TS

Legend:
TS—TriState.
OD—Open Drain.
2S—Two State, will be found in either a 1 or 0 logic level.
Ana—Analog pin (all serial interface signals).
Act—Input buffer is active during Power Down.
In Act—Input buffer is inactive during Power Down.
PU—Output in inactive state with weak internal Pull-up during Power Down.
PD—Output in inactive state with weak internal Pull-down during Power Down.
Dual—Dual function pin.

3.0 82595TX INTERNAL ARCHITECTURE OVERVIEW

Figure 1 shows a high level block diagram of the 82595TX. The 82595TX is divided into four main subsections; a system interface, a local memory sub-system interface, a CSMA/CD unit, and a serial interface.

3.1 System Interface Overview

The 82595TX's system interface subsection includes a glueless ISA or PCMCIA bus interface (selectable by strapping), and the 82595TX's IO registers (including the 82595TX's command, status, and Data In/Out registers). The system interface block also interfaces with the 82595TX's local memory interface subsystem and CSMA/CD subsystem.

The bus interface logic provides the control, address, and data interface to either an ISA compatible or PCMCIA revision 2.0 bus. The 82595TX decodes up to 1M of total memory address space. Address decoding within 16K block increments (A14–A19) are used for Flash or Boot EPROM. IO accesses are decoded throughout the 1 Kbyte PC IO address range (A10 and A11 provide up to 4K of IO addressing and are used for Plug N' Play). The 82595TX data bus interface provides either an 8- or 16-bit interface to the host system's data bus. The control interface provides complete handshaking interface with the system bus to enable transfer of data between the 82595TX solution and the host system. This logic also controls the direction of the Data Bus transceivers.

The 82595TX's IO registers provide 3 banks of directly addressable registers which are used as the control and data interface to the 82595TX. There are 16 IO registers per bank, with only one bank enabled at a time. This allows the complete 82595TX software interface to be contained in one 16-byte IO space. The base address of this IO space is selectable via either software (which can be stored in a serial EEPROM interfaced to either of two ports in the 82595TX), or by strapping the 82595TX IO Jumper block (J0–J2). The 82595TX can also detect conflicts to its base IO space, and automatically resolve these conflicts either by allowing the selection of one Plug N' Play card from multiple cards (using Plug N' Play software), or by mapping itself into an un-used IO space (Automatic IO Resolution). Included in the 82595TX IO registers are the Command Register, the Status Register, and the Local Memory IO Port register, which provides the data interface to the local DRAM buffer contained in an 82595TX solution. Functions such as IO window mapping, Interrupt enable, RCV and XMT buffer initialization, etc. are also configured and controlled through the IO registers.

3.1.1 CONCURRENT PROCESSING FUNCTIONALITY

The 82595TX's Concurrent Processing feature significantly enchances data throughput performance by performing both system bus and serial link activities concurrently. Transmission of a frame is started by the 82595TX before that frame is completely copied into local memory. During reception, a frame is processed by the host CPU before that frame is entirely copied to local memory. Transmit Concurrent Processing feature is enabled by writing to BANK 2, Register 1, Bit 0. A 1 written to this bit enables this functionality, a 0 (default) disables it. To enable Receive Concurrent Processing, BANK 1, Register 7 must be programmed to value other than 00h (00h disables RCV Concurrent Processing, and is default). (See Section 4.1 for the format of IO BANK 1 and 2.) Concurrent Processing is not recommended for 8-bit interfaces. For more information on Transmit and Receive Concurrent Processing, refer to Section 7.0 and Section 8.0.

3.2 Local Memory Interface

The 82595TX's local memory interface includes a DMA unit which controls data transfers to or from the 82595TX's local DRAM, control for access to an IA PROM and a Boot EPROM/FLASH, and two interfaces to a serial EEPROM. The local memory interface subsection also arbitrates accesses to the local memory by the host CPU and the 82595TX.

Data transfers between the 82595TX and the local DRAM are always through the 82595TX's Local Memory 16-bit/32-bit IO Port. This allows the entire DRAM memory (up to 64 Kbytes) to be mapped into one IO location in the host systems IO map. By setting a configuration bit in the 82595TX's IO Registers (32IO/HAR#), the local memory can be extended from 16 bits to a full 32 bits. During 32-bit accesses, the CPU would perform a doubleword access addressed to register 12 of BANK0. The ISA bus will break this access up into two 16-bit accesses to Registers 12/13 followed by Registers 14/15, (or 4 sequential 8-bit accesses in an 8-bit interface). The CPU always accesses the 82595TX IO Port for Receive or Transmit data transfers, while the 82595TX automatically increments the address to the DRAM after each CPU access. The DRAMs data path is a 4-bit interface (typically 64K by 4-bits wide, or 256K by 4-bits wide) to allow for the lowest possible solution cost. The 82595TX implements a prefetch mechanism to the local DRAM so that the data is always available to the CPU as either an 8- or 16-bit word. In the case of the CPU reading from the DRAM, the 82595 TX reads the next four 4-bit nibbles from the DRAM, the 82595TX between CPU cycles so that the data is always available as a word in the 82595TX's Local Memory IO Port register. In the case of the CPU writing to the DRAM, the data is

written into the 82595TX's Local Memory IO Port then transferred to the DRAM by the 82595TX between CPU cycles. This prefetch mechanism of the 82595TX allows for IO read and writes to the local memory to be performed with no additional wait-states (3 clocks per data transfer cycle).

The DMA unit provides addressing and control to move RCV or XMT data between the 82595TX and the local DRAM. For transmission, the CPU is required only to copy the data to the local memory, initialize the 82595TX's DMA Current Address Register (CAR) to point to the beginning of the frame, and issue a Transmit Command to the 82595TX. The DMA unit facilitates the transfers from the local memory to the 82595TX as transmission takes place. The DMA unit will reset upon collision during a transmission, enabling automatic re-transmission of the transmit frame. During reception, the DMA unit implements a recyclable ring buffer structure which can receive continuous back to back frames without CPU intervention on a per frame basis (see Section 8.2 for details).

The 82595TX provides address decoding and control to allow access to an external Boot EPROM/FLASH or an IA PROM if these components are utilized in an 82595TX design (an IA PROM cannot be used for Plug N' Play). The 82595TX also provides two complete interfaces to a serial EEPROM (Port1 or Port2) to replace jumper blocks used to contain configuration information. Port1 is used to store configuration information such as IO Mapping Window, Interrupt line selection, etc., and is backwards pin compatible to the 82595TX EEPROM interface. Port2 is used to store configuration information as in Port1; in addition, it is used to store Plug N' Play information as defined in the Plug N' Play Specification.

The 82595TX arbitrates accesses to the local memory sub-system by the CPU and the 82595TX. The arbitration unit will hold off an 82595TX DMA cycle to the local memory if a CPU cycle is already in progress. Likewise, it will hold off the CPU if an 82595TX cycle is already in progress. The cycle which is held off will be completed on termination of the preceding cycle.

3.3 CSMA/CD Unit

The CSMA/CD unit implements the IEEE 802.3 CSMA/CD protocol. It performs such functions as transmission deferral to link traffic, interframe spacing, exponential backoff for collision handling, address recognition, etc. The CSMA/CD unit serves as the interface between the local memory and the serial interface. It serializes data transferred from the local memory before it is passed to the serial interface unit for transmission. During frame reception, it converts the serial data received from the serial interface to a byte format before it is transferred to local memory. The CSMA/CD unit strips framing parameters such as the Preamble and SFD fields before the frame is passes to memory for reception. For transmission, the CSMA/CD unit builds the frame format before the frame is passed to the serial interface for transmission.

3.4 Serial Interface

The 82595TX's serial interface provides either an AUI port interface or a Twisted Pair Ethernet (TPE) interface. The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully compliant IEEE 802.3 AUI interface. The AUI port can also interface to a transceiver device to provide a fully compliant IEEE 802.3 10BASE2 (Cheapernet) interface. The TPE port provides a fully compliant 10BASE-T interface. The 82595TX automatically enables either to the AUI or TPE interface depending on which medium is connected to the chip. Software configuration can override this automatic selection.

4.0 ACCESSING THE 82595TX

All access to the 82595TX is made through one of three banks of IO registers. Each bank contains 16 registers. Each register in a bank is directly accessible via addressing. Through the use of bank switching, the 82595TX utilizes only 16 IO locations in the host system's IO map to access each of its registers. The different banks are accessed by setting the POINTER field in the 82595TX Command Register to select each bank. The Command Register is Register for each bank.

4.1 82595TX Register Map

The 82595TX registers are contained in three banks of 16 IO registers per bank. These three banks are shown in the following three pages.

4.1.1 IO BANK 0

The format for IO Bank 0 is shown below.

7	6	5	4	3	2	1	0	
POINTER		ABORT	COMMAND OP CODE					Reg 0 (CMD Reg)
RCV States		EXEC States		EXEC INT	TX INT	RX INT	RX STP INT	Reg 1
ID REGISTER (Counter)		1	(Auto En)	0	1	0 RESERVED	0	Reg 2
0 Resvrd	0 Resvrd	Cur/ $\overline{\text{Base}}$	32 IO/ $\overline{\text{HAR}}$	EXEC Mask	TX Mask	RX Mask	RX STP Mask	Reg 3
RCV CAR/BAR (Low)								Reg 4
RCV CAR/BAR (High)								Reg 5
RCV STOP REG (Low)								Reg 6
RCV STOP REG (High)								Reg 7
RCV Copy Threshold REG								Reg 8
0	0	0	0	0	0	0	0	
(Reserved)								Reg 9
XMT CAR/BAR (Low)								Reg 10
XMT CAR/BAR (High)								Reg 11
Host Address Reg/32-Bit I/O (Byte 0) (Low)								Reg 12
Host Address Reg/32-Bit I/O (Byte 1) (High)								Reg 13
Local Memory/32-Bit I/O (Byte 2) IO Port (Low)								Reg 14
Local Memory/32-Bit I/O (Byte 3) IO Port (High)								Reg 15

4.1.2 IO BANK 1

The format for IO Bank 1 is shown below.

7	6	5	4	3	2	1	0	
POINTER		ABORT	COMMAND OP CODE					Reg 0 (CMD Reg)
$\overline{\text{Tri-ST}}$ INT	Alt RDY Tm	0 Resvrd	0 Resvrd	0 Resvrd	0 Resvrd	Host Bus Wd	0 Resvrd	Reg 1
FL/$\overline{\text{BT}}$ Detect	Boot EPROM/FLASH Decode Window			0 Resvrd	INT Select			Reg 2
0	0	I/O Mapping Window						Reg 3
0	0	0	0	0	0	0	0	Reg 4
(Reserved)								
0	0	0	0	0	0	0	0	Reg 5
(Reserved)								
0	0	0	0	0	0	0	0	Reg 6
(Reserved)								
RCV BOF Threshold REG								Reg 7
RCV LOWER LIMIT REG (High Byte)								Reg 8
RCV UPPER LIMIT REG (High Byte)								Reg 9
XMT LOWER LIMIT REG (High Byte)								Reg 10
XMT UPPER LIMIT REG (High Byte)								Reg 11
FLASH PAGE SELECT HIGH		FLASH WRITE ENABLE		FLASH PAGE SELECT				Reg 12
0	0	0	0	0	$\overline{\text{SMOUT}}$ OUT EN	AL RDY TEST	AL RDY PAS/FL	Reg 13
0	0	0	0	0	0	0	0	Reg 14
(Reserved)								
0	0	0	0	0	0	0	0	Reg 15
(Reserved)								

4.1.3 IO BANK 2

The format for IO Bank 2 is shown below.

7	6	5	4	3	2	1	0	
POINTER		ABORT	COMMAND OP CODE					Reg 0 (CMD Reg)
Disc Bad Fr	Tx Chn $\overline{\text{ErStp}}$	Tx Chn Int Md	PCMCIA/ $\overline{\text{ISA}}$	0	0	0	TX Con Proc En	Reg 1
LoopBack		Multi IA	No SA Ins	Length $\overline{\text{Enable}}$	RX CRC $\overline{\text{InMem}}$	BC DIS	PRMSC Mode	Reg 2
Test1	Test2	BNC/ $\overline{\text{TPE}}$	$\overline{\text{APORT}}$	Jabber Disabl	TPE/ $\overline{\text{AUI}}$	Pol $\overline{\text{Corr}}$	Lnk In Dis	Reg 3
INDIVIDUAL ADDRESS REGISTER 0								Reg 4
INDIVIDUAL ADDRESS REGISTER 1								Reg 5
INDIVIDUAL ADDRESS REGISTER 2								Reg 6
INDIVIDUAL ADDRESS REGISTER 3								Reg 7
INDIVIDUAL ADDRESS REGISTER 4								Reg 8
INDIVIDUAL ADDRESS REGISTER 5								Reg 9
STEPPING			Trnoff Enable	EEDO	EEDI	EECS	EESK	Reg 10
RCV NO RESOURCE COUNTER								Reg 11
IAPROM IO Port								Reg 12
0	0	0	0	0	0	0	0	Reg 13
(Reserved)								
0	0	0	0	0	0	0	0	Reg 14
(Reserved)								
0	0	0	0	0	0	0	0	Reg 15
(Reserved)								

4.2 Writing to the 82595TX

Writing to the 82595TX is accomplished by an IO Write instruction (such as an OUT instruction) from the host processor to one of the 82595TX registers. The 82595TX registers reside in a block of 16 contiguous addresses contained within the PC IO address space. The mapping of this address block is programmable throughout the 1 Kbyte PC IO address map.

The 82595TX registers are contained within three banks of IO registers. When writing to a particular register, the processor must first select the correct bank (Bank 0, 1 or 2) in which the register resides. Once a bank is selected, all register accesses are made in that bank until a switch to another bank is performed. Switching banks is accomplished by writing to the PTR field of Reg 0 in any bank. Reg 0 is the command register of the 82595TX and its functionality is identical in each bank. Once in the appro-

priate bank, the processor can write directly to any of the 82595TX registers by simply issuing an OUT instruction to the IO address of the register.

4.3 Reading from the 82595TX

Reading from the 82595TX is accomplished by an IO Read instruction (such as an IN instruction) from the host processor to one of the 82595TX registers. When reading from a particular register, the processor must first select the correct bank (Bank 0, 1 or 2) in which the register resides. Once in the appropriate bank, the processor can read directly from any of the 82595TX registers by simply issuing an IN instruction to the IO address of the register.

4.4 Local DRAM Accesses

IO mapping the local DRAM memory of an 82595TX solution allows it to appear as simply an IO Port to the host system. This allows an 82595TX solution to work in PCs which do not have enough space in their system memory map to accommodate the addition of LAN buffer memory (typically 16 Kbytes to 64 Kbytes) into the map. The entire local memory (up to 64 Kbytes) is mapped into one 16-bit IO Port location. For all IO-mapped accesses to the local memory of a 82595TX solution, the 82595TX performs the IO address decoding and the ISA Bus interface handshake and asserts the address and control signals to the local memory.

4.4.1 WRITING TO LOCAL MEMORY

The local memory of an 82595TX solution is written to whenever the host CPU performs a Write operation to the 82595TX Local Memory IO Port. Prior to writing a block of data to the local memory, the CPU should update the 82595TX Host Address Register with the first address to be written. The CPU then copies the data to the local memory by writing it to the 82595TX Local Memory IO Port. The addressing to the local memory is provided by the Host Address Register which is automatically incremented by the 82595TX upon completion of each write cycle. This allows sequential accesses to the local memory, even though the IO port address accessed does not change.

4.4.2 READING FROM LOCAL MEMORY

The local memory of an 82595TX solution is read from whenever the host CPU performs a Read operation from the 82595TX Local Memory IO Port. Prior to reading a block of data from the local memory, the CPU should utilize the 82595TX Host Address Register to point to first address to be read. The CPU then reads the data from the local memory through the 82595TX Local Memory IO Port. The addressing to the local memory is provided by the Host Address Register which is automatically incremented by the 82595TX upon completion of each read cycle.

4.5 Serial EEPROM Interface

A Serial EEPROM, a Hyundai HY93C46 or equivalent IC, stores configuration data for the 82595TX. The use of an EEPROM enables 82595TX designs to be implemented without jumpers (the use of jumpers to select IO windows is optional.) The 85295TX provides two complete interfaces to a serial EEPROM (Port1 or Port2, and only one port can be used). Port1 is used to store configuration information in the EEPROM, such as IO Base Address and Interrupt selection, and is backwards pin compatible to the 82595 EEPROM interface. Port2 stores configuration information as in Port1; in addition, it is used to store Plug N' Play information as defined in the Plug N' Play specification. Plug N' Play allows peripheral functions to be added to a PC (such as adapter cards) without the need to individually configure each parameter (e.g. Interrupt, IO Address, etc). Information describing system resources are contained within the 82595TX configuration registers. This allows Auto-configuration software, which is usually contained in the BIOS or O/S, to identify system resource usage, identify conflicts and automatically re-configure the 82595TX.

The 82595TX automatically accesses Register 0 of the EEPROM upon a RESET in ISA Bus Interface mode. Register 0 contains the information that the 82595TX must be configured to allow CPU accesses to it (IO Mapping Window, FLASH Detect Enable, Auto I/O Enable, Boot EPROM/FLASH Window, Host Bus Width, and Plug N' Play Enable) following a system boot. The format for EEPROM Register 0 is shown in Figure 4-1. Note that all 0's are assumed to be reserved. In the case where an EEPROM is either unprogrammed (each bit defaults to a 1) or completely erased (all 0's), the 82595TX will default to IO Address 300h.

For additional information regarding a Plug N' Play implementation for the 82595TX, please consult the 82595TX User Manual and LAN595TX Specification, available through your local sales representative. The latest Plug N' Play Specification is available by Microsoft.

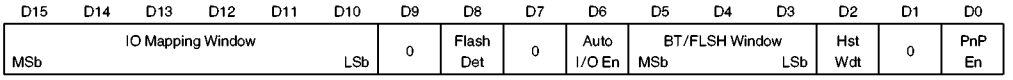


Figure 4-1. EEPROM Register 0

4.6 Boot EPROM/FLASH Interface

The Boot EPROM/FLASH of an 82595TX solution is read from or written to (FLASH only) whenever the host CPU performs a Read or a Write operation to a memory location that is within the Boot EPROM/FLASH mapping window. This window is programmable throughout the ISA PROM address range (C8000–DFFFF) by configuring the 82595TX Boot EPROM Decode Window register (Bank 1, Register 2, bits 4–6). The 82595TX asserts the BOOTCS# signal when it decodes a valid access. Up to 1 MBytes of FLASH can be addressed by the 82595TX.

4.7 IA PROM Interface

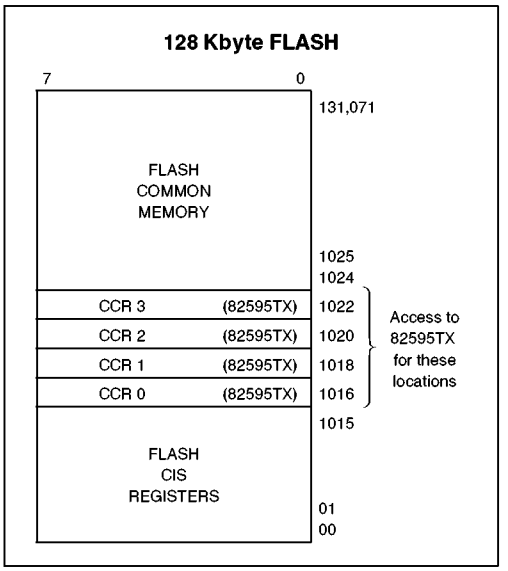
The 82595TX supports an IA PROM interface. Implementation of an IA PROM in a 82595TX solution is optional. The IA can also be stored in the serial EEPROM. In this case the IA PROM is not needed. For Plug N' Play, an IA PROM cannot be used.

4.8 PCMCIA CIS Structures

The 82595TX supports access to 1K of Attribute Memory when configured for PCMCIA support. Attribute memory is defined by the PCMCIA standard to be comprised of the Card Information Structure (FLASH memory referred to as CIS residing at memory offset 0 to 1015:decimal) and 4 8-bit Card Configuration Registers which reside at memory offset 1016 to 1022 on even boundaries only (1016, 1018, 1020, 1022). These four registers are contained in the 82595TX. They are memory mapped and are accessed when $\overline{CE1}$ and $\overline{REG}$ are asserted low along with the decode of A0–A9 and assertion of either a $\overline{OE}$ or $\overline{WE}$. The 82595TX Card Configuration Registers are shown at the bottom of this page.

4.9 PCMCIA Decode Functions

The Attribute Memory and Common Memory map for a PCMCIA card is shown below. Attribute Memory is defined as the CIS structures (residing in FLASH below 1K) and the CCR Registers (residing in the 82595TX). Common Memory is defined as the FLASH memory above 1K.



82595TX Card Configuration Registers

7	6	5	4	3	2	1	0	
RESET	0	0	0	0	0	XIP En	IO En	CCR 0 (Addr 1016)
0	0	IOIS8	EvntWk	0	0	IREQ	0	CCR 1 (Addr 1018)
0	0	0	0	0	0	0	0	CCR 2 (Addr 1020)
0	0	0	0	0	0	0	0	CCR 3 (Addr 1022)

NOTE:
All 0's in the above registers are reserved.

5.0 COMMAND AND STATUS INTERFACE

The format for the 82595TX Command Register is shown in Figure 5-1. The Command Register resides in Register 0 of each of the three IO Banks of the 82595TX, and can be accessed in any of these banks. The Command Register is accessed by writing to or reading from the IO address for Register 0.

5.1 Command OP Code Field

Bits 0 through 4 of the Command Register comprise the Command OP Code field. A command is issued to the 82595TX by writing it into the Command OP Code field. A command can be issued to the 82595TX at any time; however in certain cases the command may be ignored (for example, issuing a Transmit command while a Transmit is already in progress). In these cases the command is not performed, and no interrupt will result from it.

The Command OP Code field can also be read. In this case it will indicate an execution status event other than TRANSMIT DONE (TDR Done, DIAGNOSE Done, MC-SETUP Done, DUMP Done, INIT Done, and POWER-UP) has been completed. This field is valid only when the EXEC INT bit (Bank 0, Reg 1, Bit 3) is set.

5.2 ABORT (Bit 5)

This bit indicates if an execution command other than TRANSMIT was aborted while in progress. This bit provides status information only. It should be written to a 0 whenever the Command Register is written to.

5.3 Pointer Field (Bits 6 and 7)

The Pointer field controls which 82595TX IO register bank is currently to be accessed (Bank 0, Bank 1, or Bank 2). Writing a 00:b to the Pointer field selects Bank 0, 01:b for Bank 1, and 10:b for Bank 2. The Pointer field is valid only when the SWITCH BANK (0h) command is issued. This field will be ignored for any other command. The 82595TX will continue to operate in a current bank until a different bank is selected. Upon power up of the device or Reset, the 82595TX will default to Bank 0.

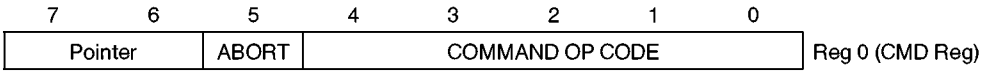


Figure 5-1. 82595TX Command Register

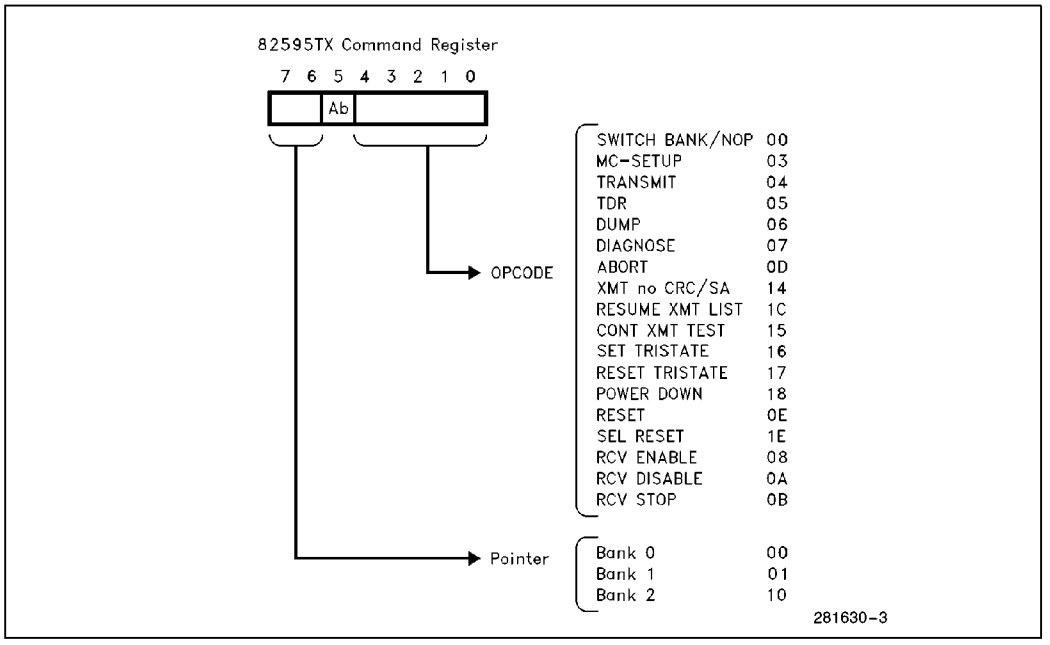


Figure 5-2. 82595TX Command Interface

5.4 82595TX Status Interface

The Status of the 82595TX can be read from Register 1 of Bank 0, with additional status information contained in Register 0 (the Command Register). Figure 5-3 shows these registers. Other information concerning the configuration and initialization of the 82595TX and its registers can be obtained by directly reading the 82595TX registers.

When read, the Command OP Code field indicates which event (MC Done, Init Done, TDR Done, or DIAG Done) has been completed. This field is valid only when the EXEC INT Bit (Bank 0, Reg 1, Bit 3) is set to a 1. Reading the Pointer field indicates which bank the 82595TX is currently operating in. Register 1 in Bank 0 contains the 82595TX interrupts status as well as the current states of the RCV and Execution units of the 82595TX. Resultant status from events such as the completion of a transmission or the reception of an incoming frame is contained in the status field of the memory structures for these particular events.

6.0 INITIALIZATION

Upon either a software or hardware RESET, the 82595TX enters into its initialization sequence. When the 82595TX is interfaced to an ISA bus, the 82595TX reads information from its EEPROM and Jumper block (if utilized) which configures critical parameters (IO Address mapping, etc.) to allow initial accesses to the 82595TX during the host system's initialization sequence and also access by the software device driver. The 82595TX can also be configured (via the EEPROM) to automatically resolve any conflicts to its IO address location either by moving its IO address offset to an unused location in the case that a conflict occurs, or by using the Plug N' Play Software to the I/O address location. This process eliminates a large majority of LAN end-user setup problems.

The 82595TX can be configured to operate with ISA systems that require early deassertion of the IOCHRDY signal to its low (not ready) state. The 82595TX, along with its software driver, can perform a test at initialization to determine if early IOCHRDY deassertion is required.

The 82595TX, when interfaced to a PCMCIA bus, simply powers up with default PCMCIA configuration values enabled. This is the only step for PCMCIA initialization, since the PCMCIA bus requires no selection of Interrupts, IO Space, etc.

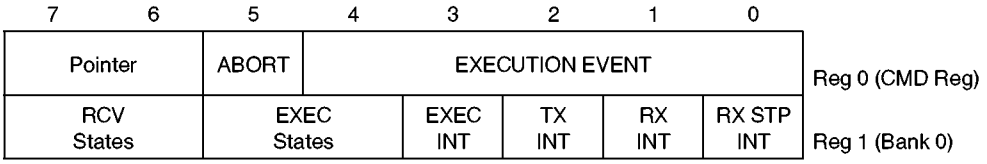


Figure 5-3. 82595TX Status Information

7.0 FRAME TRANSMISSION

The 82595TX performs all of the necessary functions needed to transmit frames from its local memory. If Transmit Concurrent Processing is enabled, the CPU must only program the Base and Host Address Register with the starting address to be transmitted, copy a portion of the frame into the 82595TX's transmit buffer located in local memory (the number of bytes for this first portion is determined by the software driver without causing an Underrun), issue a XMT command to the 82595TX, and complete the data copies for this frame to local memory. If Transmit Concurrent Processing is disabled, the CPU must copy an entire frame into the 82595TX's transmit buffer located in local memory, set up the 82595TX's Current Address Registers to point to that frame, and issue a XMT command to the 82559TX. The 82595TX performs all the link management functions, DMA operations, and statistics keeping to handle transmission onto the link and communicate the status of the transmission to the CPU. The 82595TX performs automatic retransmission on collision with no CPU interaction.

7.1 82595TX XMT Block Memory Format

The format in which a XMT block is written to memory by the CPU is shown in Figure 7-1 for a 16-bit interface. Figure 7-2 shows this structure for an 8-bit interface.

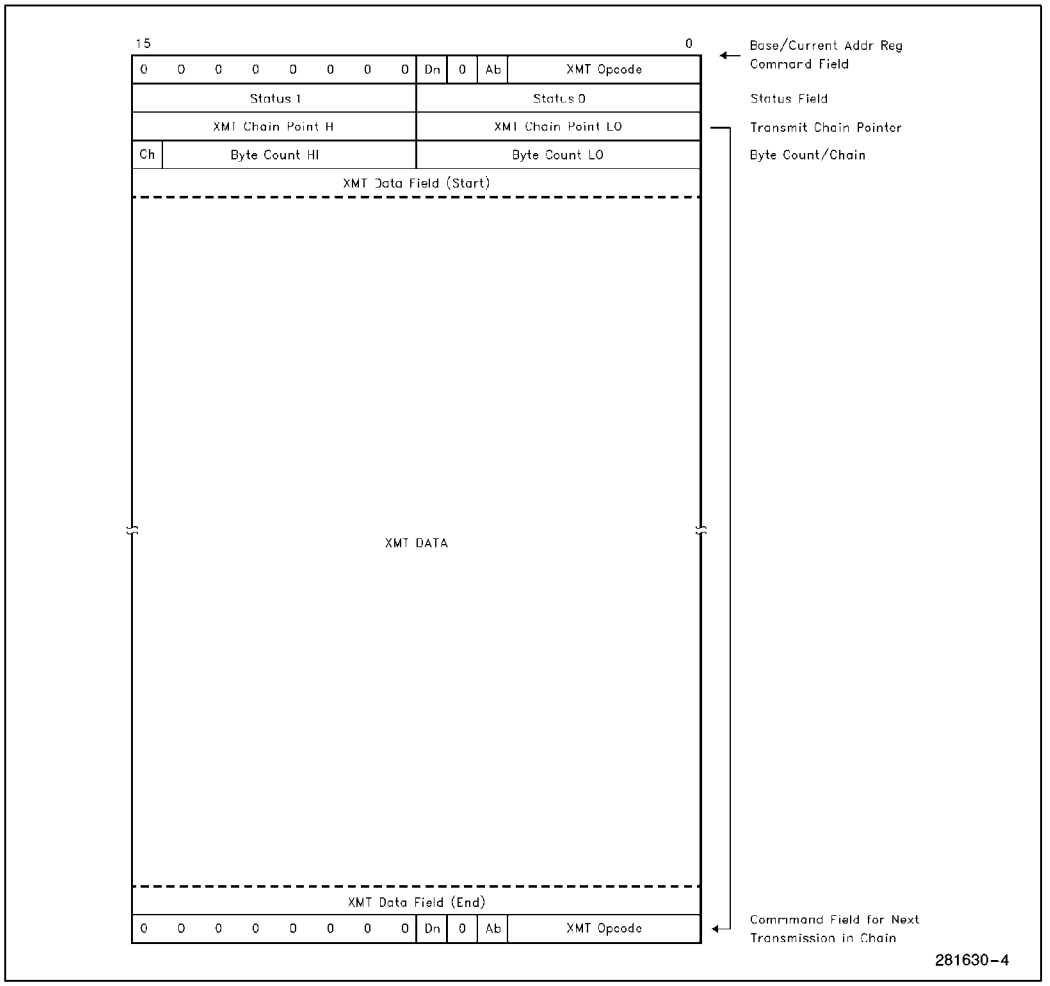


Figure 7-1. XMT Block Memory Structure (16-Bit)

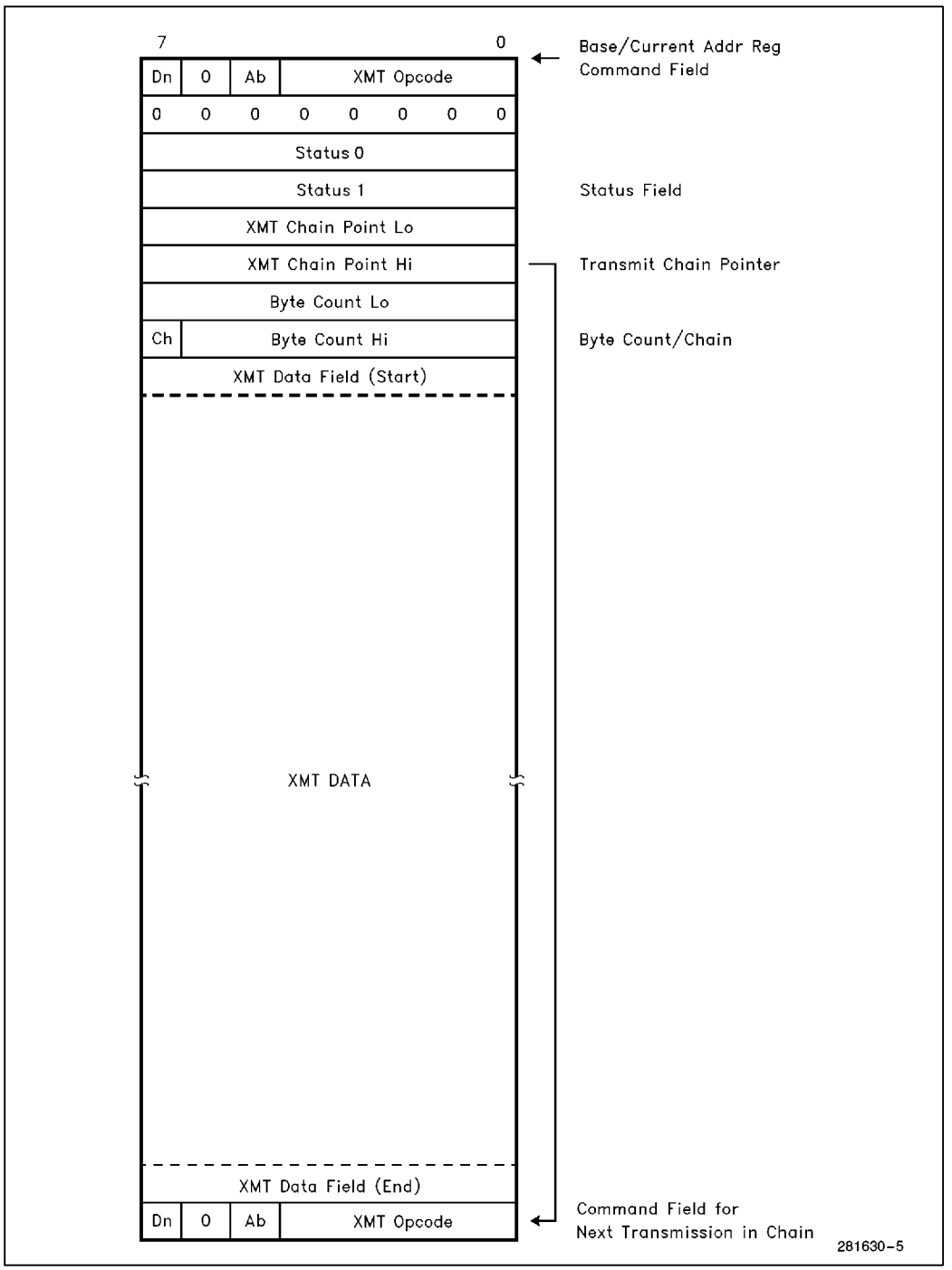


Figure 7-2. XMT Block Memory Structure (8-Bit)

Status Field

The two bytes of the Status Field (Status 0 and Status 1) are shown in detail in Figure 7-3. In a 16-bit wide interface, these two bytes will combine to form one word. This field is originally set to all 0's by the CPU as the XMT block is copied to memory. It is updated by the 82595TX upon completion of the transmission.

7.2 XMT Chaining

The 82595TX can transmit consecutive frames without the CPU having issued a separate Transmit command for each frame. This is called Transmit Chaining. The 82595TX Transmit Chaining memory structure for a 16-bit interface is shown in Figure 7-4, with an 8-bit interface shown in Figure 7-5. The 82595TX registers which control the memory structure are also shown. The CPU places multiple XMT blocks in the Transmit buffer. The 82595TX will transmit each frame in the chain, reporting the status for each frame in its status field. If Concurrent Processing is enabled, the copy of additional frames in a chain will take place while the first portion of the chain (one or more frames) is being transmitted by the 82595TX. This chain can be dynamically updated by the CPU to add more frames to the chain. The transmit chain can be configured to terminate upon an errored frame (maximum collisions, underrun, lost CRS, etc.) or it can continue to the next frame in the chain. The 82595TX can be configured to interrupt upon completion of each transmission or to interrupt at the end of the transmit chain only (it always interrupts upon an errored condition).

7	6	5	4	3	2	1	0	
TX DEF	HRT BET	MAX COL	X	No OF COLLISIONS				Status 0
COLL	X	TX OK	0	LTCOL	LST CRS	X	UND RUN	Status 1

Figure 7-3. Transmit Result

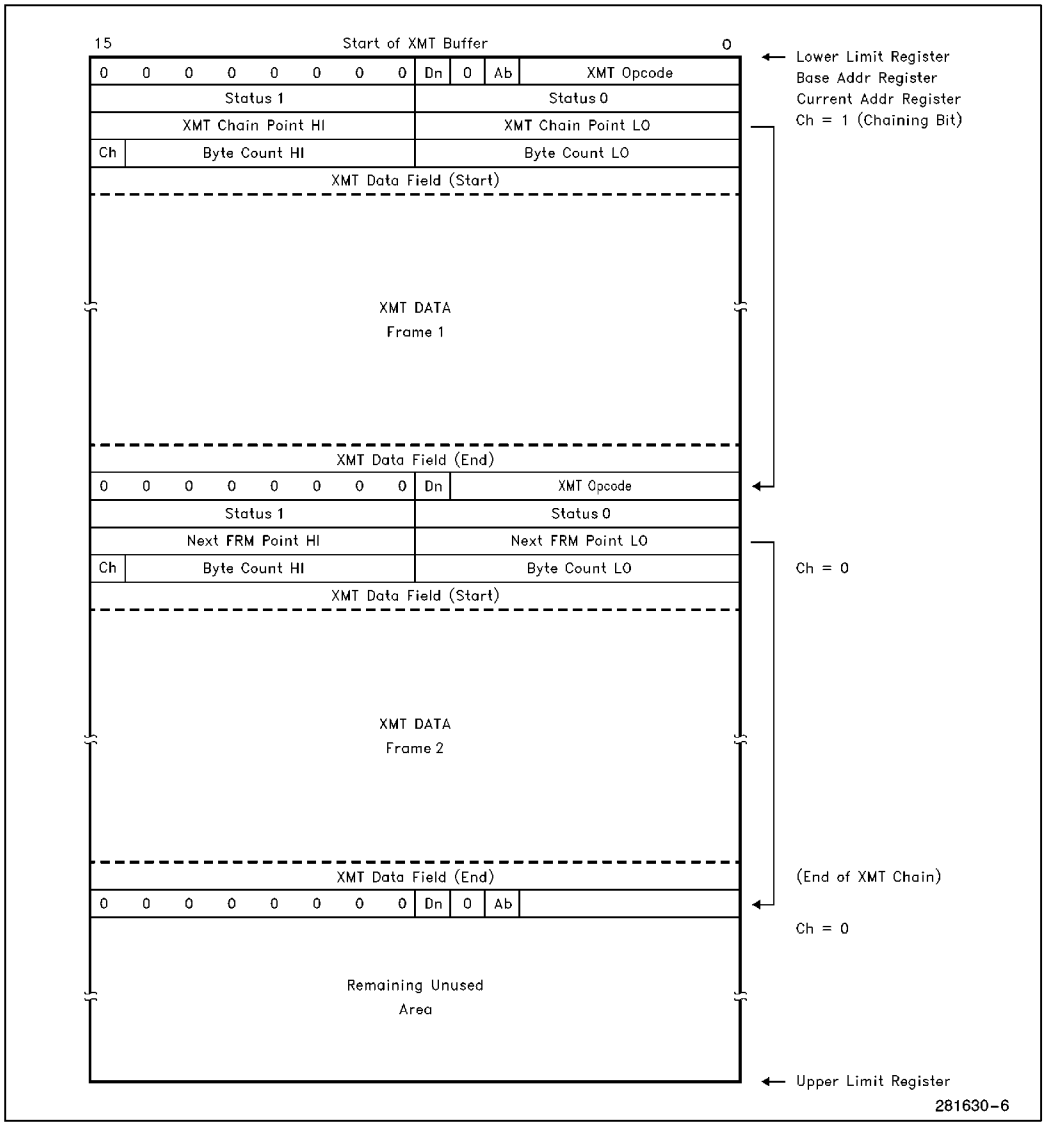


Figure 7-4. 82595TX XMT Chaining Memory Structure

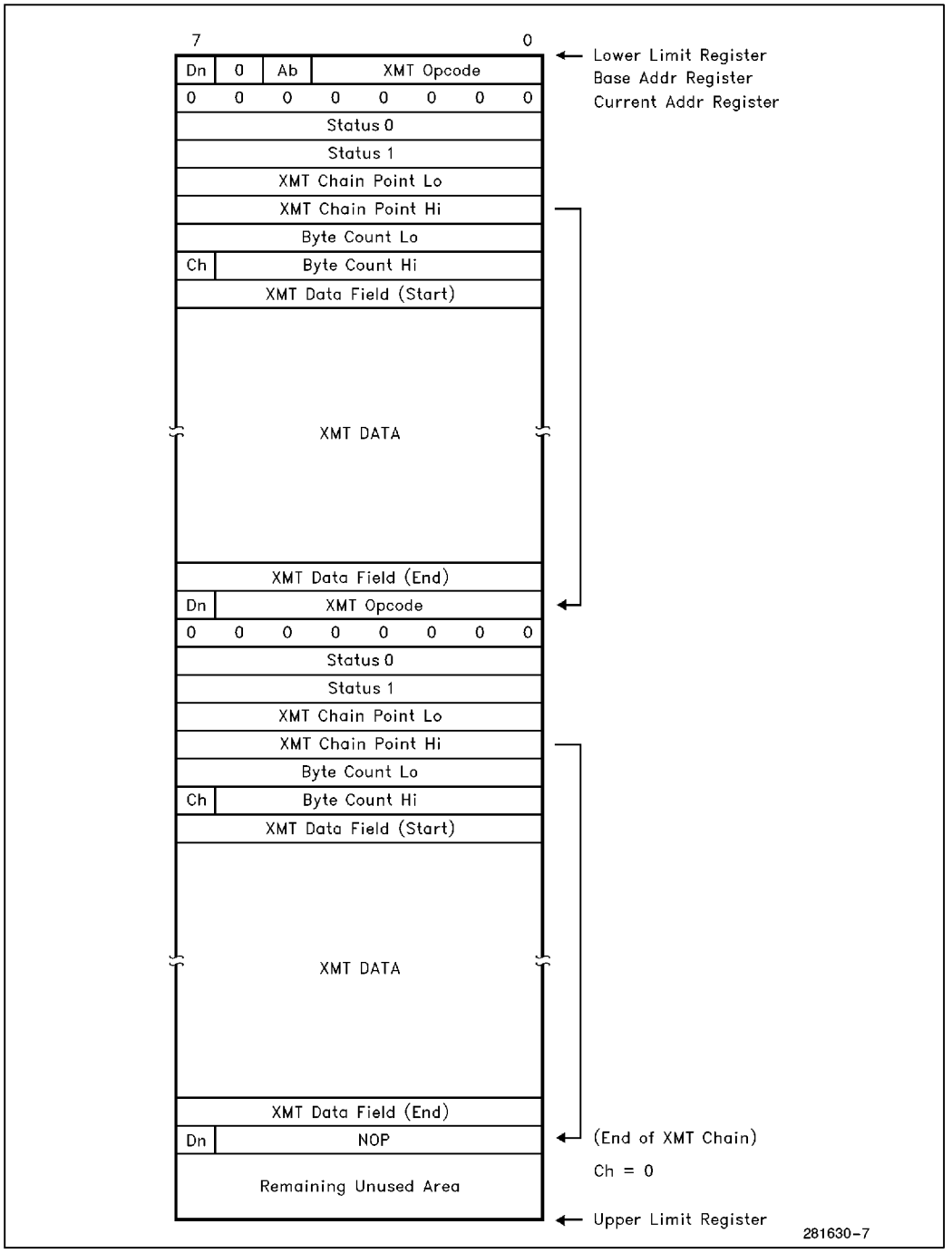


Figure 7-5. XMT Block Memory Structure (8-Bit)

7.3 Automatic Retransmission on Collision

The 82595TX performs automatic retransmission when a collision is experienced within the first slot time of the transmission with no intervention by the CPU. The 82595TX performs jamming, exponential backoff, and retransmission attempts as specified by the IEEE 802.3 spec. The 82595TX reaccesses its local memory automatically on collision. This allows the 82595TX to retransmit up to 15 times after the initial collision with no CPU interaction.

The 82595TX reaccesses the data in its transmit buffer by simply resetting the value of its Current Address Register back to the value of the Base Address Register (the beginning of the XMT block) and repeating the DMA process to access the data in the transmit buffer again. Once it regains access to the link, retransmission is attempted. When Transmit Chaining is utilized, the process for retransmission is exactly the same. Only the current frame in the chain will be retransmitted, since the Base Address Register is updated upon transmission of each frame.

8.0 FRAME RECEPTION

The 82595TX implements a recyclable ring buffer DMA structure to support the reception of back to back incoming RCV frames with minimal CPU overhead. The structure of the RCV frames in memory is optimized to allow the CPU to process each frame with as few software processing steps as possible. The frame format is arranged so that all of the required infomation for each frame (status, size, etc.) is located at the beginning of the frame.

8.1 82595TX RCV Memory Structure

The 82595TX RCV memory structure for a 16-bit interface is shown in Figure 8-1. Figure 8-2 shows this structure for the 8-bit interface. Once an incoming frame passes the 82595TX's address filtering, the 82595TX deposits the frame into the RCV Data field of the RCV Memory Structure. The fields which precede the RCV Data field, Event, Status, Byte Count, Next Frame Pointer, and the Event field of the following frame, are updated upon the end of the frame after all of the incoming data has been deposited in the RCV Data field. If Receive Concurrent Processing is enabled, the CPU processes the receive frame without the entire frame being deposited by the 82595TX to the RCV Data Field. The 85295TX, along with the software driver, determines the portion of the frame being copied to host memory before the rest of that frame is copied to local memory. An interrrupt is asserted by the 82595TX (EOF) after frame reception has been completed.

If the 82595TX is configured to Discard Bad Frames, it will discard all incoming errored frames by resetting its DMA Current Address Register back to the value of the Base Address Register and not updating any of the fields in the RCV frame structure. This area will now be reused to store the next incoming frame.

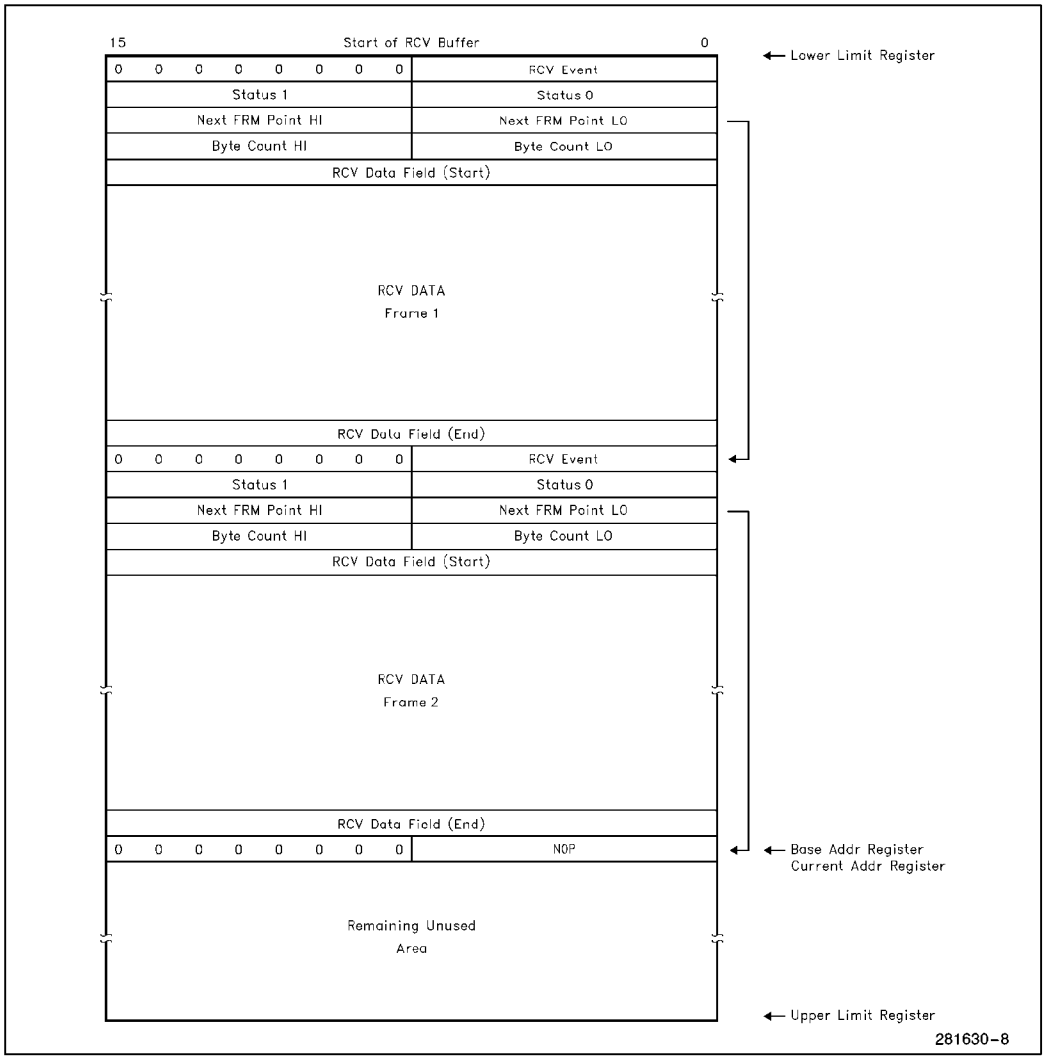


Figure 8-1. 82595TX RCV Memory Structure (16-Bit)

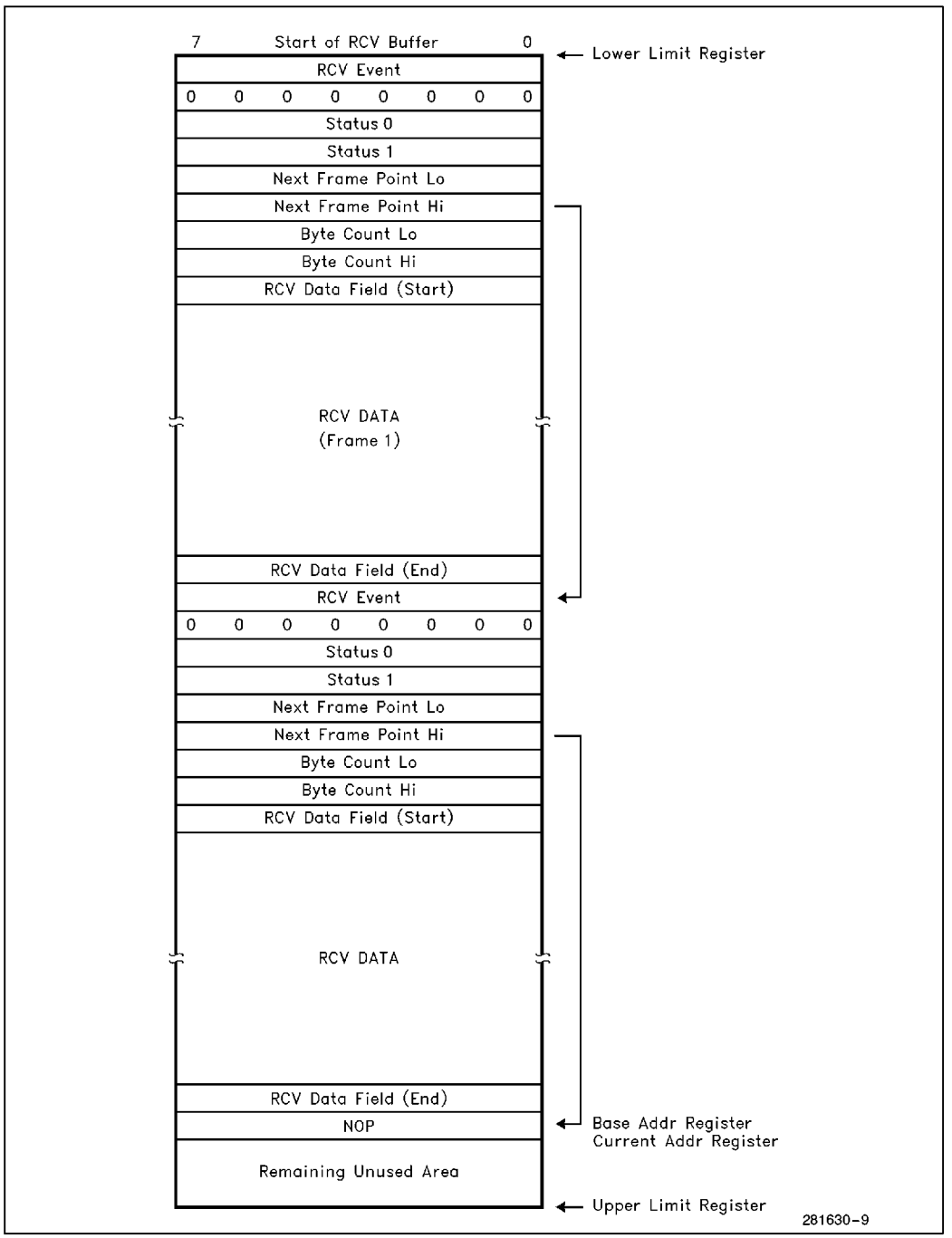


Figure 8-2. 82595TX RCV Memory Structure (8-Bit)

Status Field

The two bytes of the Status Field (Status 0 and Status 1) are shown in detail in Figure 8-3. In a 16-bit wide interface, these two bytes will combine to form one word. The 82595TX provides this field for each incoming frame.

8.2 RCV Ring Buffer Operation

The 82595TX RCV Ring Buffer operation is illustrated in Figure 8-4. The 82595TX copies received frames sequentially into the RCV Buffer area of the local memory. The CPU processes these frames by copying the frames from the local memory. After a frame is processed, the CPU updates the 82595TX's Stop Register to point to the last location processed. This indicates that the RCV Buffer memory which precedes the value programmed in the Stop Register is now free area (it has been processed by the CPU). When the 82595TX reaches the end of the RCV Buffer (the Upper Limit Register value) it will now wrap around back to the beginning of the buffer, and continue to copy RCV frames into the buffer, beginning at the value pointed to by the Lower Limit Register. The 82595TX will continue to copy frames into the RCV Buffer area as long as it does not reach the address pointed to by the Stop Register (if this does occur, the 82595TX stops copying the frames into memory and issues an Interrupt to the CPU). As the CPU processes additional incoming frames, the Stop Register value continues to be moved. This action allows the CPU to keep ahead of the incoming frames and allows the Ring Buffer to be continually recycled as the memory space consumed by an incoming frame is reused as that frame is processed.

7	6	5	4	3	2	1	0	
SRT FRM	X	X	1	X	X	IA MCH	RCLD	Status 0
TYP/$\overline{\text{LEN}}$	0	RCV OK	LEN ERR	CRC ERR	ALG ERR	0	OVR RN	Status 1

Figure 8-3. RCV Status Field

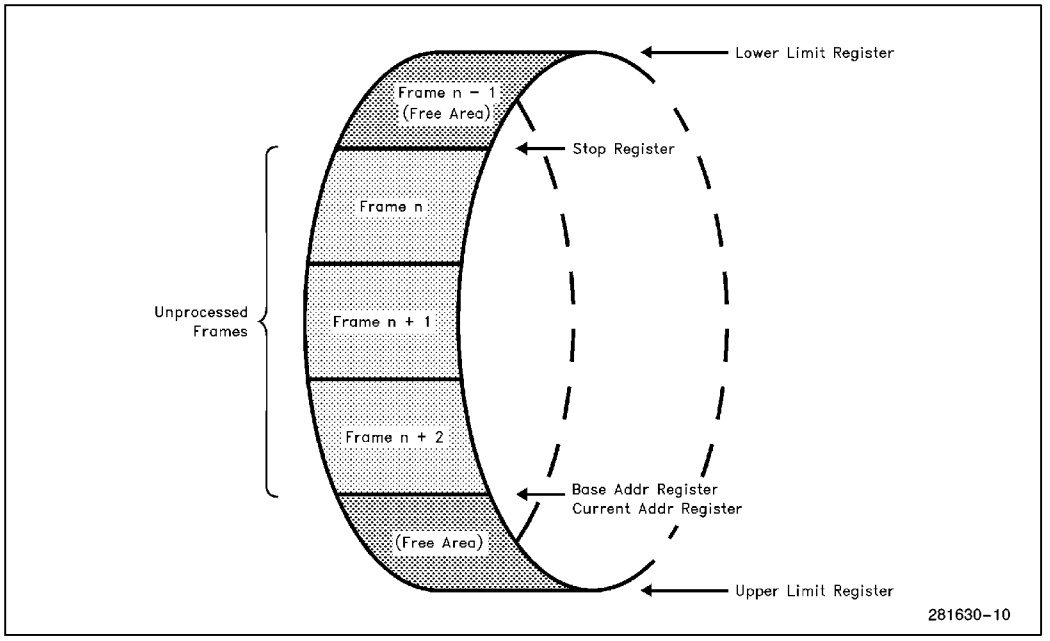


Figure 8-4. 82595TX RCV Ring Buffer Operation

9.0 SERIAL INTERFACE

The 82595TX's serial interface subsystem incorporates all the active circuitry required to interface the 82595TX to 10BASE-T networks or to the attachment unit (AUI) interface. It includes on-chip AUI and TPE drivers and receivers as well as Manchester Encoder/Decoder and Clock Recovery circuitry. The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully compliant IEEE 802.3 AUI interface. The AUI port can also be interfaced to a transceiver to provide a fully compliant IEEE 802.3 10BASE2 (Cheapernet) interface. The TPE port provides a fully compliant 10BASE-T interface. The 82595TX automatically enables either the AUI or TPE interface, depending on which medium is active. This automatic selection can be overridden by software configuration. The TPE interface also features a polarity fault detection and correction circuit which will detect and correct a polarity error on the twisted pair wire, the most common wiring fault in twisted pair networks.

A 20 MHz parallel resonant crystal is used to control the clock generation oscillator, which provides the basic 20 MHz clock source. An internal divide-by-two counter generates the 10 MHz ±0.01% clock required by the IEEE 802.3 specification.

We recommend that a crystal that meets the following specifications be used:

- Quartz Crystal
- 20.00 MHz ±0.002% at 25°C
- Accuracy ±0.005% over Full Operating Temperature, 0°C to +70°C
- Parallel resonant with 20 pF Load Fundamental Mode

Several vendors have such crystals; either off-the-shelf or custom-made. Two possible vendors are:

1. M-Tron Industries, Inc.
   Yankton, SD 57078
   Specifications:
   Part No. HC49 with 20 MHz, 50 PPM over 0°C to +70°C, and 20 pF fundamental load.
2. Crystek Corporation
   100 Crystal Drive
   Ft. Myers, FL 33907
   Part No. 013212

The accuracy of the Crystal Oscillator frequency depends on the PC board characteristics; therefore, it is advisable to keep the X1 and X2 traces as short as possible. The optimum value of C1 and C2 should be determined experimentally under nominal operating conditions. The typical value of C1 and C2 is between 22 pF and 35 pF.

An external 20 MHz MOS-level clock may be applied to pin X1, if pin X2 is left floating.

A summary of the 82595TX's serial interface subsections functions is shown below:

- **Manchester Encoder/Decoder and Clock Recovery**
- **Diagnostic Loopback**
- **Reset-Low-Power Mode**
- **Network Status Indicators**
- **Defeatable Jabber Timer**
- **User Test Modes**
- **Complies with IEEE 802.3 AUI Standard**
  - **Direct Interface to AUI Transformers**
  - **On-Chip AUI Squelch**
- **Complies with IEEE 802.3 10BASE-T for Twisted Pair Ethernet**
  - **Selectable Polarity Detection and Correction**
  - **Direct Interface to TPE Analog Filters**
  - **On-Chip TPE Squelch**
  - **Defeatable Link Integrity for Pre-Standard Networks**
  - **Supports 4 LEDs (Link Integrity, Activity, AUI/BNC DIS and Polarity Correction)**

10.0 APPLICATION NOTES

This section is intended to provide Ethernet LAN designers with a basic understanding of how the 82595TX is used in a buffered LAN design.

10.1 Bus Interface

The 82595TX Bus Interface unit integrates the interface to both an ISA compatible bus and a PCMCIA rev 2.0 bus. Selection of the desired bus interface is done by strapping the PCMCIA/ISA pin accordingly. Two 74ALS245 transceivers are used to buffer the 82595TX's data bus, with the 82595TX providing the control over the transceivers. The data bus is not buffered in a PCMCIA design. The 82595TX also provides the complete control and address interface to the host system bus. When the ISA bus interface is selected, it implements the complete ISA bus protocol. When PCMCIA interface is selected, the complete PCMCIA bus interface protocol is implemented.

10.2 Local Memory Interface

The 82595TX's local memory interface includes a DMA unit which controls data transfers between the 82595TX and the local memory DRAM. The 82595TX can support up to 64 Kbytes of local DRAM.

The 82595TX provides address decoding and control to allow access to an external Boot EPROM or a FLASH. Addition of a Boot EPROM or FLASH to an ISA solution is optional. The FLASH is always contained as part of a PCMCIA solution. The 82595TX also supports a separate IA PROM if one is desired. For this example, the IA is assumed to be stored in the serial EEPROM for the ISA solution and in the FLASH for the PCMCIA solution.

10.3 EEPROM Interface (ISA Only)

The 82595TX provides a complete interface to a serial EEPROM for ISA adapter designs. For ISA motherboard designs and PCMCIA designs, the EEPROM is not required. The EEPROM is used to store configuration information such as Memory and IO Mapping Window, Interrupt line selection, Plug N' Play resource data local bus width, etc. The EEPROM is used to replace jumper blocks which previously contained this type of information. The 82595TX also contains an optional jumper interface (J0–J2). These jumpers can be used to select the IO mapping window of the solution. In the case of this design, the jumper block is grounded (disabled) with the IO mapping window being contained in the EEPROM.

10.4 Serial Interface

The 82595TX's serial interface provides either an AUI port interface or a Twisted Pair Ethernet (TPE) interface. The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully compliant IEEE 802.3 10BASE5 interface. The AUI port can also be interfaced to a transceiver device on the adapter to provide a fully compliant IEEE 802.3 10BASE2 (Cheapernet) interface. The TPE port provides a fully compliant 10BASE-T interface. The 82595TX automatically enables either the AUI or TPE interface, depending on which medium is connected to the chip. This automatic selection can be overridden by software configuration.

10.4.1 AUI CIRCUIT

When used in conjunction with pulse transformers, the 82595TX provides a complete IEEE 802.3 AUI interface. In order to meet the 16V fault tolerance specification of IEEE 802.3, a pulse transformer is recommended. The transformer should be placed between the TRMT, RCV, and CLSN pairs of the 82595TX and the DO, DI, and CI pairs of the AUI (DB-15) connector. The pulse transformer should have the following characteristics:

- 75 μH minimum inductance (100 μH recommended)
- 2000V isolation between the primary and secondary windings
- 2000V isolation between the primaries of separate transformers
- 1:1 Turns ratio

The RCV and CLSN input pairs should each be terminated by 78.7Ω $\pm$1% resistors.

10.4.2 TPE CIRCUIT

The 82595TX provides the line drivers and receivers needed to directly interface to the TPE analog filter network. The TPE receive section requires a 100Ω termination resistor, a filter section (filter, isolation transformer, and a common mode choke) as described by the 10BASE-T 802.3i-1990 specification.

The TPE transmit section is implemented by connecting the 82595TX's four TPE outputs (TDH, $\overline{\text{TDH}}$, TDL, $\overline{\text{TDL}}$) to a resistor summing network to form the differential output signal. The parallel resistance of R5 and R6 sets the transmitters maximum output voltage, while the difference (R5 $-$ R6)/R5 + R6), is used to reduce the amplitude of the second half of the fat bit (100 ns) to a predetermined level. This predistortion reduces line overcharging, a major source of jitter in the TPE environment. The output of the summing network is then fed into the above

mentioned filter and then to the 10BASE-T connector (RJ-45). Analog Front End solutions can be purchased in a single-chip solution from several manufacturers. The solution described in this data sheet uses the Pulse Engineering (PE65434) AFE.

10.4.3 LED CIRCUIT

The 82595TX's internal LED drivers support four LED indicators displaying node status and activity (i.e., Transmit data, receive data, collisions, link integrity, polarity correction, and port (TPE/AUI). To implement the LED indicators, connect the LED driver output to an LED in series with a 510Ω resistor tied to V_{CC}. Each driver can sink up to 10 mA of current with an output impedance of less than 50Ω.

10.5 Layout Guidelines

10.5.1 GENERAL

The analog section, as well as the entire board itself, should conform to good high-frequency practices and standards to minimize switching transients and parasitic interaction between various circuits. To achieve this, follow these guidelines:

Make power supply and ground traces as thick as possible. This will reduce high-frequency cross coupling caused by the inductance of thin traces.

Connect logic and chassis ground together.

You must connect all V_{CC} pins to the same power supply and all V_{SS} pins to the same ground plane. Use separate decoupling and noise conditions per power-supply/ground pin.

Close signal paths to ground as close as possible to their sources to avoid ground loops and noise cross coupling.

Use high-loss magnetic beads on power supply distribution lines.

10.5.2 CRYSTAL

The crystal should be adjacent to the 82595TX and trace lengths should be as short as possible. the X1 and X2 traces should be symmetrical.

10.5.3 82595TX ANALOG DIFFERENTIAL SIGNALS

The differential signals from the 82595TX to the transformers, analog front end, and the connectors should be symmetrical for each pair and as short as possible.

As a general rule, the trace widths should be one to three times the distance between the PCB layers to eliminate excessive trace inductance.

The differential signals should also be isolated from the high speed logic signals on the same layer as well as on any sublayers of the PCB.

Group each of the circuits together, but keep them separate from each other. Separate their grounds.

In layout, the circuitry from the connectors to the filter network should have the ground and power planes removed from beneath it. This will prevent ground noise from being induced into the analog front end.

All trace bends should not exceed 45 degrees.

10.5.4 DECOUPLING CONSIDERATIONS

Four 0.1 μF ceramic capacitors should be used. Place one on each side in the center of the I.C. (V_{CC} pins 23, 51, 89, 125 are recommended) adjacent to the 82595TX. Connect the capacitors directly to the V_{CC} pins on the 82595TX and then directly to the ground plane. In addition to the 0.1 μF capacitors, a 10 μF tantalum should be used near one of the 82595TX's V_{CC} pins. The proximity of this capacitor to the 82595TX is not as critical as in the case of the 0.1 μF capacitors. Placement of this capacitor within approximately one inch of the 82595TX is recommended.

11.0 ELECTRICAL SPECIFICATIONS AND TIMINGS

11.1 Absolute Maximum Ratings

Case Temperature under Bias .....0°C to +85°C

Storage Temperature .....−65°C to +140°C

All Output and Supply Voltages .....−0.5V to +7V

All Input Voltages .....−1.0V to +6.0V(1)

Further information on the quality and reliability of the 82595TX may be found in the *Components Quality and Reliability Handbook*, Order Number 210997.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Table 11-1. D.C. Characteristics (T_C = 0°C to +85°C, V_{CC} = 5V ±5%)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input LOW Voltage (TTL)	−0.3	+0.8	V	
V_{IH}	Input HIGH Voltage (TTL)	2.0	V_{CC} + 0.3	V	
$V_{IH(JUMPR)}$	Input HIGH Voltage (Jumpers)	3.0	V_{CC} + 0.3	V	
V_{OL1}	Output LOW Voltage(11)		0.45	V	I_{OL} = 2 mA
V_{OL2}	Output LOW Voltage(11)		0.45	V	I_{OL} = 6 mA
V_{OL3}	Output LOW Voltage(11)		0.45	V	I_{OL} = 12 mA
V_{OL4}	Output LOW Voltage(11)		0.45	V	I_{OL} = 17 mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = −1 mA
V_{OL} (LED)(2)	Output Low Voltage		0.45	V	I_{OL} = 10 mA
V_{OH} (LED)	Output High Voltage	3.9		V	I_{OH} = −500 μA
I_{LP}	Leakage Current, Low Power Mode(3)		±10	μA	$0 \le V_I \le V_{CC}$
R_{DIFF}	Input Differential-Resistance(4)	10		KΩ	DC
V_{IDF} (TPE)(5)	Input Differential Accept Input Differential Reject	±0.5	±3.1 ±0.3	V_P V_P	5 MHz ≤ f ≤ 10 MHz
R_S (TPE)(6)	Output Source Resistance	6	13	Ω	$\|I_{LOAD}\|$ = 25 mA
V_{IDF} (AUI)(7)	Input Differential Accept Input Differential Reject	±0.3	±1.5 ±0.16	V_P V_P	
V_{ICM} (AUI)	AC Input Common Mode		±0.5 ±0.1	V_P V_P	f ≤ 40 KHz 40 KHz ≤ f ≤ 10 MHz
V_{ODF} (AUI)(8)	Output Differential Voltage	±0.45	±1.2	V	
I_{OSC} (AUI)	AUI Output Short Circuit Current		±150	mA	Short Circuit to V_{CC} or GND
VU (AUI)	Output Differential Undershoot		−100	mV	
V_{ODI} (AUI)	Differential Idle Voltage(9)		40	mV	
I_{CC}	Power Supply Current		90	mA	
I_{CCPD}	Power Supply Current– Power Down Mode		1	mA	
C_{IN}(10)	Input Capacitance		10	pF	@ f = 1 MHz

NOTES:
1. The voltage levels for RCV and CLSN pairs are −0.75V to +8.5V.
2. LED Pins: ACTLED, TPE__BNC__$\overline{AUI}$, POLED, LILED.
3. Pins: ACTLED, TPE__BNC__$\overline{AUI}$, POLED, $\overline{LILED}$.
4. Pins: RD to $\overline{RD}$, RCV to $\overline{RCV}$ and CLNS to $\overline{CLSN}$.
5. TPE input pins: RD and $\overline{RD}$.
6. TPE output pins: TDH, $\overline{TDH}$, TDL and $\overline{TDL}$, R_S measure V_{CC} or V_{SS} to pin.
7. AUI input pins: RCV and CLSN pairs.
8. AUI output pins: TPMT pair.
9. Measured 8.0 μs after last positive transition of data packet.
10. Characterized, not tested.
11. V_{OL1} is pins SD_{0-15}, $\overline{RAS}$, $\overline{CAS}$, EEPROMCS, $\overline{IAPROMCS}$, $\overline{BOOTCS}$, $\overline{DIRH}$, and $\overline{DIRL}$. V_{OL2} is pins $MDATA_{0-3}$, $MADDR_{0-8}$, TDO, $\overline{LWE}$, $\overline{SBHE}$, and $\overline{SMOUT}$. V_{OL3} is pins IOCHRDY and INT_{0-4}. V_{OL4} is $\overline{IOCS16}$.

11.1.1 PACKAGE THERMAL SPECIFICATIONS

The 82595TX is specified for operation when case temperature is within the range of 0°C to 85°C. The case temperature may be measured in any environment to determine whether the 82595TX is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

The ambient temperature is guaranteed as long as T_C is not violated. The ambient temperature can be calculated from the θ_{JA} and the θ_{JC} from the following equations:

$$T_J = T_C + P*\theta_{JC}$$
$$T_A = T_J - P*\theta_{JA}$$
$$T_C = T_A + P*\{\theta_{JA} - \theta_{JC}\}$$

θ_{JA} and θ_{JC} values for the 144 tQFP package are as follows:

Thermal Resistance (°C/Watt)

θ_{JC}	θ_{JA} − VS − Airflow ft/min (m/Sec)	
	0 (0)	200 (1.01)
17	48	38

11.2 A.C. Timing Characteristics

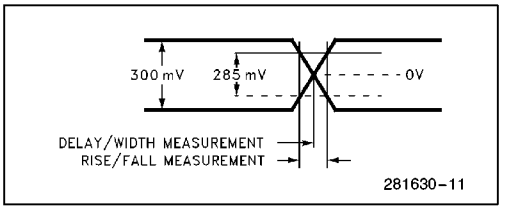


Figure 11-1. Voltage Levels for Differential Input Timing Measurements (RCV and CLSN Pairs)

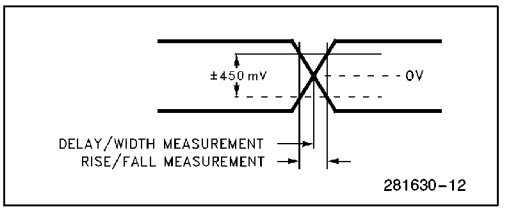


Figure 11-2. Voltage Levels for TDH, TDL, $\overline{TDH}$ and $\overline{TDL}$

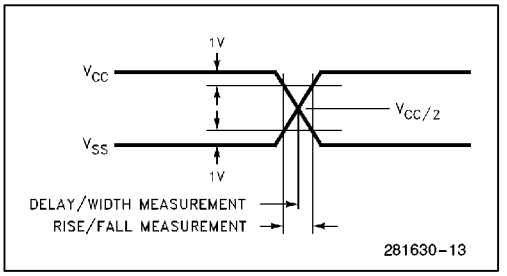


Figure 11-3. Voltage Levels for TRMT Pair Output Timing Measurements

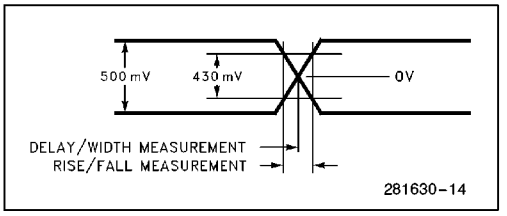


Figure 11-4. Voltage Levels for Differential Input Timing Measurements (RD Pair)

11.3 A.C. Measurement Conditions

1. T_C = 0°C to +85°C, V_{CC} = 5V ±5%
2. The signal levels are referred to in Figures 1, 2, 3 and 4.
3. A.C. Loads:
   a) AUI Differential: a 10 pF total capacitance from each terminal to ground and a load resistor of 78Ω ±1% in parallel with a 27 μH ±5% inductor between terminals.
   b) TPE: 20 pF total capacitance to ground.

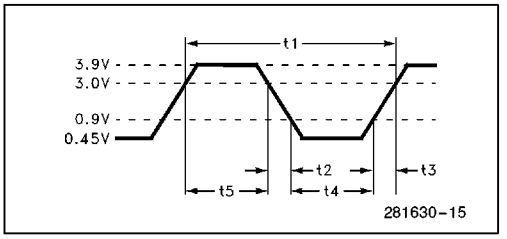


Figure 11-5. X1 Input Voltage Levels for Timing Measurements

Table 11-2. Clock Timing

Symbol	Parameter	Min	Max	Unit
t1	X1 Cycle Time	49.995	50.005	ns
t2	X1 Fall Time		5	ns
t3	X1 Rise Time		5	ns
t4	X1 Low Time	15		ns
t5	X1 High Time	15		ns

11.4 ISA Interface Timing

Table 11-3. ISA 16-Bit I/O Access

Parameter	Description	Min	Max	Units	Comments
T1a	BALE Active to Inactive	50		ns	
T2a	BALE Active from Command Inactive	35		ns	
T3a	AEN Valid to Falling Edge of BALE	20		ns	Applies for Early IOCHRDY
T4a	AEN Valid to I/O Command Active	100		ns	
T5a	AEN Valid from I/O Command Inactive	30		ns	
T6a	SA Valid to Falling BALE	20		ns	Applies for Early IOCHRDY
T7a	SA to CMD Active	63		ns	
T8a	SA Valid Hold from CMD Inactive	42		ns	
T9a	Valid SA to $\overline{\text{IOCS16}}$ Active		100	ns	
T10a	$\overline{\text{IOCS16}}$ Valid Hold from Valid SA	0		ns	
T11a	CMD Active to Inactive	125		ns	
T12a	CMD Inactive to Active	92		ns	*Before* I/O Command
T13a	Active CMD to Valid IOCHRDY		18	ns	
T14a	IOCHRDY Inactive Pulse		12	μs	
T15a	CMD Active Hold from IOCHRDY Active	80		ns	Applies to Ready Cycles
T16a	DATA Driven from READ CMD Active	0		ns	
T17a	Valid READ Data from CMD Active		54	ns	Applies to Standard Cycles Only
T18a	Valid READ Data from IOCHRDY Active		42	ns	Applies to Ready Cycles Only
T19a	READ Data Hold from CMD Inactive	0		ns	
T20a	READ CMD Inactive to Data Tristate		30	ns	
T21a	CMD to WRITE Data Active		62	ns	
T22a	WRITE Data Hold from CMD Inactive	25		ns	
T23a	WRITE CMD Inactive to Data Tristate		30	ns	
T24a	IOCHRDY Inactive to CMD Active	15		ns	Applies to Early IOCHRDY
T25a	BALE Inactive to CMD Active	55		ns	Applies to Early IOCHRDY
T26a	READ CMD Active to $\overline{\text{DIRx}}$ Active		34	ns	
T27a	READ CMD Inactive to $\overline{\text{DIRx}}$ Inactive		15	ns	

Table 11-4. ISA 8-Bit I/O Access

Parameter	Description	Min	Max	Units	Comments
T1b	BALE Active to Inactive	50		ns	
T2b	BALE Active from Command Inactive	35		ns	
T3b	AEN Valid to Falling Edge of BALE	20		ns	Applies to Early IOCHRDY
T4b	AEN Valid to I/O Command Active	100		ns	
T5b	AEN Valid from I/O Command Inactive	30		ns	
T6b	SA Valid to Falling BALE	20		ns	Applies to Early IOCHRDY
T7b	SA to CMD Active	63		ns	
T8b	SA Valid Hold from CMD Inactive	42		ns	
T9b	Valid SA to $\overline{\text{IOCS16}}$ Active		100	ns	
T10b	$\overline{\text{IOCS16}}$ Valid Hold from Valid SA	0		ns	
T11b	CMD Active to Inactive	125		ns	
T12b	CMD Inactive to Active	92		ns	*Before* I/O Command
T13b	Active CMD to Valid IOCHRDY		18	ns	
T14b	IOCHRDY Inactive Pulse		12	μs	
T15b	CMD Active Hold from IOCHRDY Active	80		ns	Applies to Ready Cycles
T16b	DATA Driven from READ CMD Active	0		ns	
T17b	Valid READ Data from CMD Active		54	ns	Applies to Standard Cycles Only
T18b	Valid READ Data from IOCHRDY Active		42	ns	Applies to Ready Cycles Only
T19b	READ Data Hold from CMD Inactive	0		ns	
T20b	READ CMD Inactive to Data Tristate		30	ns	
T21b	CMD to WRITE Data Active		62	ns	
T22b	WRITE Data Hold from CMD Inactive	15		ns	
T23b	WRITE CMD Inactive to Data Tristate		30	ns	
T24b	IOCHRDY Inactive to CMD Active	15		ns	Applies to Early IOCHRDY
T25b	BALE Inactive to CMD Active	55		ns	Applies to Early IOCHRDY
T26b	READ CMD Active to $\overline{\text{DIRx}}$ Active		34	ns	
T27b	READ CMD Inactive to $\overline{\text{DIRx}}$ Inactive		15	ns	

Table 11-5. ISA 8-Bit Memory Access

Parameter	Description	Min	Max	Units	Comments
T1c	BALE Active to Inactive	50		ns	
T2c	BALE Active from Command Inactive	35		ns	
T4c	AEN Valid to Command Active	100		ns	
T5c	AEN Valid from Command Inactive	30		ns	
T7c	SA to CMD Active	63		ns	
T8c	SA Valid Hold from CMD Inactive	42		ns	
T11c	CMD Active to Inactive	125		ns	
T12c	CMD Inactive to Active	60		ns	*Before* Memory Command
T13c	Active CMD to Valid IOCHRDY		18	ns	
T14c	IOCHRDY Inactive Pulse		12	μs	
T15c	CMD Active Hold from IOCHRDY Active	80		ns	Applies to Ready Cycles
T16c	DATA Driven from READ CMD Active	0		ns	
T18c	Valid READ Data from IOCHRDY Active		42	ns	Applies to Ready Cycles Only
T19c	READ Data Hold from CMD Inactive	0		ns	
T20c	READ CMD Inactive to Data Tristate		30	ns	
T21c	CMD to WRITE Data Active		52	ns	
T23c	WRITE CMD Inactive to Data Tristate		30	ns	
T26c	READ CMD Active to $\overline{\text{DIRx}}$ Active		34	ns	
T27c	READ CMD Inactive to $\overline{\text{DIRx}}$ Inactive		15	ns	

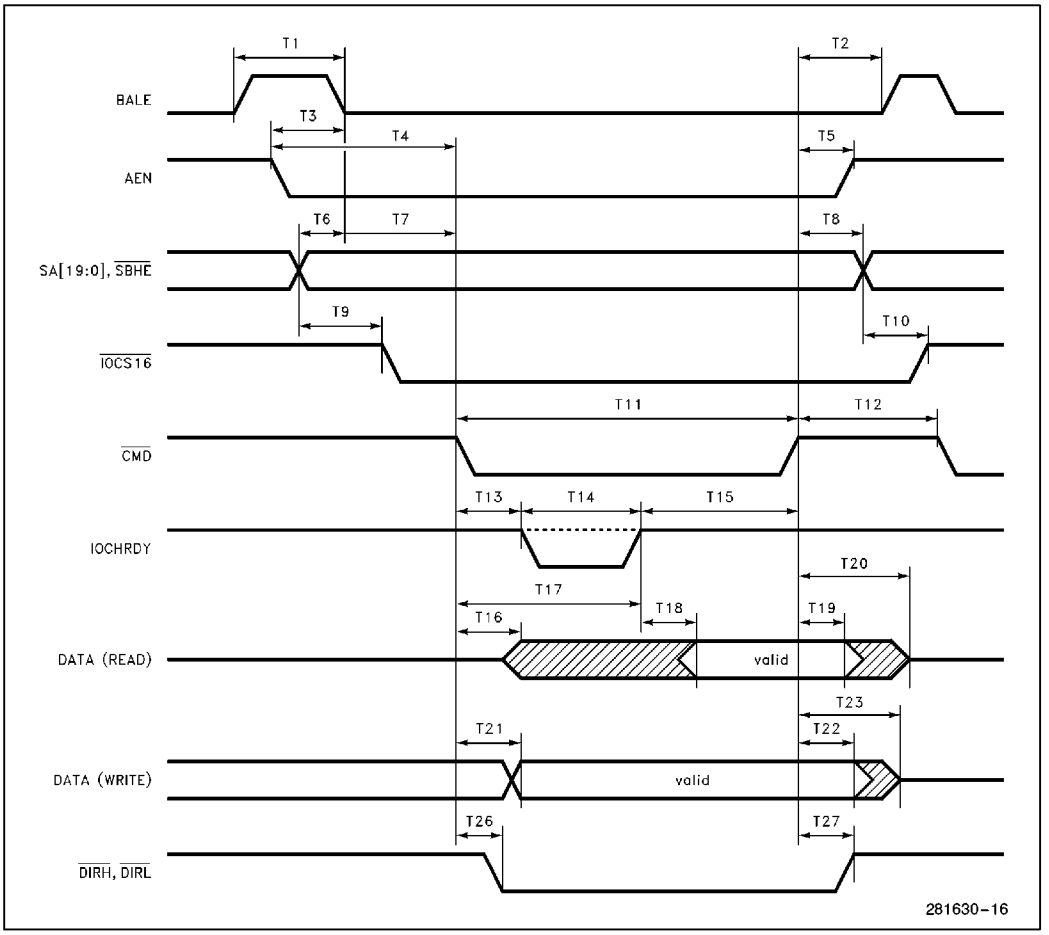


Figure 11-6. ISA-Compatible Cycle

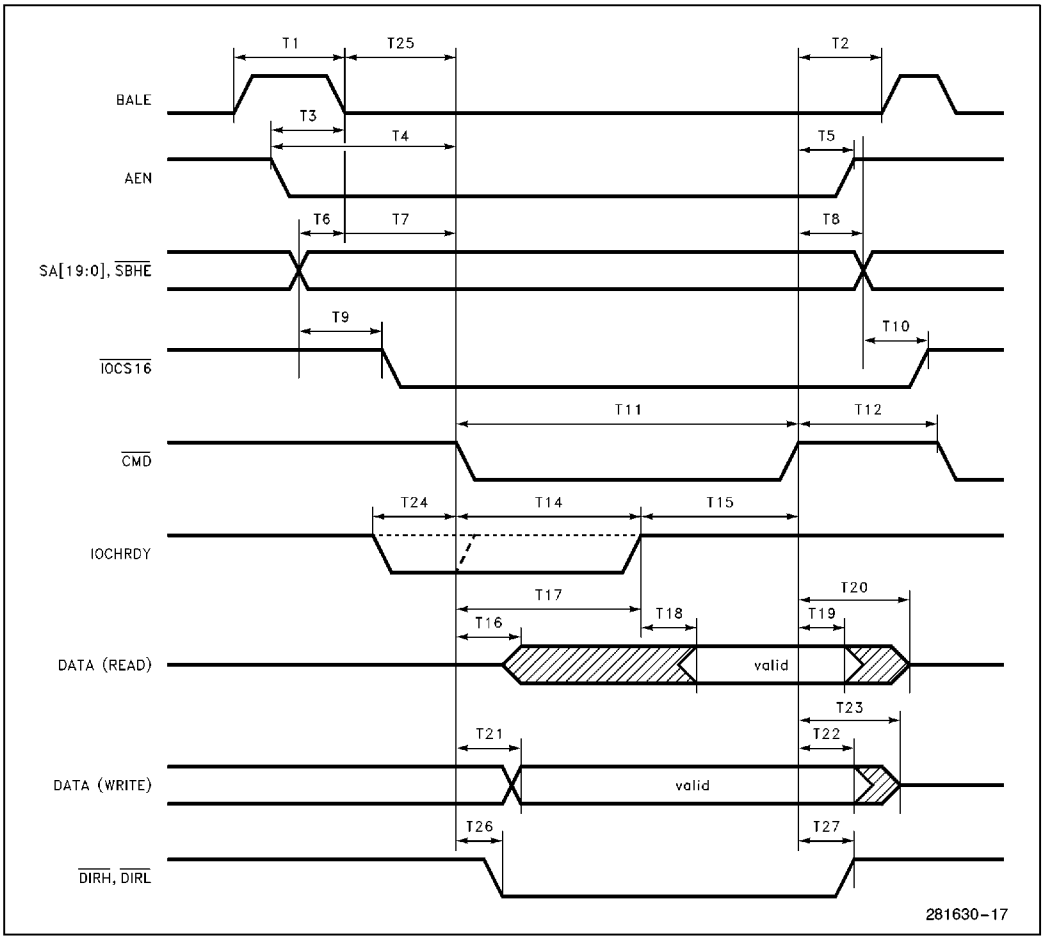


Figure 11-7. Early IOCHRDY Cycle

11.5 PCMCIA Interface Timing

Table 11-6. PCMCIA I/O Access

Parameter	Description	Min	Max	Units	Comments
T30a	ADDRESS Valid to CMD Active	70		ns	
T31a	CMD Inactive to ADDRESS Change	20		ns	
T32a	ADDRESS Valid to $\overline{IOIS16}$ Active/Inactive		35	ns	
T33a	ADDRESS Change to $\overline{IOIS16}$ Change		35	ns	
T34a	$\overline{REG}$ Active before CMD Active	5		ns	
T35a	$\overline{REG}$ Active after CMD Inactive	0		ns	
T36a	$\overline{CE}$ Active/Inactive before CMD Active	5		ns	
T37a	$\overline{CE}$ Active/Inactive after CMD Inactive	20		ns	
T38a	CMD Active to Inactive	165		ns	
T39a	$\overline{CMD}$ Active to $\overline{WAIT}$ Active/Inactive		35	ns	
T40a	$\overline{WAIT}$ Active Duration		12	μs	
T41a	$\overline{WAIT}$ Inactive to CMD Inactive	0		ns	
T42a	CMD Active to DATA READ Valid		90	ns	
T43a	$\overline{WAIT}$ Inactive to DATA READ Valid		25	ns	Applies to Extended Cycles Only
T44a	DATA READ Valid after CMD Inactive	0		ns	
T45a	DATA WRITE Valid to CMD Active	50		ns	
T46a	DATA WRITE Valid after CMD Inactive	30		ns	
T184a	Data Driven from READ CMD Active	0		ns	
T185a	READ CMD Inactive to Data Tri-State		30	ns	

Table 11-7. PCMCIA Memory Access

Parameter	Description	Min	Max	Units	Comments
T30b	ADDRESS Valid to CMD Active	30		ns	
T31b	CMD Inactive to ADDRESS Change	20		ns	
T34b	$\overline{\text{REG}}$ Inactive before CMD Active	30		ns	
T35b	$\overline{\text{REG}}$ Inactive after CMD Inactive	20		ns	
T36b	$\overline{\text{CE}}$ Active/Inactive before CMD Active	0		ns	
T37b	$\overline{\text{CE}}$ Active/Inactive after CMD Inactive	20		ns	
T38b	CMD Active to Inactive	100		ns	
T39b	$\overline{\text{CMD}}$ Active to $\overline{\text{WAIT}}$ Active/Inactive		35	ns	
T40b	$\overline{\text{WAIT}}$ Active Duration		12	μs	
T41b	$\overline{\text{WAIT}}$ Inactive to CMD Inactive	0		ns	
T43b	$\overline{\text{WAIT}}$ Inactive to DATA READ Valid		−10	ns	
T44b	DATA READ Valid after CMD Inactive	0		ns	
T45b	CMD Active to DATA WRITE Valid	125		ns	
T46b	DATA WRITE Valid after CMD Inactive	25		ns	
T184b	Data Driven from READ CMD Active	5		ns	
T185b	READ CMD Inactive to Data Tri-State		100	ns	

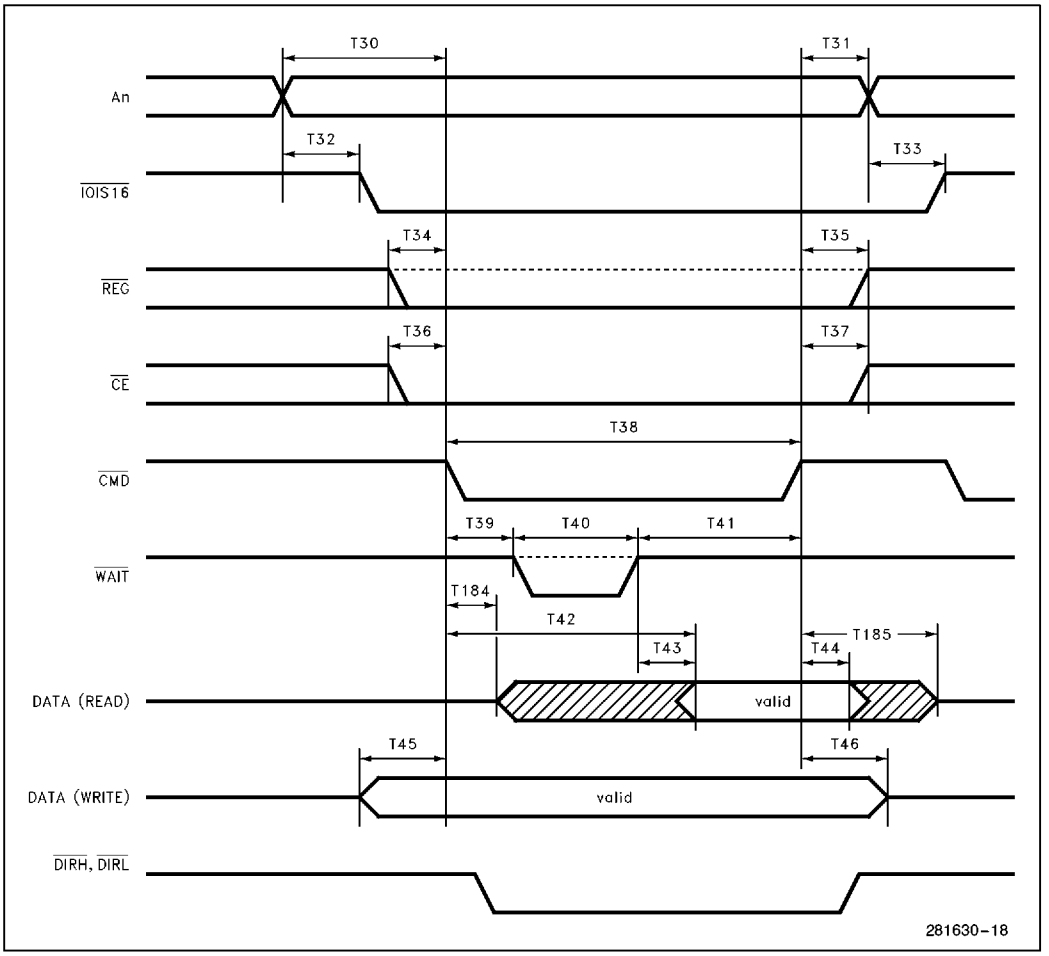


Figure 11-8. PCMCIA Cycle

11.6 Local Memory Timings

11.6.1 DRAM TIMINGS

The 82595TX supports up to 80 ns DRAM producing:

Word transfer every 400 ns.

Byte transfer every 250 ns.

Refresh cycle—200 ns.

The 82595TX supports 64K x 4 or 256K x 4 DRAM in fast page mode only. Write cycles are produced in *EARLY WRITE* mode. This eliminates using the DRAM $\overline{OE}$ signal (it must be connected to GND).

Table 11-8. DRAM—A.C. Characteristics

Symbol	Parameter	Timing		Units	Notes
		Min	Max		
T49	Access Time from $\overline{RAS}$		80	ns	
T50	Access Time from $\overline{CAS}$		30	ns	
T51	Access Time from Column Address		40	ns	
T52	$\overline{CAS}$ to Output Low Z	0		ns	
T53	Output Buffer Turn-Off Delay Time	0	40	ns	
T54	$\overline{RAS}$ Precharge Time	75		ns	
T55	$\overline{RAS}$ Pulse Width	80		ns	
T56	$\overline{RAS}$ Hold Time	30		ns	
T57	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	20		ns	
T58	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	30		ns	
T59	$\overline{CAS}$ Pulse Width	35		ns	
T60	$\overline{CAS}$ Hold Time	80		ns	
T61	Row Address Set-Up Time	0		ns	
T62	Row Address Hold Time	15		ns	
T63	Column Address Set-Up Time	0		ns	
T64	Column Address Hold Time	20		ns	
T65	Column Address Time Referenced to $\overline{RAS}$	65		ns	
T66	$\overline{RAS}$ to Column Address Delay Time	20		ns	
T67	Column Address to $\overline{RAS}$ Lead Time	40		ns	
T68	Write Command Set-Up Time	0		ns	
T69	Write Command Hold Time	15		ns	
T70	Write Command to $\overline{CAS}$ Lead Time	30		ns	
T71	D_{IN} Set-Up Time	0		ns	
T72	D_{IN} Hold Time	15		ns	
T73	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	10		ns	
T74	$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	25		ns	
T75	Fast Page Mode Cycle Time	55		ns	
T76	Fast Page Mode $\overline{CAS}$ Precharge Time	15		ns	
T77	Random Read or Write Cycle Time	190		ns	
T78	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time	100		ns	

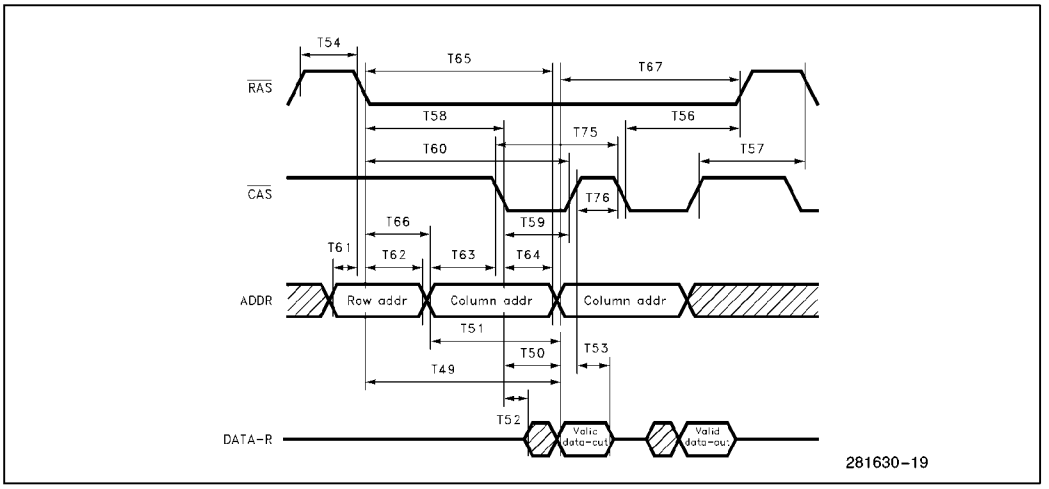


Figure 11-9. DRAM Timing Diagram: Fast Page Mode—Read Cycle

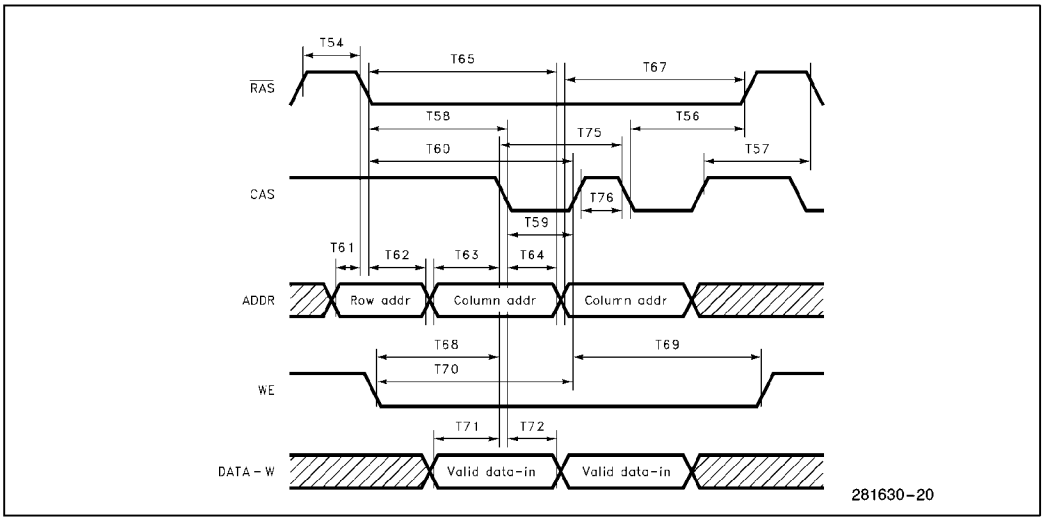


Figure 11-10. DRAM Timing Diagrams: Fast Page Mode—Write Cycle

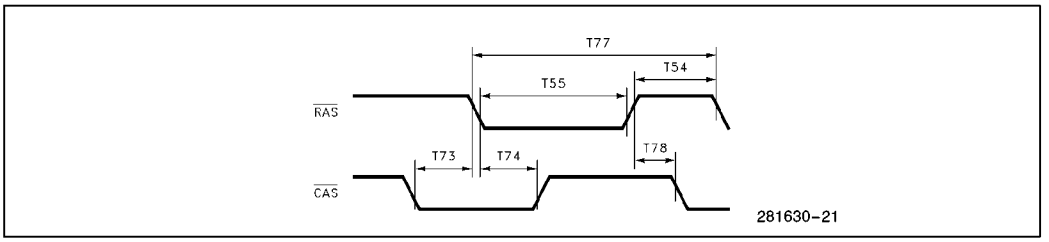


Figure 11-11. DRAM Timing Diagrams: $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle

11.6.2 FLASH/EPROM TIMINGS

- The 82595TX is designed to support a FLASH or EPROM up to 200 ns access time.
- The V_{PP} signal in FLASH implementation is connected always to 12V. Thus writing to the FLASH is controlled only by the $\overline{WE}$ signal.

Table 11-9. FLASH—A.C. Characteristics

Symbol	Parameter	Min	Max	Units	Notes
T79	Address Access Time		200	ns	
T80	Chip Enable Access Time		200	ns	
T81	Output Enable Access Time		100	ns	
T82	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$	0		ns	
T84	Address Set-Up Time	0			
T85	Address Hold Time	100		ns	
T86	Chip Enable Set-Up Time before Write	15		ns	
T87	Chip Enable Hold Time	0		ns	
T88	Data Set-Up Time	60		ns	
T89	Data Hold Time	15		ns	

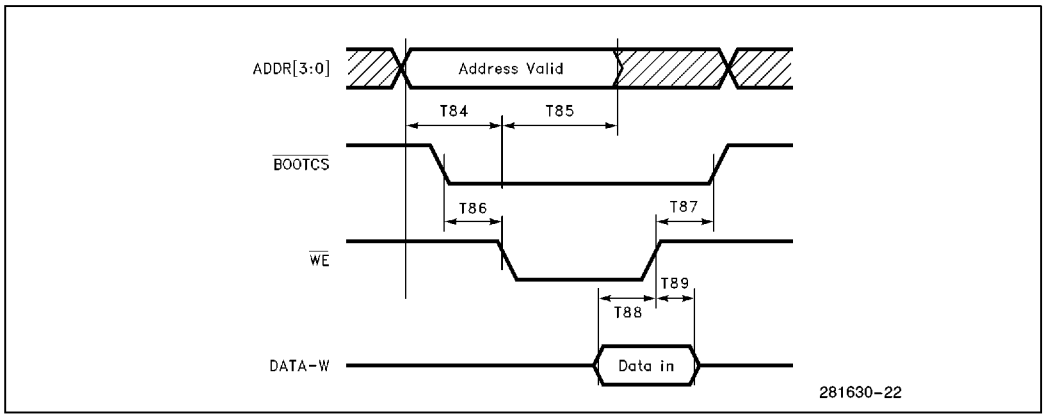


Figure 11-12. FLASH Timings—Write Cycle

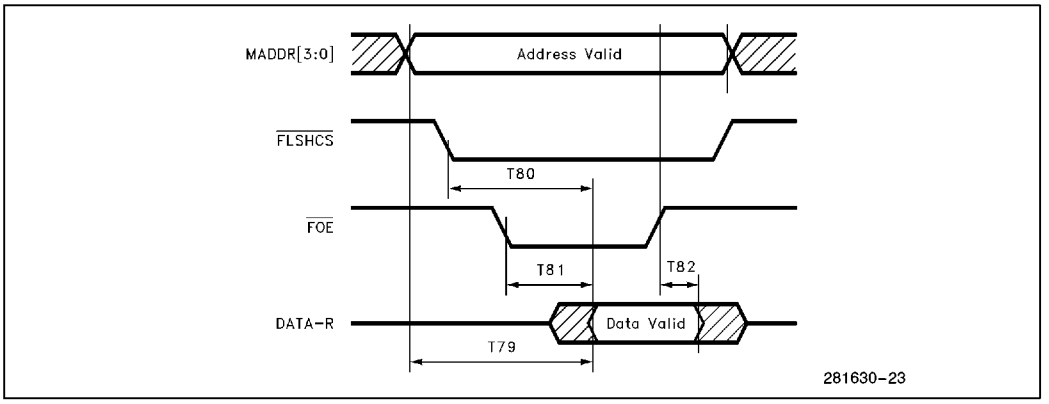


Figure 11-13. Flash Timings—Read Cycle

Table 11-10. EEPROM Timings

Symbol	Description	Min	Max	Units	Comments
T193	CS Setup Time	1.0		µs	
T194	SK High Time	3.0		µs	
T195	SK Low Time	3.0		µs	
T196	CS Hold Time	0		µs	
T197	CS Low Time	1.0		µs	
T198	DI Setup Time	0.4		µs	
T199	DI Hold Time	0.4		µs	
T200	Data Out Valid Time		0.4	µs	EEProm Restriction
T201	CS Inactive to DO Floated		0.4	µs	EEProm Restriction

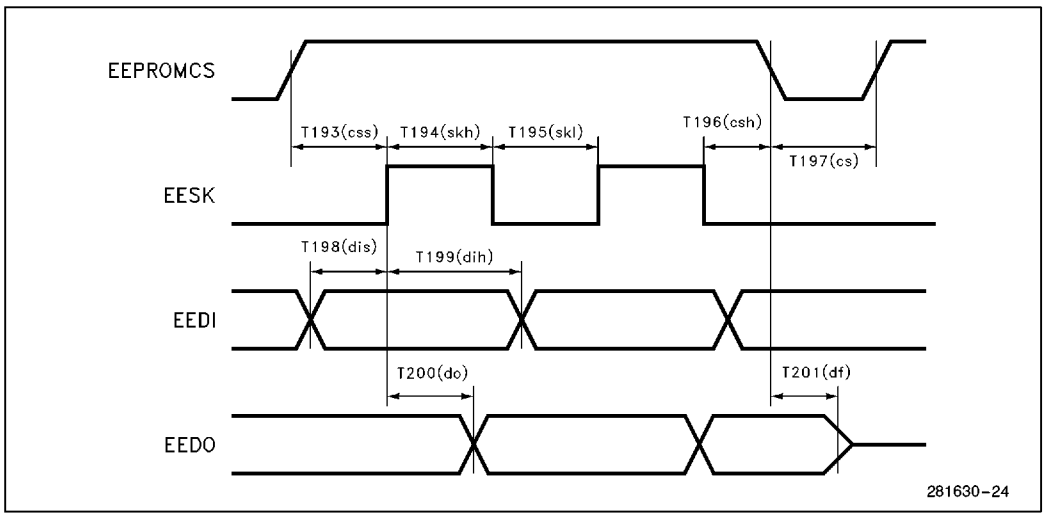


Figure 11-14. EEPROM Timings

11.6.3 IA PROM TIMINGS

*The PROM used is a TTL 32 x 8 bit.

Table 11-11. IA PROM A.C. Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
T174	Address Access Time		60	ns	
T175	Chip Enable Access Time		40	ns	

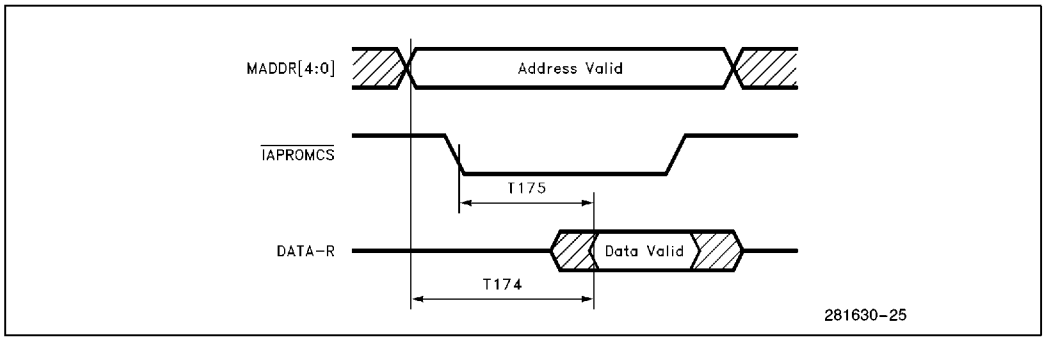
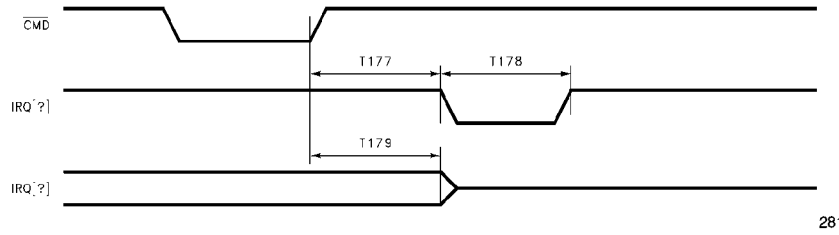


Figure 11-15. IA PROM Timings

11.7 Interrupt Timing

Table 11-12. Interrupt Timing

Parameter	Description	Min	Max	Units	Notes
T177	Interrupt Ack $\overline{CMD}$ Inactive to IRQ[4:0] Inactive		500	ns	
T178	IRQ[4:0] Inactive to IRQ[4:0] Active	100		ns	
T179	Tri-state $\overline{CMD}$ Inactive to IRQ[4:0] Tri-State		500	ns	



NOTE:
For ISA bus, IRQ is Active high.
For PCMCIA bus, IRQ is Active low.

Figure 11-16. Interrupt Timing

11.8 RESET and $\overline{SMOUT}$ Timing

General Comments

- Both signals are asynchronous signals and have minimum pulse duration specification only.
- $\overline{SMOUT}$ during Hardware power down activation.

Table 11-13. RESET and $\overline{SMOUT}$ Timing

Parameter	Description	Min	Max	Units	Notes
T180	RESET Minimum Duration	32		ms	1
T181	$\overline{SMOUT}$ Minimum Duration	100		ns	2
T182	$\overline{SMOUT}$ Activation by Power Down Command	150		ns	3
T183	$\overline{SMOUT}$ Deactivation	25		ns	3

NOTES:
1. Noise spikes of maximum TBD ns are allowed on Reset.
2. $\overline{SMOUT}$ is input.
3. $\overline{SMOUT}$ is output after configuration.

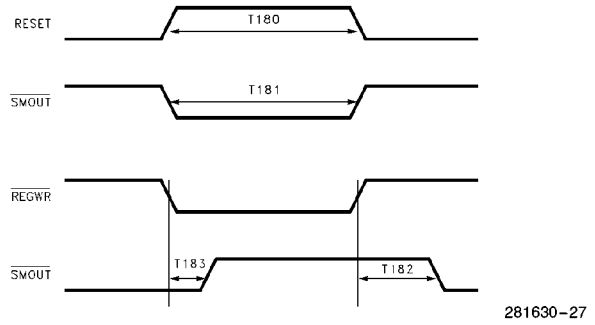


Figure 11-17. $\overline{SMOUT}$ Timing

11.9 JTAG Timing

Table 11-14. 82595TX JTAG Timing

Symbol	Parameter	Min	Max	Unit	Notes
T184	TMS Set-Up Time	15		ns	
T185	TMS Hold Time	10		ns	
T186	TDI Set-Up Time	15		ns	
T187	TDI Hold Time	10		ns	
T188	Input Signals Set-Up Time	15		ns	
T189	Input Signals Hold Time	10		ns	
T190	Outputs Valid Delay		150	ns	
T191	TDO Valid Delay		40	ns	
T192	TCK Cycle Time (Period)	100		ns	50% Duty Cycle

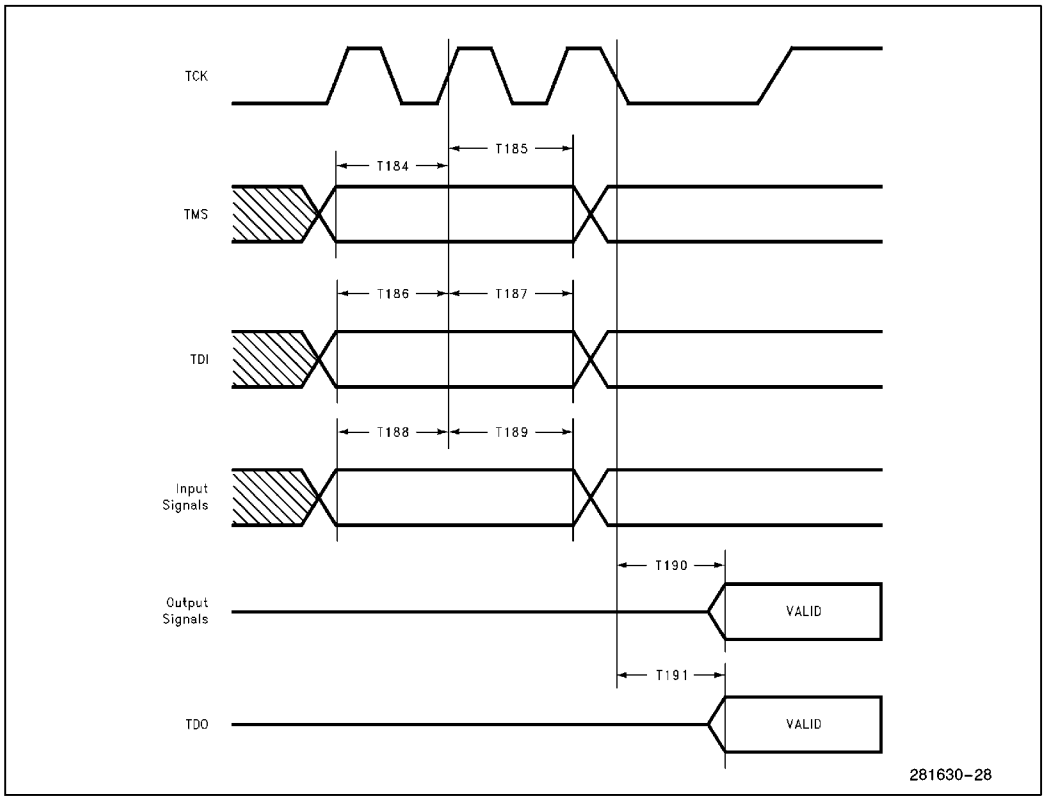
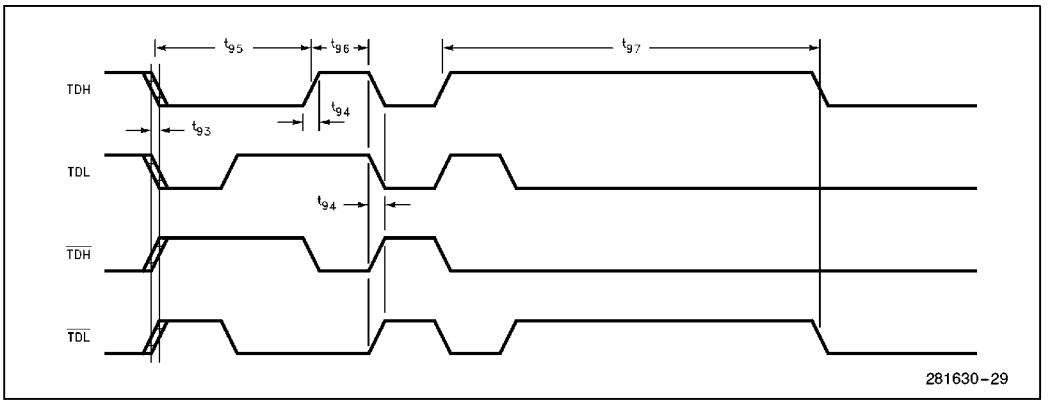


Figure 11-18. 82595TX JTAG Timing

11.10 Serial Timings

Table 11-15. TPE Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{90}	Number of TxD Bit Loss at Start of Packet			2	bits
t_{91}	Internal Steady State Propagation Delay			400	ns
t_{92}	Internal Start UP Delay			600	ns
t_{93}	TDH and TDL Pairs Edge Skew (@ $V_{CC}/2$)		1.5	3	ns
t_{94}	TDH and TDL Pairs Rise/Fall Times (@ 0.5V to V_{CC} − 0.5V)		2	5	ns
t_{95}	TDH and TDL Pairs Bit Cell Center to Center	99	100	101	ns
t_{96}	TDH and TDL Pairs Bit Cell Center to Boundary	49	50	51	ns
t_{97}	TDH and TDL Pairs Return to Zero from Last TDH	250		400	ns
t_{98}	Link Test Pulse Width	98	100	100	ns
t_{99}	Last TD Activity to Link Test Pulse	8	13	24	ms
t_{100}	Link Test Pulse to Data Separation	190	200		ns



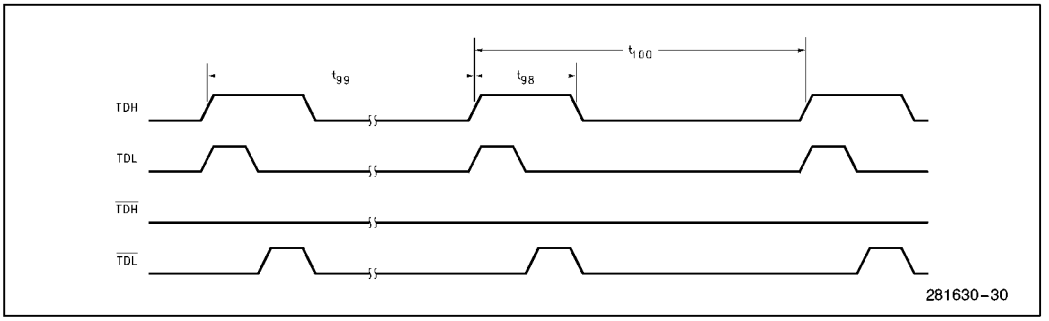


Figure 11-19. TPE Transmit Timings (Link Test Pulse)

Table 11-16. TPE Receive Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{105}	RD to RxD Bit Loss at Start of Packet	4		19	bits
t_{106}	RD Invalid Bits Allowed at Start of Packet			1	bits
t_{107}	RD to Internal Steady State Propagation Delay			400	ns
t_{108}	RD to Internal Start Up Delay			2.4	μs
t_{109}	RD Pair Bit Cell Center Jitter			±13.5	ns
t_{110}	RD Pair Bit Cell Boundry Jitter			±13.5	ns
t_{111}	RD Pair Held High from Last Valid Position Transition	230		400	ns

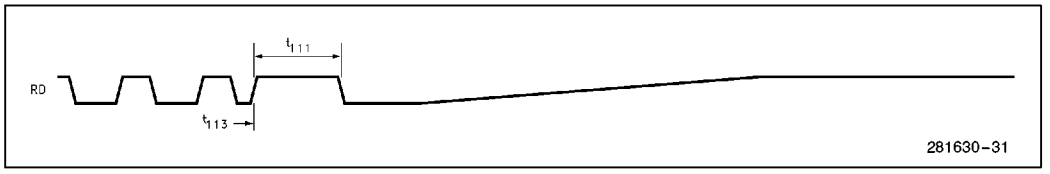


Figure 11-20. TPE Receive Timings (End of Frame)

Table 11-17. TPE Link Integrity Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{120}	Last RD Activity to Link Fault (Link Loss Timer)	50	100	150	ms
t_{121}	Minimum Received Linkbeat Separation(1)	2	5	7	ms
t_{122}	Maximum Received Linkbeat Separation(2)	25	50	150	ms

NOTES:
1. Linkbeats closer in time to this value are considered noise and rejected.
2. Linkbeats further apart in time than this value are not considered consecutive and are rejected.

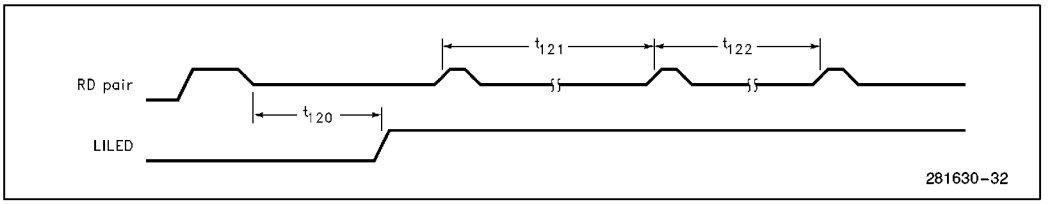


Figure 11-21. TPE Link Integrity Timings

Table 11-18. AUI Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{126}	TRMT Pair Rise/Fall Times		3	5	ns
t_{127}	Bit Cell Center to Bit Cell Center of TRMT Pair	99.5	50	100.5	ns
t_{128}	Bit Cell Center to Bit Cell Boundary of TRMT Pair	49.5	50	50.5	ns
t_{129}	TRMT Pair Held at Positive Differential at Start of Idle	200			ns
t_{130}	TRTM Pair Return to $\leq$ 40 mVp from Last Positive Transition			8.0	μs

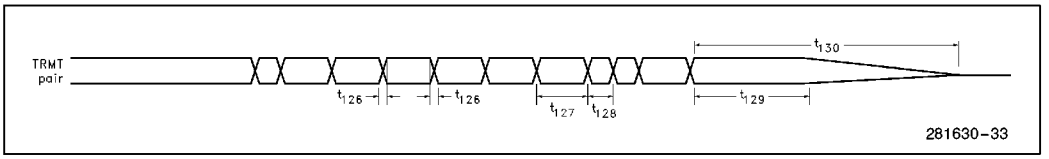


Figure 11-22. AUI Transmit Timings

Table 11-19. AUI Receive Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{135}	RCV Pair Rise/Fall Times			10	ns
t_{136}	RCV Pair Bit Cell Center Jitter in Preamble			$\pm$12	ns
t_{137}	RCV Pair Bit Cell Center/Boundary Jitter in Data			$\pm$18	ns
t_{138}	RCV Pair Idle Time after Transmission	8			μs
t_{139}	RCV Pair Return to Zero from Last Positive Transition	160			ns

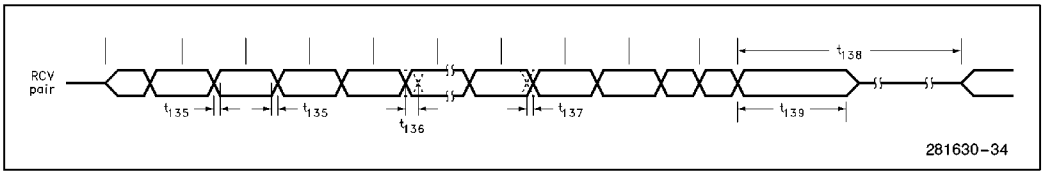


Figure 11-23. AUI Receive Timings

Table 11-20. AUI Collision Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{145}	CLSN Pair Cycle Time	80		118	ns
t_{146}	CLSN Pair Rise/Fall Times			10	ns
t_{147}	CLSN Pair Return to Zero from Last Positive Transition	160			ns
t_{148}	CLSN Pair High/Low Times	35		70	ns

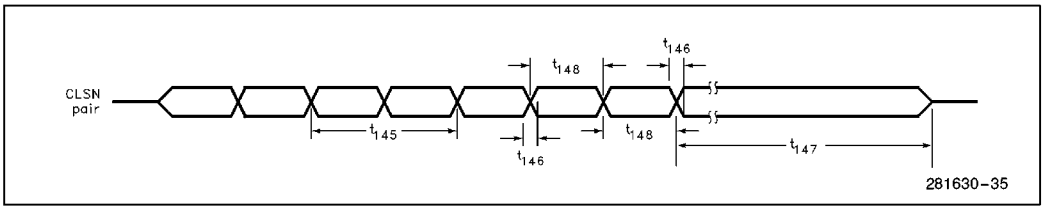


Figure 11-24. AUI Collision Timings

Table 11-21. AUI Noise Filter Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{152}	RCV Pair Noise Filter Pulse Width Accept (@ −285 mV)	25			ns
t_{153}	CLSN Pair Noise Filter Pulse Width Accept (@ −285 mV)	25			ns

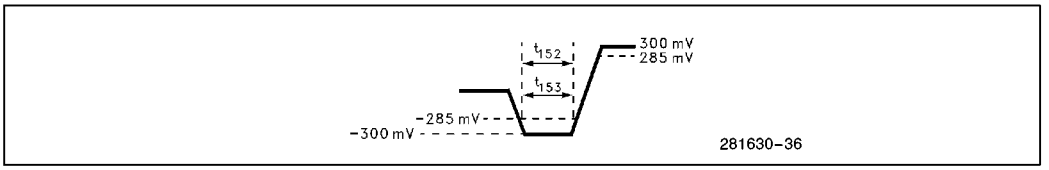


Figure 11-25. AUI Noise Filter Timings

Table 11-22. Jabber Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{165}	Maximum Length Transmission before Jabber Fault (TPE)	20	25	150	ms
t_{166}	Maximum Length Transmission before Jabber Fault (AUI)	10	13	18	ms
t_{167}	Minimum Idle Time to Clear Jabber Function	250	275	750	ms

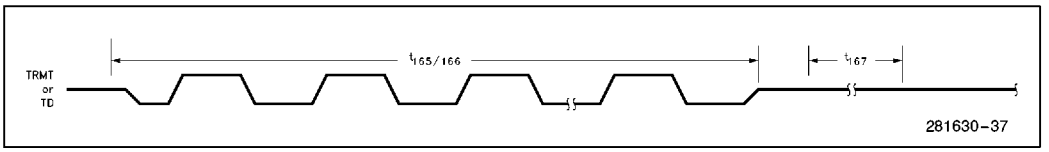


Figure 11-26. Jabber Timings

Table 11-23. LED Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{170}	ACTLED On Time	50		450	ms
t_{171}	ACTLED Off Time	50			ms
t_{172}	LILED On Time	50			ms
t_{173}	LILED Off Time	100			ms

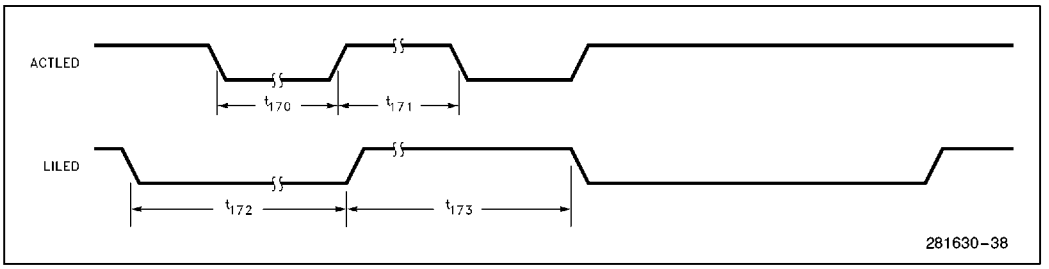
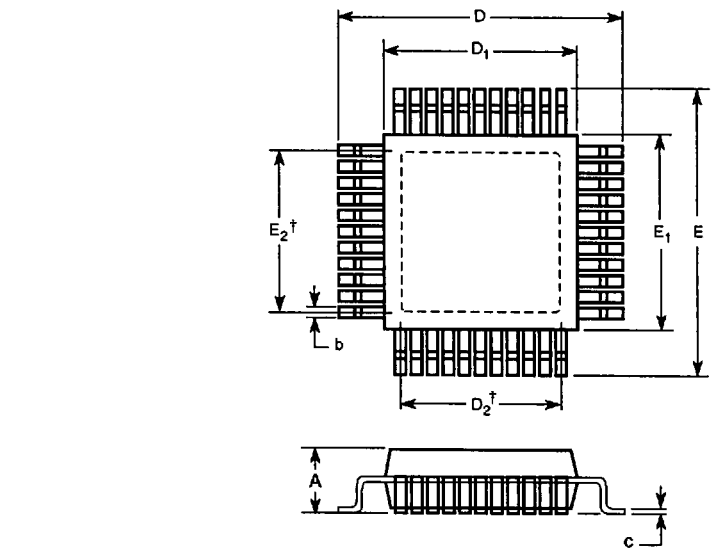


Figure 11-27. LED Timings

Additional 82595TX Documentation

This datasheet provides complete pinout and pin definitions, and electrical specifications and timings. It also includes an overview of the various subsections listed in Figure 1. For more complete information on the 82595TX, please ask your local sales representative for the 82595TX User Manual and LAN595TX Specification. The 82595TX User Manual contains detailed information on the 82595TX feature set, including register descriptions and implementation steps for various 82595TX functions (initialization, transmission, reception). The LAN595TX Specification describes various hardware/software implementations and configuration techniques. Hardware compatible with this interface can work with software developed by Intel and other NOS vendors which conform to this specification.

2.11.1.1 Principal Dimensions and Data for QFP (Square)/TQFP/SQFP Packages



NOTES:
All dimensions in millimeters
†Optional exposed heatslug

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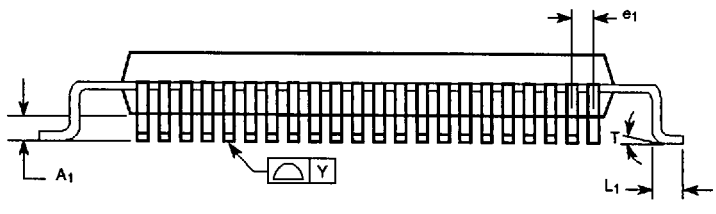
2.11.1.2 Terminal Details



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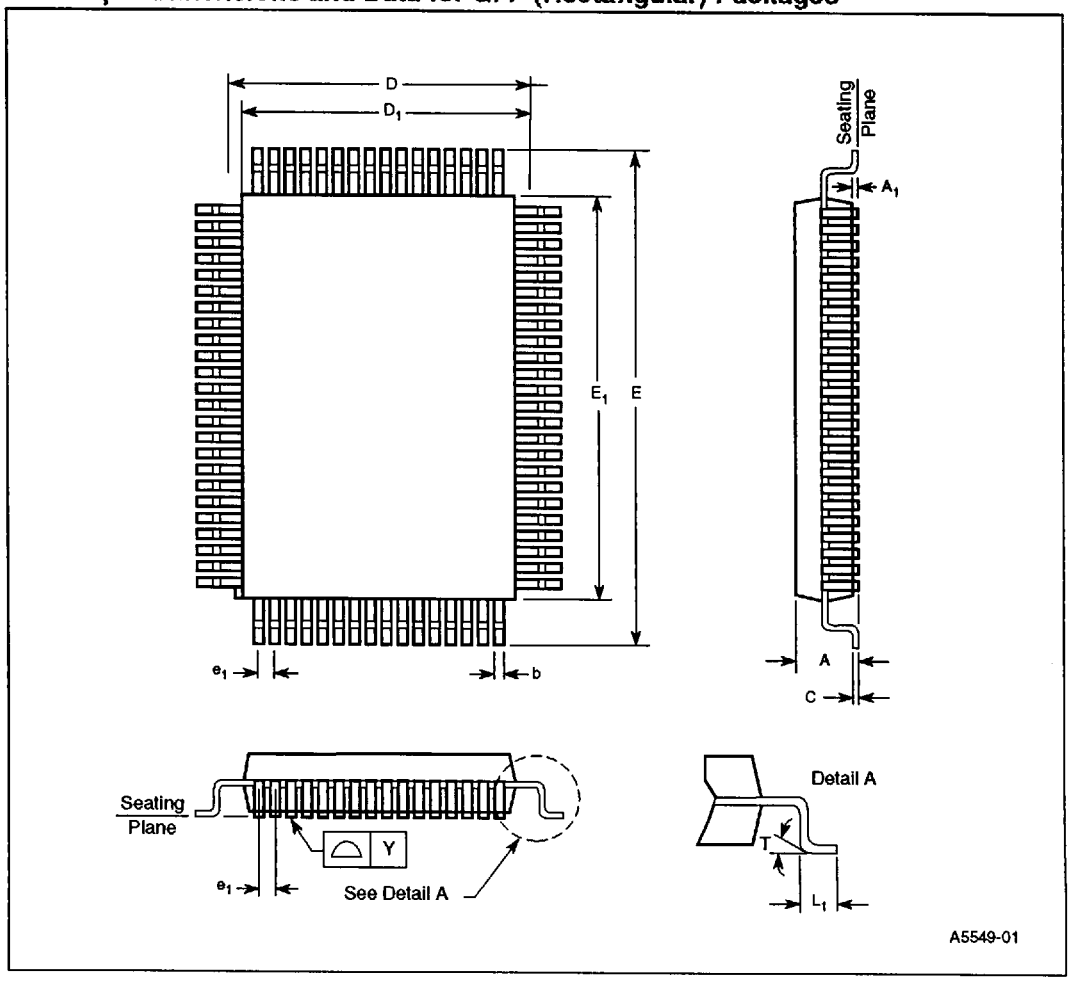
Quad Flatpack (Square Packages)							
Symbol	**Description**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
N	Lead Count		44			48	
A	Overall Height			2.35			2.55
A_1	Stand Off	0.05			0.05		0.25
b	Lead Width	0.20	0.30	.040	0.25	0.30	0.40
c	Lead Thickness	0.10	0.15	0.20	0.11	0.15	0.20
D	Terminal Dimension	12.0	12.4	12.8	15.1	15.3	15.5
D_1	Package Body		10.0		11.9	12.0	12.1
E	Terminal Dimension	12.0	12.4	12.8	15.1	15.3	15.5
E_1	Package Body		10.0		11.9	12.0	12.1
e_1	Lead Pitch	0.65	0.80	0.95	0.70	0.80	0.90
L_1	Foot Length	0.38	0.58	0.78	0.65	0.85	1.05
T	Lead Angle	0.0°		10.0°	0.0°		7.0°
Y	Coplanarity			0.10			0.10

Quad Flatpack (Square Packages) (Continued)								
Symbol	**Description**	**Min**	**Nom**	**Max**	**Min**	**Max**	**Min**	**Max**
N	Lead Count		64		128		160	
A	Overall Height			2.55	3.23	3.75		4.00
A_1	Stand Off	0.05			0.05	0.30	0.05	0.30
b	Lead Width	0.20	0.30	0.40	0.25	0.45	0.20	0.45
c	Lead Thickness	0.10	0.15	0.20	0.150	0.188	0.150	0.188
D	Terminal Dimension	14.9	15.3	15.7	31.6	32.4	30.2	31.0
D_1	Package Body		12.0		27.9	28.1	27.9	28.1
E	Terminal Dimension	14.9	15.3	15.7	31.6	32.4	30.2	31.0
E_1	Package Body		12.0		27.9	28.1	27.9	28.1
e_1	Lead Pitch	0.53	0.65	0.77	0.70	0.90	0.55	0.75
L_1	Foot Length	0.65	0.85	1.05	0.60	1.0	0.60	1.0
T	Lead Angle	0.0°		10.0°	0°	10°	0°	10°
Y	Coplanarity			0.10	0.1		0.1	

Shrink Quad Flatpack												
Symbol	**Description**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Max**
A	Overall Height			1.7			1.7			3.15		3.75
A_1	Stand Off	0.00			0.00			0.05		0.40	0.05	0.30
b	Lead Width	0.14	0.20	0.26	0.14	0.20	0.26	0.14	0.22	0.28	0.14	0.26
c	Lead Thickness	0.117	0.127	0.177	0.117	0.127	0.177	0.10	0.15	0.20	0.150	0.188
D	Terminal Dimension	13.70	14.00	14.30	15.70	16.00	16.30	17.5	17.9	18.3	30.2	31.0
D_1	Package Body		12.0			14.00			14.0		27.9	28.1
E	Terminal Dimension	13.70	14.00	14.30	15.70	16.00	16.30	23.5	23.9	24.3	30.2	31.0
E_1	Package Body		12.0			14.00			20.0		27.9	28.1
e_1	Lead Pitch	0.40	0.50	0.60	0.40	0.50	0.60	0.40	0.50	0.60	0.40	0.60
L_1	Foot Length	0.35	0.50	0.70	0.30	0.50	0.70	0.60	0.80	1.00	0.30	0.70
N	Lead Count	80			100			128			208	
T	Lead Angle	0.0°		10.0°	0.0°		10.0°	0.0°		10.0°	0.0°	10.0°
Y	Coplanarity			0.10			0.10			0.10	0.08	
D_2/E_2	Heatspreader										21	

Thin Quad Flatpack							
Symbol	**Description**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
A	Overall Height		1.7	1.3	1.7	1.3	1.7
A_1	Stand Off	0.05	0.20	0.05	0.20	0.50	
b	Lead Width	0.16	0.28	0.16	0.28	0.16	0.28
c	Lead Thickness	0.117	0.127	0.122	0.160	0.122	0.160
D	Terminal Dimension	15.70	16.30	21.6	22.4	25.6	26.4
D_1	Package Body	13.9	14.1	19.9	20.1	23.9	24.1
E	Terminal Dimension	15.7	16.30	21.6	22.4	25.6	26.4
E_1	Package Body	13.9	14.1	19.9	20.1	23.9	24.1
e_1	Lead Pitch	0.40	0.60	0.40	0.60	0.40	0.60
L_1	Foot Length	0.30	0.70	0.40	0.80	0.40	0.80
N	Lead Count	100		144		176	
T	Lead Angle	0.0°	10.0°	0.0°	10.0°	0.0°	1.0°
Y	Coplanarity	0.10		0.8		0.8	

Figure 2-1. Principle Dimensions and Data for QFP (Rectangular) Packages



Quad Flatpack (Rectangular Packages)							
Symbol	**Description**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
N	Lead Count		80			100	
A	Overall Height			3.15			3.15
A_1	Stand Off	0.05		0.40	0.05		0.40
B	Lead Width	0.25	0.35	0.45	0.20	0.30	0.40
C	Lead Thickness	0.10	0.15	0.20	0.10	0.15	0.20
D	Terminal Dimension	17.5	17.9	18.3	17.5	17.9	18.3
D_1	Package Body		14.0			14.0	
E	Terminal Dimension	23.5	23.9	24.3	23.5	23.9	24.3
E_1	Package Body		20.0			20.0	
e_1	Lead Pitch	0.65	0.80	0.95	0.53	0.65	0.77
L_1	Foot Length	0.60	0.80	1.00	0.60	0.80	1.00
T	Lead Angle	0.0°		10.0°	0.0°		10.0°
Y	Coplanarity			0.10			0.10