Ordering number : EN5055A

CMOS LSI

No. 5055A

LC382161T-17

2 MEG (65536 words × 16 bits × 2 banks) Synchronous DRAM

Overview

The LC382161T is a 3.3 V single-voltage power supply synchronous DRAMs with a 65536-word × 16-bit × 2-bank organization. This DRAM features a large capacity, high speed, and low power due to the provision of synchronization circuits and the use of CMOS peripheral circuits. Thus this is optimal for use in a wide range of applications, from main and graphic memory in computers to consumer products.

The LC382161T DRAM uses multiplexed address inputs and is packaged in a 50-pin TSOP package that supports high-density mounting. This DRAM uses auto-refresh (CBR refresh) performed 512 times every 8 ms as the refresh technique.

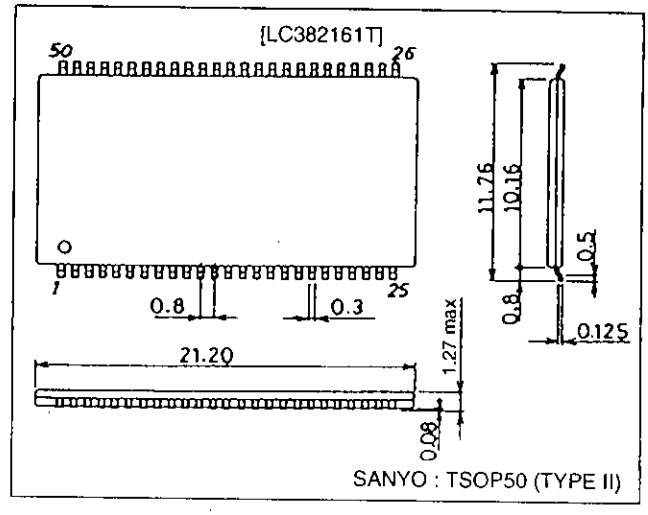
Features

- Organization: 65536 words × 16 bits × 2 banks
- All I/O signals (except CKE) are synchronized with the rising edge of the system clock.
- Basic specifications conform to the JEDEC standards for 16 Mbit synchronous DRAM.
- A pulse $\overline{RAS}$ scheme is used.
- Two bank internal structure (2 banks × 65536 words × 16 bits). Continuous operation across the two banks is supported via the A9 pin.
- Burst length setting (1, 2, 4, 8, or full page)
- Burst type setting (sequential or interleaved)
- Burst output operations are interruptible.
- The $\overline{CAS}$ latency can be set using an address key. ($\overline{CAS}$ latency: 1 or 2)
- Auto-refresh function
- Power-down and suspend operations can be controlled from the CKE pin.
- I/O byte order is controlled by the DQM pin.
- Fabrication in a CMOS process
- Single 3.3 V power supply
- LVTTL compatible
- Low power
  Standby: 7.2 mW
  Operating: 324 mW
- Package:
  TSOP 50-pin (400 mil) plastic package : LC382161T

Package Dimensions

unit: mm

3211-TSOP50



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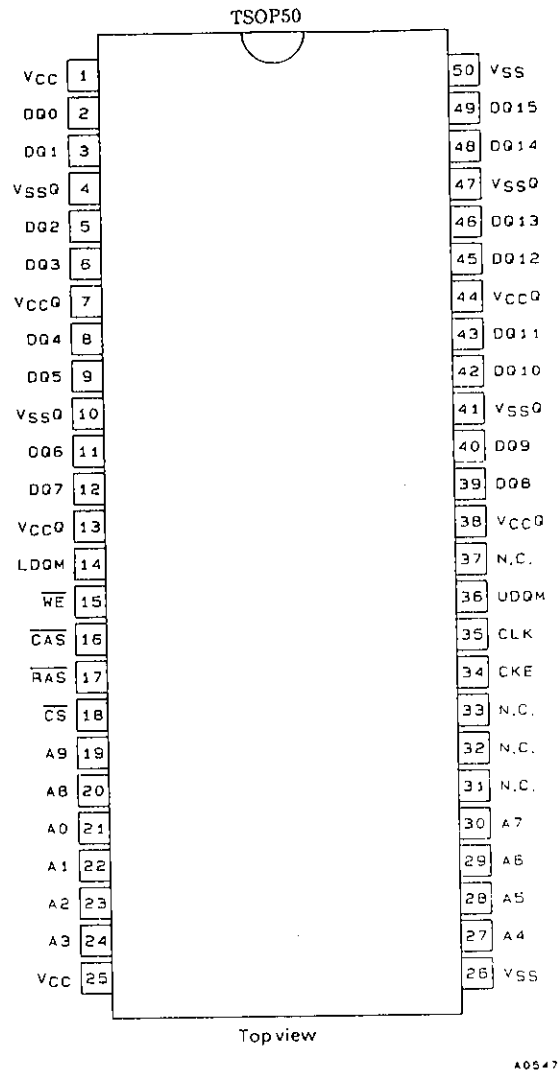
Pin Assignment



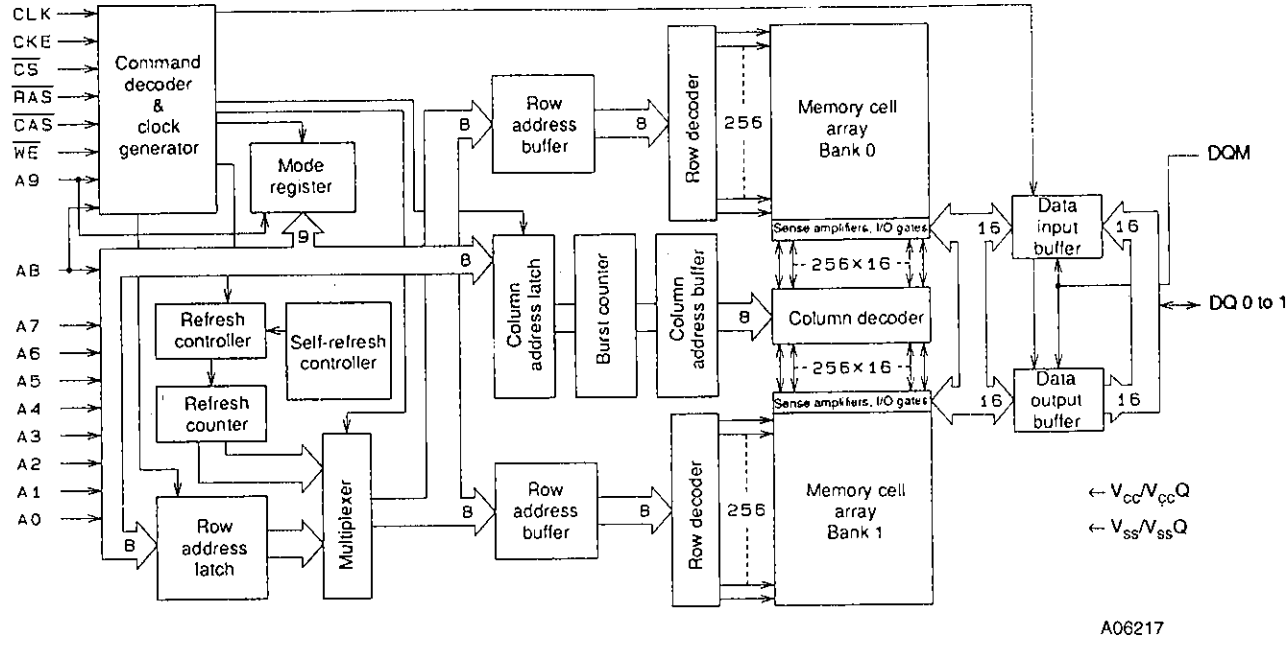
Pin Functions

Pin	Function	Pin	Function
A0 to A9	Address input	$\overline{CAS}$	Column address strobe command
A0 to A6, A9	Row address input	$\overline{WE}$	Write enable
A8	Row address, auto-precharge input	LDQM, UDQM	Data mask enable
A0 to A6, A7, A9	Column address input	V_{CC}	Power supply
DQ0 to DQ15	Data I/O	V_{SS}	Ground
CLK	System clock input	$V_{CC}Q$	Data output power supply
CKE	Clock enable	$V_{SS}Q$	Data output ground
$\overline{CS}$	Chip select	N.C.	No connection
$\overline{RAS}$	Row address strobe command		

Pin Functions

Pin No.	Symbol	Type	Function (in detail)
35	CLK	Input pin	CLK is the master clock input for this device. Except for CKE, all inputs to this device are acquired in synchronization with the rising edge of this pin.
34	CKE	Input pin	The CKE input determines whether the CLK input is enabled within the device. When CKE is high, the next rising edge on the CLK signal will be valid, and when low, invalid. When CKE is low, the device will be in either the power-down mode, the clock suspend mode, or the self refresh mode. The CKE signal must remain low for these modes to remain in effect. CKE is an asynchronous input.
18	$\overline{CS}$	Input pin	The $\overline{CS}$ input determines whether command input is enabled within the device. Command input is enabled when $\overline{CS}$ is low, and disabled when $\overline{CS}$ is high. The device remains in the previous state when $\overline{CS}$ is high.
17	$\overline{RAS}$	Input pin	$\overline{RAS}$, in conjunction with $\overline{CAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" item for details on device commands.
16	$\overline{CAS}$	Input pin	$\overline{CAS}$, in conjunction with $\overline{RAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" item for details on device commands.
15	$\overline{WE}$	Input pin	$\overline{WE}$, in conjunction with $\overline{RAS}$ and $\overline{CAS}$, forms the device command. See the "Command Truth Table" item for details on device commands.
14, 36	LDQM, UDQM	Input pin	LDQM and UDQM control the lower and upper bytes of the I/O buffers. In read mode, LDQM and UDQM control the output buffer. When LDQM or UDQM is low, the corresponding buffer byte is enabled, and when high, disabled. The outputs go to the high impedance state when LDQM/UDQM is high. This function corresponds to $\overline{OE}$ in general-purpose DRAMs. In write mode, LDQM and UDQM control the input buffer. When LDQM or UDQM is low, the corresponding buffer byte is enabled, and data can be written to the device. When LDQM or UDQM is high, input data is masked and cannot be written to the device.
19	A9	Input pin	A9 is the bank selection signal. When A9 is low, bank 0 is selected and when high, bank 1 is selected. This signal becomes part of the OP code during mode register set command input.
20	A8	Input pin	A8 is used as a row address during active command input, and is used to determine the precharge mode during other commands. If A8 is low during precharge command input the bank selected by A9 is precharged, but if A8 is high, both banks will be precharged. This signal becomes part of the OP code during mode register set command input.
30	A7	Input pin	A7 is a column address input. This signal becomes part of the OP code during mode register set command input.
21 to 24, 27 to 29	A0 to A6	Input pin	A0 to A6 are address inputs. They are used as row address inputs during active command input and as column address inputs during read or write command input. These signals become part of the OP code during mode register set command input.
2, 3, 5, 6, 8, 9, 11, 12, 39, 40, 42, 43, 45, 46, 48, 49	DQ0 to DQ15	I/O pin	DQ0 to DQ15 are I/O pins. I/O through these pins can be controlled in byte units using the LDQM and UDQM pins.
7, 13, 38, 44	$V_{CC}Q$	Power supply pin	$V_{CC}Q$ is the output buffer power supply.
4, 10, 41, 47	$V_{SS}Q$	Power supply pin	$V_{SS}Q$ is the output buffer ground.
1, 25	V_{CC}	Power supply pin	V_{CC} is the device internal power supply.
26, 50	V_{SS}	Power supply pin	V_{SS} is the device internal ground.

Block Diagram



Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit	Note
Maximum supply voltage	V_{CC} max		−1.0 to +4.6	V	1
Maximum output supply voltage	$V_{CC}Q$ max		−1.0 to +4.6	V	1
Input voltage	V_{IN}		−1.0 to +5.5	V	1
Output voltage	V_{OUT}		−1.0 to +4.6	V	1
Allowable power dissipation	Pd max		1	W	1
Output shorted current	I_{OS}		50	mA	1
Operating temperature	Topr		0 to +70	°C	1
Storage temperature	Tstg		−55 to +150	°C	1

Note: 1. This device may be destroyed if stresses in excess of the absolute maximum ratings are applied.

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	Conditions	min	typ	max	Unit	Note
Supply voltage	V_{CC}, $V_{CC}Q$		3.0	3.3	3.6	V	2
Input high level voltage	V_{IH}		2.0		5.5	V	2
Input low level voltage	V_{IL}		−0.3		+0.8	V	2

Note: 2. All voltages are referenced to V_{SS}.

DC Electrical Characteristics at Ta = 0 to +70°C, $V_{CC} = V_{CC}Q = 3.3 \pm 0.3$ V

Parameter	Symbol	Conditions		min	max	Unit	Note
Operating current (average current during operation)	$I_{CC\,1}$	Burst length = 1, $t_{RAS} \geq t_{RAS}$ (min), $t_{RP} \geq t_{RP}$ (min), I_{OUT} = 0 mA			85	mA	3, 4
Precharge standby current (in power-down mode)	$I_{CC\,2P}$	CKE ≤ V_{IL} (max)	t_{CK} = 34 ns		3	mA	
	$I_{CC\,2PS}$		t_{CK} = ∞		2	mA	
Precharge standby current (in non power-down mode)	$I_{CC\,2N}$	CKE ≥ V_{IH} (min)	t_{CK} = 34 ns		16	mA	
	$I_{CC\,2NS}$		t_{CK} = ∞		10	mA	
Active standby current (in power-down mode)	$I_{CC\,3P}$	CKE ≥ V_{IL} (max)	t_{CK} = 34 ns		3	mA	
	$I_{CC\,3PS}$		t_{CK} = ∞		2	mA	
Active standby current (in non power-down mode)	$I_{CC\,3N}$	CKE ≥ V_{IH} (min)	t_{CK} = 34 ns		16	mA	
	$I_{CC\,3NS}$		t_{CK} = ∞		10	mA	
Operating current (in burst mode)	$I_{CC\,4}$	$t_{CK} \geq t_{CK}$ (min), I_O = 0 mA	$\overline{CAS}$ latency = 2		90	mA	3, 4
			$\overline{CAS}$ latency = 1		90		
Refresh current	$I_{CC\,5}$	$t_{RC} \geq t_{RC}$ (min)			80	mA	
Input leakage current	I_{IL}	0 V ≤ V_{IN} ≤ V_{CC}, with pins other than the tested pin at 0 V		−10	+10	µA	
Output leakage current	I_{OL}	output disabled, 0 V ≤ V_{OUT} ≤ V_{CC}		−10	+10	µA	
Output high level voltage	V_{OH}	I_{OUT} = −2 mA		2.4		V	
Output low level voltage	V_{OL}	I_{OUT} = 2 mA			0.4	V	

Note: 3. These are the values at the minimum cycle time. Since the currents are transient, these values decrease as the cycle time increases. Also note that a bypass capacitor of at least 0.01 µF should be inserted between V_{CC} and V_{SS} for each memory chip to suppress power supply voltage noise (voltage drops) due to these transient currents.

4. ICC1 and ICC4 depend on the output load. The maximum values for ICC1 and ICC4 occur in the output open state.

Input/Output Capacitance at Ta = 25°C, V_{CC} = $V_{CC}Q$ = 3.3 ± 0.3 V, f = 1 MHz

Parameter	Symbol	max	Unit
Input capacitance (A0 to A9)	C_{IN1}	5	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, LDQM, UDQM)	C_{IN2}	5	pF
I/O capacitance (DQ0 to DQ15)	$C_{I/O}$	7	pF

AC Electrical Characteristics at Ta = 0 to +65°C, V_{CC} = $V_{CC}Q$ = 3.135 V to 3.6 V (Notes 5, 6, 7)

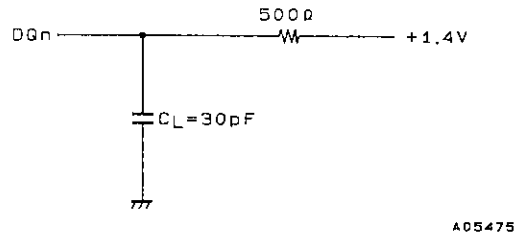
Parameter		Symbol	min	max	Unit	Note
Clock cycle time	$\overline{CAS}$ latency = 2	t_{CK2}	34		ns	
	$\overline{CAS}$ latency = 1	t_{CK1}	34		ns	
Access time referenced to CLK	$\overline{CAS}$ latency = 2	t_{AC2}		17	ns	8
	$\overline{CAS}$ latency = 1	t_{AC1}		30	ns	8
CLK high level width		t_{CHI}	7		ns	
CLK low level width		t_{CL}	7		ns	
Output data hold time	$\overline{CAS}$ latency = 2	t_{OH2}	4		ns	
	$\overline{CAS}$ latency = 1	t_{OH1}	10		ns	
Output low impedance time		t_{LZ}	0		ns	
Output high impedance time		t_{HZ}	10	17	ns	9
Input data setup time		t_{DS}	4		ns	
Input data hold time		t_{DH}	2		ns	
Address setup time		t_{AS}	4		ns	
Address hold time		t_{AH}	2		ns	
CKE setup time		t_{CKS}	4		ns	
CKE hold time		t_{CKH}	2		ns	
CKE-CLK recovery delay time		t_{CKA}	1 CLK + 4		ns	
Command setup time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)		t_{CS}	4		ns	
Command hold time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)		t_{CH}	2		ns	
Command cycle time (Ref to Ref/Act to Act)		t_{RC}	136		ns	
Command cycle time (Act to Pre)		t_{RAS}	102	12000	ns	
Command cycle time (Pre to Act)		t_{RP}	34		ns	
Active command to R/W command delay time		t_{RCD}	34		ns	
Command cycle time (Act 0 to Act1)		t_{RRD}	34		ns	
Input data precharge command delay time	$\overline{CAS}$ latency = 2	t_{DPL2}	34		ns	
	$\overline{CAS}$ latency = 1	t_{DPL1}	34		ns	
Input data active (refresh) command delay time (during auto-precharge)	$\overline{CAS}$ latency = 2	t_{DAL2}	1 CLK + 34		ns	
	$\overline{CAS}$ latency = 1	t_{DAL1}	1 CLK + 34		ns	
Transition time		t_T	1	30	ns	
Refresh cycle time		t_{REF}		8	ms	

Note: 5. When power is first applied, memory operation should be started 100 µs after V_{CC} and $V_{CC}Q$ reach their stipulated voltages. Also note that the power on sequence and an auto-refresh operation must be executed before starting memory operation.
6. Measured with t_T = 1 ns.
7. The reference level is 1.4 V when measuring input signal timing. Rise and fall times are measured between V_{IH} and V_{IL}.
8. Measured with the load shown in the figure below.
9. The time t_{HZ} (max) is defined as the time required for the output voltage to transition by ±200 mV from V_{OH} (min) or V_{OL} (max) when the output is in the high impedance state.

Operating Frequency/Latency Relationships

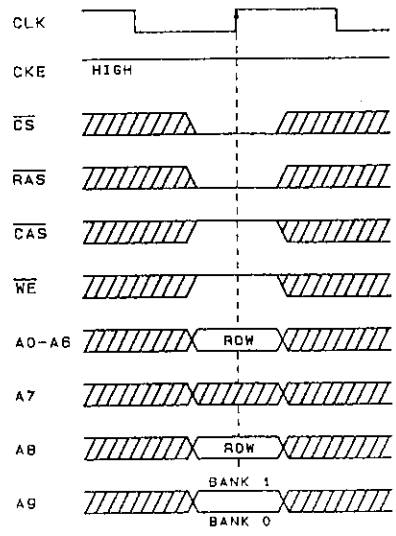
Parameter	Symbol	-17		Unit
Clock cycle time	t_{CK}	34	34	ns
Operating frequency	-	29	29	MHz
$\overline{CAS}$ latency	t_{CAC}	2	1	cycle
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	1	1	cycle
$\overline{RAS}$ latency	t_{RAC}	3	2	cycle
Command cycle time	t_{RC}	4	4	cycle
$\overline{RAS}$ cycle time	t_{RAS}	3	3	cycle
Precharge cycle time	t_{RP}	1	1	cycle
Command cycle time (Act to Act)	t_{RRD}	2	1	cycle
Column command cycle time (READ, READA, WRIT, WRITA)	t_{CCD}	1	1	cycle
Input data precharge command delay time	t_{DPL}	1	1	cycle
Input data active (refresh) command delay time	t_{DAL}	2	2	cycle
Burst stop delay time (read)	t_{RBD}	2	1	cycle
Burst stop delay time (write)	t_{WBD}	0	0	cycle
Burst stop delay time due to precharge (read)	t_{RQL}	2	1	cycle
Burst stop delay time due to precharge (write)	t_{WDL}	0	0	cycle
Auto-precharge start delay time (read)	t_{PQL}	−1	0	cycle
DQM to data delay time (read)	t_{QMD}	2	2	cycle
DQM to data delay time (write)	t_{DMD}	0	0	cycle
Mode register set to command delay time	t_{MCD}	2	2	cycle

Output Load

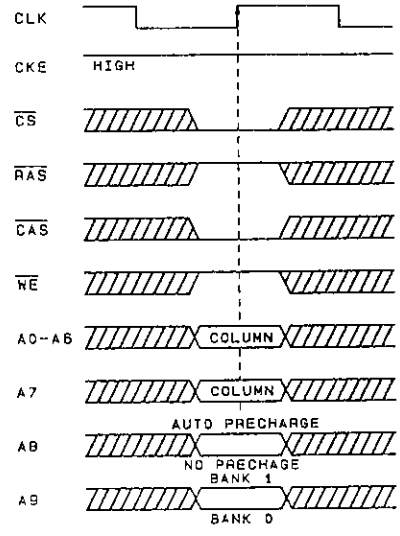


Commands

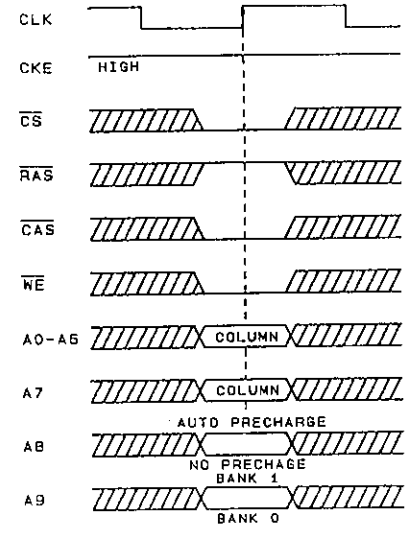
Active Command



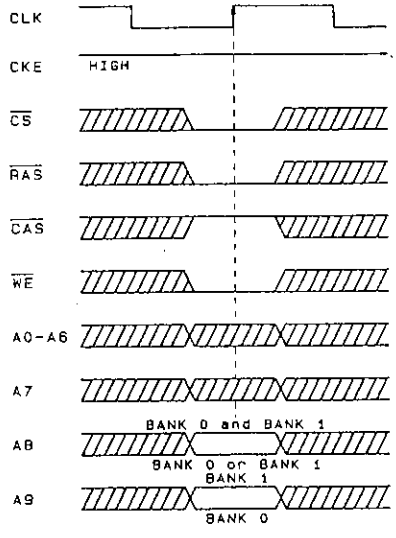
Read Command



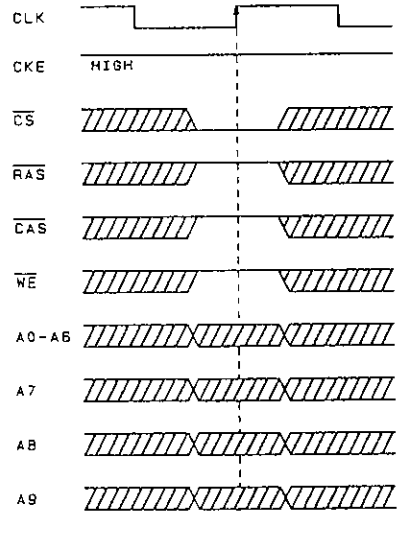
Write Command



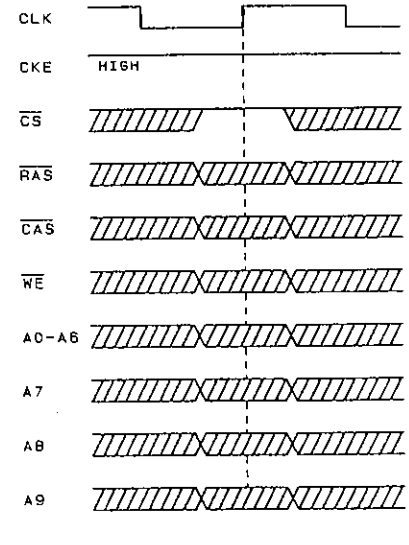
Precharge Command



No-Operation Command



Device Deselect Command



DON'T CARE

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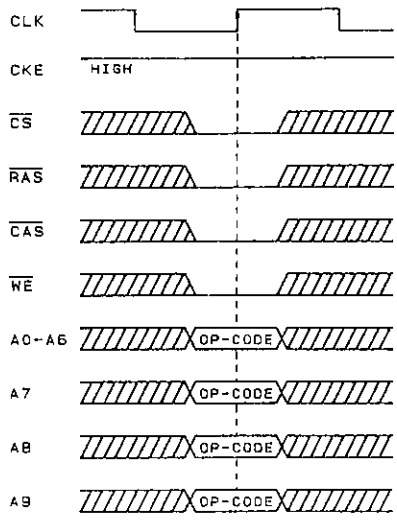
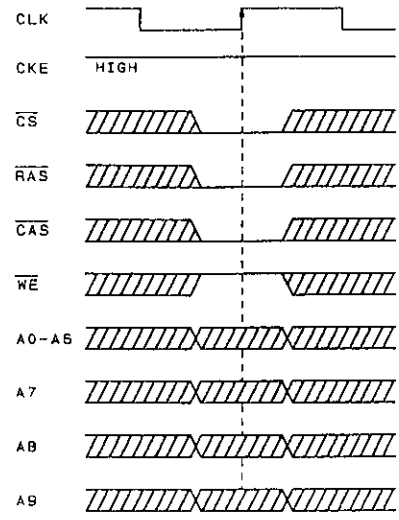
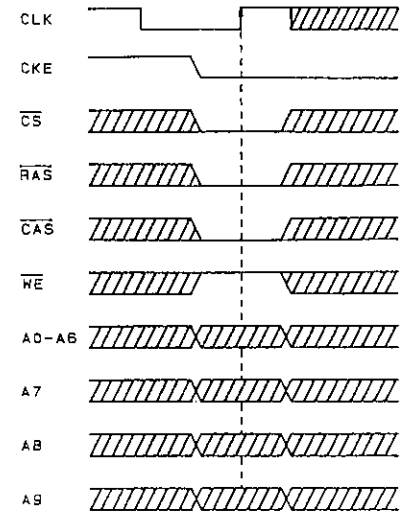
Mode Register Set Command



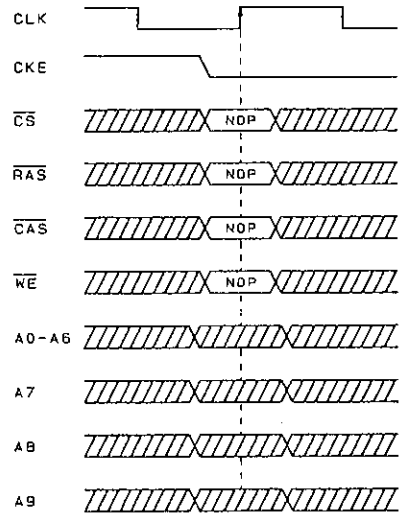
Auto-Refresh Command



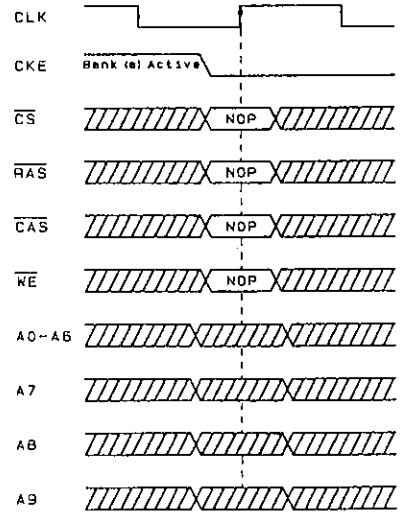
Self-Refresh Command



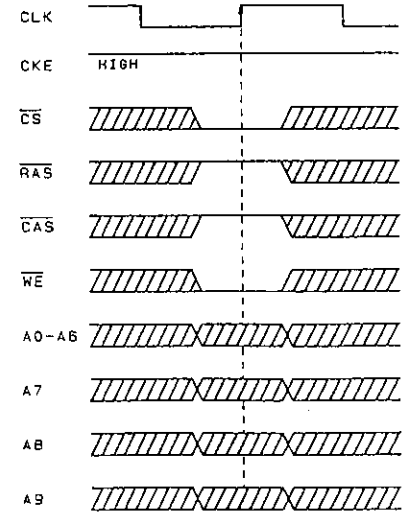
Power Down Command



Clock Suspend Command



Burst Stop Command



DON' T CARE

A03621

Mode Register Set Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = Low)

The LC382161T incorporates a register that defines the device operating mode. This command functions as a data input pin that loads this register from the pins A0 to A9. When power is first applied, the stipulated power on sequence should be executed and then the LC382161 should be initialized by executing a mode register set command.
Note that the mode register set command can be executed only when both banks are in the idle state, i.e., deactivated.
Another command cannot be executed after a mode register set command until after the passage of the period t_{MCD}, which is the period required for mode register set command execution.

Active Command ($\overline{CS}$, $\overline{RAS}$ = Low, $\overline{CAS}$, $\overline{WE}$ = High)

The LC382161T includes two banks of 256 rows each. This command selects one of the two banks according to the A9 pin and activates the row selected by the pins A0 to A6 and A8.
This command corresponds to the fall of the $\overline{RAS}$ signal from high to low in a general-purpose DRAM.

Precharge Command ($\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ = Low, $\overline{CAS}$ = High)

This command starts precharging the bank selected by pins A8 and A9. When A8 is high, both banks are precharged at the same time. When A8 is low, the bank selected by A9 is precharged. After executing this command, the next command for the selected bank(s) is executed after passage of the period t_{RP}, which is the period required for bank precharging.
This command corresponds to the rise of the $\overline{RAS}$ signal from low to high in a general-purpose DRAM.

Read Command ($\overline{CS}$, $\overline{CAS}$ = Low, $\overline{RAS}$, $\overline{WE}$ = High)

This command selects the bank specified by the A9 pin and starts a burst read operation at the start address specified by pins A0 to A6 and A7. Data is output following $\overline{CAS}$ latency.
The selected bank must be activated before executing this command.
When the A8 pin is high, this command functions as a read and auto-precharge command. After the burst read completes, the bank selected by pin A9 is precharged. When the A8 pin is low, the bank selected by the A9 pin remains in the activated state after the burst read completes.

Write Command ($\overline{CS}$, $\overline{CAS}$, $\overline{WE}$ = Low, $\overline{RAS}$ = High)

When burst write mode has been selected with the mode register set command, this command selects the bank specified by the A9 pin and starts a burst write operation at the start address specified by pins A0 to A6 and A7. The first data must be input to the DQ pins in the cycle in which this command is executed.
The selected bank must be activated before executing this command.
When the A8 pin is high, this command functions as a write and auto-precharge command. After the burst write completes, the bank selected by pin A9 is precharged. When the A8 pin is low, the bank selected by the A9 pin remains in the activated state after the burst write completes.
After the input of the last burst write data, the application must wait for the write recovery period (t_{DPL}, t_{DAL}) to elapse according to $\overline{CAS}$ latency.

Auto-Refresh Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ = Low, $\overline{WE}$, CKE = High)

This command executes the auto-precharge operation. The row address and bank to be refreshed are automatically generated during this operation.
Both banks must be placed in the idle state before executing this command.
The stipulated period (t_{RC}) is required for a single refresh operation, and no other commands can be executed during this period. The device goes to the idle state after the device internal refresh operation completes.
This command must be executed at least 512 times every 8 ms.
This command corresponds to CBR auto-refresh in general-purpose DRAMs.

Self-Refresh Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, CKE = Low, $\overline{WE}$ = High)

This command executes the self-refresh operation. The row address to be refreshed, the bank, and the refresh interval are generated automatically internally during this operation. The self-refresh operation is started by dropping the CKE pin from high to low. The self-refresh operation continues as long as the CKE pin remains low and there is no need for external control of any other pins. The self-refresh operation is terminated by raising the CKE pin from low to high. The next command cannot be executed until the device internal recovery period (t_{RC}) has elapsed.
Both banks must be placed in the idle state before executing this command.

Burst Stop Command ($\overline{CS}$, $\overline{WE}$ = Low, $\overline{RAS}$, $\overline{CAS}$ = High)

The command forcibly terminates burst read and write operations. When this command is executed during a burst read operation data output stops after the $\overline{CAS}$ latency period has elapsed.

No Operation ($\overline{CS}$ = Low, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = High)

This command has no effect on the device.

Device Deselect Command ($\overline{CS}$ = High)

This command does not perform any object operation selection with respect to the device. In other words, it performs no operation with respect to the device.

Power-Down Command (CKE = Low)

When both banks are in the idle (inactive) state, or when at least one of the banks is not in the idle state (inactive) state, this command can be used to suppress device power dissipation by reducing device internal operations to the absolute minimum. Power-down mode is started by dropping the CKE pin from high to low. Power-down mode continues as long as the CKE pin is held low. All input pins other than the CKE pin are invalid and none of the other commands can be executed in this mode. The power-down operation is terminated by raising the CKE pin from low to high. The next command cannot be executed until the recovery period (t_{CKA}) has elapsed.
Since this command differs from the self-refresh command described above in that the refresh operation is not performed automatically internally, the refresh operation must be performed within the refresh period (t_{REF}). Thus the maximum time that power-down mode can be held is just under the refresh cycle time.

Clock Suspend (CKE = Low)

This command can be used to stop the device internal clock temporarily during a read or write cycle. Clock suspend mode is started by dropping the CKE pin from high to low. Clock suspend mode continues as long as the CKE pin is held low. All input pins other than the CKE pin are invalid and none of the other commands can be executed in this mode. Also note that the device internal state is maintained. Clock suspend mode is terminated by raising the CKE pin from low to high, at which point device operation restarts. The next command cannot be executed until the recovery period (t_{CKA}) has elapsed.
Since this command differs from the self-refresh command described above in that the refresh operation is not performed automatically internally, the refresh operation must be performed within the refresh period (t_{REF}). Thus the maximum time that clock suspend mode can be held is just under the refresh cycle time.

Command Truth Table (Notes 10, 11)

Command	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A9	A8	A7	A6 to A0	DQn	Note
		n−1	n											
Mode register set command	MRS	H	X	L	L	L	L	X	OP CODE				X	12, 13
Auto-refresh command	REF	H	H	L	L	L	H	X	X	X	X	X	High-Z	14
Self-refresh command	SREF	H	L	L	L	L	H	X	X	X	X	X	High-Z	14, 15
Precharge selected bank command	PRE	H	X	L	L	H	L	X	BS	L	X	X	X	
Precharge both banks command	PALL	H	X	L	L	H	L	X	BS	H	X	X	X	
Bank activate/row selected command	ACT	H	X	L	L	H	H	X	BS	Row		Row	X	16
Write command	WRIT	H	X	L	H	L	L	X	BS	L	Column		X	17
Write/auto-precharge command	WRITA	H	X	L	H	L	L	X	BS	H	Column		X	17
Read command	READ	H	X	L	H	L	H	X	BS	L	Column		X	17
Read/auto-precharge command	READA	H	X	L	H	L	H	X	BS	H	Column		X	17
Burst stop command	BST	H	X	L	H	H	L	X	X	X	X	X	X	18
No operation	NOP	H	X	L	H	H	H	X	X	X	X	X	X	
Device deselect command	DESL	H	X	H	X	X	X	X	X	X	X	X	X	
Clock suspend/standby mode	SBY	L	X	X	X	X	X	X	X	X	X	X	X	
Data write/output enable	ENB	H	X	X	X	X	X	L	X	X	X	X	Active	
Data mask/output disable	MASK	H	X	X	X	X	X	H	X	X	X	X	High-Z	

DQM Truth Table (Notes 10, 11)

Command	Symbol	CKE		DQM	
		n−1	n	Upper	Lower
Data write/output enable	ENB	H	X	L	L
Data mask/output disable	MASK	H	X	H	H
Upper byte data write/output enable	ENBU	H	X	L	X
Lower byte data write/output enable	ENBL	H	X	X	L
Upper byte data mask/output disable	MASKU	H	X	H	X
Lower byte data mask/output disable	MASKL	H	X	X	H

CKE Truth Table (Notes 10, 11)

Current state	Command	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A9	A8	A7 to A0
			n−1	n							
Active	Start clock suspend mode	SPND	H	L	X	X	X	X	X	X	X
Other states	Clock suspend		L	L	X	X	X	X	X	X	X
Clock suspend	Terminate clock suspend mode		L	H	X	X	X	X	X	X	X
Idle	Auto-refresh command	REF	H	H	L	L	L	H	X	X	X
Idle	Start self-refresh mode	SELF	H	L	L	L	L	H	X	X	X
Self-refresh	Terminate self-refresh mode		L	H	L	H	H	H	X	X	X
			L	H	H	X	X	X	X	X	X
Idle	Start power-down mode	PDWN	H	L	L	H	H	H	X	X	X
			H	L	H	X	X	X	X	X	X
Power-down	Terminate power-down mode		L	H	X	X	X	X	X	X	X

H: A high level input with V_{IN} between V_{IH} (min) and 4.6 V
L: A low level input with V_{IN} between −0.3 V and V_{IL} (max)
X: Either a high or low level input
High-Z: A high impedance output

Operation Command Table (Notes 10, 11)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A9	A8	A7	A6 to A0	Command	Operation	Note
Idle	H	X	X	X	X	X	X	X	DESL	No operation or power-down	21
	L	H	H	H	X	X	X	X	NOP	No operation or power-down	21
	L	H	H	L	X	X	X	X	BST	No operation or power-down	
	L	H	L	H	V	V	V	V	READ/READA	Illegal	
	L	H	L	L	V	V	V	V	WRIT/WRITA	Illegal	
	L	L	H	H	V	V	X	V	ACT	Row active	
	L	L	H	L	V	V	X	X	PRE/PALL	No operation	
	L	L	L	H	X	X	X	X	REF/SELF	Auto-refresh or self-refresh	22
	L	L	L	L	OP CODE				MRS	Mode register set	
Row active	H	X	X	X	X	X	X	X	DESL	No operation	
	L	H	H	H	X	X	X	X	NOP	No operation	
	L	H	H	L	X	X	X	X	BST	No operation	
	L	H	L	H	V	V	V	V	READ/READA	Read start	27
	L	H	L	L	V	V	V	V	WRIT/WRITA	Write start	27
	L	L	H	H	V	V	X	V	ACT	Illegal	19
	L	L	H	L	V	V	X	X	PRE/PALL	Precharge	24
	L	L	L	H	X	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE				MRS	Illegal	
Read	H	X	X	X	X	X	X	X	DESL	Burst read continues, row active when done	
	L	H	H	H	X	X	X	X	NOP	Burst read continues, row active when done	
	L	H	H	L	X	X	X	X	BST	Burst read interrupted, row active after interrupt	
	L	H	L	H	V	V	V	V	READ/READA	Burst read interrupted, read restart after interrupt	25
	L	H	L	L	V	V	V	V	WRIT/WRITA	Burst read interrupted, write start after interrupt	20, 25
	L	L	H	H	V	V	X	V	ACT	Illegal	19
	L	L	H	L	V	V	X	X	PRE/PALL	Burst read interrupted, precharge after interrupt	
	L	L	L	H	X	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE				MRS	Illegal	
Write	H	X	X	X	X	X	X	X	DESL	Burst write continues, write recovery when done	
	L	H	H	H	X	X	X	X	NOP	Burst write continues, write recovery when done	
	L	H	H	L	X	X	X	X	BST	Burst write interrupted, row active after interrupt	
	L	H	L	H	V	V	V	V	READ/READA	Burst write interrupted, read start after interrupt	20, 25
	L	H	L	L	V	V	V	V	WRIT/WRITA	Burst write interrupted, write restart after interrupt	25
	L	L	H	H	V	V	X	V	ACT	Illegal	19
	L	L	H	L	V	V	X	X	PRE/PALL	Burst write interrupted, precharge after interrupt	26
	L	L	L	H	X	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE				MRS	Illegal	
Read & auto-precharge	H	X	X	X	X	X	X	X	DESL	Burst read continues, precharge when done	
	L	H	H	H	X	X	X	X	NOP	Burst read continues, precharge when done	
	L	H	H	L	X	X	X	X	BST	Illegal	
	L	H	L	H	V	V	V	V	READ/READA	Illegal	
	L	H	L	L	V	V	V	V	WRIT/WRITA	Illegal	
	L	L	H	H	V	V	X	V	ACT	Illegal	19
	L	L	H	L	V	V	X	X	PRE/PALL	Illegal	19
	L	L	L	H	X	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE				MRS	Illegal	

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Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A9	A8	A7	A6 to A0	Command	Operation	Note
Write & auto-precharge	H	X	X	X	X	X	X	X	DESL	Burst write continues, write recovery and precharge when done	
	L	H	H	H	X	X	X	X	NOP	Burst write continues, write recovery and precharge when done	
	L	H	H	L	X	X	X	X	BST	Illegal	
	L	H	L	H	V	V	V	V	READ/READA	Illegal	
	L	H	L	L	V	V	V	V	WRIT/WRITA	Illegal	
	L	L	H	H	V	V	X	V	ACT	Illegal	19
	L	L	H	L	V	V	X	X	PRE/PALL	Illegal	19
	L	L	L	H	X	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE				MRS	Illegal	
Row precharge	H	X	X	X	X	X	X	X	DESL	No operation, idle state after t_{RP} has elapsed	
	L	H	H	H	X	X	X	X	NOP	No operation, idle state after t_{RP} has elapsed	
	L	H	H	L	X	X	X	X	BST	No operation, idle state after t_{RP} has elapsed	
	L	H	L	H	V	V	V	V	READ/READA	Illegal	19
	L	H	L	L	V	V	V	V	WRIT/WRITA	Illegal	19
	L	L	H	H	V	V	X	V	ACT	Illegal	19
	L	L	H	L	V	V	X	X	PRE/PALL	No operation, idle state after t_{RP} has elapsed	19
	L	L	L	H	X	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE				MRS	Illegal	
Immediately following row active	H	X	X	X	X	X	X	X	DESL	No operation, row active after t_{RCD} has elapsed	
	L	H	H	H	X	X	X	X	NOP	No operation, row active after t_{RCD} has elapsed	
	L	H	H	L	X	X	X	X	BST	No operation, row active after t_{RCD} has elapsed	
	L	H	L	H	V	V	V	V	READ/READA	Illegal	19
	L	H	L	L	V	V	V	V	WRIT/WRITA	Illegal	19
	L	L	H	H	V	V	X	V	ACT	Illegal	19, 23
	L	L	H	L	V	V	X	X	PRE/PALL	Illegal	19
	L	L	L	H	X	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE				MRS	Illegal	
Write recovery	H	X	X	X	X	X	X	X	DESL	No operation, row active after t_{DPL} has elapsed	
	L	H	H	H	X	X	X	X	NOP	No operation, row active after t_{DPL} has elapsed	
	L	H	H	L	X	X	X	X	BST	No operation, row active after t_{DPL} has elapsed	
	L	H	L	H	V	V	V	V	READ/READA	Read start	
	L	H	L	L	V	V	V	V	WRIT/WRITA	Write restart	
	L	L	H	H	V	V	X	V	ACT	Illegal	19
	L	L	H	L	V	V	X	X	PRE/PALL	Illegal	19
	L	L	L	H	X	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE				MRS	Illegal	
Write recovery & auto-precharge	H	X	X	X	X	X	X	X	DESL	No operation, idle state after t_{DAL} has elapsed	
	L	H	H	H	X	X	X	X	NOP	No operation, idle state after t_{DAL} has elapsed	
	L	H	H	L	X	X	X	X	BST	No operation, idle state after t_{DAL} has elapsed	
	L	H	L	H	V	V	V	V	READ/READA	Illegal	19
	L	H	L	L	V	V	V	V	WRIT/WRITA	Illegal	19
	L	L	H	H	V	V	X	V	ACT	Illegal	19
	L	L	H	L	V	V	X	X	PRE/PALL	Illegal	19
	L	L	L	H	X	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE				MRS	Illegal	

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Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A9	A8	A7	A6 to A0	Command	Operation	Note
Refresh	H	X	X	X	X	X	X	X	DESL	No operation, idle state after t_{RC} has elapsed	
	L	H	H	H	X	X	X	X	NOP	No operation, idle state after t_{RC} has elapsed	
	L	H	H	L	X	X	X	X	BST	No operation, idle state after t_{RC} has elapsed	
	L	H	L	H	V	V	V	V	READ/READA	Illegal	
	L	H	L	L	V	V	V	V	WRIT/WRITA	Illegal	
	L	L	H	H	V	V	X	V	ACT	Illegal	
	L	L	H	L	V	V	X	X	PRE/PALL	Illegal	
	L	L	L	H	X	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE				MRS	Illegal	
Mode register set	H	X	X	X	X	X	X	X	DESL	No operation, idle state after t_{MCD} has elapsed	
	L	H	H	H	X	X	X	X	NOP	No operation, idle state after t_{MCD} has elapsed	
	L	H	H	L	X	X	X	X	BST	No operation, idle state after t_{MCD} has elapsed	
	L	H	L	H	V	V	V	V	READ/READA	Illegal	
	L	H	L	L	V	V	V	V	WRIT/WRITA	Illegal	
	L	L	H	H	V	V	X	V	ACT	Illegal	
	L	L	H	L	V	V	X	X	PRE/PALL	Illegal	
	L	L	L	H	X	X	X	X	REF/SELF	Illegal	
	L	L	L	L	OP CODE				MRS	Illegal	

Note: 10. H: High level input, L: Low level input, X: High or low level input (undefined state), V: Direct input voltage at a stipulated high or low level
11. All input signals are latched on the rising edge of the CLK signal.
12. Both banks must be placed in the inactive (idle) state in advance.
13. The state of the A0 to A9 pins is loaded into the mode register as an OP code.
14. The row address is generated automatically internally at this time. The DQ pin and the address pin data is ignored.
15. During a self-refresh operation, all pin data (states) other than CKE is ignored.
16. The selected bank must be placed in the inactive (idle) state in advance.
17. The selected bank must be placed in the active state in advance.
18. This command is valid only when the burst length is set to full page.
19. This is possible depending on the state of the bank selected by the A9 pin.
20. Time to switch internal busses is required.
21. The LC382161 can be switched to power-down mode by dropping the CKE pin low when both banks are in the idle state.
Input pins other than CKE are ignored at this time.
22. The LC382161 can be switched to self refresh mode by dropping the CKE pin low when both banks are in the idle state.
Input pins other than CKE are ignored at this time.
23. Possible if t_{RRD} is satisfied.
24. Possible if t_{RAS} is satisfied.
25. The conditions for burst interruption must be observed.
Also note that the LC382161 will enter the precharged state immediately after the burst operation completes if auto-precharge is selected.
26. Data must be masked by setting the DQM pin high when input data is available during the t_{DPL} period.
27. Command input becomes possible after the period t_{RCD} has elapsed.
Also note that the LC382161 will enter the precharged state immediately after the burst operation completes if auto-precharge is selected.

CKE Related Command Truth Table (Note 28)

Current state	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A9	A8	A7 to A0	Operation	Note
	n−1	n									
Self-refresh	H	X	X	X	X	X	X	X	X	Undefined	
	L	H	H	X	X	X	X	X	X	Self-refresh recovery	29
	L	H	L	H	H	X	X	X	X	Self-refresh recovery	29
	L	H	L	H	L	X	X	X	X	Illegal	29
	L	H	L	L	X	X	X	X	X	Illegal	29
	L	L	X	X	X	X	X	X	X	Self-refresh	
Self-refresh recovery	H	H	H	X	X	X	X	X	X	Idle state after tRC has elapsed	
	H	H	L	H	H	X	X	X	X	Idle state after tRC has elapsed	
	H	H	L	H	L	X	X	X	X	Illegal	
	H	H	L	L	X	X	X	X	X	Illegal	
	H	L	H	X	X	X	X	X	X	Power-down on the next cycle	32
	H	L	L	H	H	X	X	X	X	Power-down on the next cycle	32
	H	L	L	H	L	X	X	X	X	Illegal	
	H	L	L	L	X	X	X	X	X	Illegal	
	L	H	X	X	X	X	X	X	X	Clock suspend termination on the next cycle	29
	L	L	X	X	X	X	X	X	X	Clock suspend	
Power-down	H	X	X	X	X	X	X	X	X	Undefined	
	L	H	X	X	X	X	X	X	X	Power-down mode termination, idle after that termination	29
	L	L	X	X	X	X	X	X	X	Power-down mode	
Both banks idle	H	H	H	X	X	X	X	X	X	No operation	
	H	H	L	H	X	X	X	X	X	See the operation command table	
	H	H	L	L	H	X	X	X	X	Bank active or precharge	
	H	H	L	L	L	H	X	X	X	Auto-precharge	
	H	H	L	L	L	L	OP CODE			Mode register set	
	H	L	H	X	X	X	X	X	X	See the operation command table	
	H	L	L	H	X	X	X	X	X	See the operation command table	
	H	L	L	L	H	X	X	X	X	See the operation command table	
	H	L	L	L	L	H	X	X	X	Self-refresh	30
	H	L	L	L	L	L	OP CODE			See the operation command table	
	L	X	X	X	X	X	X	X	X	Power-down mode	30
Other states	H	H	X	X	X	X	X	X	X	See the operation command table	
	H	L	X	X	X	X	X	X	X	Clock suspend on the next cycle	31
	L	H	X	X	X	X	X	X	X	Clock suspend termination on the next cycle	
	L	L	X	X	X	X	X	X	X	Clock suspend termination on the next cycle	

Note: 28. H: High level input, L: Low level input, X: High or low level input (undefined state), V: Direct input voltage at a stipulated high or low level
29. The CLK pin and the other inputs are reactivated asynchronously by the transition of the CKE level from low to high.
The minimum setup time required before all commands other than mode termination commands must be satisfied.
30. Both banks must be set to the inactive (idle) state in advance to switch to power-down mode or self-refresh mode.
31. The input must be a command defined in the operation command table.
32. The period t_{SREX} must be satisfied.

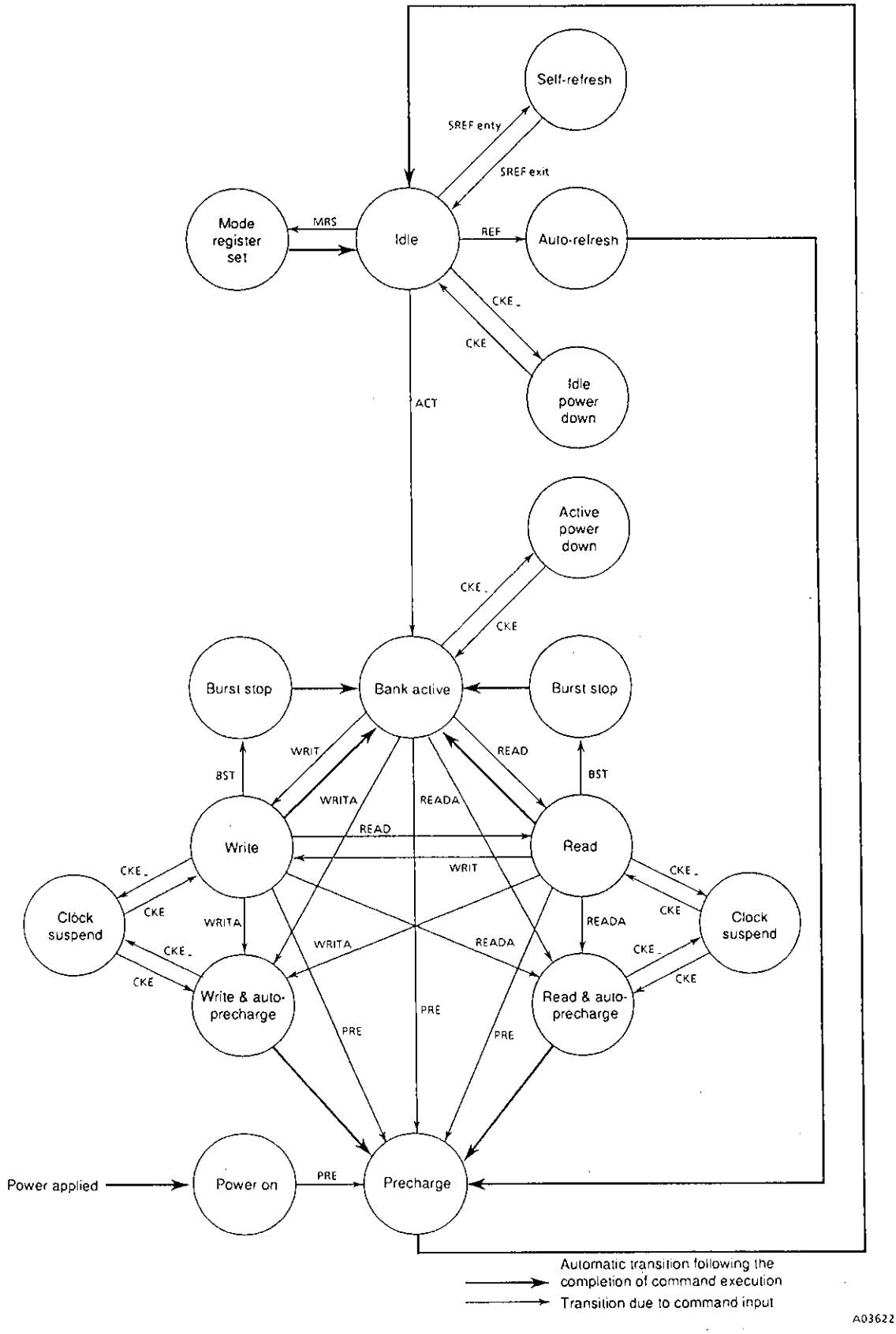
Two-Bank Manipulation Command Truth Table (Notes 33, 34)

$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A9	A8	A7	A6 to A0	Operation	Previous state		Next state	
									Bank 0	Bank 1	Bank 0	Bank 1
H	X	X	X	X	X	X	X	DESL	Any	Any	Any	Any
L	H	H	H	X	X	X	X	NOP	Any	Any	Any	Any
L	H	H	L	X	X	X	X	BST	R/W/A	I/A	A	I/A
									I	I/A	I	I/A
									I/A	R/W/A	I/A	A
									I/A	I	I/A	I
L	H	L	H	H	H	CA		READ	I/A	R/W/A	I/A	RP
				H	H	CA			R/W	A	A	RP
				H	L	CA			I/A	R/W/A	I/A	R
				H	L	CA			R/W	A	A	R
				L	H	CA			R/W/A	I/A	RP	I/A
				L	H	CA			A	R/W	RP	A
				L	L	CA			R/W/A	I/A	R	I/A
				L	L	CA			A	R/W	R	A
L	H	L	L	H	H	CA		WRIT	I/A	R/W/A	I/A	WP
				H	H	CA			R/W	A	A	WP
				H	L	CA			I/A	R/W/A	I/A	W
				H	L	CA			R/W	A	A	W
				L	H	CA			R/W/A	I/A	WP	I/A
				L	H	CA			A	R/W	WP	A
				L	L	CA			R/W/A	I/A	W	I/A
				L	L	CA			A	R/W	W	A
L	L	H	H	H	RA	X	RA	ACT	Any	I	Any	A
				L	RA	X	RA		I	Any	A	Any
L	L	H	L	X	H	X	X	PRE	R/W/A/I	I/A	I	I
				X	H	X	X		I/A	R/W/A/I	I	I
				H	L	X	X		I/A	R/W/A/I	I/A	I
				H	L	X	X		R/W/A/I	I/A	R/W/A/I	I
				L	L	X	X		R/W/A/I	I/A	I	I/A
				L	L	X	X		I/A	R/W/A/I	I	R/W/A/I
L	L	L	H	X	X	X	X	REF	I	I	I	I
L	L	L	L	OP CODE				MRS	I	I	I	I

Note: 33. H: High level input, L: Low level input, X: High or low level input (undefined state), V: Direct input voltage at a stipulated high or low level
RA: Row address, CA: Column address

34. The device state symbols are interpreted as follows.
- I: Idle (inactive) state
- A: Row active state
- R: Read
- W: Write
- RP: Read & auto-precharge
- WP: Write & auto-precharge
- Any: Any state

Simplified State Transition Diagram



Device Initialization at Power-on (power-on sequence)

As is the case with general-purpose DRAMs, the LC382161T must be initialized by executing a stipulated power-on sequence after power is applied.
After power is applied and V_{CC} and $V_{CC}Q$ reach their stipulated voltages, set and hold the CKE and DQM pins high for 100 µs. Then, execute the precharge command to precharge both banks. Next, execute the auto-precharge command twice and define the device operating mode by executing a mode register set command.

Mode Register Settings

The mode register set command sets the mode register. When this command is executed, pins A0 to A6, A7, A8, and A9 function as data input pins for setting the register, and this data becomes the device internal OP code. This OP code has four fields as listed in the table below.

Input pin	Field
A9, A8, A7	Option
A6, A5, A4	$\overline{CAS}$ latency
A3	Burst type
A2, A1, A0	Burst length

Note that the mode register set command can be executed only when both banks are in the idle (inactive) state. Wait at least two cycles after executing a mode register set command before executing the next command.

$\overline{CAS}$ Latency

During a read operation, the delay between the execution of the read command and data output is stipulated as the $\overline{CAS}$ latency. This period can be set using the mode register set command. The optimal $\overline{CAS}$ latency is determined by the clock frequency. See the "Operating Frequency/Latency Relationships" item on page 7 for details on the relationship between the clock frequency and the $\overline{CAS}$ latency. See the table on the next page for details on setting the mode register.

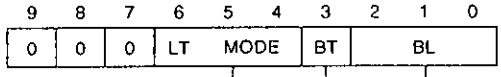
Burst Length

When writing or reading, data can be input or output data continuously. In these operations, an address is input only once and that address is taken as the starting address internally by the device. The device then automatically generates the following addresses. The mode register set command burst length field stipulates the number of data items input or output in sequence. In the LC382161T, a burst length of 1, 2, 4, 8, or full page can be specified. See the table on the next page for details on setting the mode register.

Burst Type

The burst data order during a read or write operation is stipulated by the burst type, which can be set by the mode register set command. The LC382161T supports sequential mode and interleaved mode burst type settings. See the table on the next page for details on setting the mode register. See the "Burst Length and Column Address Sequence" item on page 21 for details on I/O data orders in these modes.

Mode Register



Address bus
Mode register (Mx)

	M2	M1	M0	Sequential	Interleaved
Burst length	0	0	0	1	Reserved
	0	0	1	2	2
	0	1	0	4	4
	0	1	1	8	8
	1	0	0	Reserved	Reserved
	1	0	1	Reserved	Reserved
	1	1	0	Reserved	Reserved
	1	1	1	Full page	Reserved

	M3	Type
Burst type	0	Sequential
	1	Interleaved

	M6	M5	M4	$\overline{CAS}$ latency
Latency mode	0	0	0	Reserved
	0	0	1	1
	0	1	0	2
	0	1	1	Reserved
	1	0	0	Reserved
	1	0	1	Reserved
	1	1	0	Reserved
	1	1	1	Reserved

M9	M8	M7	M6 to M0	Functions
0	0	0	Defined	Mode register set
0	0	1	Defined	JEDEC standard test setting
1	0	0	Defined	Burst read & single write
—	—	—	—	Other combinations are undefined.

Burst Length and Column Address Sequence

Burst length	Column address			Address sequence	
	A2	A1	A0	Sequential	Interleaved
2	×	×	0	0–1	0–1
	×	×	1	1–0	1–0
4	×	0	0	0–1–2–3	0–1–2–3
	×	0	1	1–2–3–0	1–0–3–2
	×	1	0	2–3–0–1	2–3–0–1
	×	1	1	3–0–1–2	3–2–1–0
8	0	0	0	0–1–2–3–4–5–6–7	0–1–2–3–4–5–6–7
	0	0	1	1–2–3–4–5–6–7–0	1–0–3–2–5–4–7–6
	0	1	0	2–3–4–5–6–7–0–1	2–3–0–1–6–7–4–5
	0	1	1	3–4–5–6–7–0–1–2	3–2–1–0–7–6–5–4
	1	0	0	4–5–6–7–0–1–2–3	4–5–6–7–0–1–2–3
	1	0	1	5–6–7–0–1–2–3–4	5–4–7–6–1–0–3–2
	1	1	0	6–7–0–1–2–3–4–5	6–7–4–5–2–3–0–1
	1	1	1	7–0–1–2–3–4–5–6	7–6–5–4–3–2–1–0
Full page (256)	n	n	n	Cn, Cn + 1, Cn + 2,	None
				Cn + 3, Cn + 4.....	
				...Cn – 1 (Cn + 255)	
				Cn (Cn + 256)	

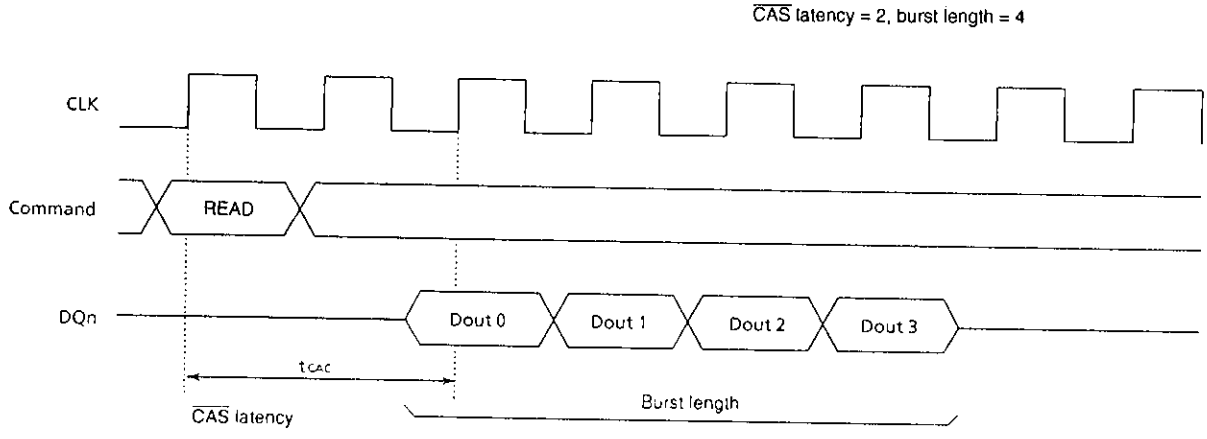
Note: The burst length in full page mode is 256.

Bank Select and Precharge Address Allocation

Row	X0	—	Row address	
	X1	—	Row address	
	X2	—	Row address	
	X3	—	Row address	
	X4	—	Row address	
	X5	—	Row address	
	X6	—	Row address	
	X7	—	Invalid	
	X8	0	Precharge of the selected bank (precharge command)	Row address (active command)
		1	Precharge of both banks (precharge command)	
	X9	0	Bank 0 selected (precharge and active commands)	
		1	Bank 1 selected (precharge and active commands)	
Column	Y0	—	Column address	
	Y1	—	Column address	
	Y2	—	Column address	
	Y3	—	Column address	
	Y4	—	Column address	
	Y5	—	Column address	
	Y6	—	Column address	
	Y7	—	Column address	
	Y8	0	Auto-precharge not performed	
		1	Auto-precharge performed	
	Y9	0	Bank 0 select (read and write commands)	
		1	Bank 1 select (read and write commands)	

Burst Read

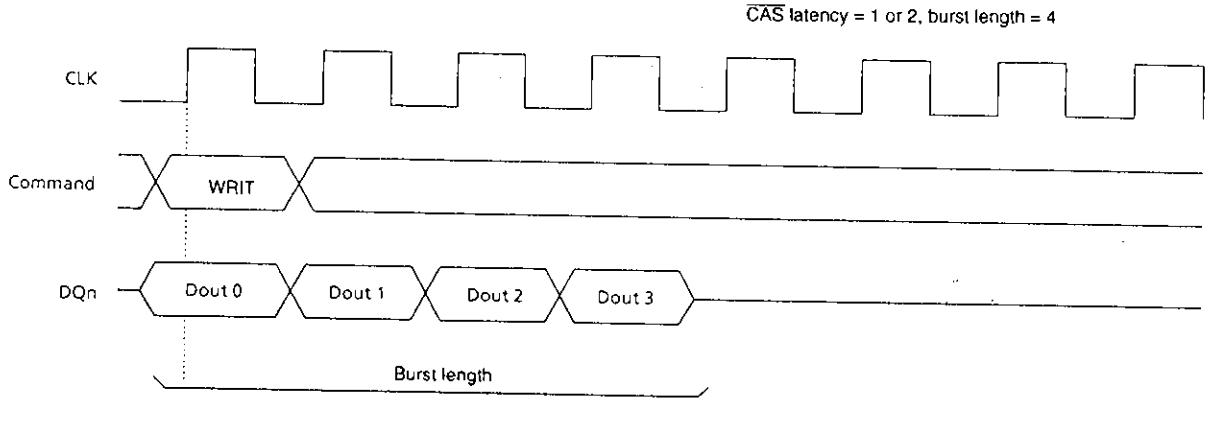
The read cycle is started by executing the read command. The address provided during read command execution is used as the starting address. First, the data corresponding to this address is output in synchronization with the clock signal after the $\overline{CAS}$ latency period. Next, data corresponding to an address generated automatically by the device is output in synchronization with the clock signal.
The output buffers go to the low impedance state $\overline{CAS}$ latency minus one cycles after the read command, and go to the high impedance state automatically after the last data is output. However, the case where the burst length is a full page is an exception. In this case the output buffers must be set to the high impedance state by executing a burst stop command.
Note that the upper byte and lower byte output data can be masked independently under control of the signals applied to the U/LDQM pins. The delay period (t_{QMD}) is fixed at two, regardless of the $\overline{CAS}$ latency setting, when this function is used.
The selected bank must be set to the active state before executing this command.



A03623

Burst Write

The write cycle is started by executing the write command. The address provided during write command execution is used as the starting address, and at the same time data for this address is input in synchronization with the clock signal. Next, data is input in order in synchronization with the clock signal. During this operation, data is written to addresses generated automatically by the device. This cycle terminates automatically after a number of clock cycles determined by the stipulated burst length. However, the case where the burst length is a full page is an exception. In this case the write cycle must be terminated by executing a burst stop command.
The latency for DQ pin data input is zero, regardless of the $\overline{CAS}$ latency setting. However, a wait period (write recovery: t_{DPL}) after the last data input is required for the device to complete the write operation.
Note that the upper byte and lower byte input data can be masked independently under control of the signals applied to the U/LDQM pins. The delay period (t_{DMD}) is fixed at zero, regardless of the $\overline{CAS}$ latency setting, when this function is used.
The selected bank must be set to the active state before executing this command.



A03624

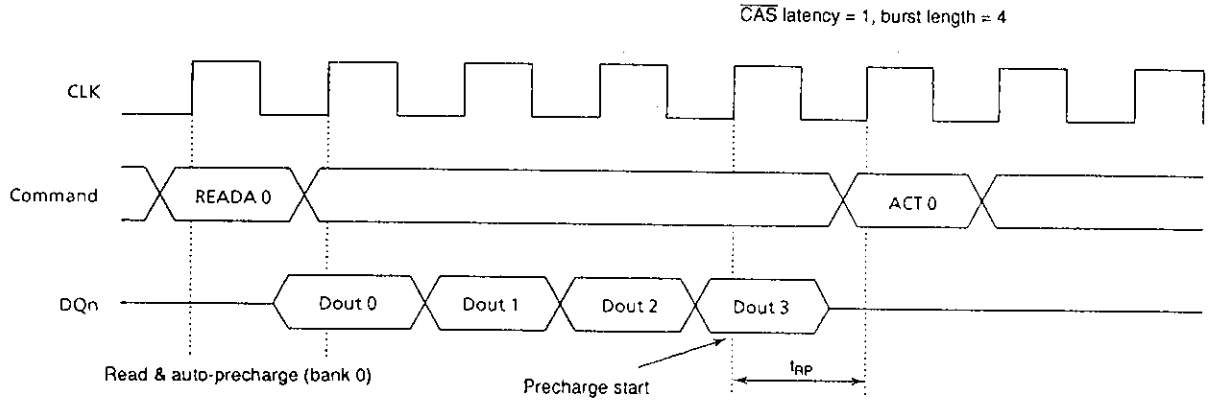
Read & Auto-Precharge

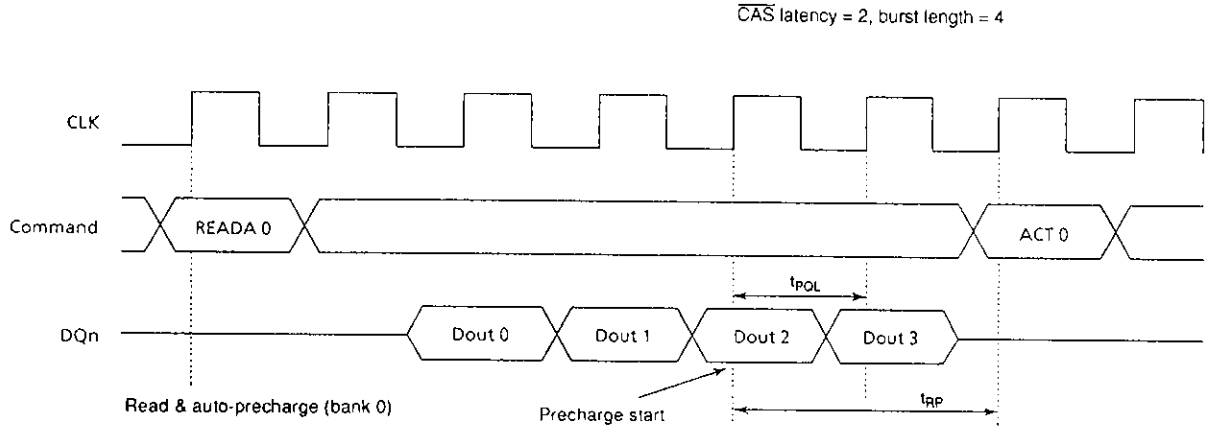
The read & auto-precharge command first executes a burst read operation and then puts the selected bank in the precharged state automatically. After the precharge completes, the bank goes to the idle state. Thus this command performs a read command and a precharge command in a single operation.

During this operation, the delay period (t_{PQL}) between the last burst data output and the start of the precharge operation differs depending on the $\overline{CAS}$ latency setting. When the $\overline{CAS}$ latency setting is one, the precharge operation starts at the same time as the last burst data is output ($t_{PQL} = 0$), and when the $\overline{CAS}$ latency setting is two, the precharge operation starts on the clock cycle one cycle before the last burst data is output ($t_{PQL} = -1$). Therefore, the selected bank can be made active after a delay of t_{RP} from the start position of this precharge operation.

The selected bank must be set to the active state before executing this command.

The auto-precharge function is invalid if the burst length is set to full page.





A03625

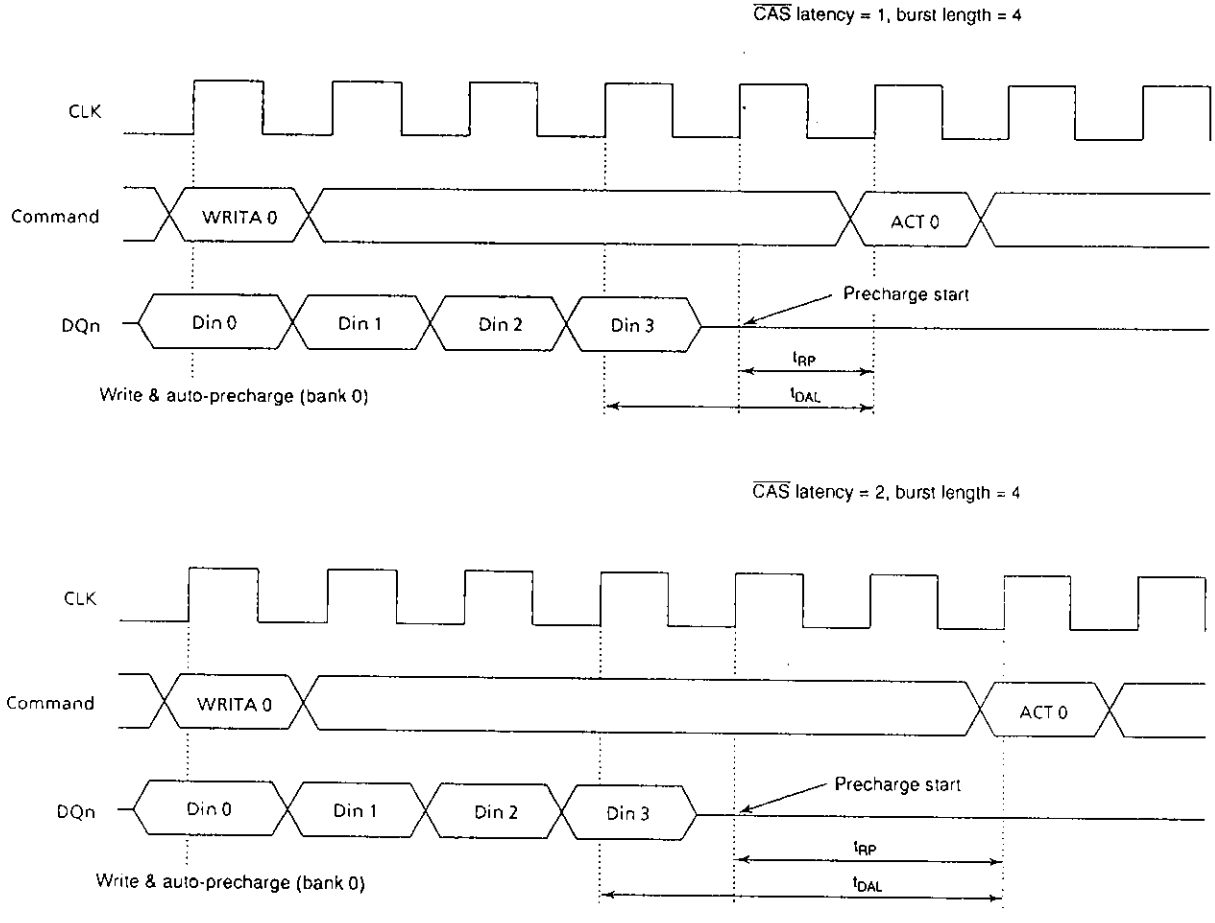
Write & Auto-Precharge

The write & auto-precharge command first executes a burst write operation and then puts the selected bank in the precharged state automatically. After the precharge completes the bank goes to the idle state. Thus this command performs a write command and a precharge command in a single operation.

During this operation, the delay period (t_{DAL}) between the last burst data input and the completion of the precharge operation is t_{RP} plus one CLK period. That is, the precharge operation starts one clock period after the last burst data input. Therefore, the selected bank can be made active after a delay of t_{DAL}.

The selected bank must be set to the active state before executing this command.

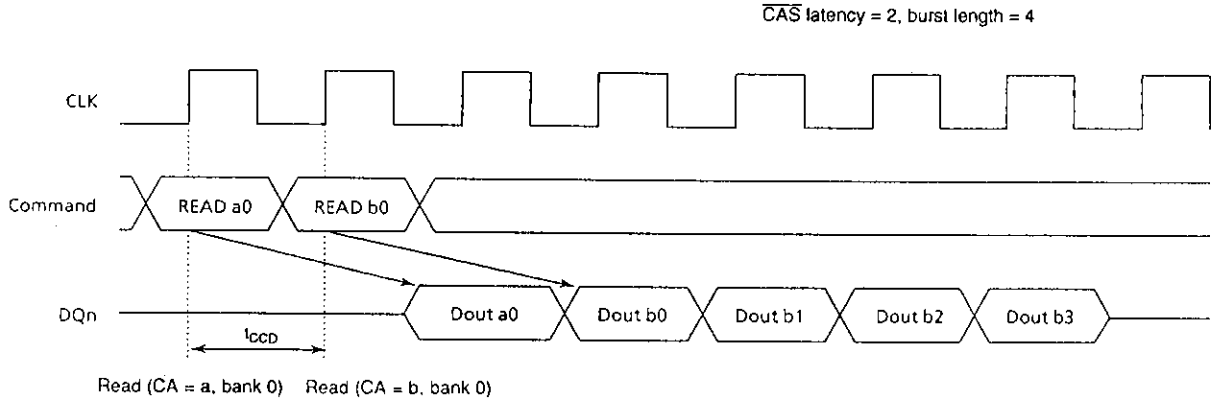
The auto-precharge function is invalid if the burst length is set to full page.



A03626

Spacing between Read Commands

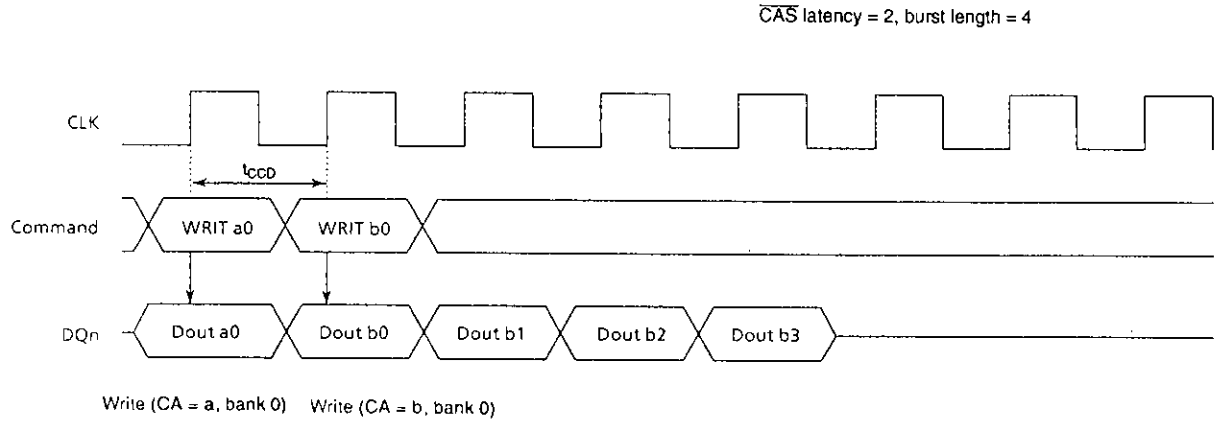
A new read command can be executed while a read cycle is in progress, i.e., before that cycle completes. When the second read command is executed, after the $\overline{CAS}$ latency has elapsed, data corresponding to the new read command is output in place of the data due to the previous read command.
The interval between two read commands (t_{CCD}) must be at least one clock cycle.
The selected bank must be set to the active state before executing this command.



A03627

Spacing between Write Commands

A new write command can be executed while a write cycle is in progress, i.e., before that cycle completes. At the point the second write command is executed, data corresponding to the new write command can be input in place of the data for the previous write command.
The interval between two write commands (t_{CCD}) must be at least one clock cycle.
The selected bank must be set to the active state before executing this command.

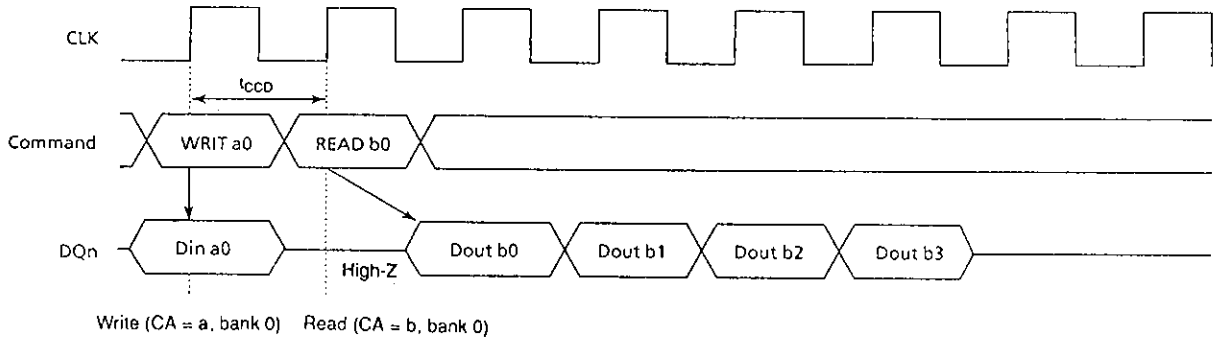


A03628

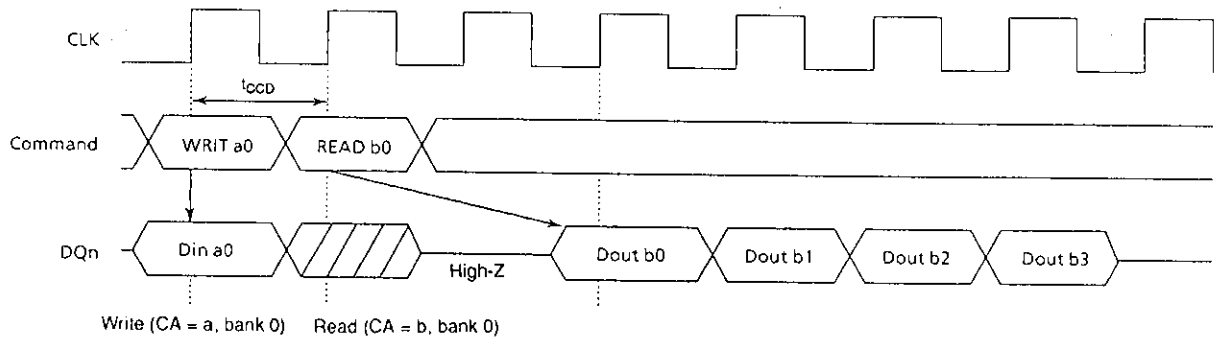
Spacing between Write and Read Commands

A new read command can be executed while a write cycle is in progress, i.e., before that cycle completes. Data corresponding to the new read command is output after the $\overline{CAS}$ latency has elapsed from the point the new read command was executed. The DQn pins must be placed in the high impedance state at least one clock cycle before data is output during this operation.
The interval (t_{CCD}) between commands must be at least 1 clock cycle.
The selected bank must be set to the active state before executing this command.

$\overline{CAS}$ latency = 1, burst length = 4



$\overline{CAS}$ latency = 2, burst length = 4

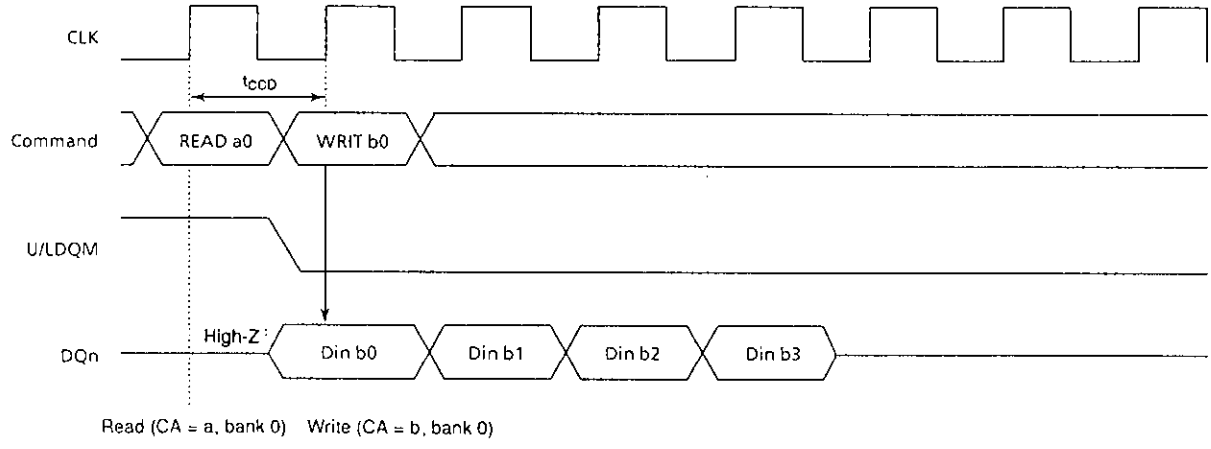


A03629

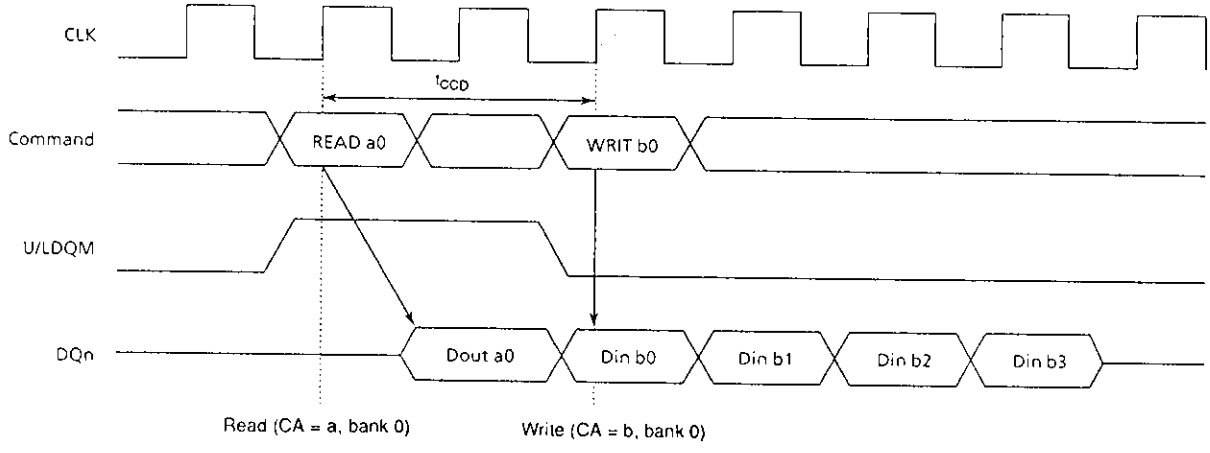
Spacing between Read and Write Commands

A read command can be interrupted and a new write command executed while the read cycle is in progress, i.e., before that cycle completes. Data corresponding to the new write command can be input at the point the new write command is executed. To prevent collision between input and output data at the DQn pins during this operation, the output data must be masked using the U/LDQM pins. The interval (t_{CCD}) between these commands must be at least 1 clock cycle.
The selected bank must be set to the active state before executing this command.

$\overline{CAS}$ latency = 1 or 2, burst length = 4



$\overline{CAS}$ latency = 1, burst length = 4



A03630

Precharge

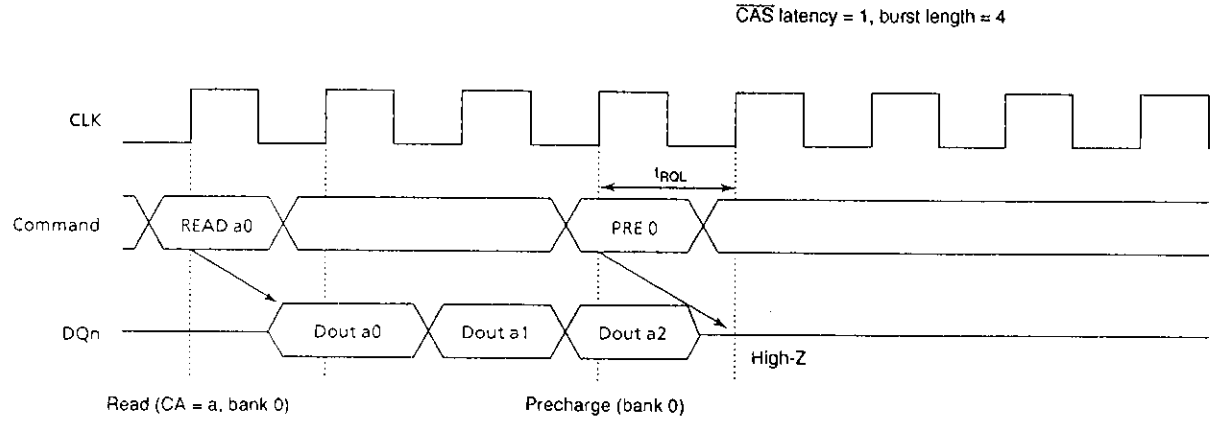
The precharge command sets the bank selected by pin A9 to the precharged state. This command can be executed at a time t_{RAS} following the execution of an active command applied to the same bank. The selected bank goes to the idle state at time t_{RP} following the execution of the precharge command, and an active command can be executed again for that bank.

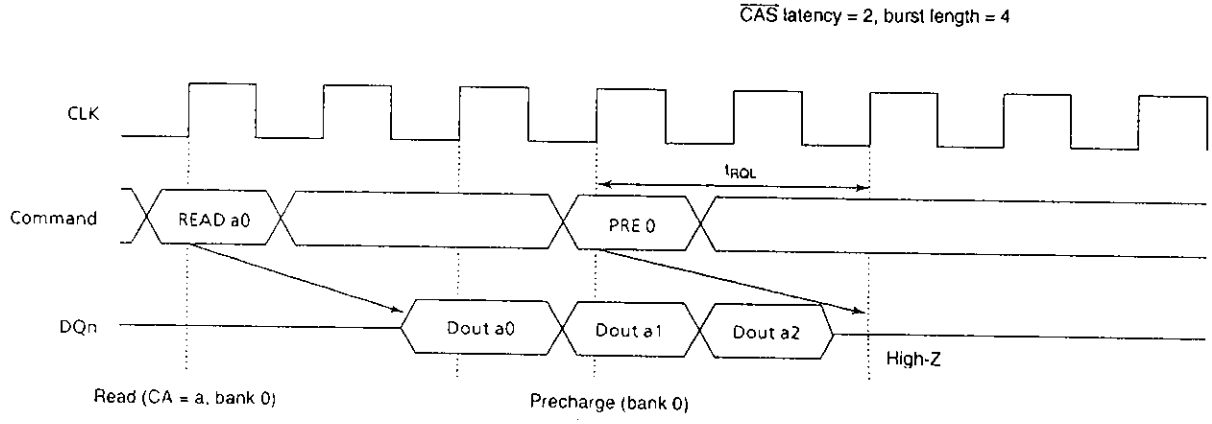
If pin A8 is low when this command is executed, the bank selected by pin A9 will be precharged, and if pin A8 is high, both banks will be precharged at the same time. The input to pin A9 is ignored in the latter case.

Read Cycle Interruption Using the Precharge Command

A read cycle can be interrupted by the execution of the precharge command before that cycle completes. The delay time (t_{RQL}) from the execution of the precharge command to the completion of the burst output, i.e., the point the outputs go to the high impedance state will be one clock cycle if the $\overline{CAS}$ latency is one, and two clock cycles if the $\overline{CAS}$ latency is two.

Inversely, to output burst data through the completion of the burst cycle, the precharge command must be executed either at the same time as or later than the last burst data output if the $\overline{CAS}$ latency is one, or no more than one clock cycle before the last output if the $\overline{CAS}$ latency is two.

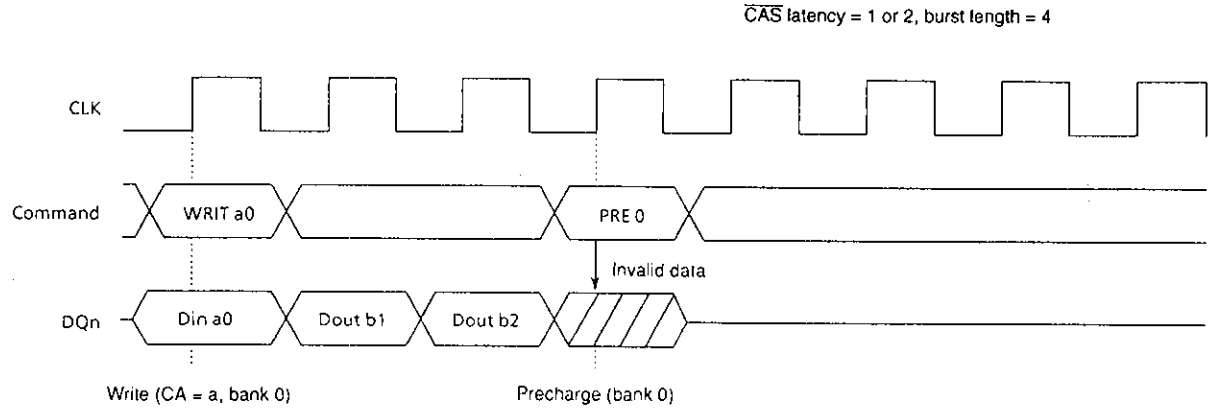


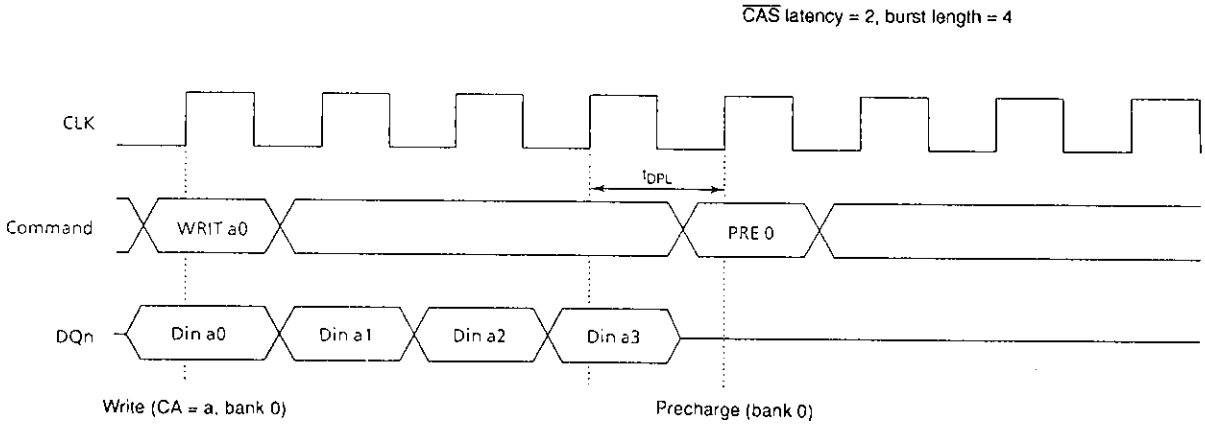


A03631

Write Cycle Interruption Using the Precharge Command

A write cycle can be interrupted by the execution of the precharge command before that cycle completes. The delay time (t_{WDL}) from the execution of the precharge command to the point where burst input is invalid, i.e., the point where input data is no longer written to device internal memory, is zero clock cycles, regardless of the $\overline{CAS}$ latency.
Inversely, to write all the burst data to the device, the precharge command must be executed after the write data recovery period (t_{DPL}) has elapsed. Therefore, the precharge command must be executed on a clock cycle that follows the input of the last burst data item.

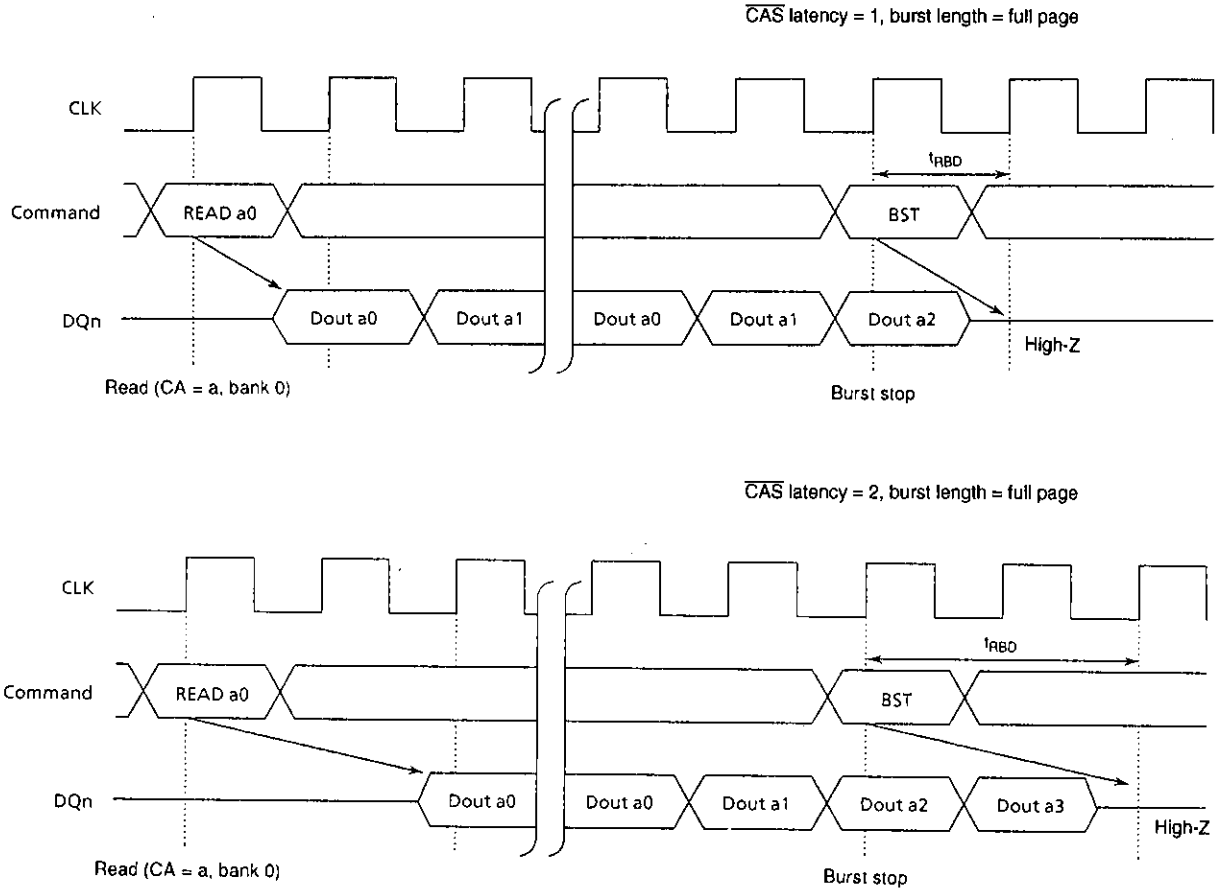




A03632

Read Cycle (full page) Interruption Using the Burst Stop Command

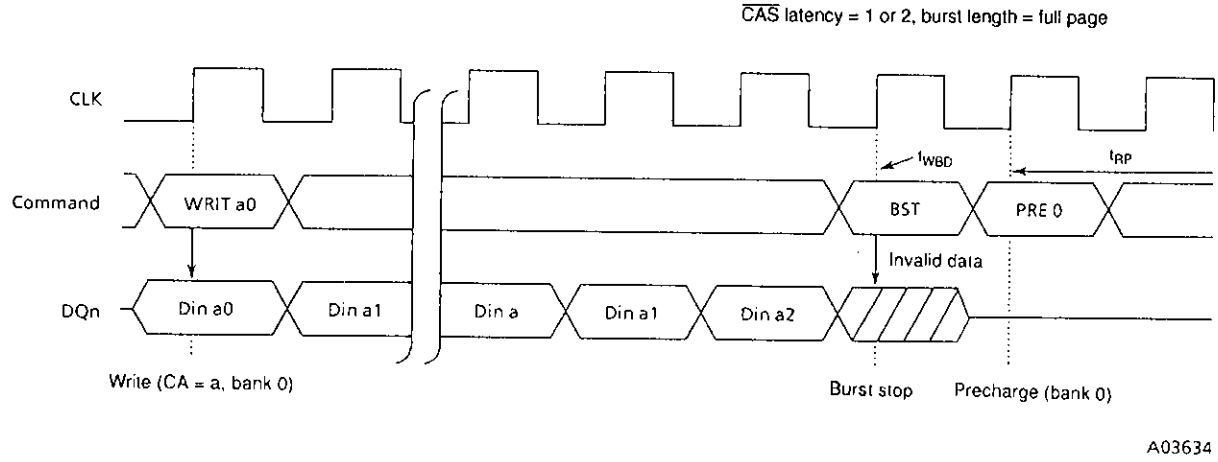
The LC382161 can output data continuously from the burst start address (a) to location a + 255 during a read cycle in which the burst length is set to full page. The LC382161 repeats the operation starting with the 256th cycle, with the data output returning to location (a) and continuing with a + 1, a + 2, a + 3, etc. A burst stop command must be executed to terminate this cycle. A precharge command must be executed within the $\overline{RAS}$ cycle time ($t_{RAS\ max}$) following the burst stop command. After the period (t_{RBD}) required for burst data output to stop following the execution of the burst stop command has elapsed, the outputs go to the high impedance state. This period (t_{RBD}) is one clock cycle when the $\overline{CAS}$ latency is one and two clock cycles when the $\overline{CAS}$ latency is two.



A03633

Write Cycle (full page) Interruption Using the Burst Stop Command

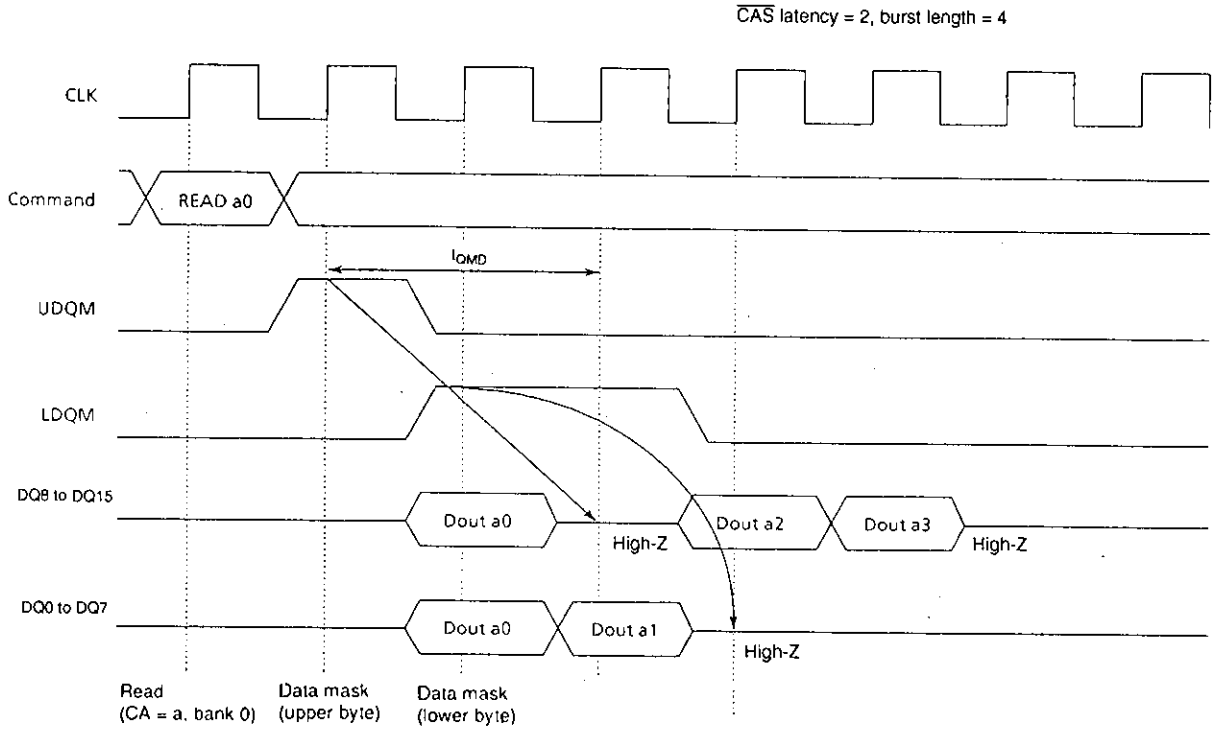
The LC382161 can input data continuously from the burst start address (a) to location a + 255 during a write cycle in which the burst length is set to full page. The LC382161 repeats the operation starting with the 256th cycle, with data input returning to location (a) and continuing with a + 1, a + 2, a + 3, etc. A burst stop command must be executed to terminate this cycle. A precharge command must be executed within the $\overline{RAS}$ cycle time ($t_{RAS\ max}$) following the burst stop command. After the period (t_{WBD}) required for burst data input to stop following the execution of the burst stop command has elapsed, the write cycle terminates. This period (t_{WBD}) is zero clock cycles, regardless of the $\overline{CAS}$ latency.



Burst Data Interruption Using the U/LDQM Pins (read cycle)

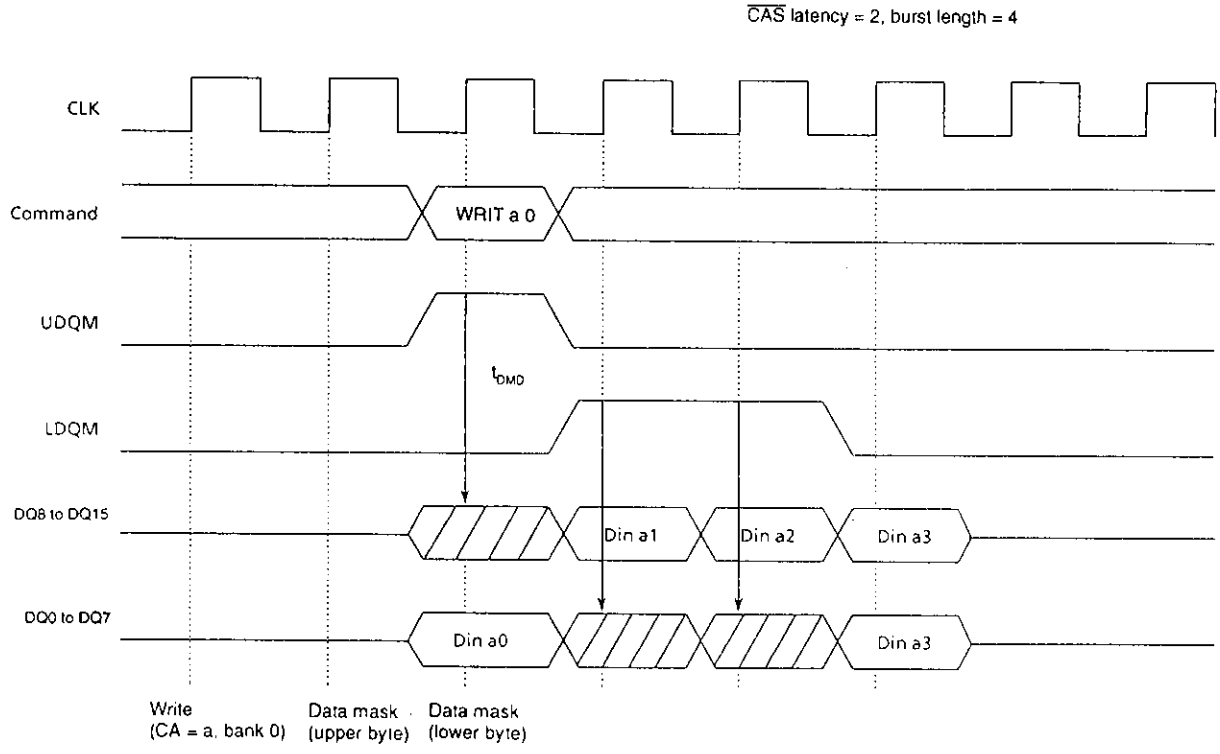
Burst data output can be temporarily interrupted (masked) during a read cycle using the U/LDQM pins. Regardless of the $\overline{CAS}$ latency, two clock cycles (t_{QMD}) after one of the U/LDQM pins goes high, the corresponding outputs go to the high impedance state. Subsequently, the outputs are maintained in the high impedance state as long as that U/LDQM pin remains high. When the U/LDQM pin goes low, output is resumed at a time t_{QMD} later. This output control operates independently on a byte basis with the UDQM pin controlling upper byte output (pins DQ8 to DQ15) and the LDQM pin controlling lower byte output (pins DQ0 to DQ7).

Since the U/LDQM pins control the device output buffers only, the read cycle continues internally and, in particular, incrementing of the internal burst counter continues.



Burst Data Interruption Using the U/LDQM Pins (write cycle)

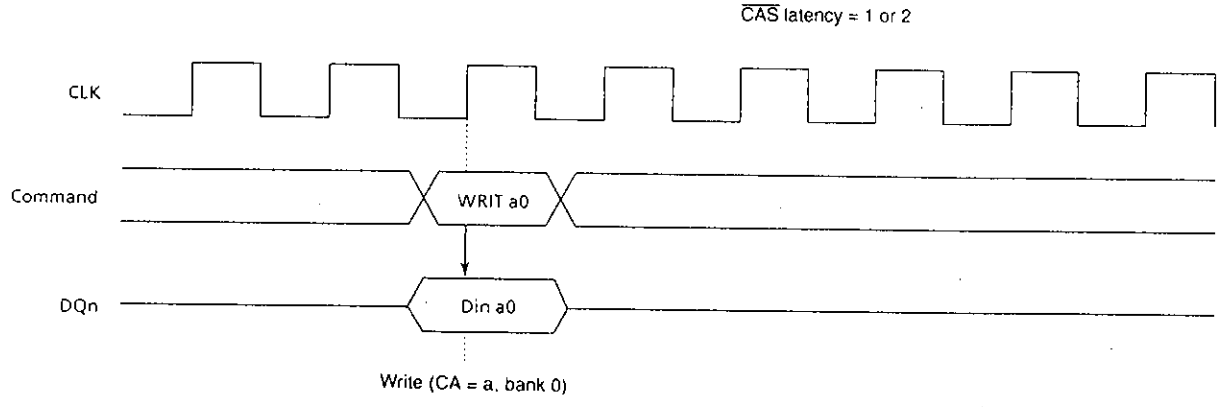
Burst data input can be temporarily interrupted (muted) during a write cycle using the U/LDQM pins. Regardless of the $\overline{CAS}$ latency, as soon as one of the U/LDQM pins goes high, the corresponding externally applied input data will no longer be written to the device internal circuits. Subsequently, the corresponding input continues to be muted as long as that U/LDQM pin remains high. The LC382161 will revert to accepting input as soon as that pin is dropped to low and data will be written to the device. This input control operates independently on a byte basis with the UDQM pin controlling upper byte intput (pins DQ8 to DQ15) and the LDQM pin controlling the lower byte input (pins DQ0 to DQ7).
Since the U/LDQM pins control the device input buffers only, the write cycle continues internally and, in particular, incrementing of the internal burst counter continues.



A03636

Burst Read & Single Write

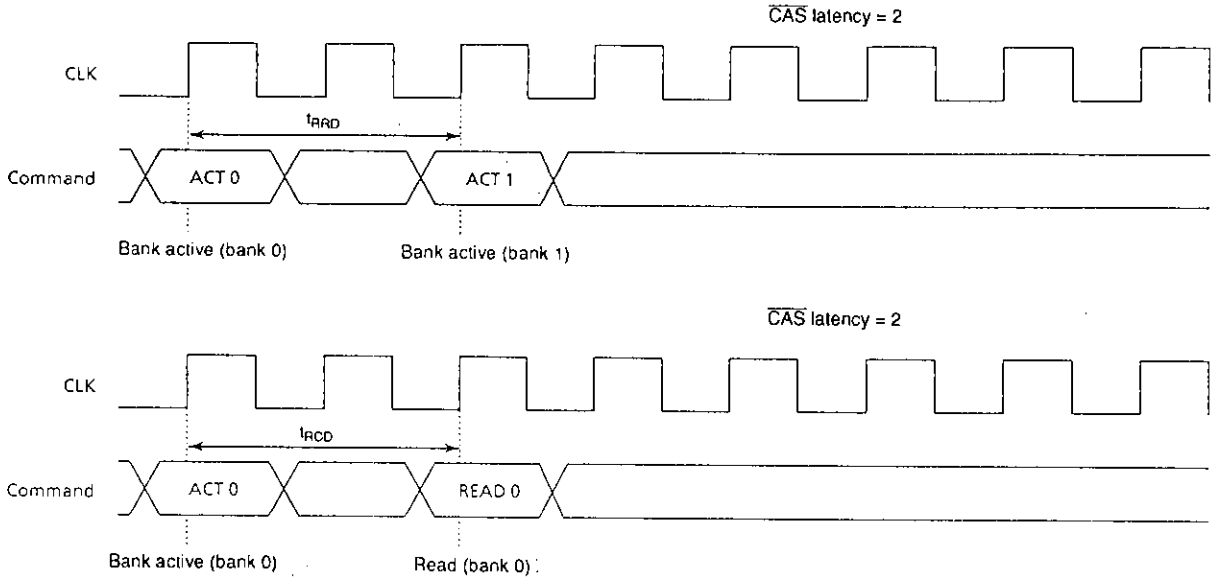
The burst read & single write command is set up using the mode register set command. During this operation, the burst read cycle operates normally but the write cycle only writes a single data item for each write cycle. The $\overline{CAS}$ latency and DQM latency are the same as in normal mode.



A03637

Bank Active Command Spacing

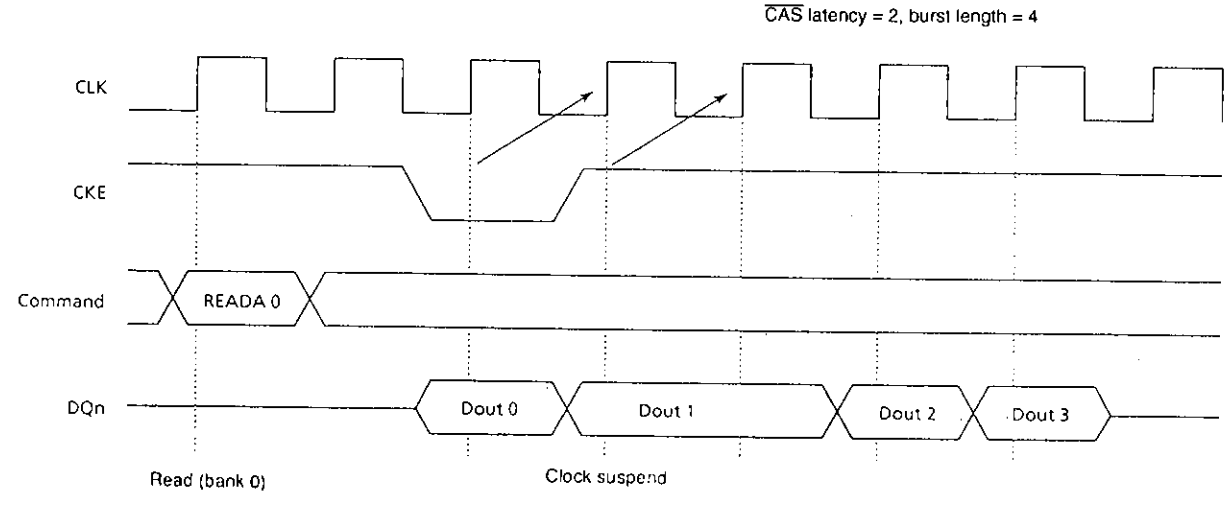
When the selected bank is precharged, the period t_{RP} has elapsed and the bank has entered the idle state, the bank can be activated by executing the active command. If the other bank is in the idle state at that time, the active command can be executed for that bank after the period t_{RRD} has elapsed. At that point both banks will be in the active state.
When a bank active command has been executed, a precharge command must be executed for that bank within the $\overline{RAS}$ cycle time ($t_{RAS\ max}$). Also note that a precharge command cannot be executed for an active bank before $t_{RAS\ min}$ has elapsed.
After a bank active command has been executed and the t_{RCD} period has elapsed, read and write (including auto-precharge) commands can be executed for that bank.



A03638

Clock Suspend

When the CKE pin is dropped from high to low during a read or write cycle, the LC382161T enters clock suspend mode on the next CLK rising edge. This command reduces the device power dissipation by stopping the device internal clock. Clock suspend mode continues as long as the CKE pin remains low. In this state, all inputs other than the CKE pin are invalid and no other commands can be executed. Also, the device internal states are maintained. When the CKE pin goes from low to high, clock suspend mode is terminated on the next CLK rising edge and device operation resumes. The next command cannot be executed until the recovery period (t_{CKA}) has elapsed.
Since this command differs from the self-refresh command described previously in that the refresh operation is not performed automatically internally, the refresh operation must be performed within the refresh period (t_{REF}). Thus the maximum time that clock suspend mode can be held is just under the refresh cycle time.

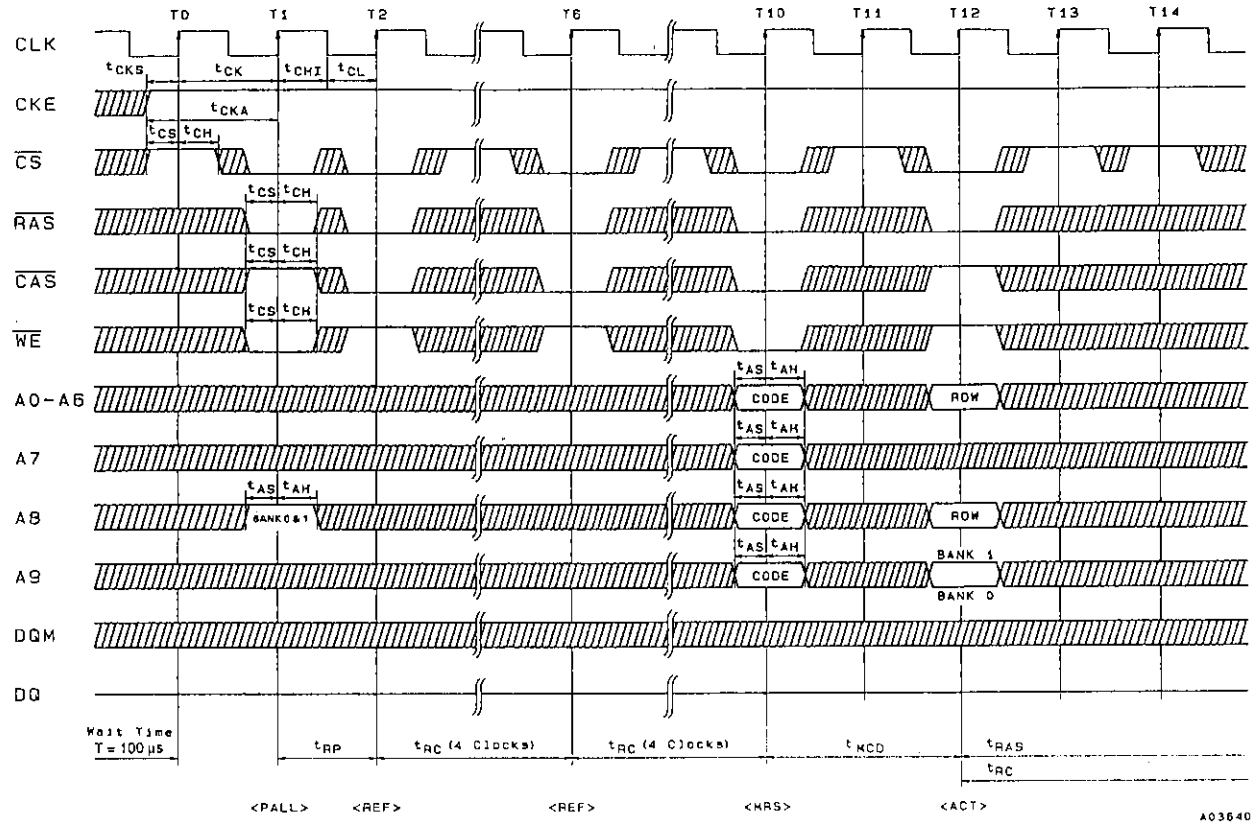


A03639

Operation Timing Examples

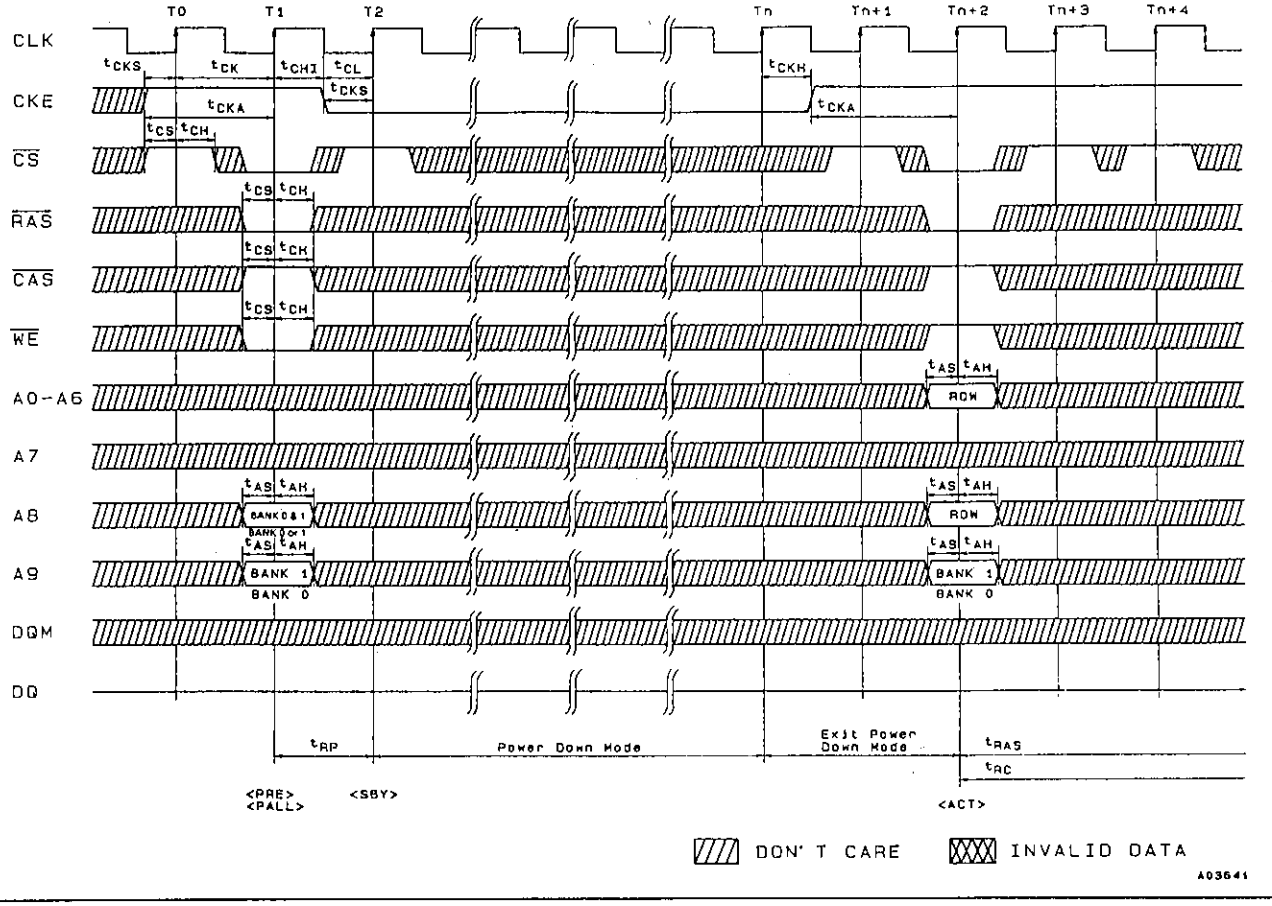
Power-On Sequence, Mode Register Set Cycle

$\overline{CAS}$ latency = 1



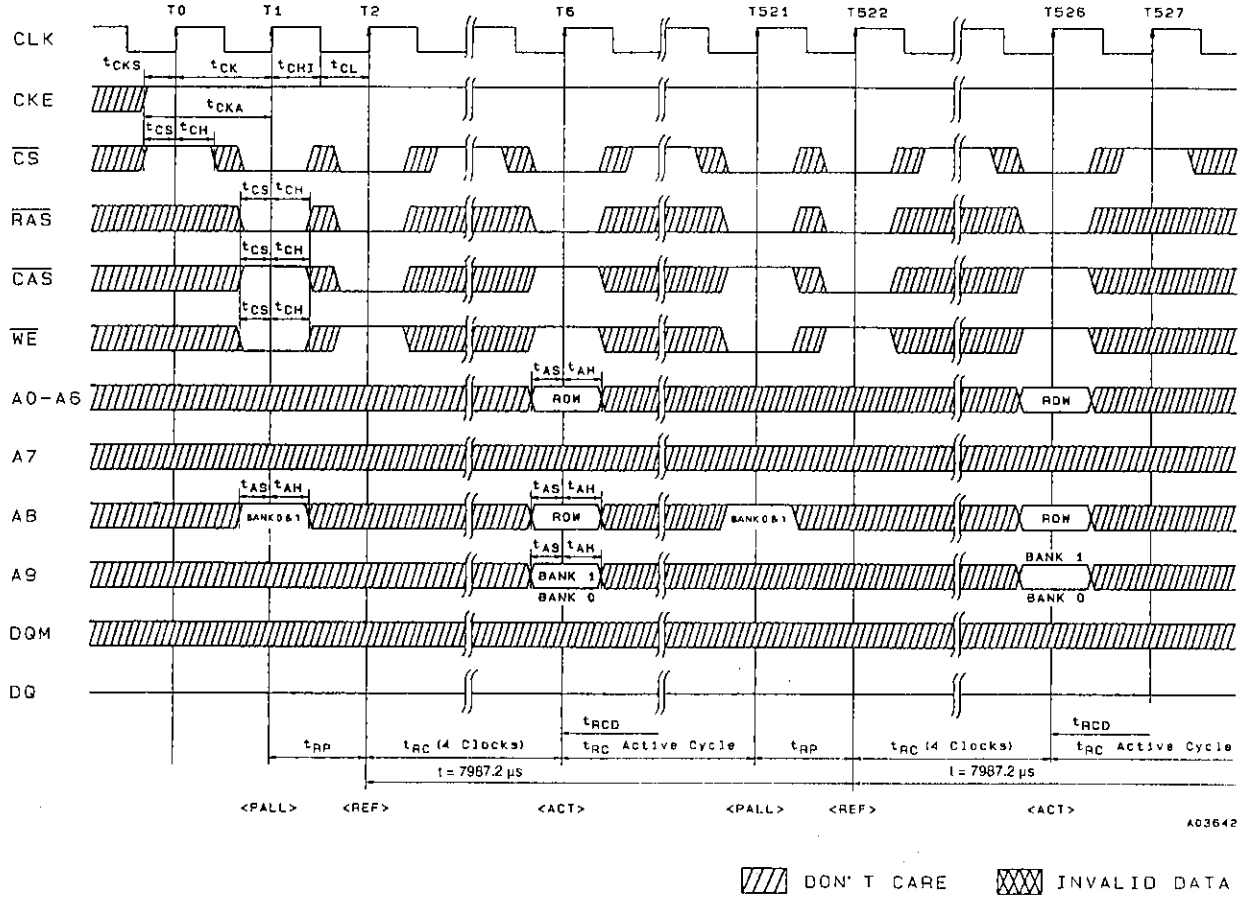
Power-Down Mode Cycle

$\overline{CAS}$ latency = 1



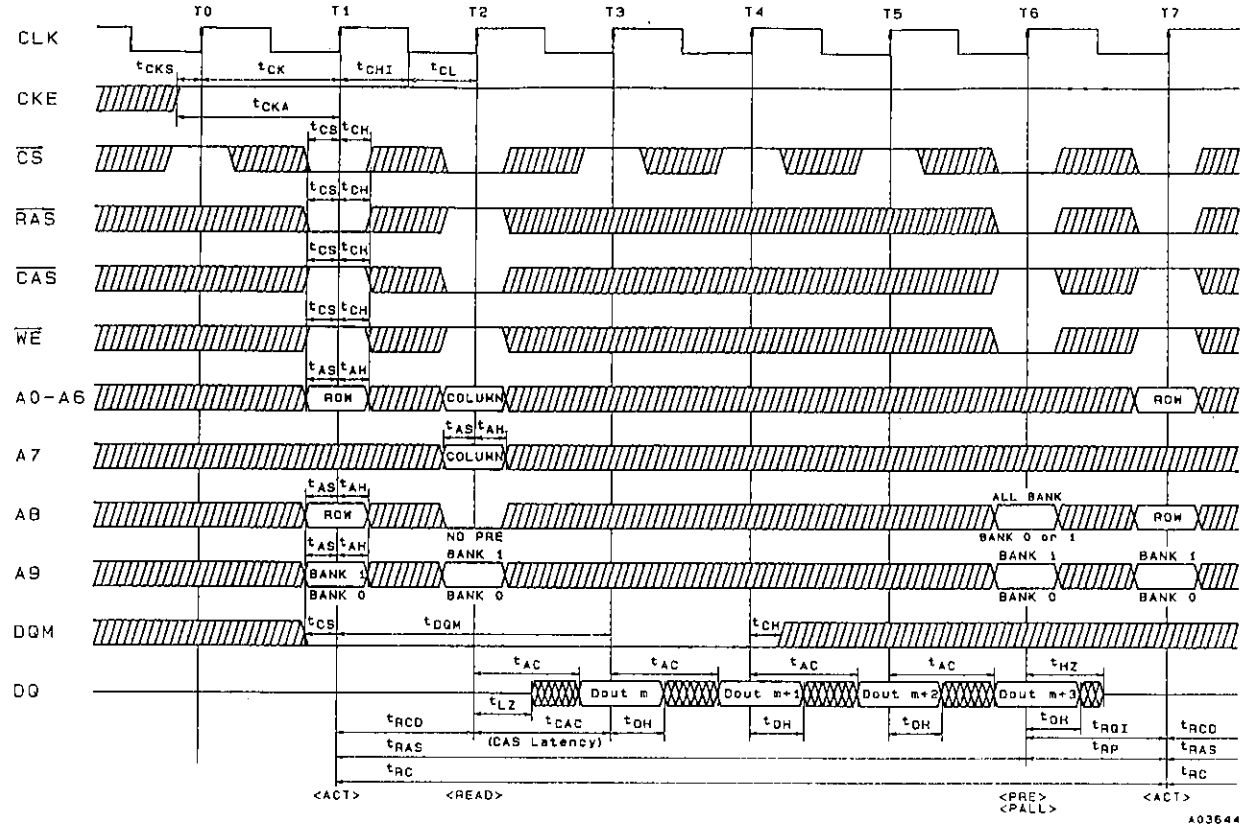
Auto-Refresh Cycle

$\overline{CAS}$ latency = 1



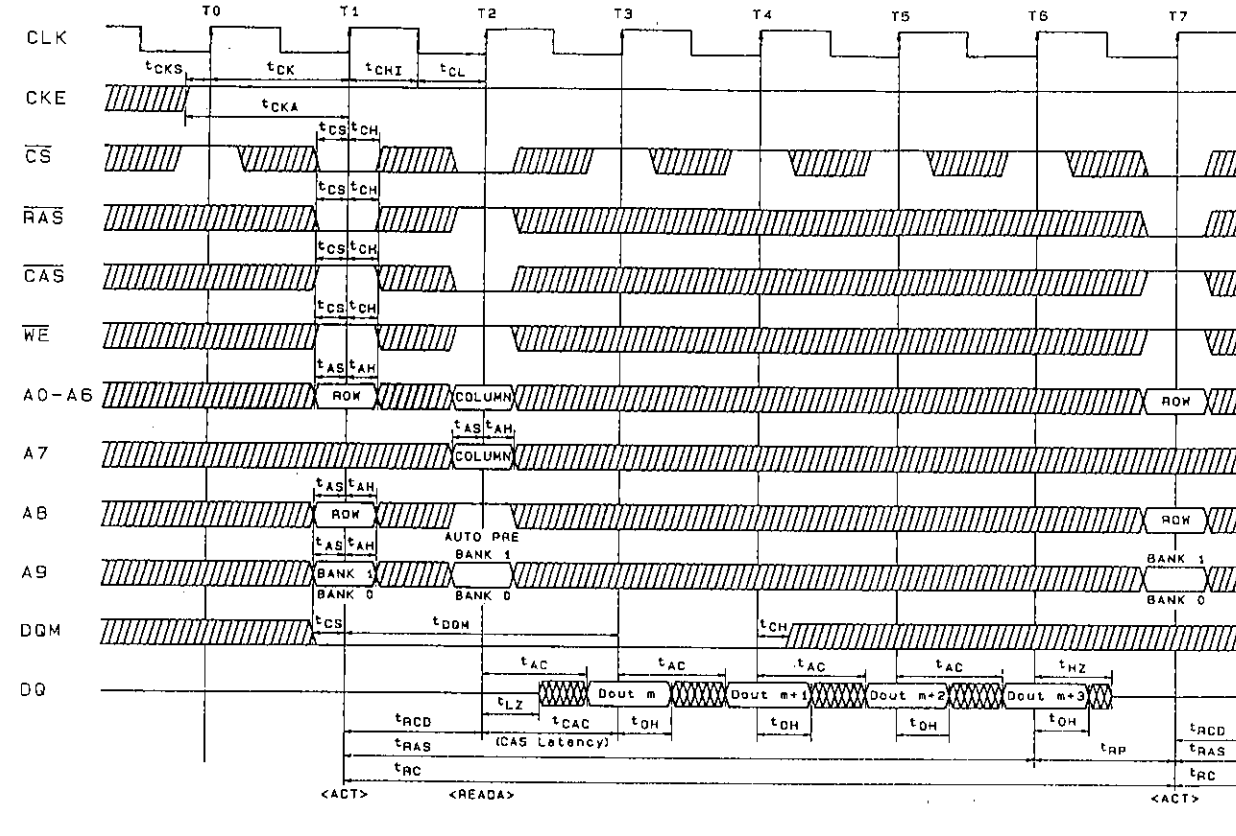
Read Cycle

$\overline{CAS}$ latency = 1, burst length = 4



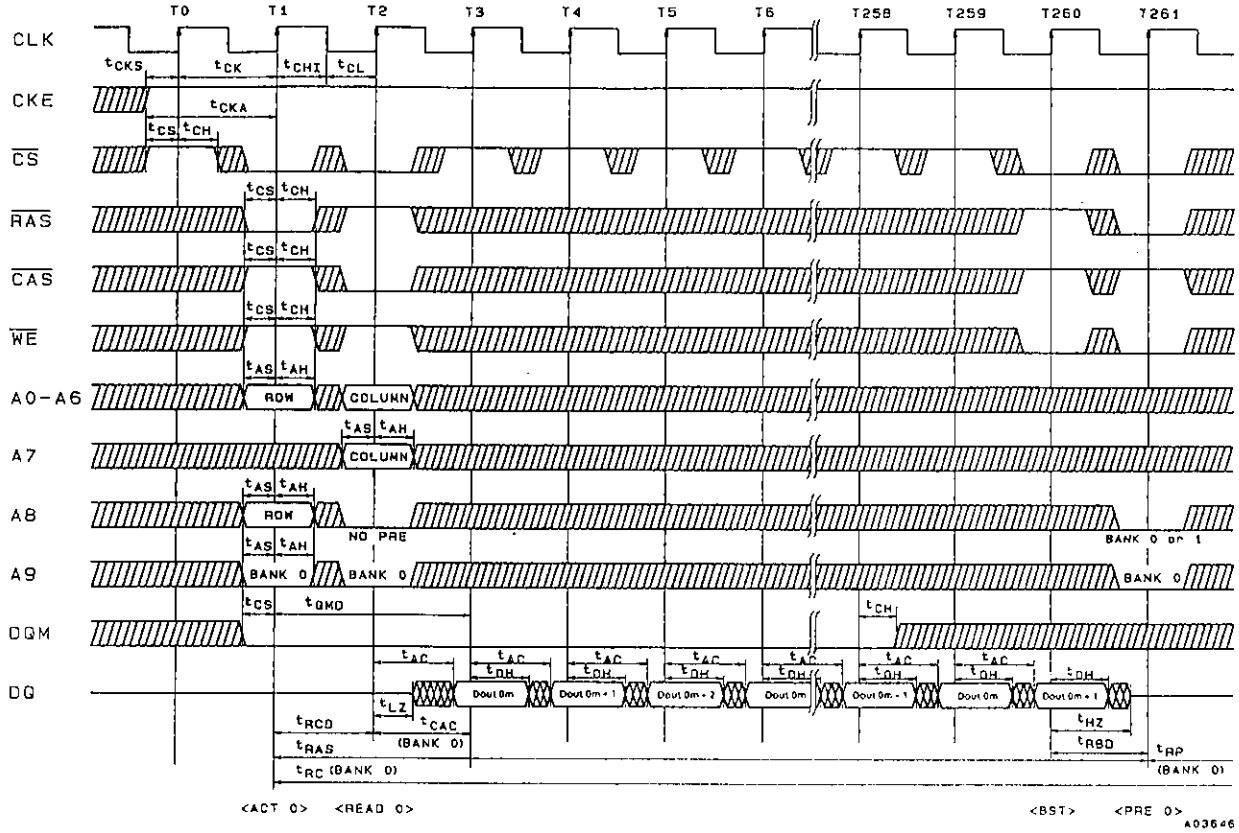
Read Cycle/Auto-Precharge

$\overline{CAS}$ latency = 1, burst length = 4



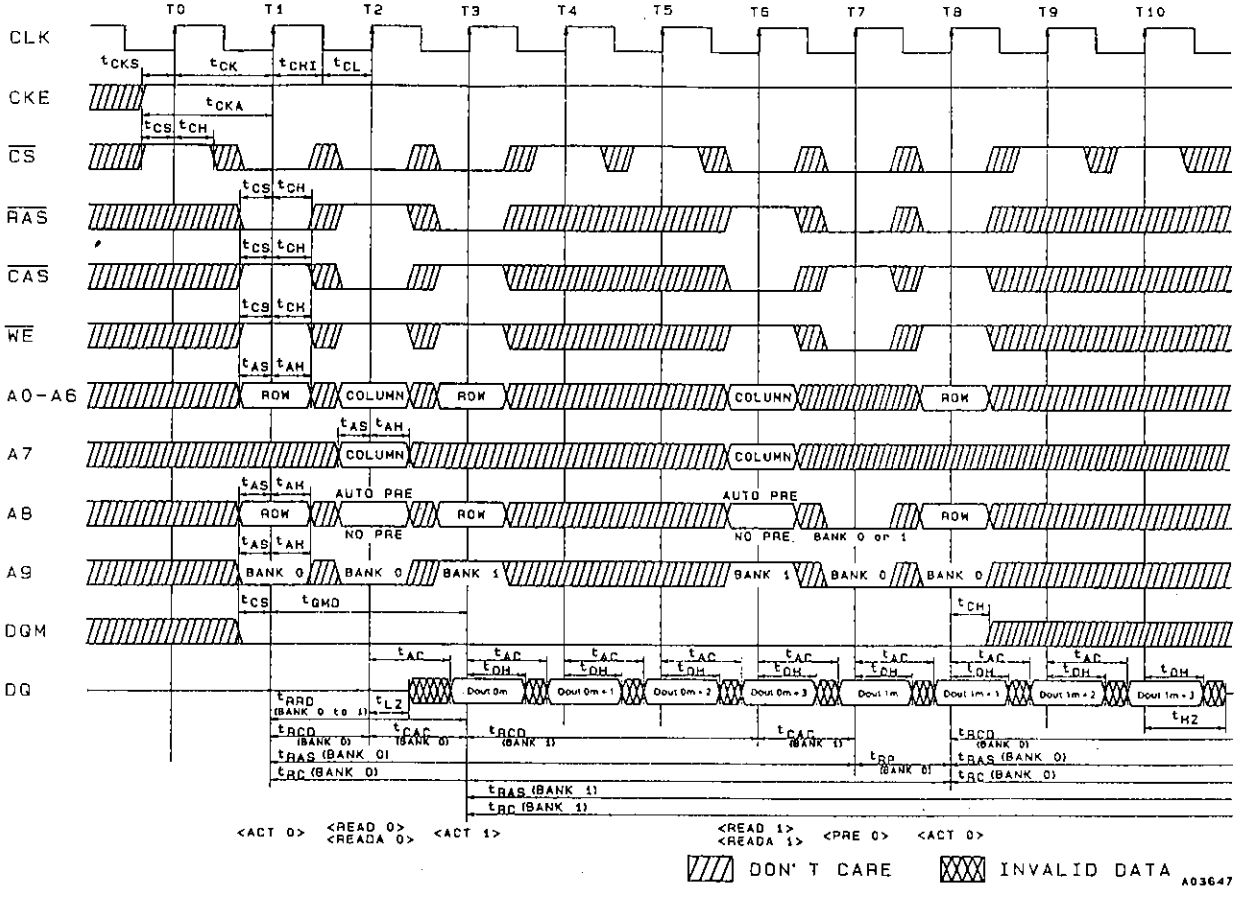
Read Cycle/Full Page

$\overline{CAS}$ latency = 1, burst length = full page



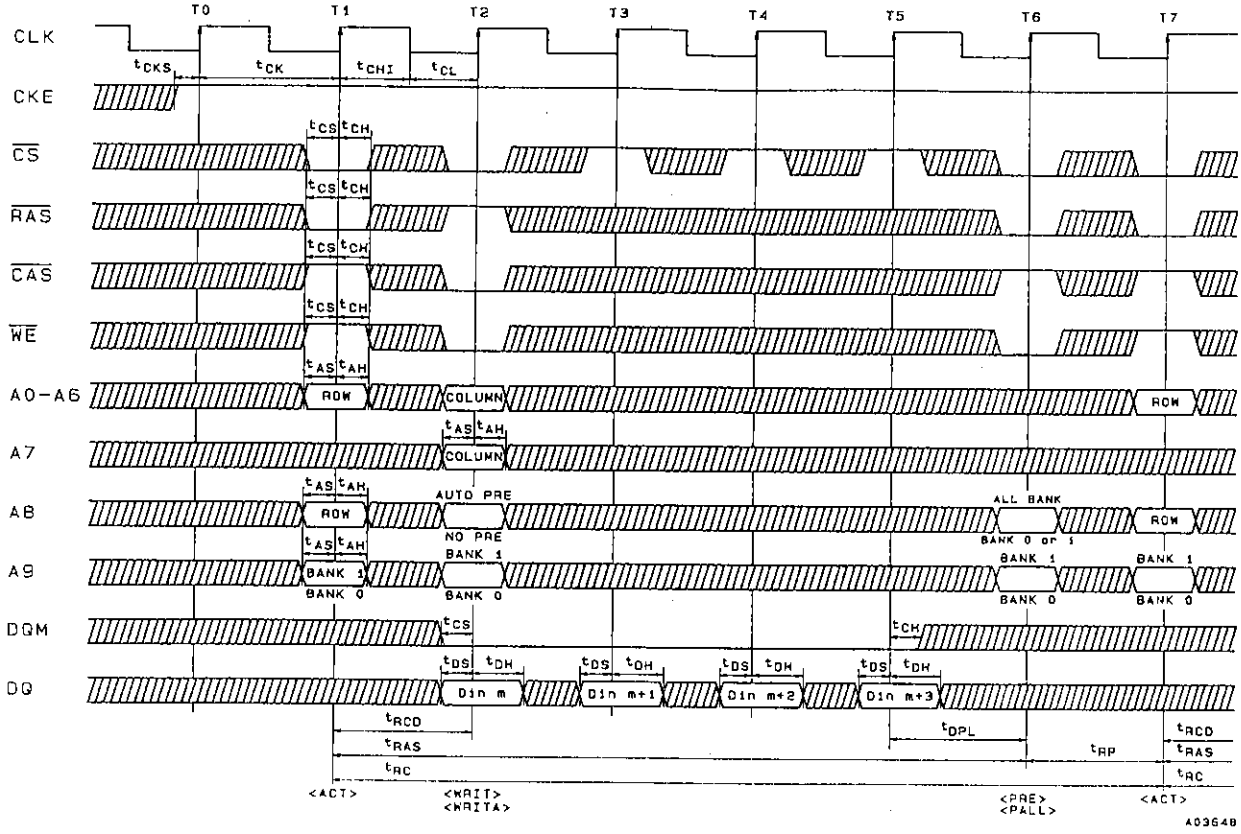
Read Cycle/Ping-Pong Operation (bank switching)

$\overline{CAS}$ latency = 1, burst length = 4



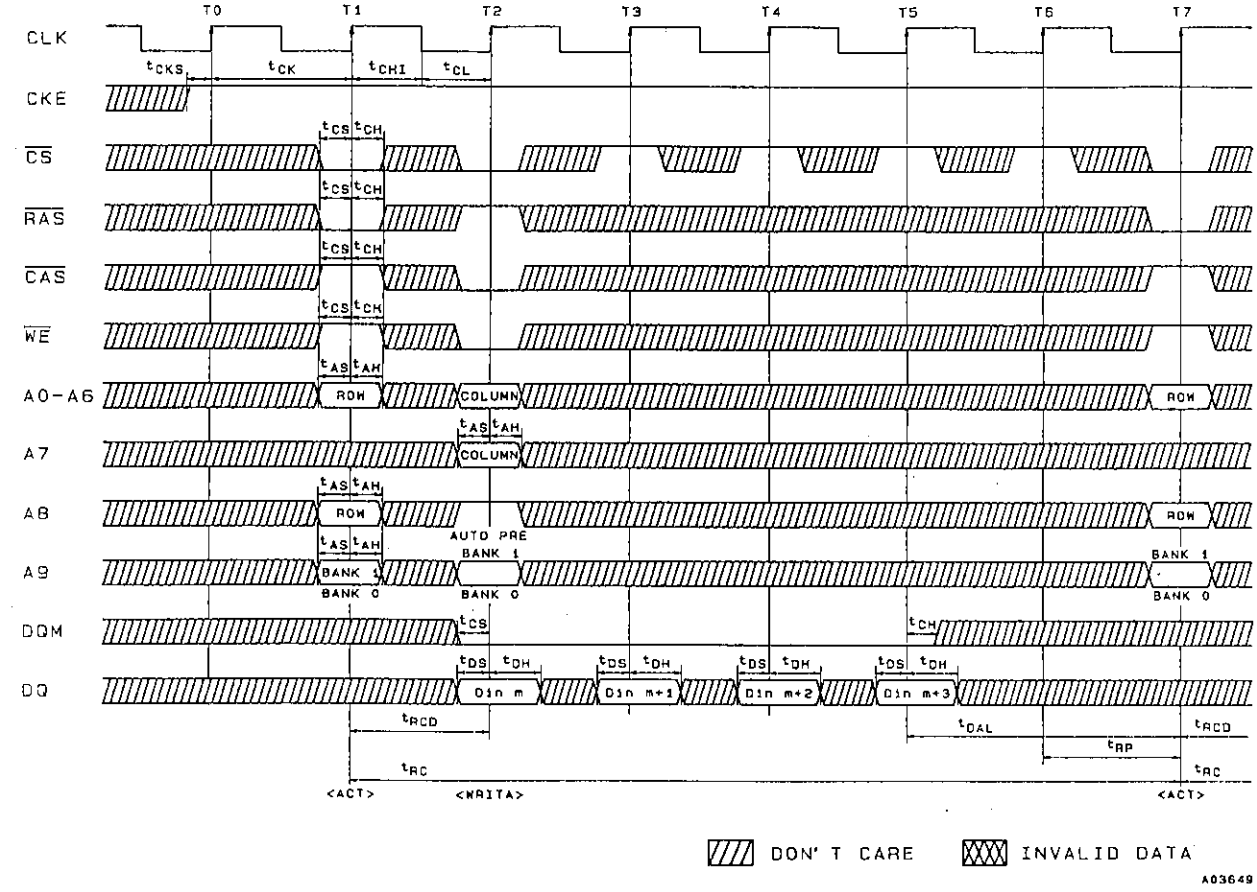
Write Cycle

$\overline{CAS}$ latency = 1, burst length = 4



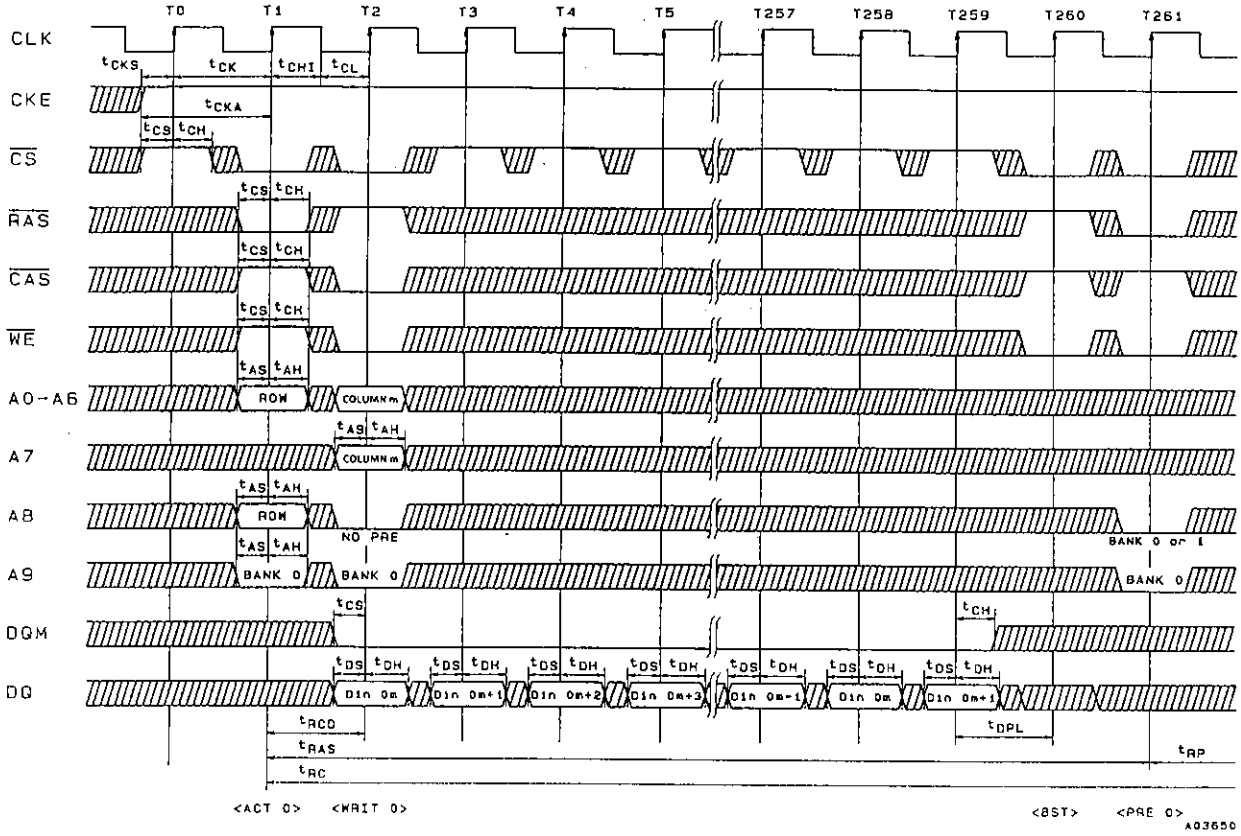
Write Cycle/Auto-Precharge

$\overline{CAS}$ latency = 1, burst length = 4



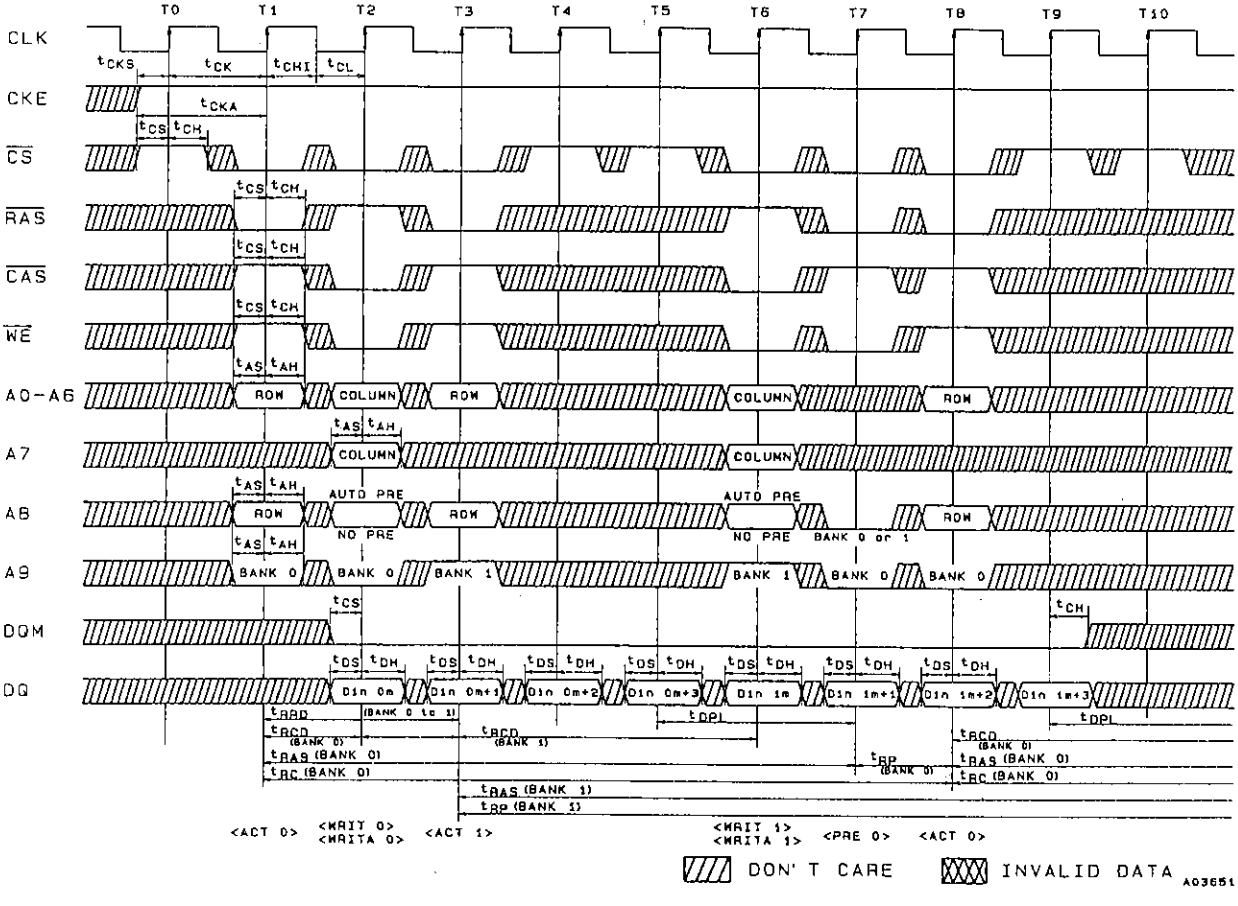
Write Cycle/Full Page

$\overline{CAS}$ latency = 1, burst length = full page



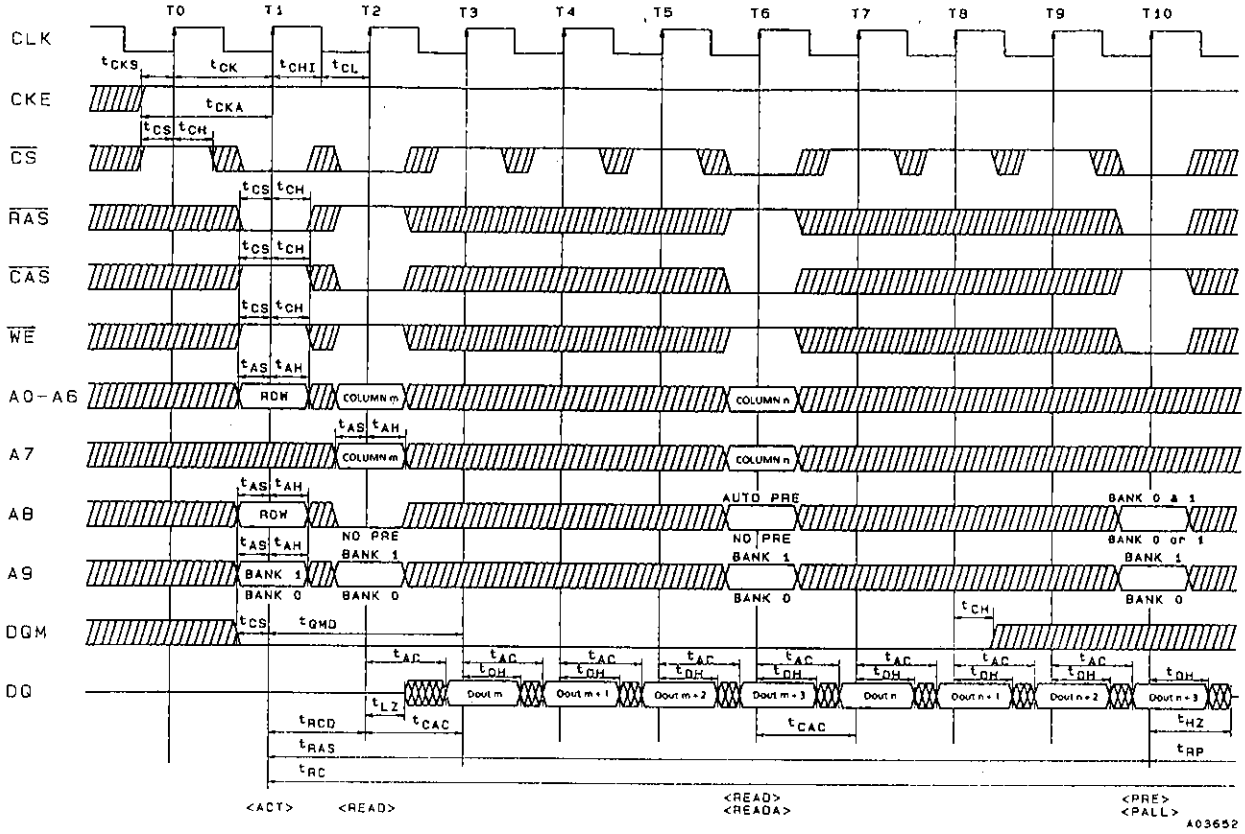
Write Cycle/Ping-Pong Operation (bank switching)

$\overline{CAS}$ latency = 1, burst length = 4



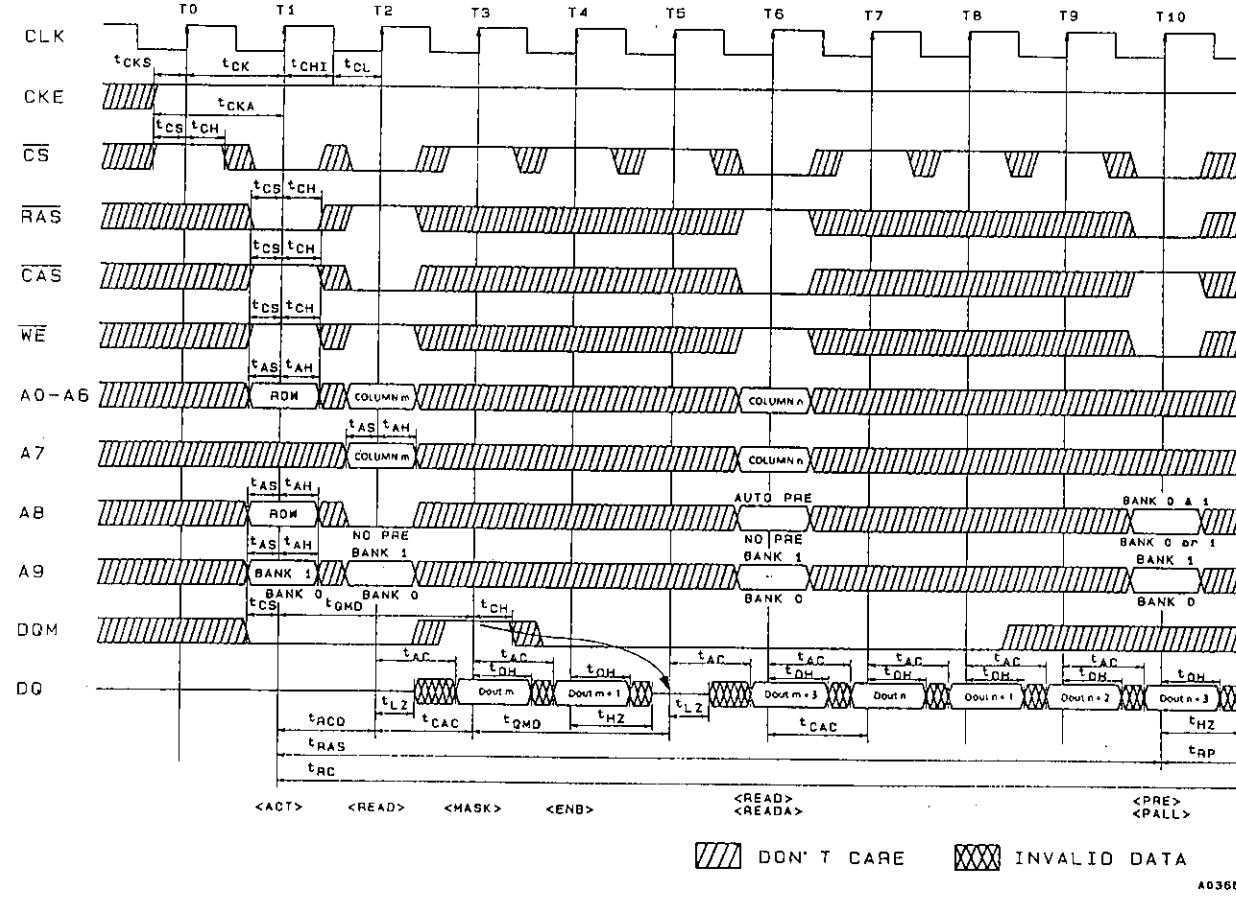
Read Cycle/Page Mode

$\overline{CAS}$ latency = 1, burst length = 4



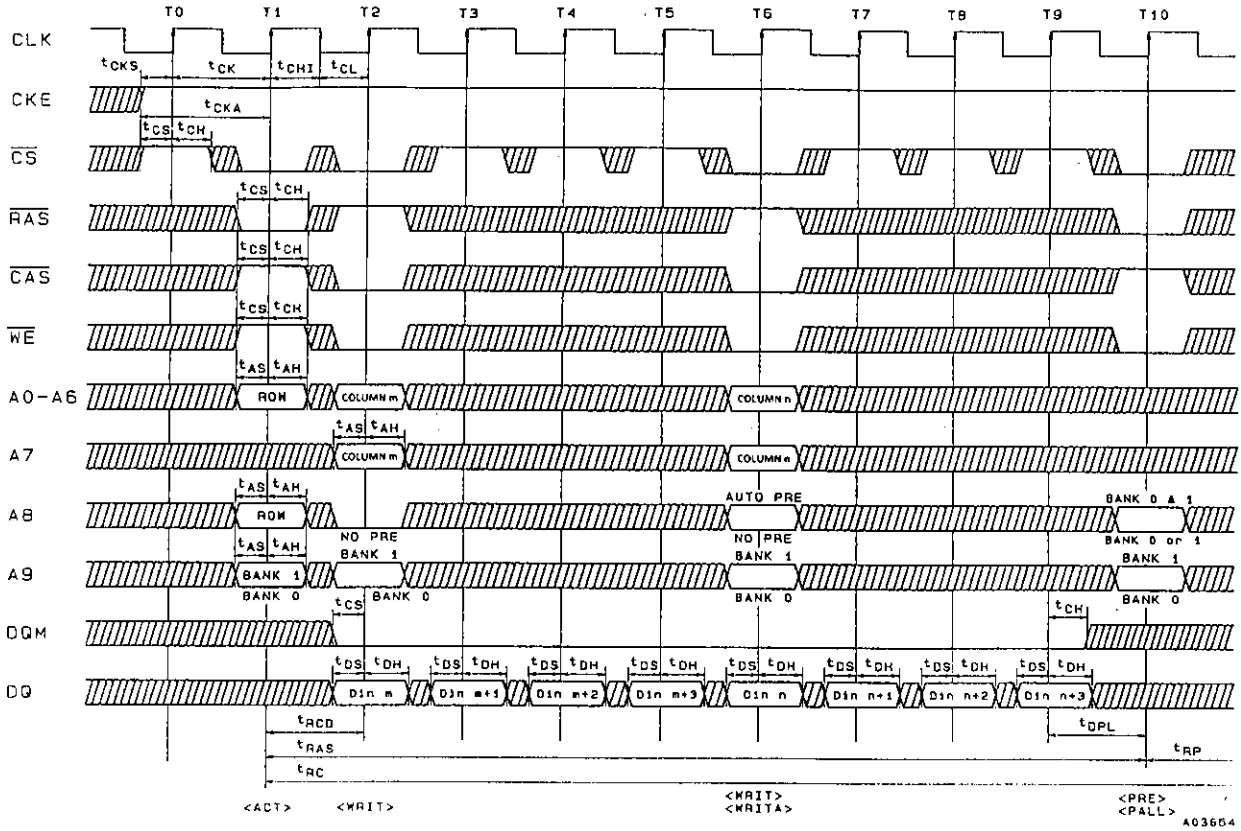
Read Cycle/Page Mode; Data Masking

$\overline{CAS}$ latency = 1, burst length = 4



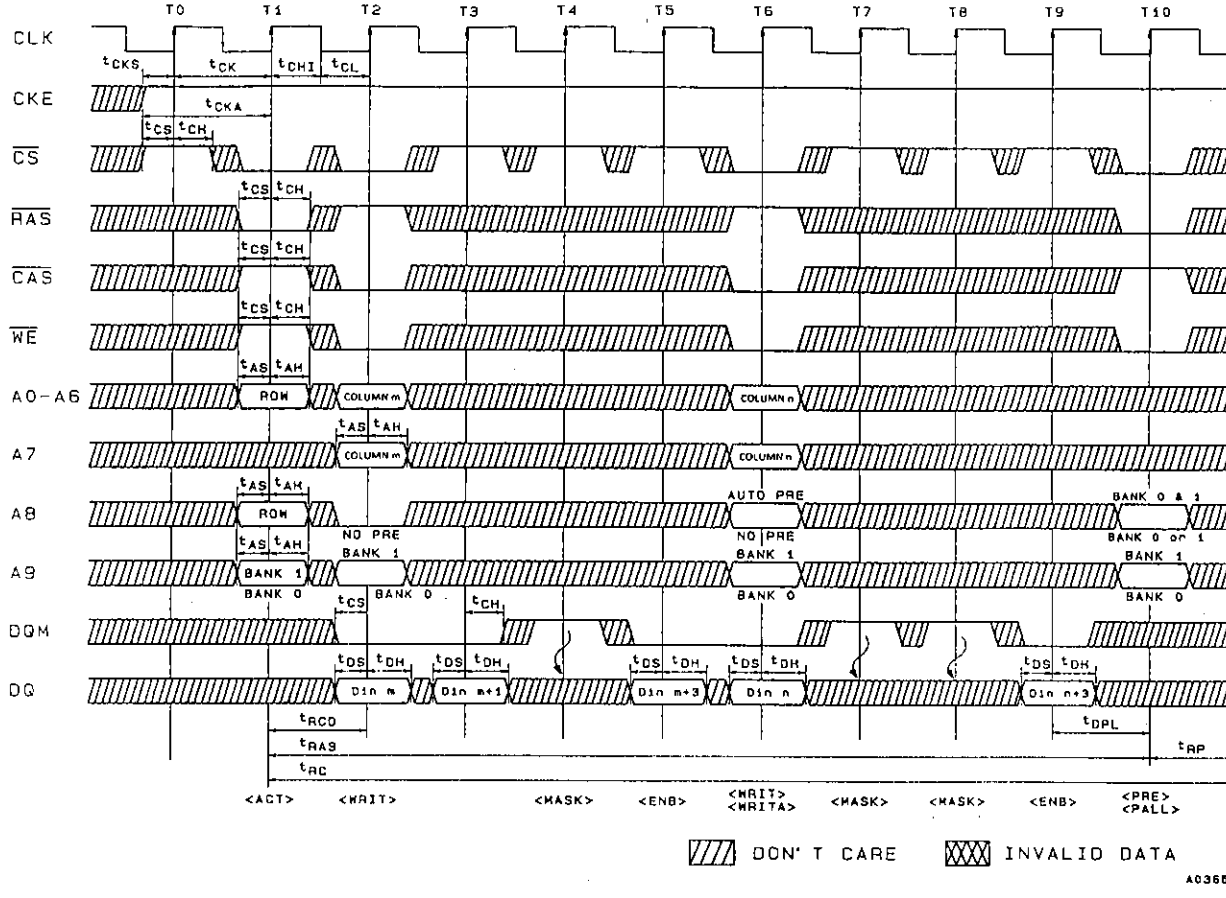
Write Cycle/Page Mode

$\overline{CAS}$ latency = 1, burst length = 4



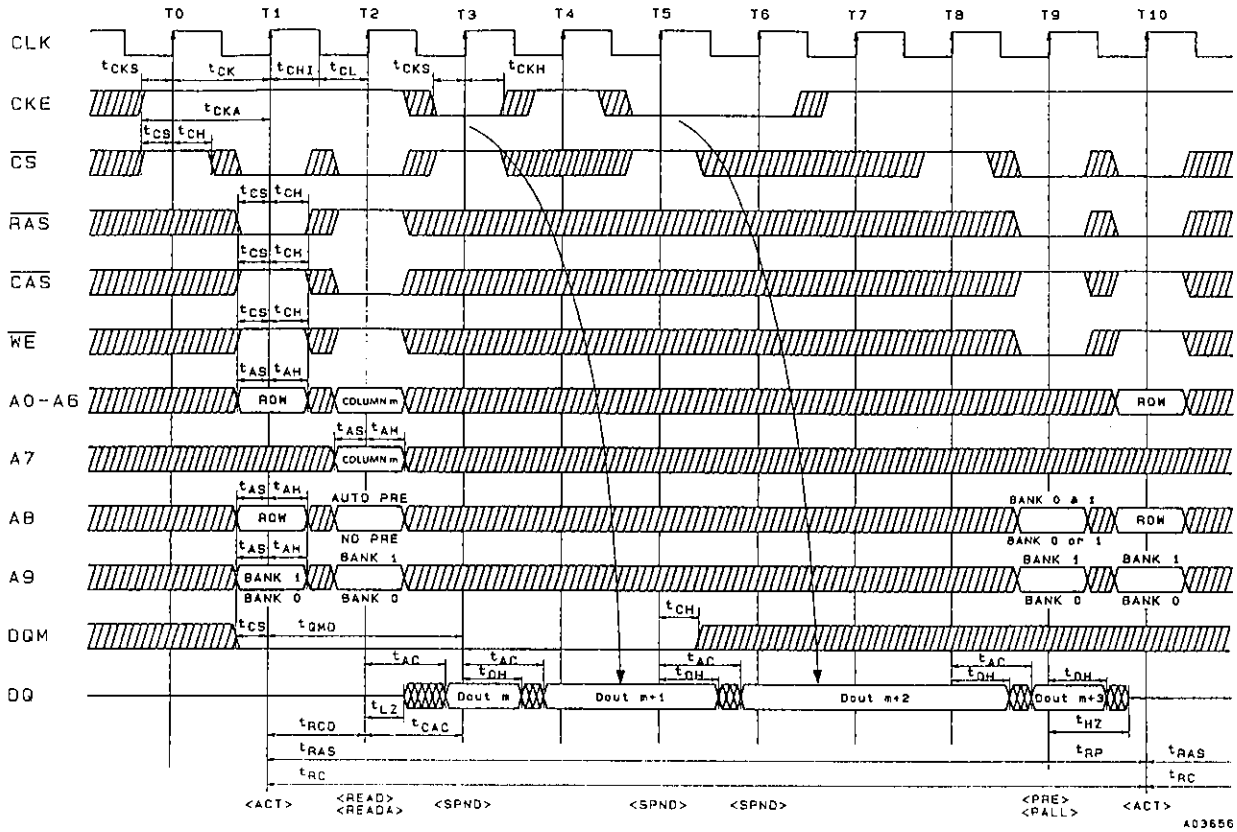
Write Cycle/Page Mode; Data Masking

$\overline{CAS}$ latency = 1, burst length = 4



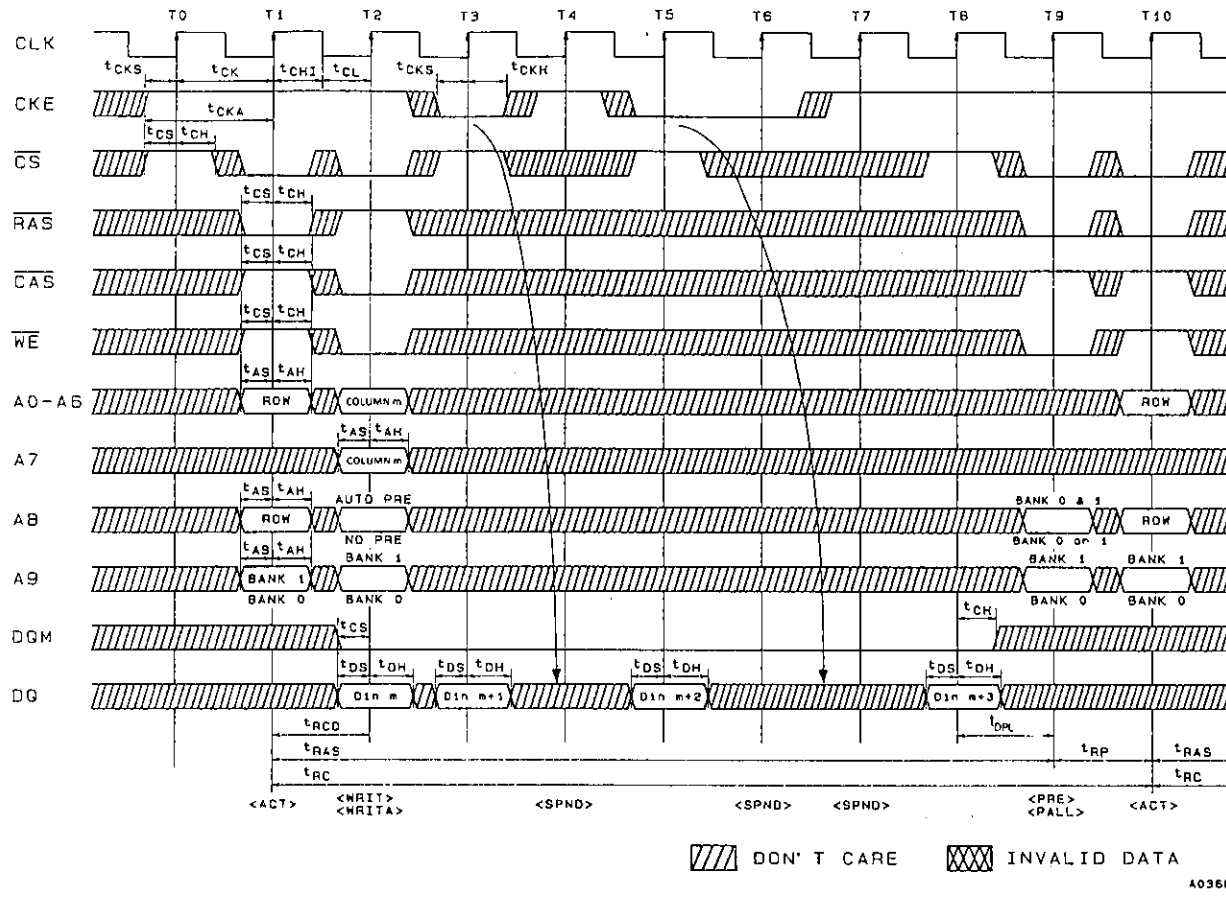
Read Cycle/Clock Suspend

$\overline{CAS}$ latency = 1, burst length = 4



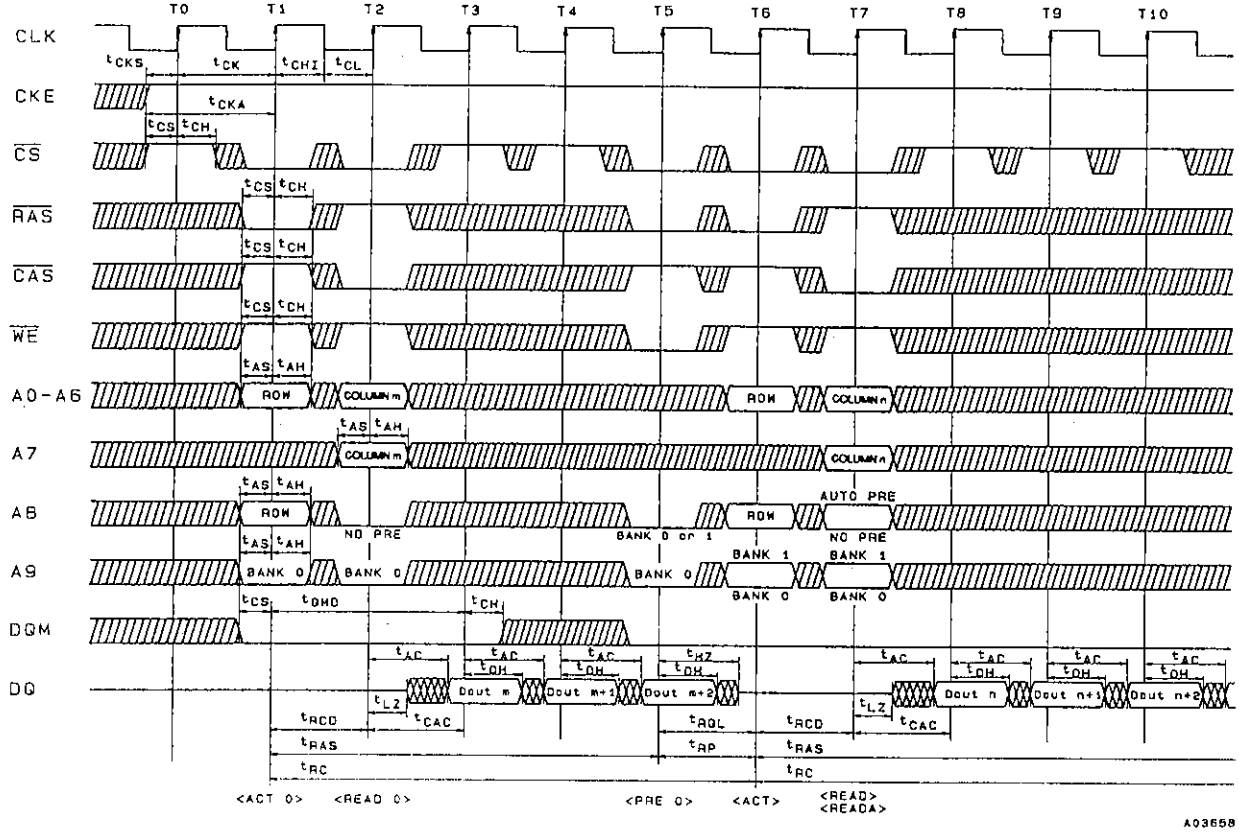
Write Cycle/Clock Suspend

$\overline{CAS}$ latency = 1, burst length = 4



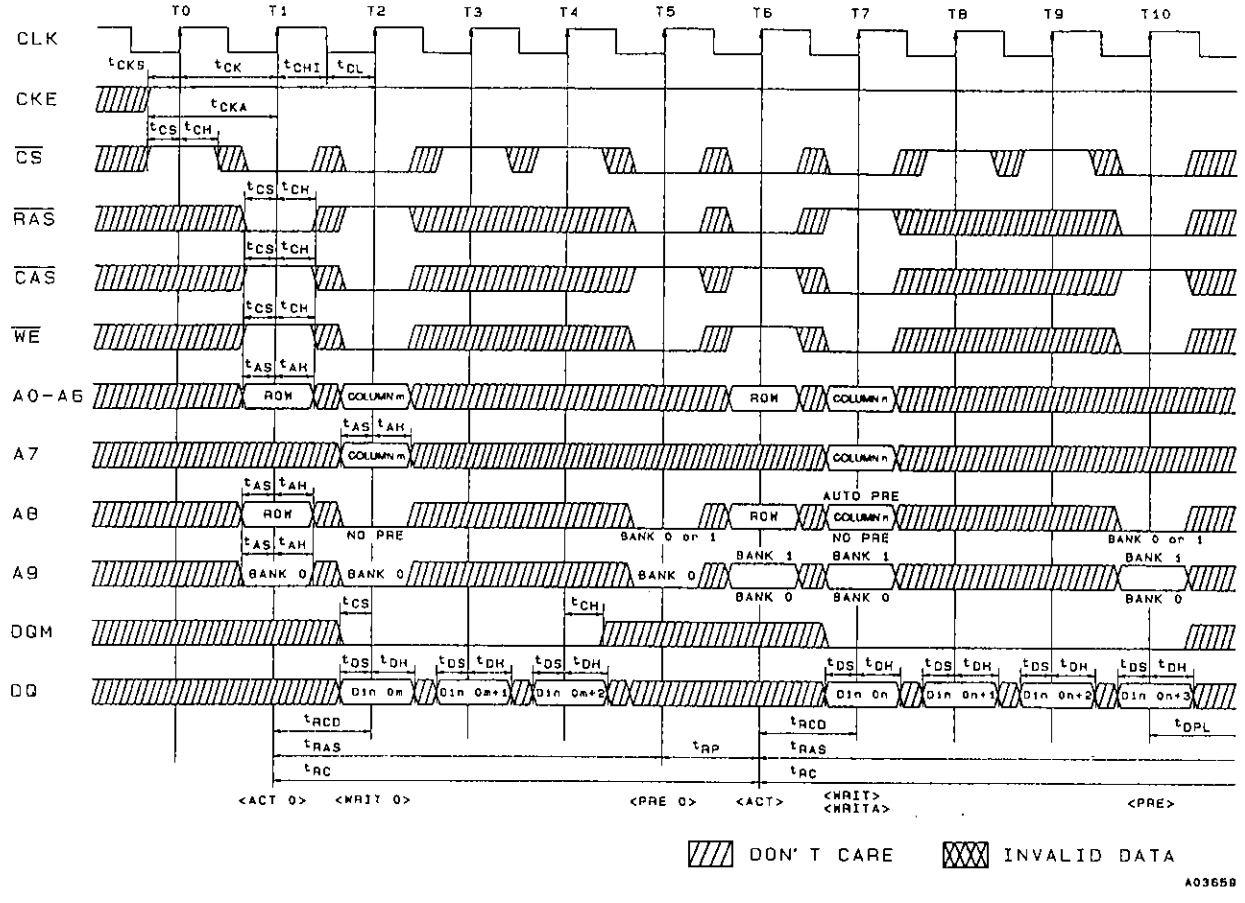
Read Cycle/Precharge Termination

$\overline{CAS}$ latency = 1, burst length = 4



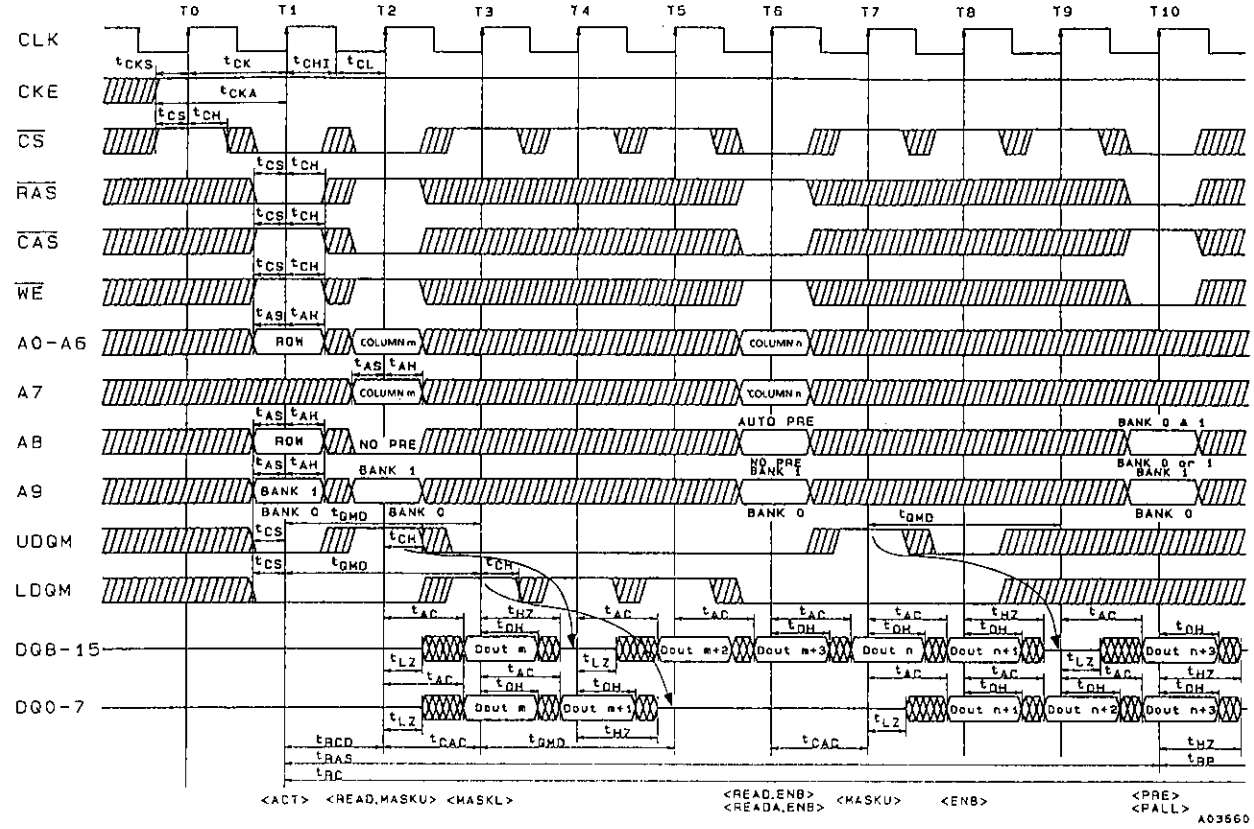
Write Cycle/Precharge Termination

$\overline{CAS}$ latency = 1, burst length = 4



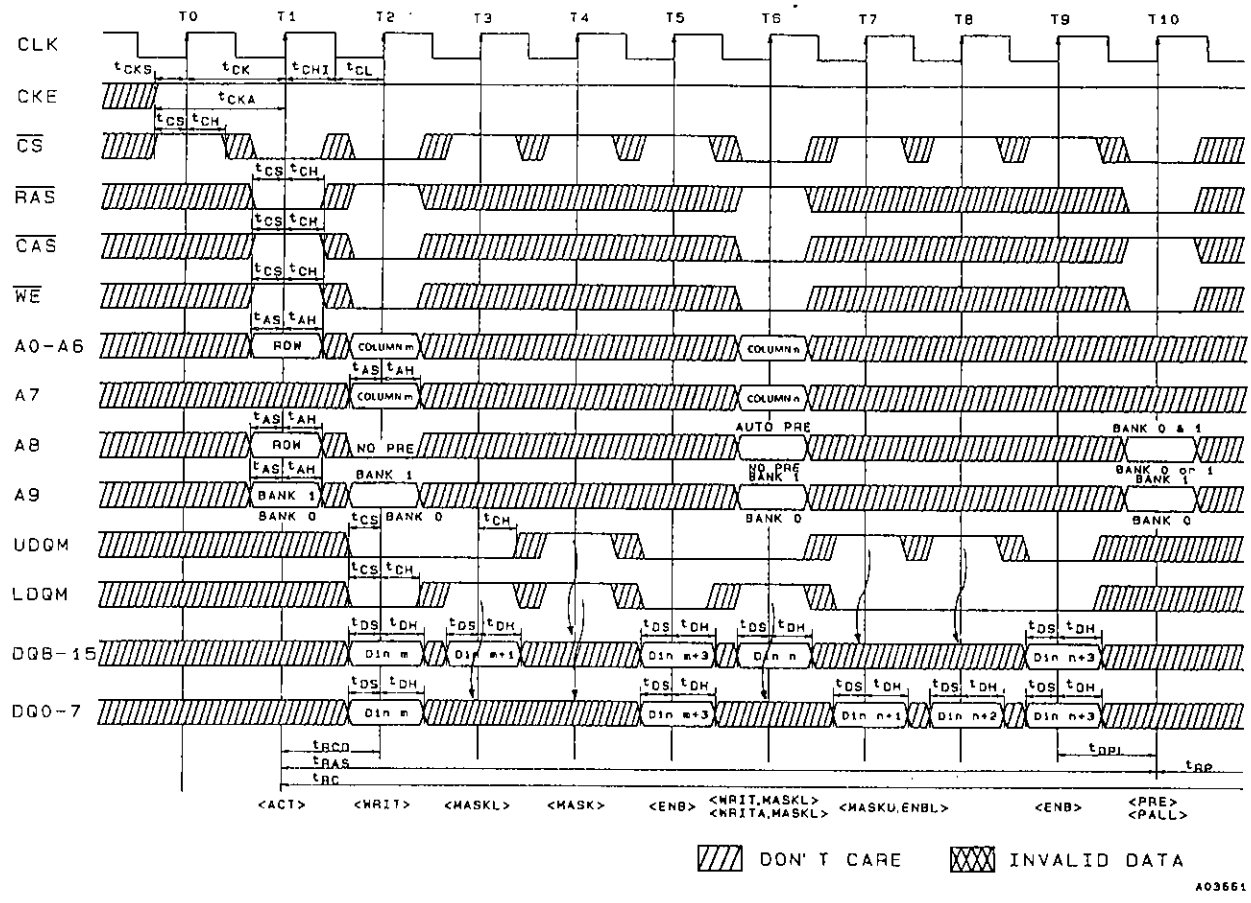
Read Cycle/Byte Operation

$\overline{CAS}$ latency = 1, burst length = 4



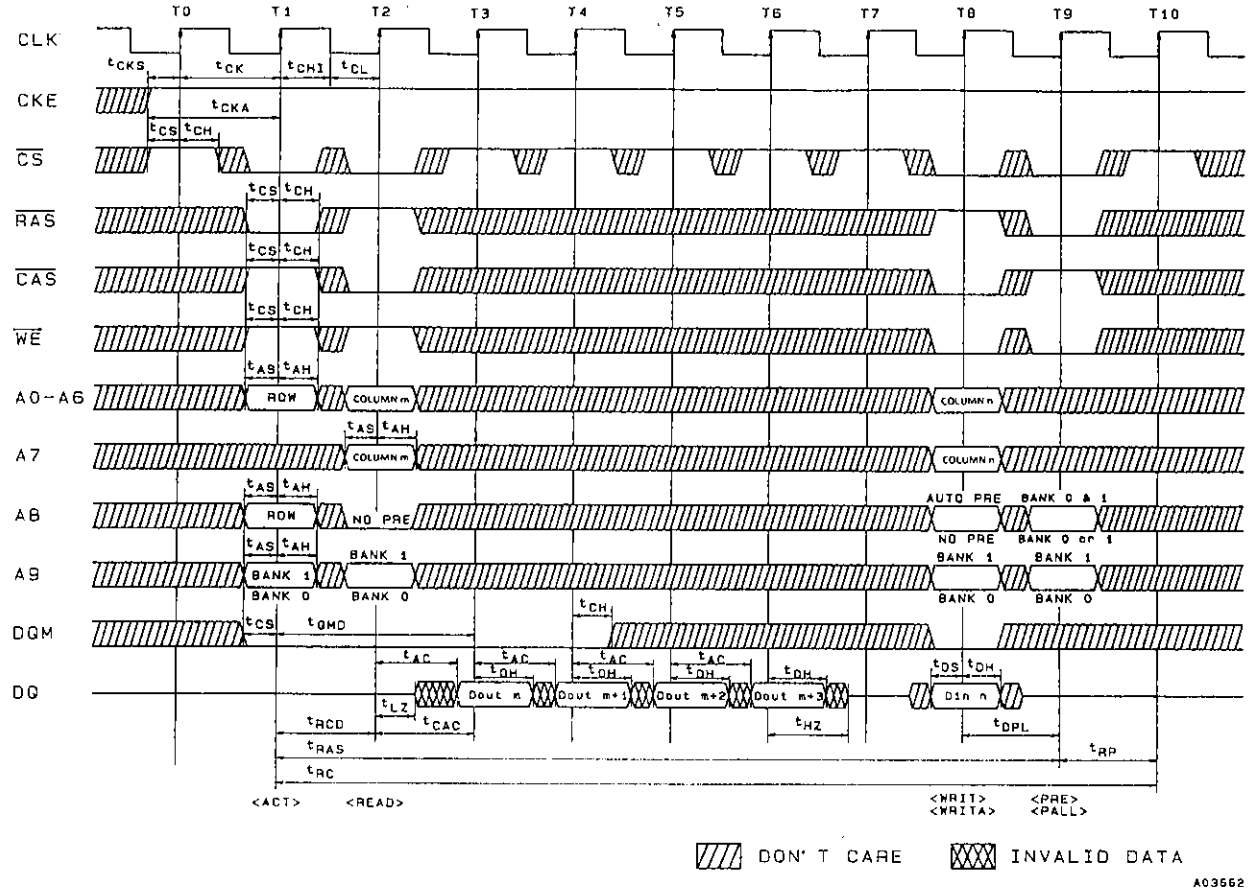
Write Cycle/Byte Operation

$\overline{CAS}$ latency = 1, burst length = 4



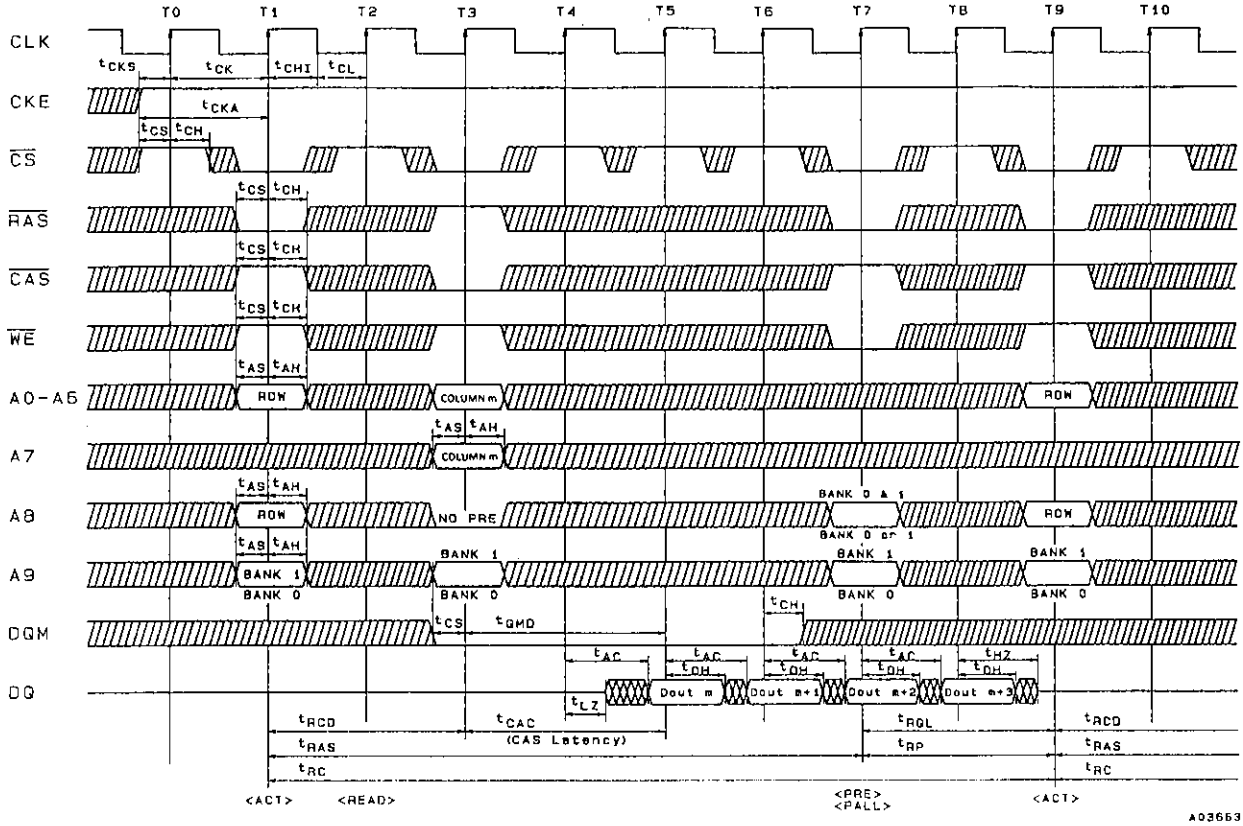
Read Cycle, Write Cycle/Burst Read, Single Write

$\overline{CAS}$ latency = 1, burst length = 4



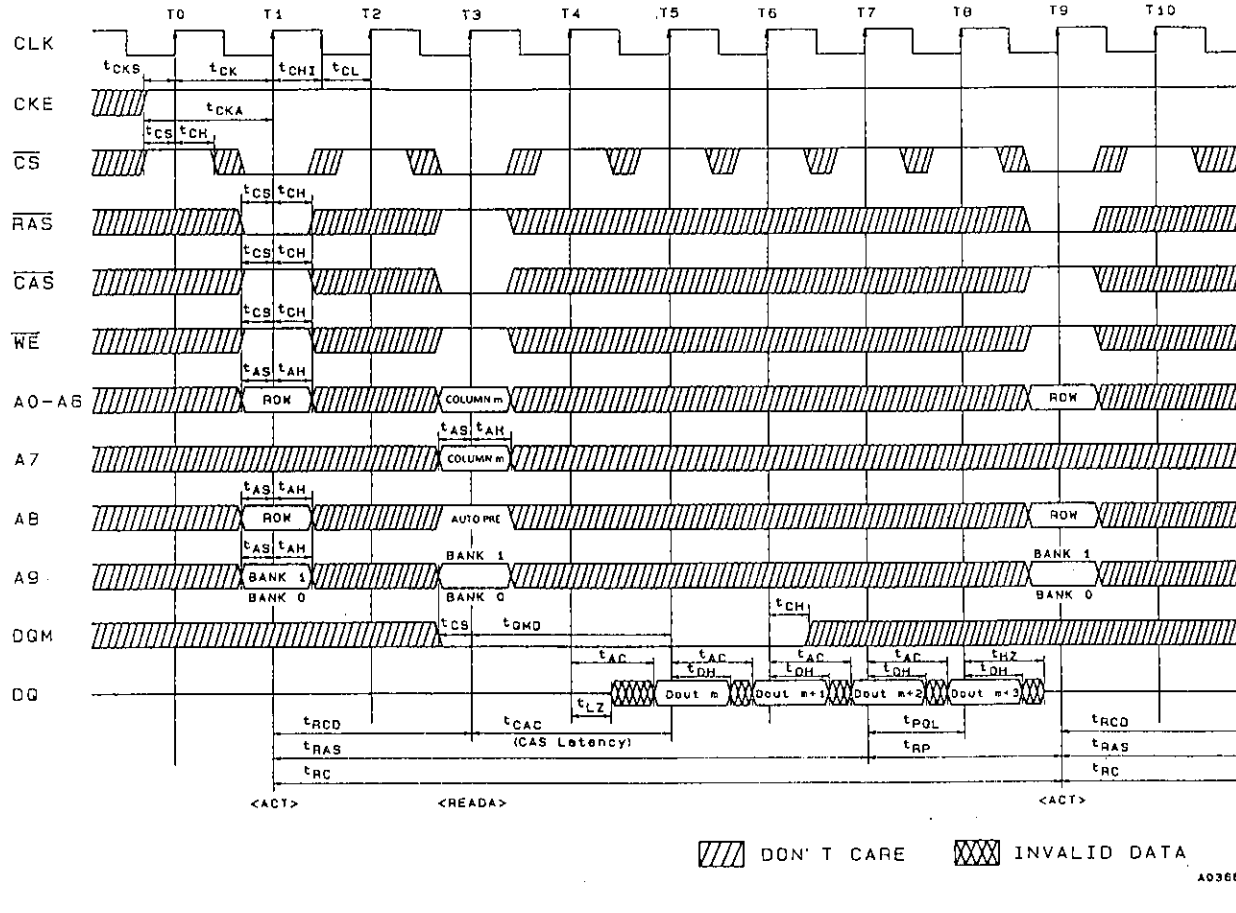
Read Cycle

$\overline{CAS}$ latency = 2, burst length = 4



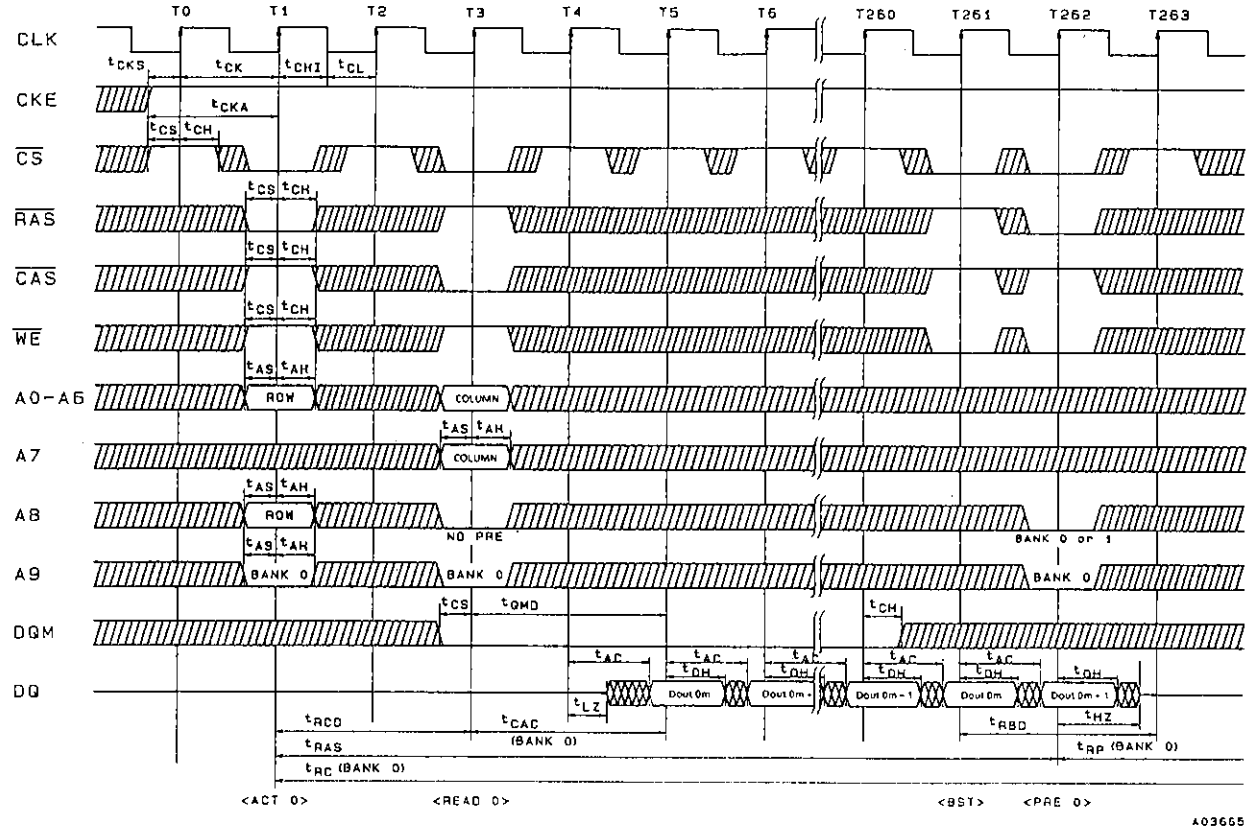
Read Cycle/Auto-Precharge

$\overline{CAS}$ latency = 2, burst length = 4



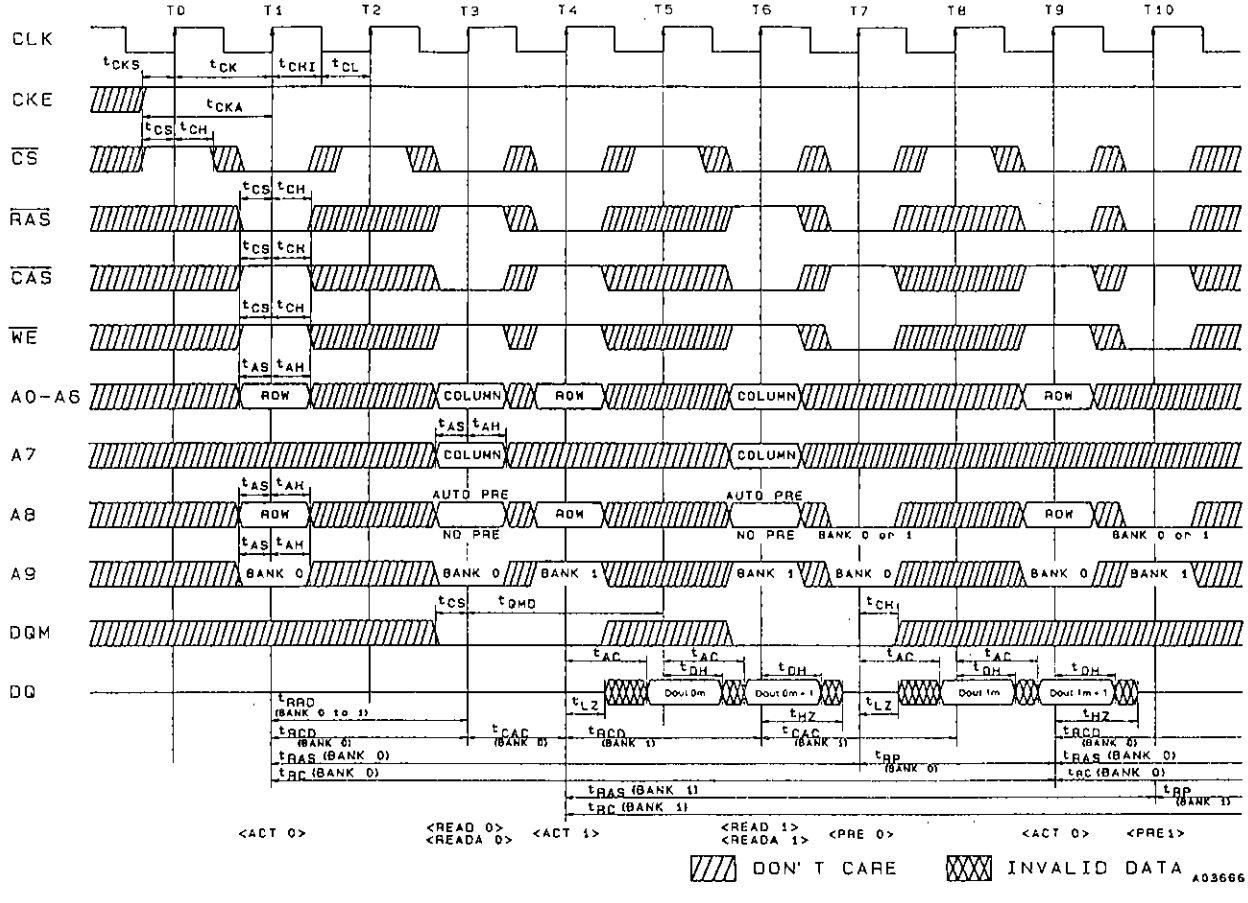
Read Cycle/Full Page

$\overline{CAS}$ latency = 2, burst length = full page



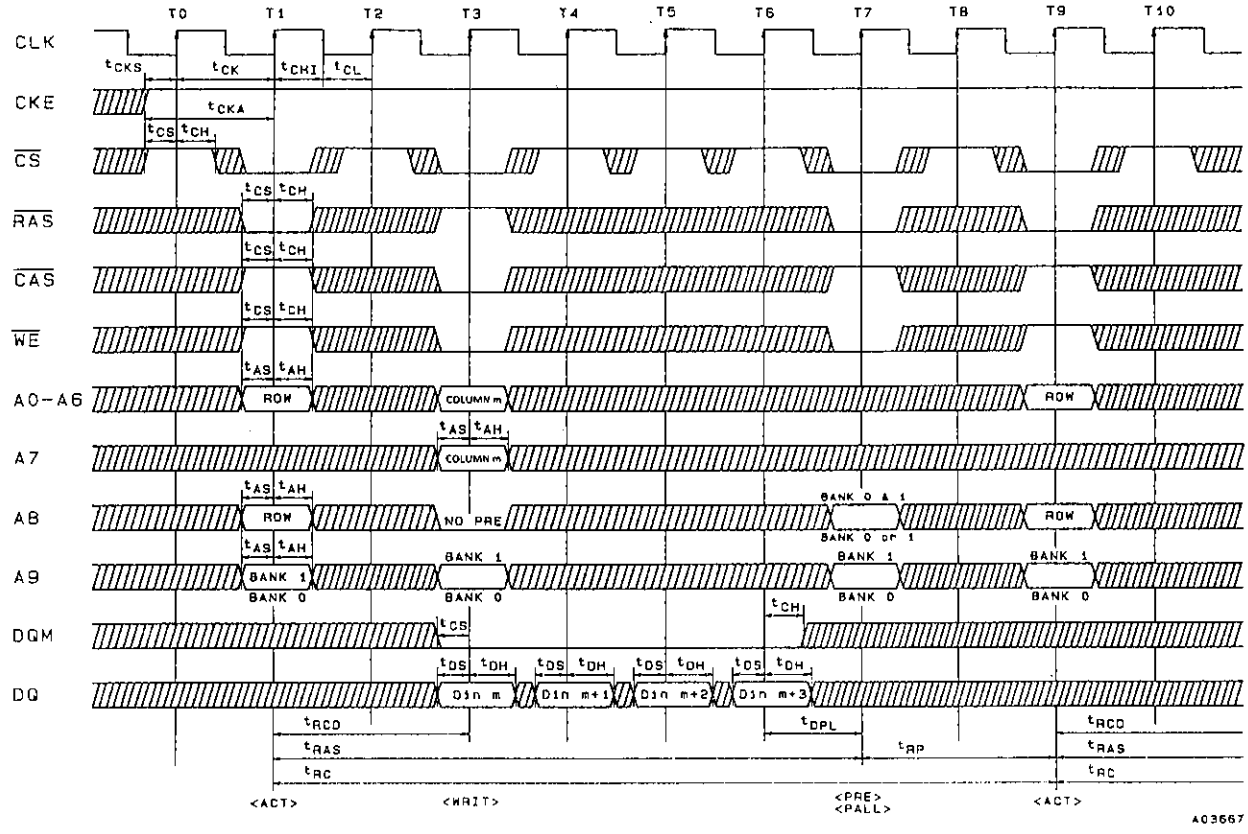
Read Cycle/Ping-Pong Operation (bank switching)

$\overline{CAS}$ latency = 2, burst length = 4



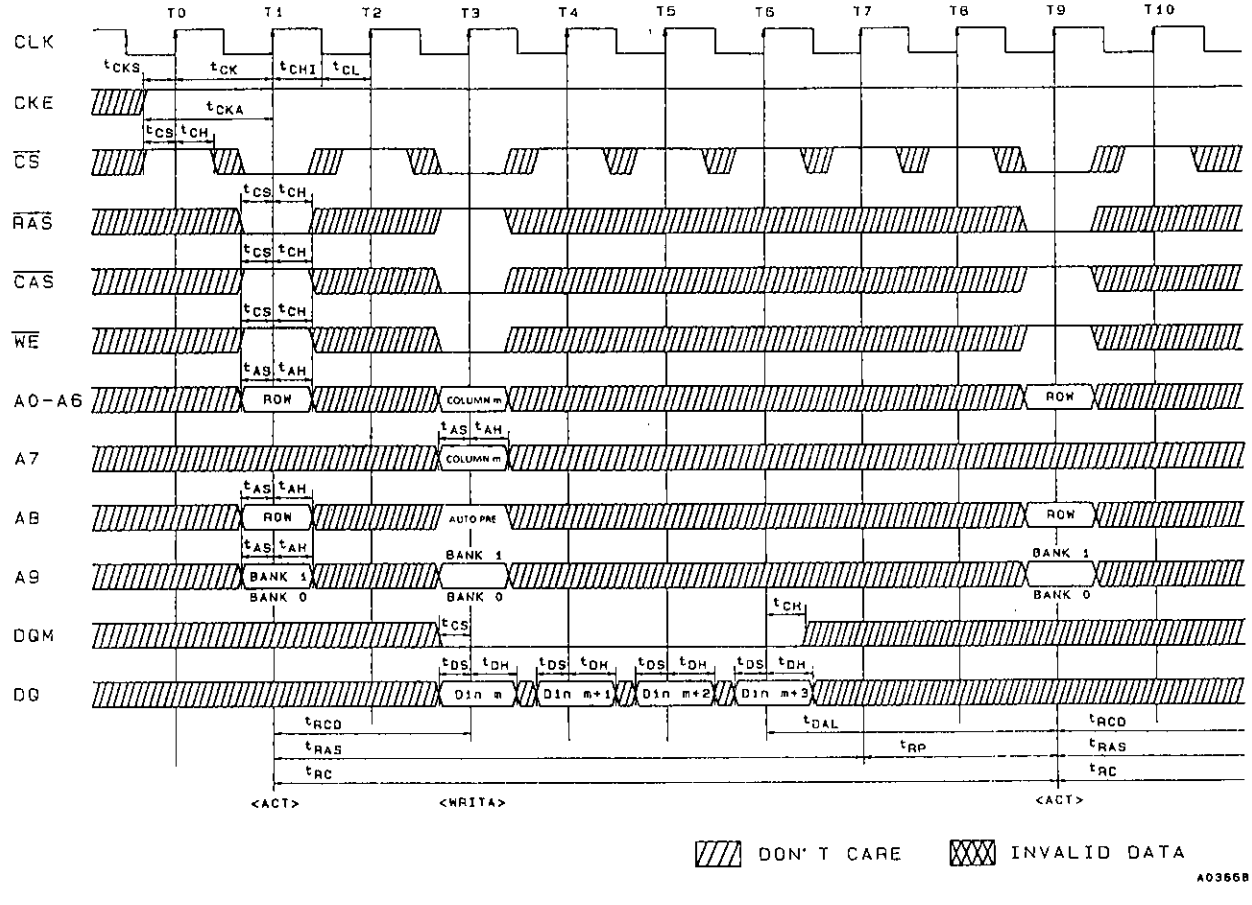
Write Cycle

$\overline{CAS}$ latency = 2, burst length = 4



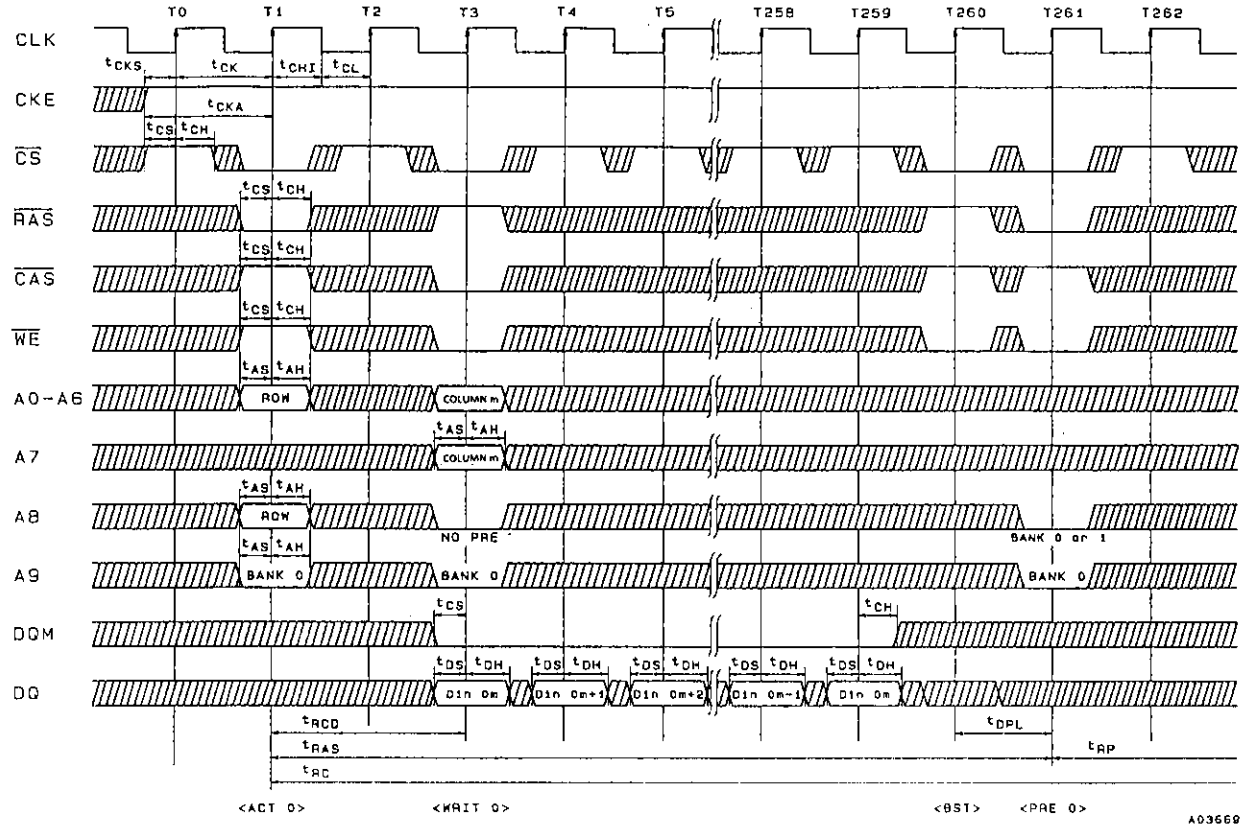
Write Cycle/Auto-Precharge

$\overline{CAS}$ latency = 2, burst length = 4



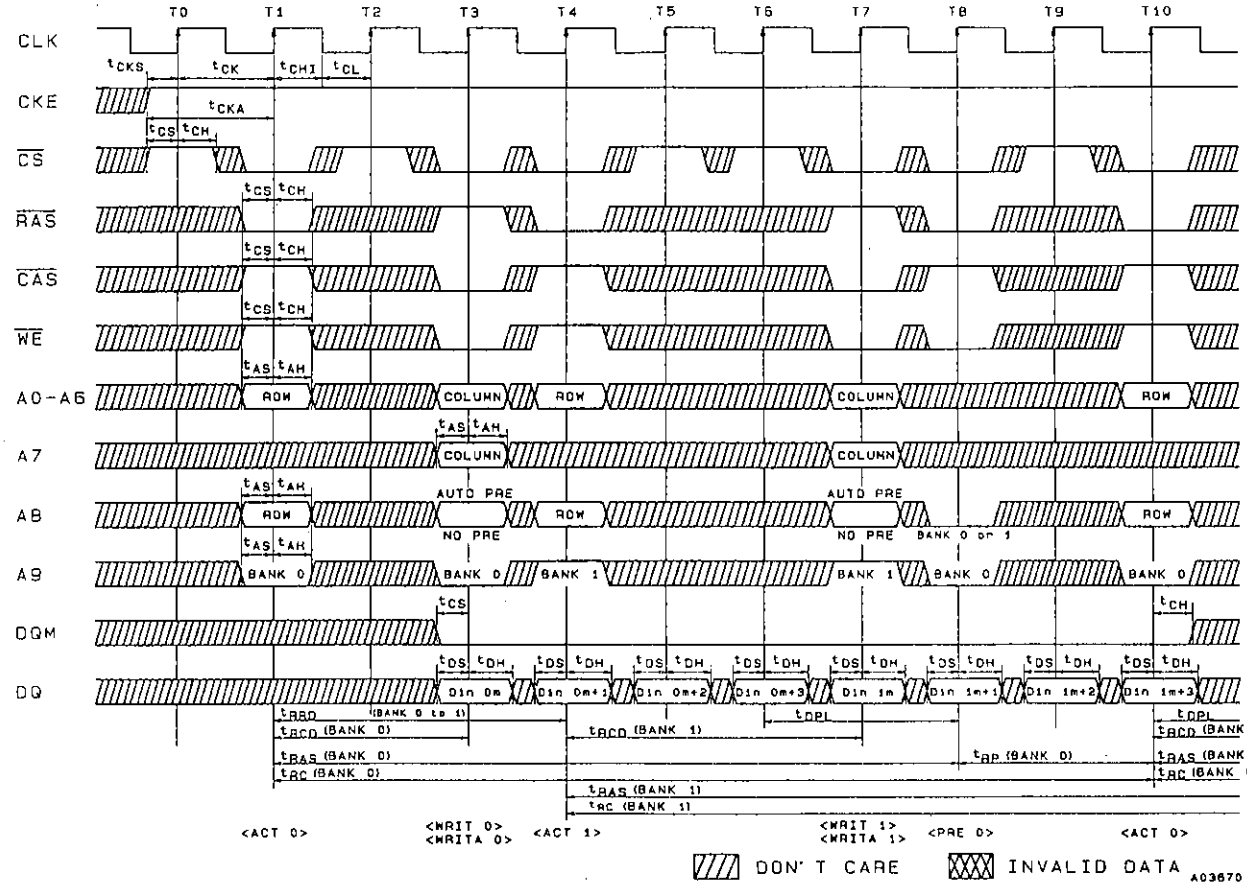
Write Cycle/Full Page

$\overline{CAS}$ latency = 2, burst length = full page



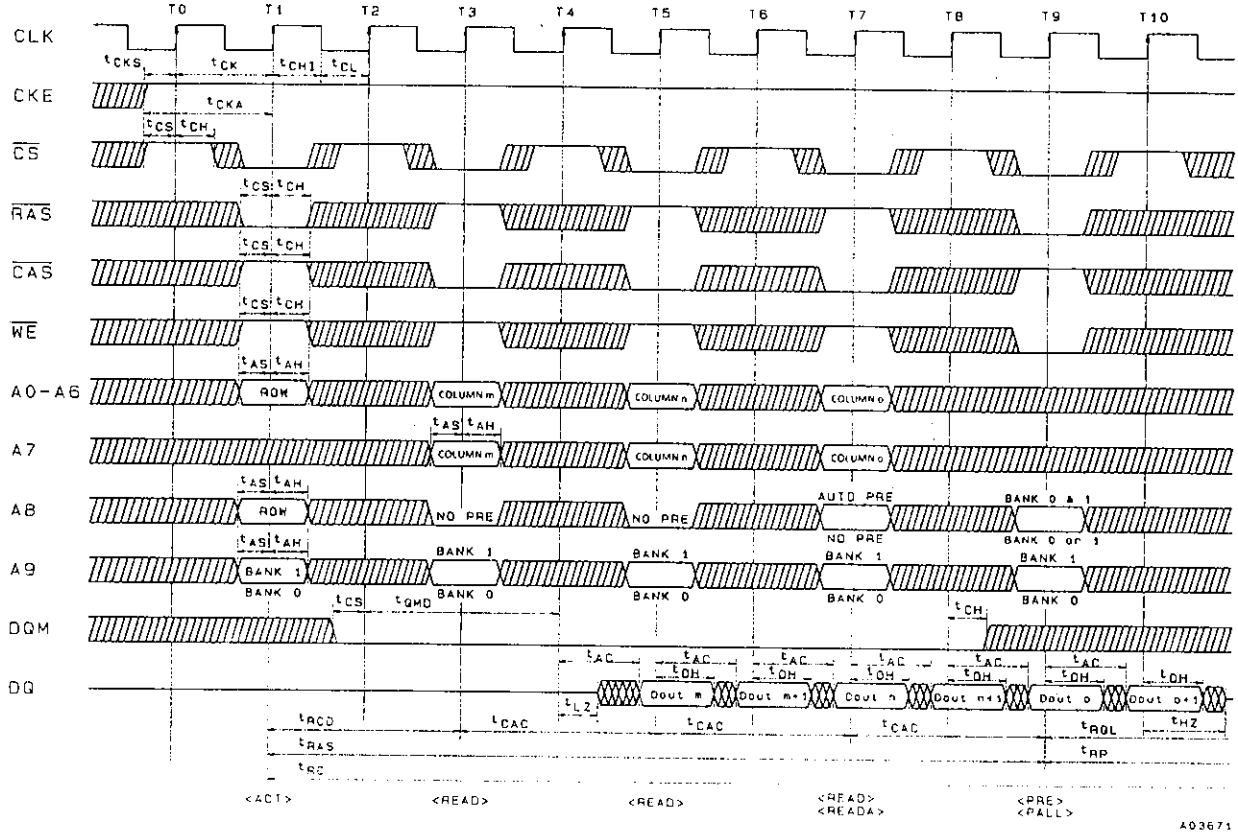
Write Cycle/Ping-Pong Operation (bank switching)

$\overline{CAS}$ latency = 2, burst length = 4



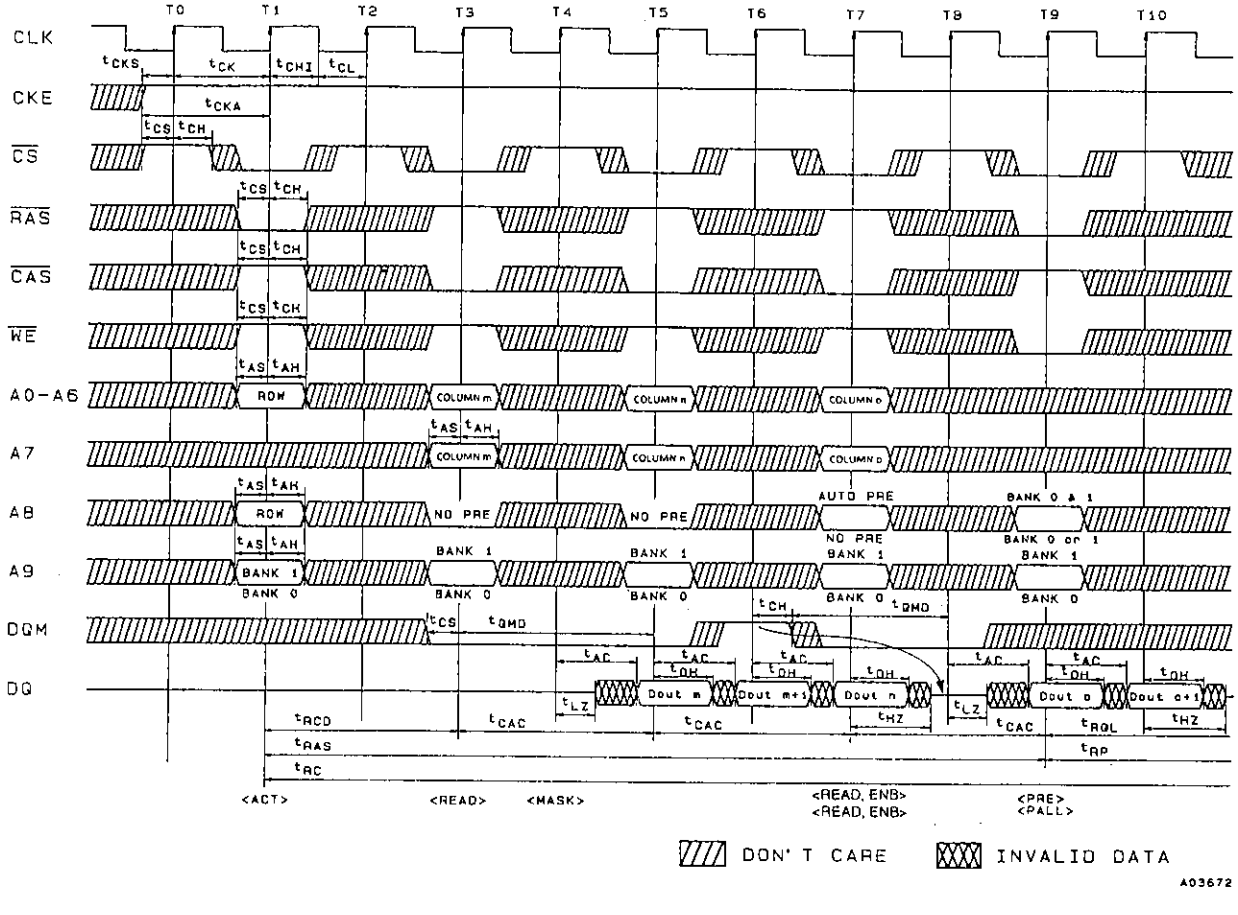
Read Cycle/Page Mode

$\overline{CAS}$ latency = 2, burst length = 2



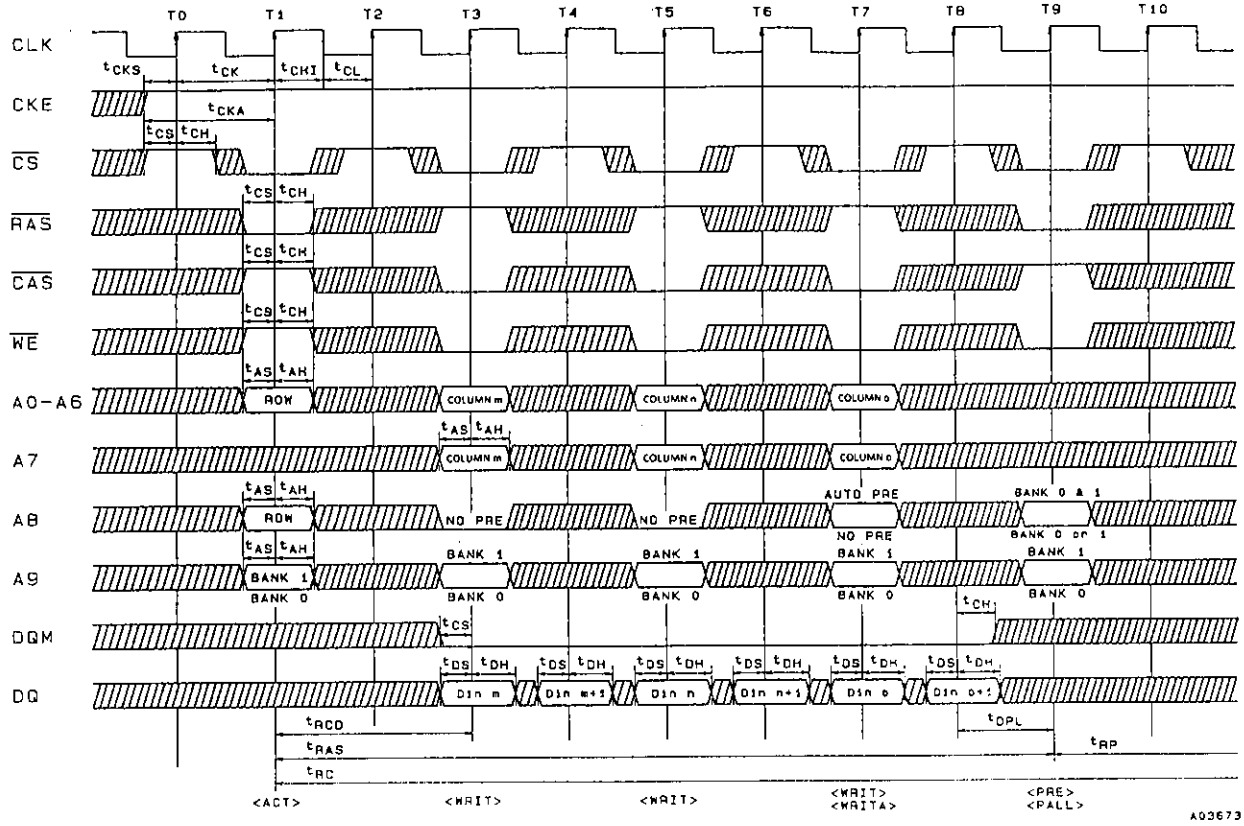
Read Cycle/Page Mode; Data Masking

$\overline{CAS}$ latency = 2, burst length = 2



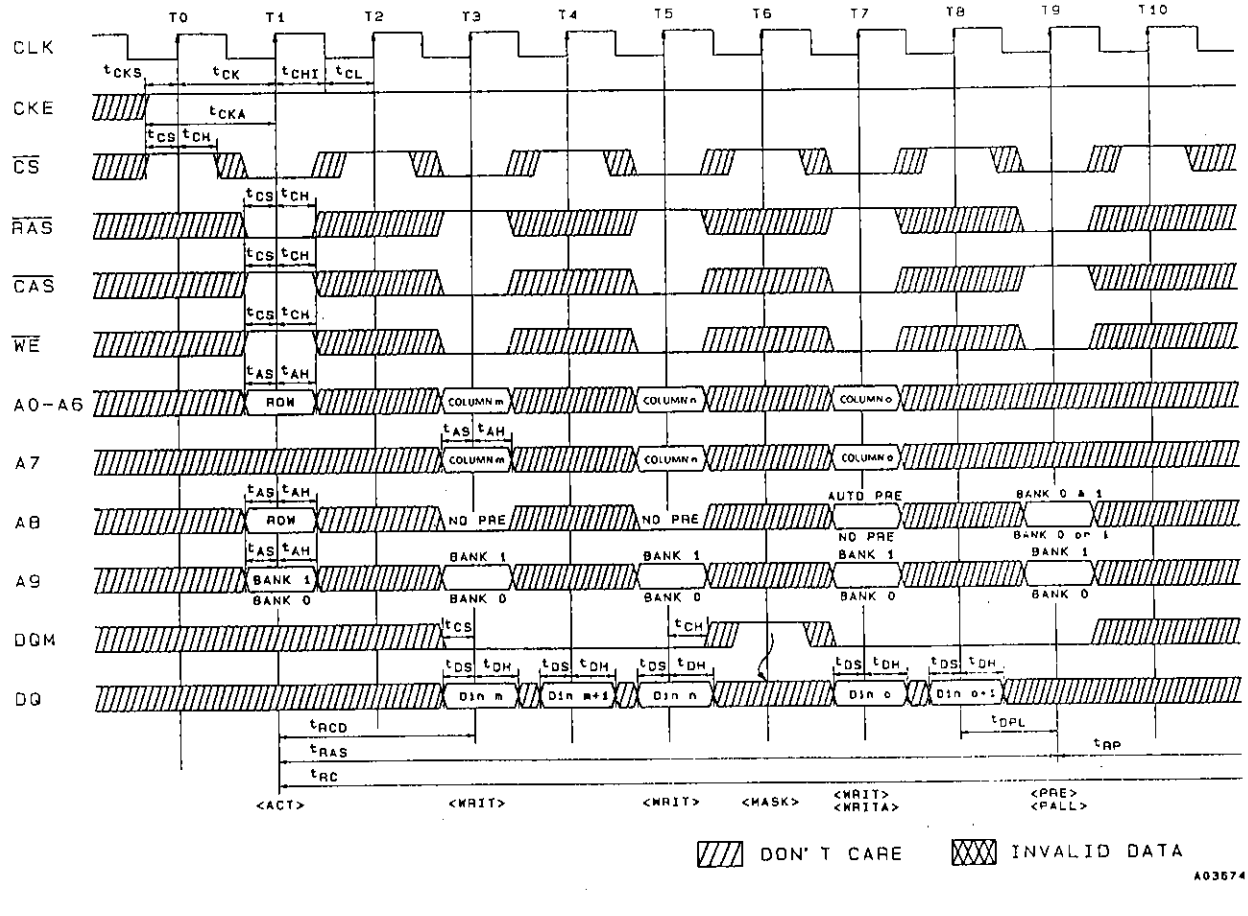
Write Cycle/Page Mode

$\overline{CAS}$ latency = 2, burst length = 2



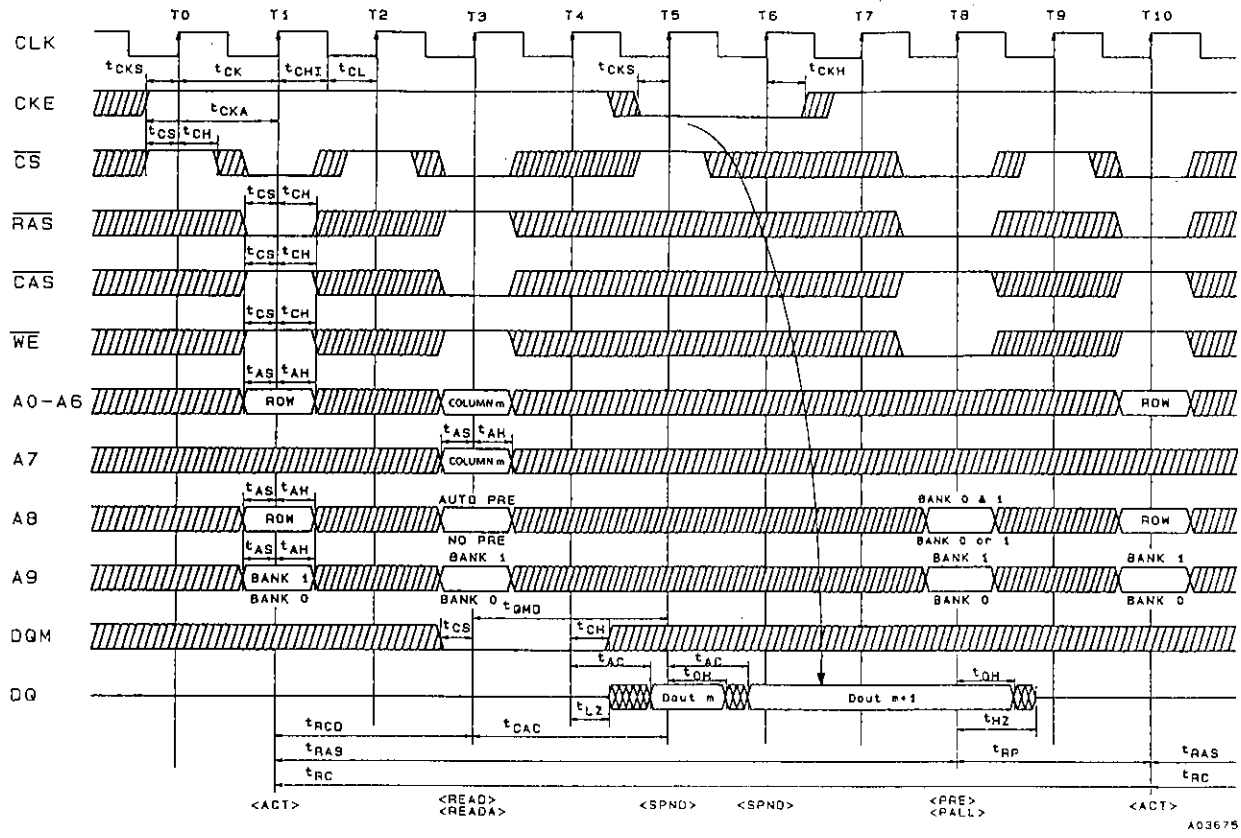
Write Cycle/Page Mode; Data Masking

$\overline{CAS}$ latency = 2, burst length = 2



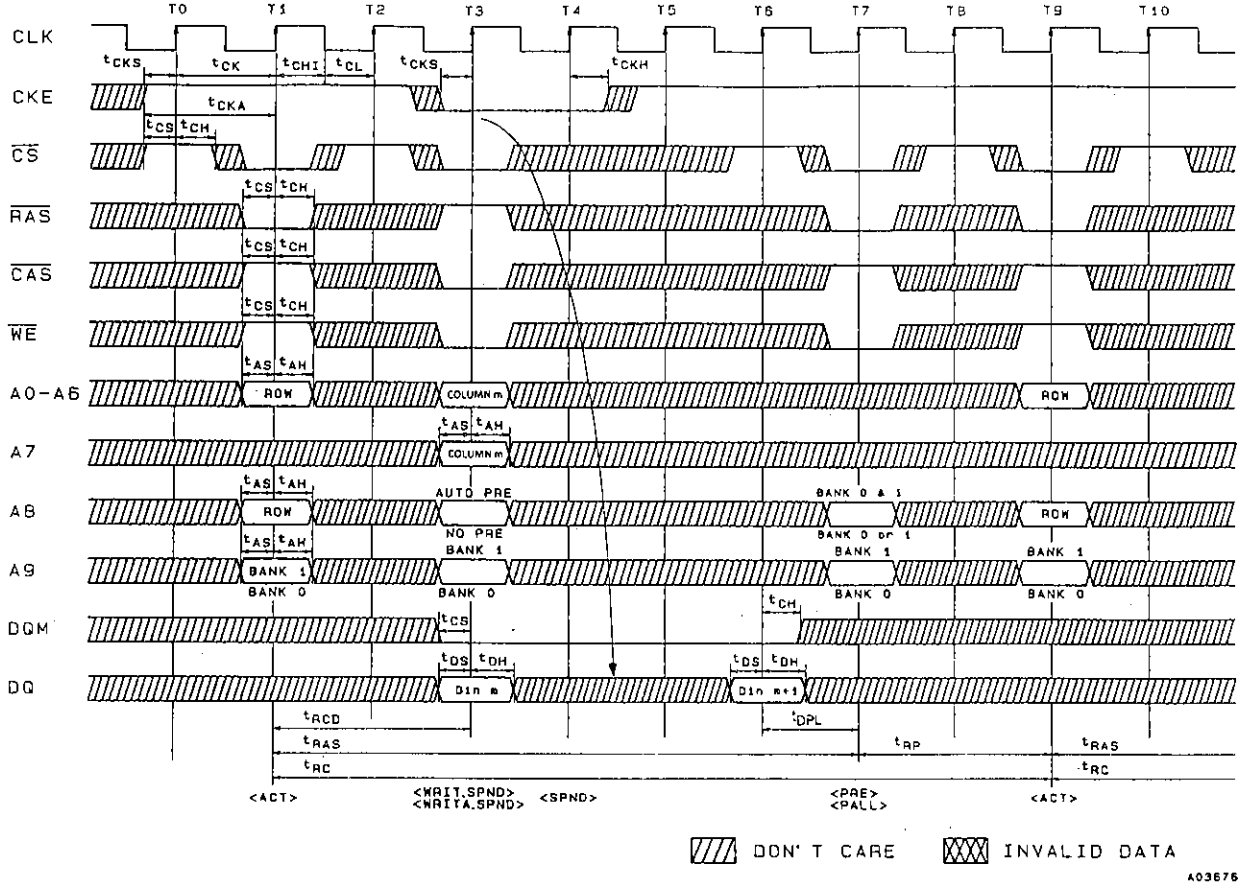
Read Cycle/Clock Suspend

$\overline{CAS}$ latency = 2, burst length = 2



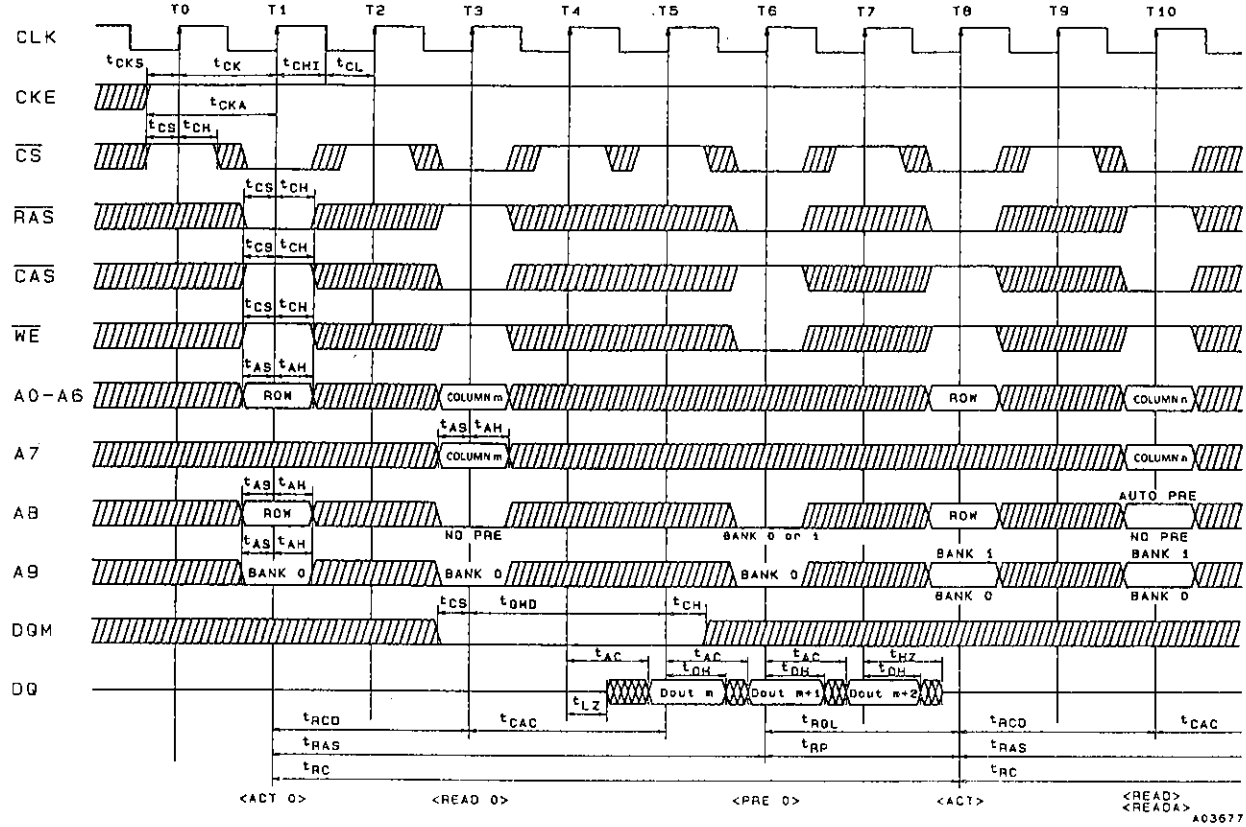
Write Cycle/Clock Suspend

$\overline{CAS}$ latency = 2, burst length = 2



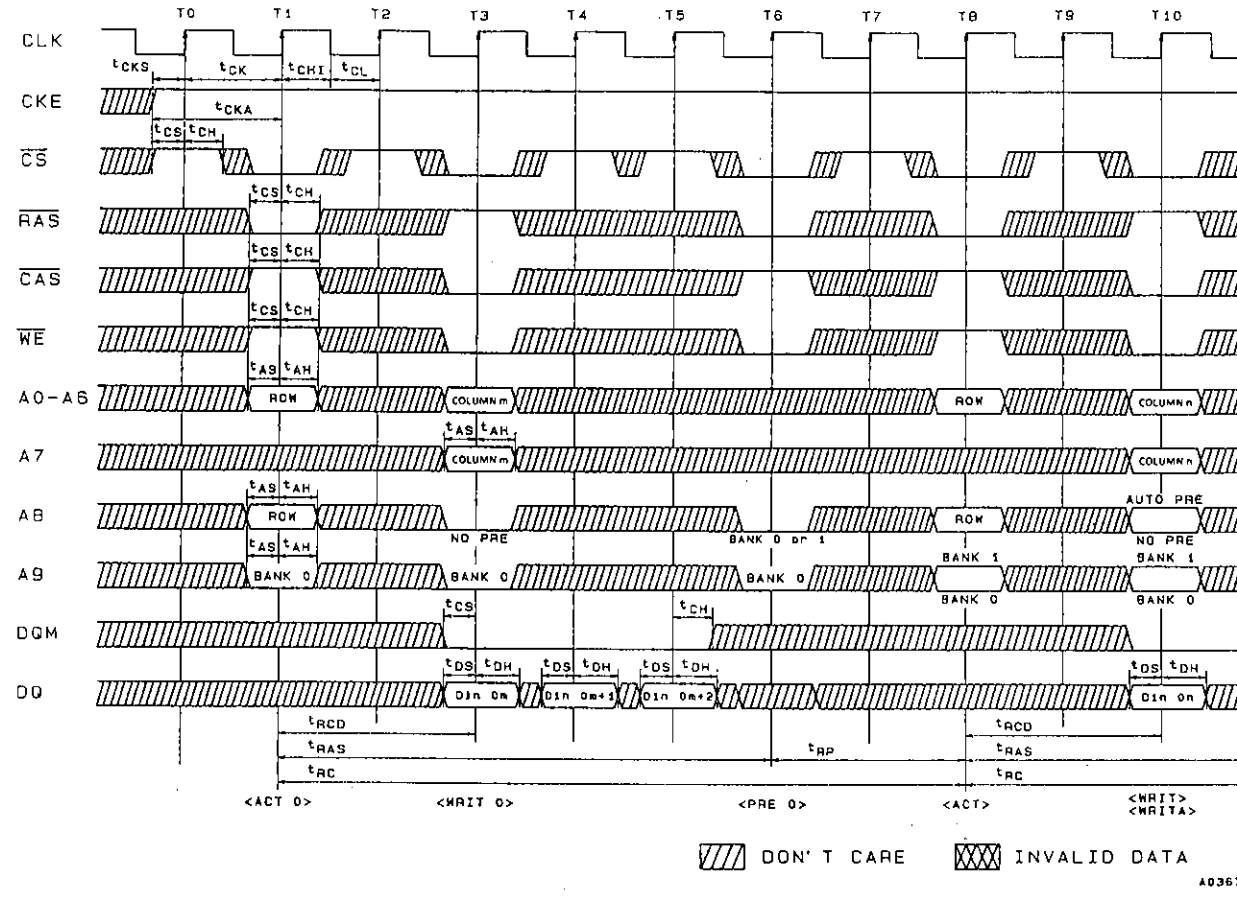
Read Cycle/Precharge Termination

$\overline{CAS}$ latency = 2, burst length = 2



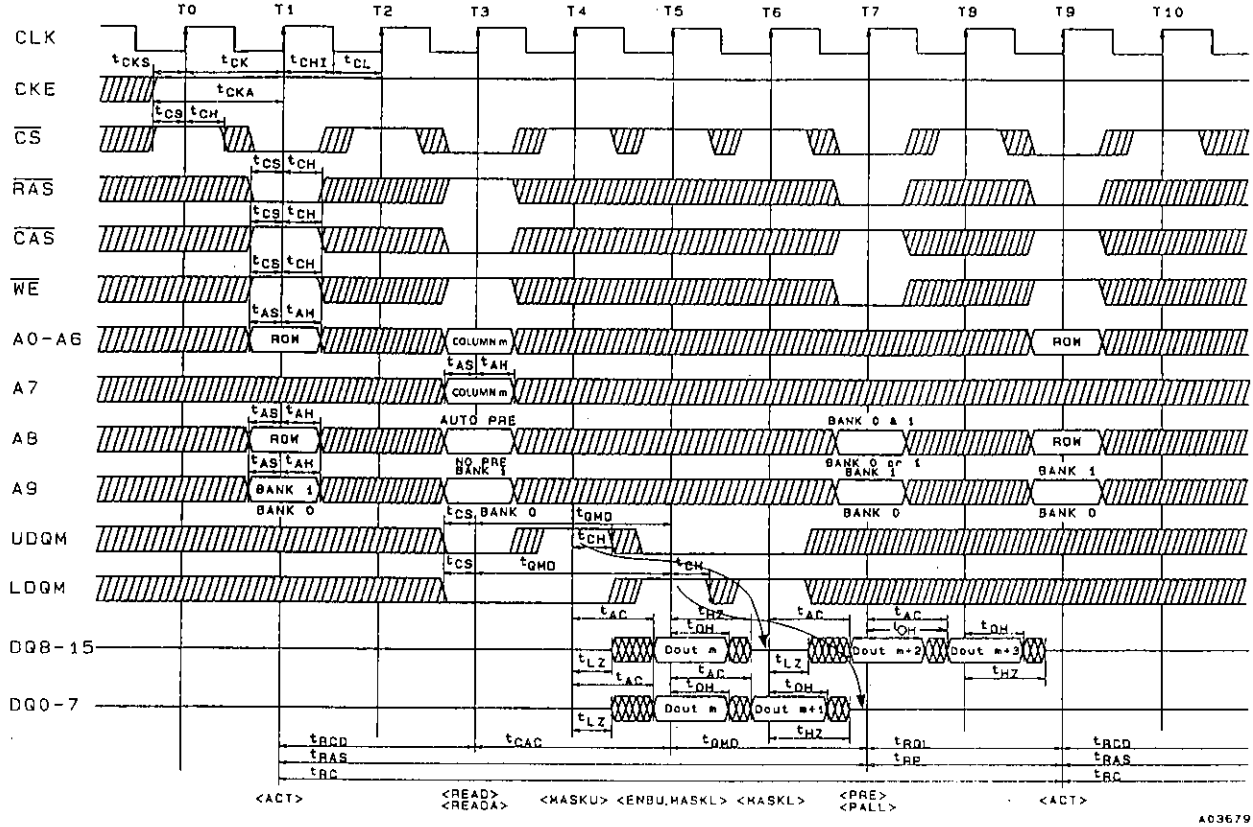
Write Cycle/Precharge Termination

$\overline{CAS}$ latency = 2, burst length = 2



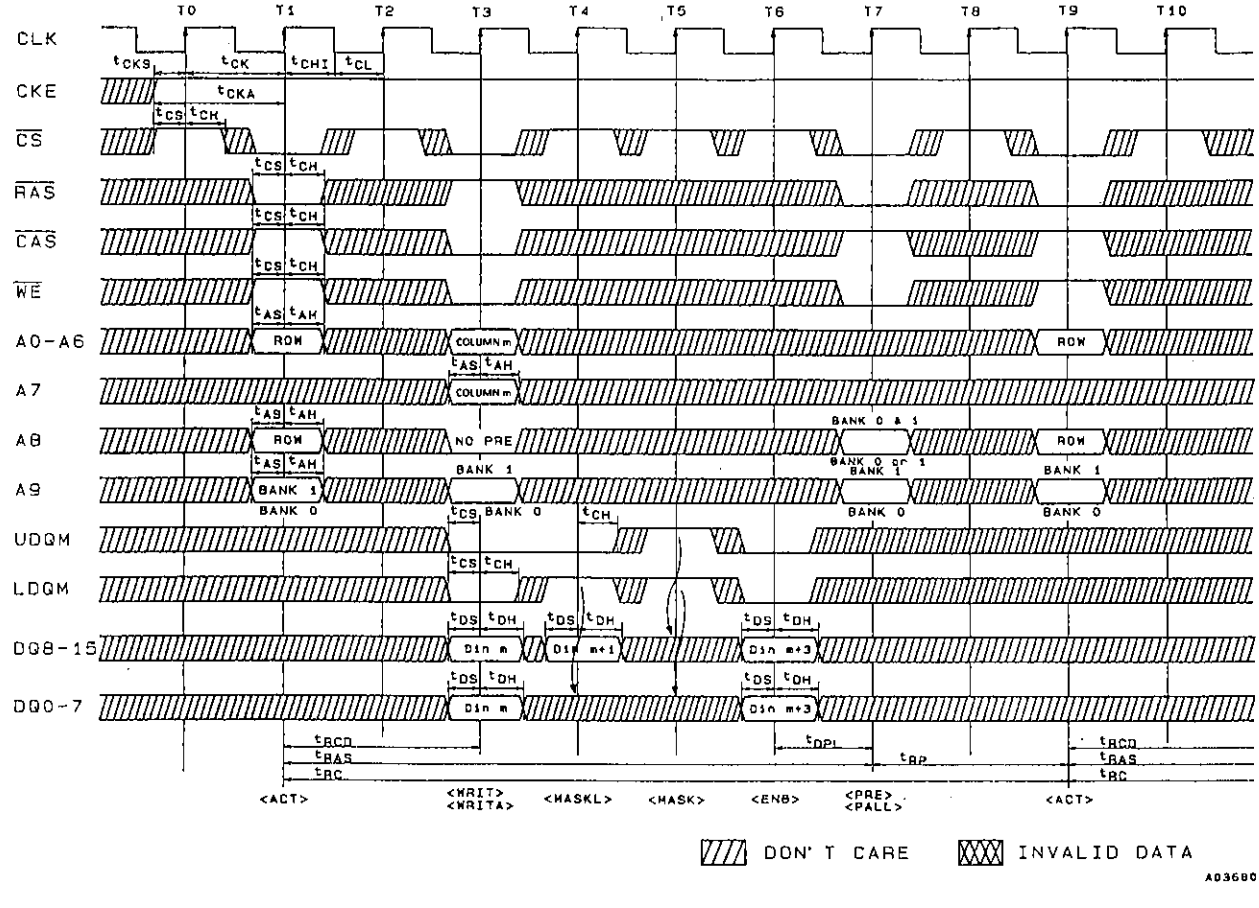
Read Cycle/Byte Operation

$\overline{CAS}$ latency = 2, burst length = 4



Write Cycle/Byte Operation

$\overline{CAS}$ latency = 2, burst length = 4



Read Cycle, Write Cycle/Burst Read, Single Write

$\overline{CAS}$ latency = 2, burst length = 4