FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-22307-5E

ASSP Communication Control

Data Link Controller (DLC)

MB89374

■ DESCRIPTION

The MB89374 Data Link Controller (DLC) controls transfer of serial data in accordance with Bit Oriented Protocol (BOP). It supports protocols such as High level Data Link Control (HDLC) (the BOP mode) and Serial Data Link Control (SDLC) LOOP secondary station (the LOOP mode).

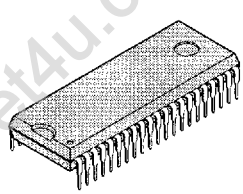
■ FEATURES

- Supports BOP serial data transfer procedure
- Supports SDLC LOOP mode
- Internal full-duplex communications channel
- Data transfer at rates up to 2.5 Mbps (at 10 MHz)
  However, in the LOOP mode, the maximum transfer rates are 1.25 Mbps for NRZ/NRZI code and 833 kpbs for FM/Manchester code.
- 10 MHz system clock with 1/2 duty, or 8 MHz with 1/3 duty
- Internal inter frame spacing counter
- Receive address field data compared with address data register
- One-byte address compare (multicasting address collating)
  - Two-byte address compare
  - One-byte two-address compare
  - Global address compare
- Supports two type of CRC checks (CRC16/CCITT)

(Continued)

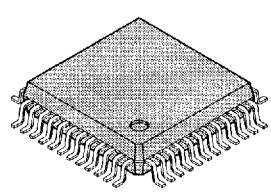
■ PACKAGES

42 pin, Plastic SH-DIP



(DIP-42P-M02)

48 pin, Plastic QFP



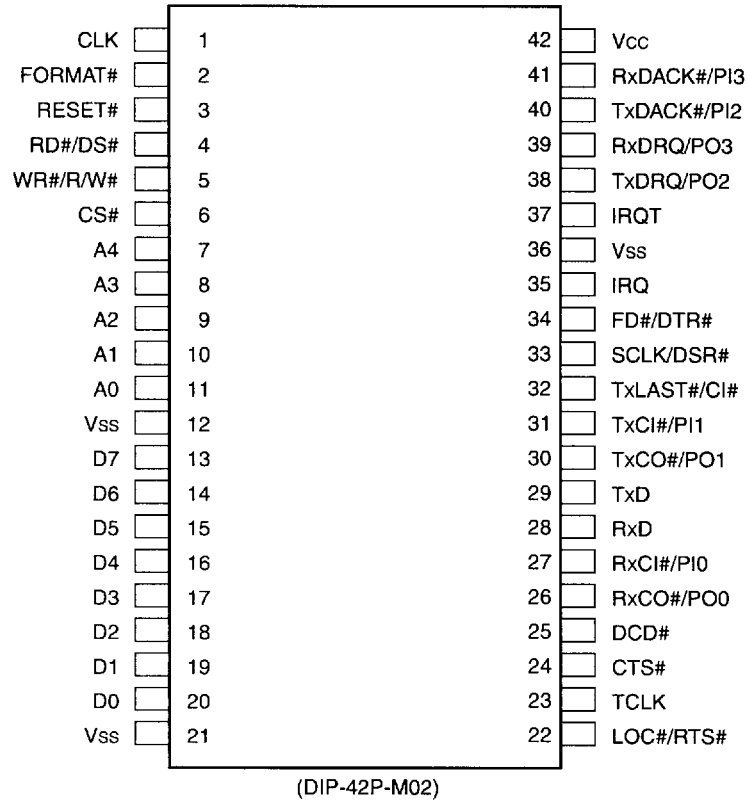
(FPT-48P-M13)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised tha normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

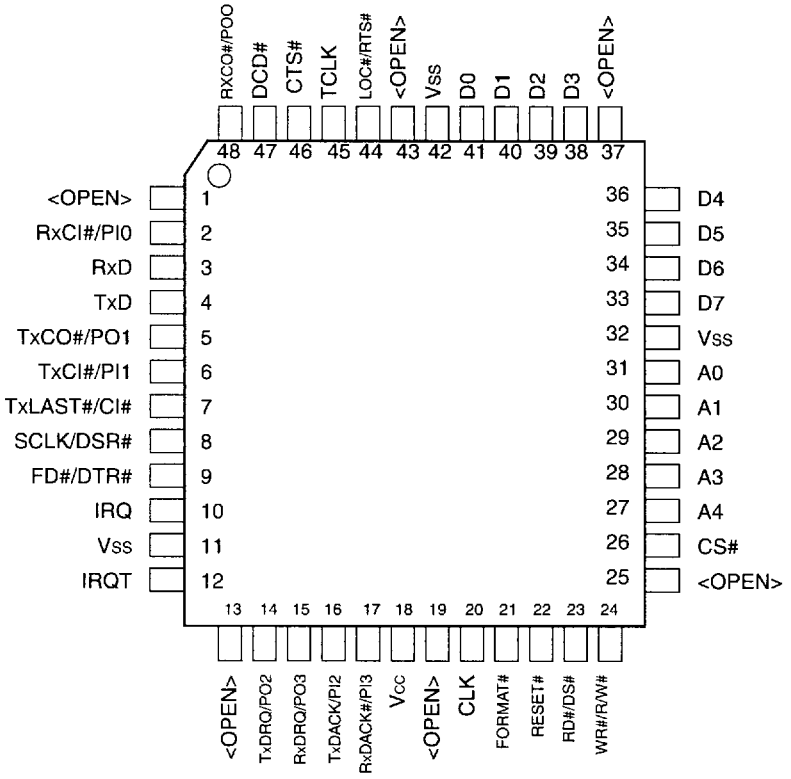
(Continued)

- FIFO transmit data (4 bytes) and receive data (8 bytes)
- Supports various codings (NRZ/NRZI/Manchester/FM0/FM1)
- Automatic return mode selectable in NRZI coding mode
- Various error interrupt request functions
- DMA interface function
- Two bit-rate generator channels for SIU transfer clock (Transmit and Receive)
  The bit rate generators can also be used as interval timers.
- Direct register access method
- MBL8086/88-family or GMICRO-family bus interface selectable
- Single +5 V power supply

■ PIN ASSIGNMENTS



(DIP-42P-M02)



(FPT-48P-M13)

Note: OPEN pins require no connection.

■ PIN DESCRIPTION

Pin No. DIP	Pin No. QFP	Symbol	I/O	Level*	Description
30	5	TxCO#/PO1	O	L	Transmit clock-output or port-output 1 pin: This pin is selected as the clock-output pin or port-output pin by the TxC0 and TxC1 bits of the transfer mode register (SMR2) and by the TxBRGEN bit of the transmit mode register (SMR3).
31	6	TxCI#/PI1	I	—	Transmit clock-input or port-input 1 pin: This pin is selected as the clock-input pin or port-input pin by the TxC0 and TxC1 bits of the transfer mode register (SMR2) and by the TxBRGEN bit of the transmit mode register (SMR3).
26	48	RxCO#/PO0	O	L	Receive clock-output or port-output 0 pin: This pin is selected as the clock-output pin or port-output pin by the RxC0 and RxC1 bits of the transfer mode register (SMR2).
27	2	RxCI#/PI0	I	—	Receive clock-input or port-input 0 pin: This pin is selected as the clock-input pin or port-input pin by the RxC0 and RxC1 bits of the transfer mode register (SMR2).
22	44	LOC#/RTS#	O	H	Loop on-line control or request-to-send pin: This pin serves as the LOC# output pin in the LOOP mode and as the RTS# output pin in the BOP mode. If it is used as the LOC# output pin, it functions as an on-line/off-line control pin. If it is used as the RTS# output pin, it outputs a LOW level when the RTS bit of the modem control register (MCR) is set to 1, and outputs a HIGH level when the RTS bit is set to 0.
34	9	FD#/DTR#	O	H	Flag-detect or data-terminal-ready pin: This pin is selected as the flag-detect or data-terminal-ready pin by the FD or DTR bits of the transmit mode register (SMR3). If it is used as the FD# pin, it outputs a LOW level during one cycle of the receive clock after receiving the last bit of the flag. If it is used as the DTR# pin, it outputs a LOW level when the DTR bit of the modem control register (MCR) is set to 1, and a HIGH level when the DTR bit is set to 0.
25	47	DCD#	I	—	Data-carrier-detect pin: The DCD bit of the modem status register (MSR) displays 1 when the pin input level is LOW and 0 when the input level is HIGH.
24	46	CTS#	I	—	Clear-to-send pin: The CTS bit of the modem status register (MSR) displays 1 when the pin input level is LOW, and displays 0 when the input level is HIGH. The DLC is placed in the transmission-enable state when this pin is set to the CTSAUTO mode, and by the TxE bit of the transmission control register (TxCR). Transmission is enabled/disabled according to the input level of the CTS# pin; transmission is enabled when the pin input level is LOW and disabled when the input level is HIGH.

Signals suffixed by the symbol # are negative logic.

(Continued)

* : Pin output level when reset

(Continued)

Pin No. DIP	Pin No. QFP	Symbol	I/O	Level*	Description
32	7	TxLAST#/CI#	I	—	Transmit DMA-end-signal or calling-indication pin: This pin serves as the TxLAST# input pin when the DMA mode is selected by the TxD/I bit of the transmit interrupt enable register (TxIER), and by the enabling TxLASTEND bit of the transmit mode register (SMR3). In other cases, this pin serves as the CI# input pin. If this pin is used as the CI# input pin, the CI bit of the modem status register (MSR) displays 1 when the pin input level is LOW, and 0 when the input level is HIGH.
29	4	TxD	O	H	Transmit-data pin: This pin is used to output serial data.
28	3	RxD	I	—	Receive-data pin: This pin is used to input serial data.
33	8	SCLK/DSR#	I	—	Source-clock input or data-set-ready pin: This pin serves as the SCLK input pin for BRG1/BRG2 or DPLL when: • BRG, DPLL or BRG + DPLL are selected by the TxC0 and TxC1 bits of the transfer mode register (SMR2). • BRG, DPLL or BRG + DPLL are selected by the RxC0 and RxC1 bits of the transfer mode register (SMR2). • The BRG1OUTIE bit of the BRG1/DPLL control register (B1PCR) is set to 1. • The BRG2CLK bit of the BRG2 control register (B2CR) is set to 1. In other cases, this pin serves as the DSR# input pin. If this pin is used as the DSR# input pin, the DSR bit of the modem status register (MSR) displays 1 when the pin input level is LOW, and 0 when the input level is HIGH.
23	45	TCLK	I	—	BRG2 clock-input pin: This pin is used only when the clock source for BRG2 is not set at the SCLK pin (by setting the BRG2CLK bit of the BRG2 control register (B2CR)).
3	22	RESET#	I	—	Reset pin: This pin is used to input system reset signals.
4	23	RD#/DS#3	I	—	Read/data strobe pin: This pin serves as the RD# input pin in the MBL8086/88 mode. A LOW level is input to this pin when reading the registers in the DLC. This pin serves as the DS# input pin in the GMICRO mode. Strobe signals are input to this pin when accessing the registers in the DLC.

Signals suffixed by the symbol # are negative logic. *(Continued)*

* : Pin output level when reset

(Continued)

Pin No. DIP	Pin No. QFP	Symbol	I/O	Level*	Description
5	24	WR#/R/W#	I	—	Write or read/write pin: This pin serves as the WR# input pin in the MBL8086/88 mode. A LOW level is input to this pin when writing to the registers in the DLC. This pin serves as the R/W# input pin in the GMICRO mode. It determines the data direction when accessing the registers in the DLC.
6	26	CS#	I	—	Chip-select pin: A LOW level is input to this pin when accessing the registers in the DLC.
2	21	FORMAT#	I	—	CPU-interface mode-setting pin: This pin is set to the GMICRO mode when the input level is LOW, and to the MBL8086/88 mode when the input level is HIGH. The pin input level must be fixed to LOW or HIGH.
13 to 20	33 to 36, 38 to 41	D7 to D0	I/O	Hi-Z	Data-bus (tristate) pins: These pins are used to input and output 8-bit data.
7 to 11	27 to 31	A4 to A0	I	—	Address pins: These pins are used to input addresses to select the registers in the DLC.
35	10	IRQ	O	L	Interrupt-request pin: This pin is used to generate HIGH interrupt requests by using bits other than the BRG2OUT bit of the BRG2 status register (B2SR) as interrupt trigger bits.
37	12	IRQT	O	L	Interrupt-request pin: This pin is used to generate HIGH interrupt requests by using the BRG2OUT bit of the BRG2 status register (B2SR) as the interrupt trigger bit.
39	15	RxDRQ/PO3	O	L	Receive DMA-request or port-output 3 pin: The receive DMA-request pin or port-output pin is selected by the RxD/I bit of the receive interrupt enable register (RxIER). If this pin is used as the RxDRQ pin, it outputs a HIGH level to request DMA transfer of receive data. If this pin is used as the PO3 pin, it outputs a HIGH level when the PO3 bit of the port register (PORTR) is 1, and a LOW level when the PO3 bit is 0.
38	14	TxDRQ/PO2	O	L	Transmit DMA-request or port-output 2 pin: The transmit DMA-request pin or port-output pin is selected by the TxD/I bit of the transmit interrupt enable register (TxIER). If this pin is used as the TxDRQ pin, it outputs a HIGH level to request the DMA transfer of transmit data. If this pin is used as the PO2 pin, it outputs a HIGH level when the PO2 bit of the port register (PORTR) is 1, and a LOW level when the PO2 bit is 0.

Signals suffixed by the symbol # are negative logic. *(Continued)*

* : Pin output level when reset

(Continued)

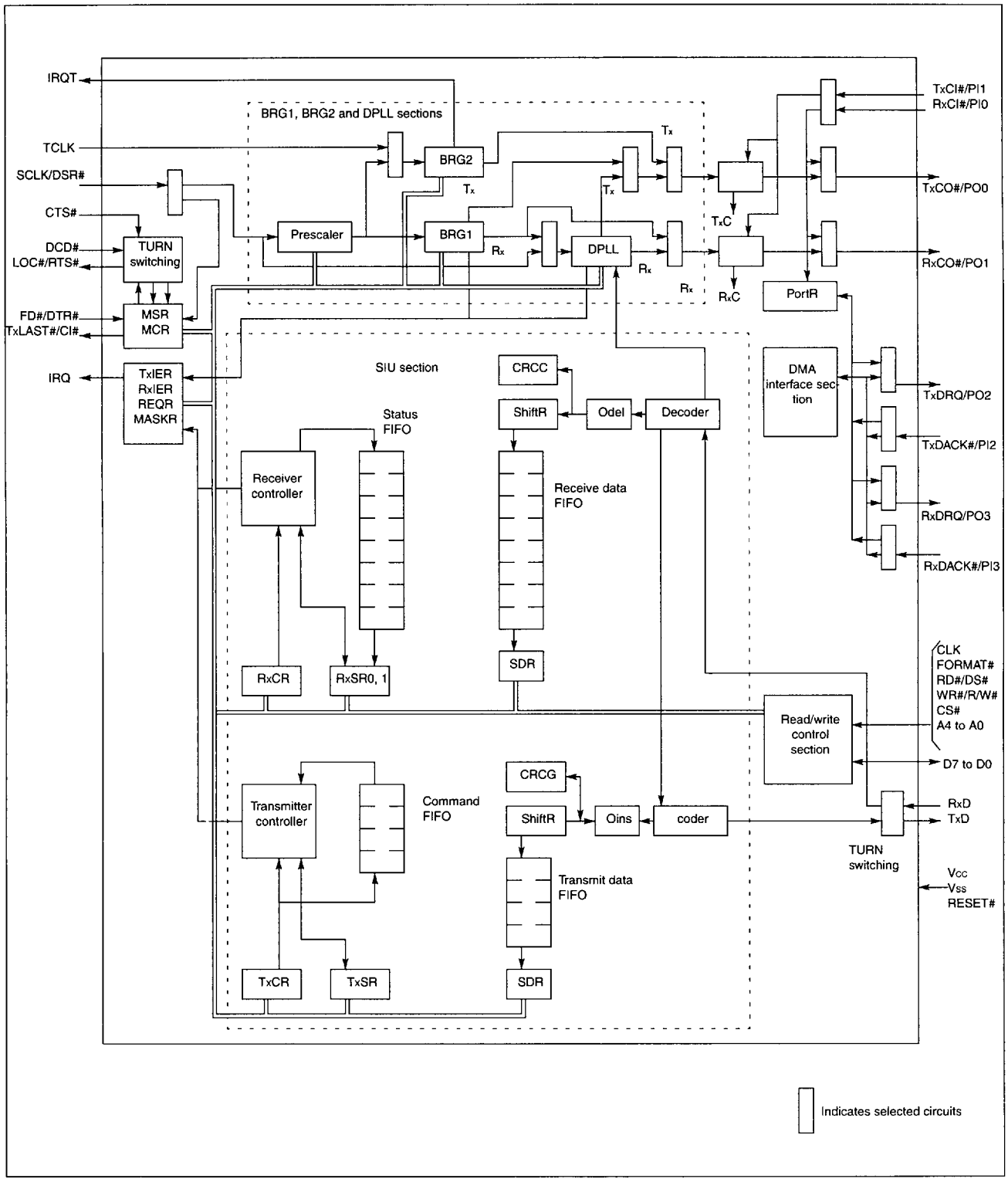
Pin No.		Symbol	I/O	Level*	Description
DIP	QFP				
41	17	RxDACK#/ PI3	I	—	Receive DMA-acknowledge or port-input 3 pin: The receive DMA-acknowledge pin or port-input pin is selected by the RxD/I bit of the receive interrupt enable register (RxIER). If this pin is used as the RxDACK# pin, it inputs acknowledge signals for DMA transfer of receive data. If this pin is used as the PI3 pin, the PI3 bit of the port register (PORTR) is set to 1 when the pin input level is HIGH, and 0 when the input level is LOW.
40	16	TxDACK#/ PI2	I	—	Transmit DMA-acknowledge or port-input 2 pin: The transmit DMA-acknowledge pin or port-input pin is selected by the TxD/I bit of the transmit interrupt enable register (TxIER). If this pin is used as the TxDACK# pin, it inputs acknowledge signals for the DMA transfer of transmit data. If this pin is used as the PI2 pin, the PI2 bit of the port register (PORTR) is set to1 when the pin input level is HIGH, and 0 when the input level is LOW.
1	20	CLK	I	—	System clock pin: This pin is used to input clocks for DLC operation.
12, 21, 36	11, 32, 42	V_{SS}	-	—	Ground pins
42	18	V_{CC}	-	—	+5 VDC ±10% power-supply pin
—	1, 13, 19, 25, 37, 43	<OPEN>	-	—	OPEN pins always require no connection.

Signals suffixed by the symbol # are negative logic.

* : Pin output level when reset

■ BLOCK DIAGRAM

The DLC internal block diagram is shown below. The DLC consists of the SIU, BRG, DPLL, read/write control, and DMA interface sections.



■ FUNCTIONAL DESCRIPTION OF EACH BLOCK

- **SIU section**
  - Detects and generates flags
  - Inserts and deletes 0
  - Compares address field data
  - Generates and checks CRC
- **BRG1 section (Selectable among three below)**
  - Generates transfer clock
  - Generates clock for DPLL operation
  - Functions as interval timer
- **BRG2 section (Selectable among two below)**
  - Generates transfer clock
  - Functions as interval timer
- **DPLL section**
  Generates receive clock synchronized with received serial data
- **CPU interface section**
  - Read/write control
  - DMA interface control

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC} + 0.3	V
Ambient temperature	Ta	0 to +70	°C
Storage temperature	T_{stg}	−55 to +150	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0 V (Voltage referenced to V_{SS})

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{CC}	+4.5	5	+5.5	V
Ambient temperature	Ta	0	—	+70	°C

■ PIN CAPACITANCE

(Ta = +25°C)

Parameter	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	fc = 1 MHz	—	20	pF
Output capacitance	C_{OUT}		—	20	pF
Input/output capacitance	$C_{I/O}$		—	20	pF

■ ELECTRICAL CHARACTERISTICS

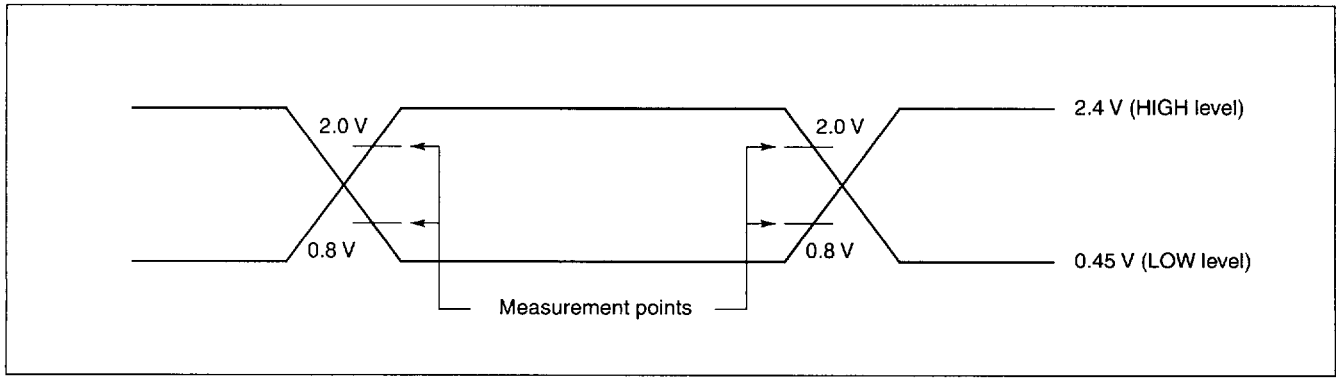
1. DC Characteristics

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

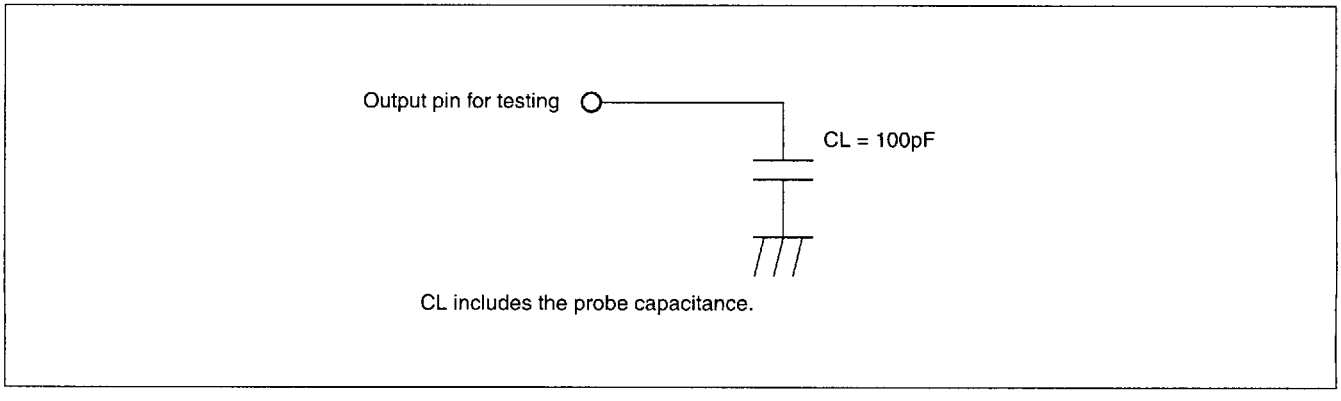
Parameter	Symbol	Conditions	Min.	Max.	Unit
Power supply current	I_{CC}	Output open, input 0 V or V_{CC}, when operating at 10 MHz	—	15	mA
Input leakage current	I_{ILK}	0 V ≤ V_{IN} ≤ V_{CC}	—	±10	µA
Output leakage current	I_{OLK}	0 V ≤ V_{IN} ≤ V_{CC} Output in high impedance state	—	±10	µA
Low-level input voltage	V_{IL}	Pins other than CLK	–0.3	0.8	V
High-level input voltage	V_{IH}	Pins other than CLK	2.0	V_{CC}+0.3	V
Low-level output voltage	V_{OL}	I_{OL} = 2.5 mA	–	0.4	V
High-level output voltage	V_{OH}	I_{OH} = –2.5 mA	3.0	—	V
		I_{OH} = –100 µA	V_{CC}–0.4	—	
Low-level clock input voltage	V_{CL}	CLK pin	–0.3	0.6	V
High-level clock input voltage	V_{CH}	CLK pin	3.9	V_{CC}+0.3	V

2. AC Characteristics Measurement Conditions

• AC Test Waveform



• AC Test Load Circuit

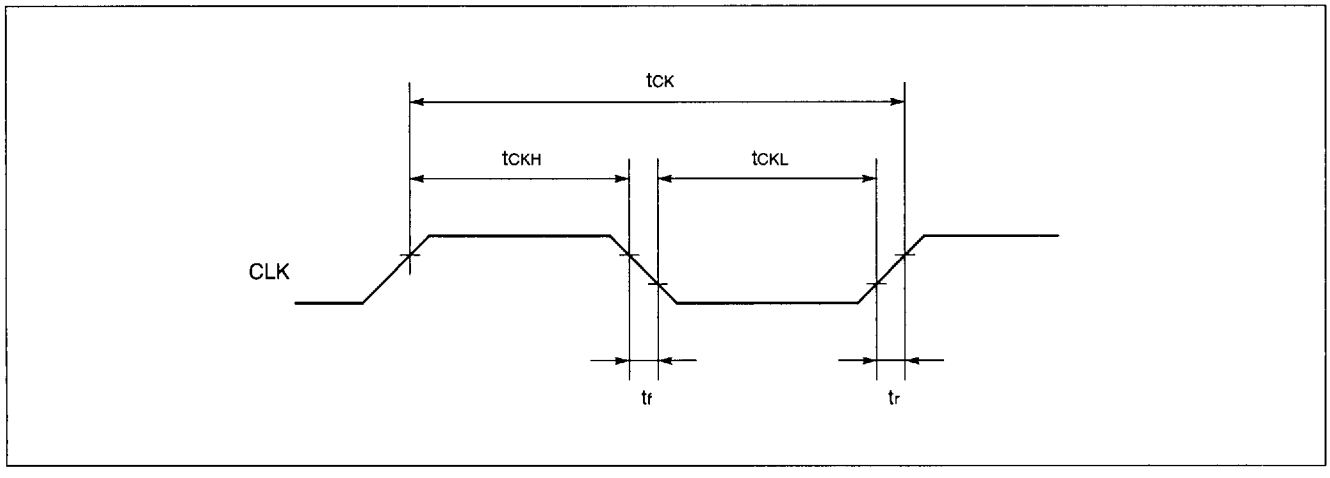


3. AC Characteristics

(1) System Clock

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

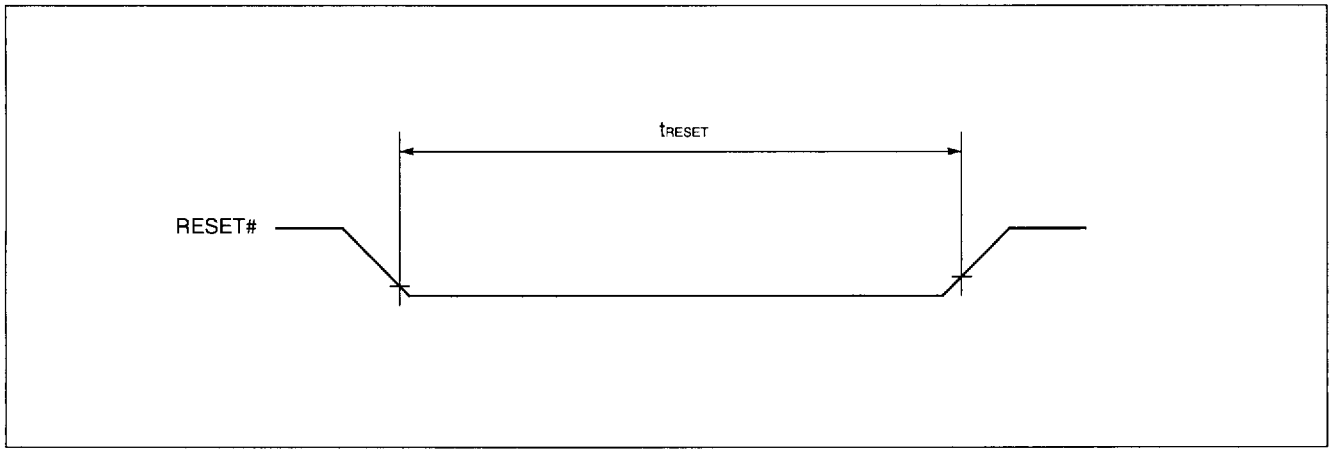
Parameter	Symbol	Min.	Max.	Unit
Clock period	t_{CK}	100	—	ns
Low-level clock pulse duration	t_{CKL}	40	—	
High-level clock pulse duration	t_{CKH}	40	—	
Clock pulse rise time, fall time	t_r, t_f	—	10	



(2) System Reset

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

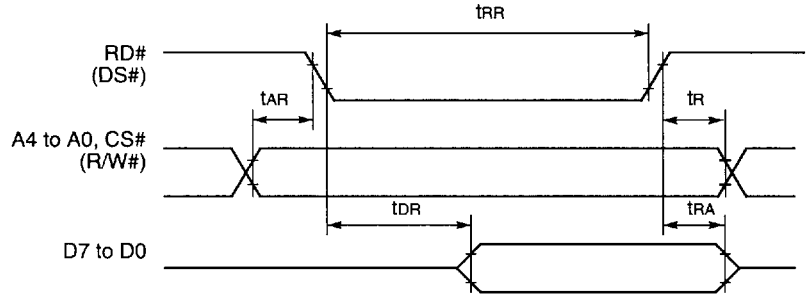
Parameter	Symbol	Min.	Max.	Unit
Reset pulse width	t_{RESET}	5t_{CK}	—	ns



(3) Read Timing

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
Read pulse width	t_{RR}	1tck +20	—	ns
Address setup time (RD#, DS# ↓)	t_{AR}	30	—	
Address hold time (RD#, DS# ↑)	t_{RA}	0	—	
Data delay (RD#, DS# ↓)	t_{DR}	—	90	
Data hold time (RD#, DS# ↑)	t_{RD}	10	60	

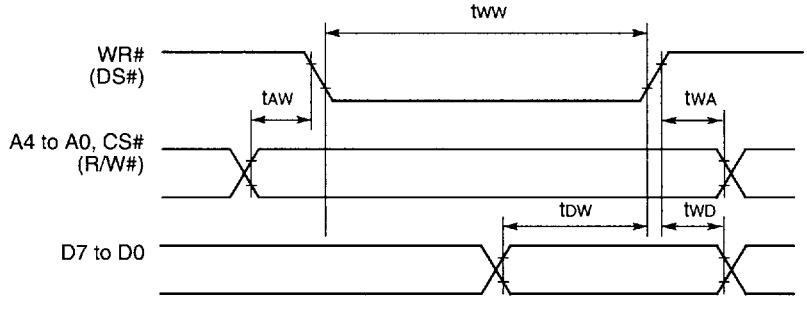


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(4) Write Timing

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
Write pulse width	t_{WW}	1tck +20	—	ns
Address setup time (WR#, DS# ↓)	t_{AW}	30	—	
Address hold time (WR#, DS# ↑)	t_{WA}	0	—	
Data setup time (WR#, DS# ↑)	t_{DW}	60	—	
Data hold time (WR#, DS# ↑)	t_{WD}	10	—	

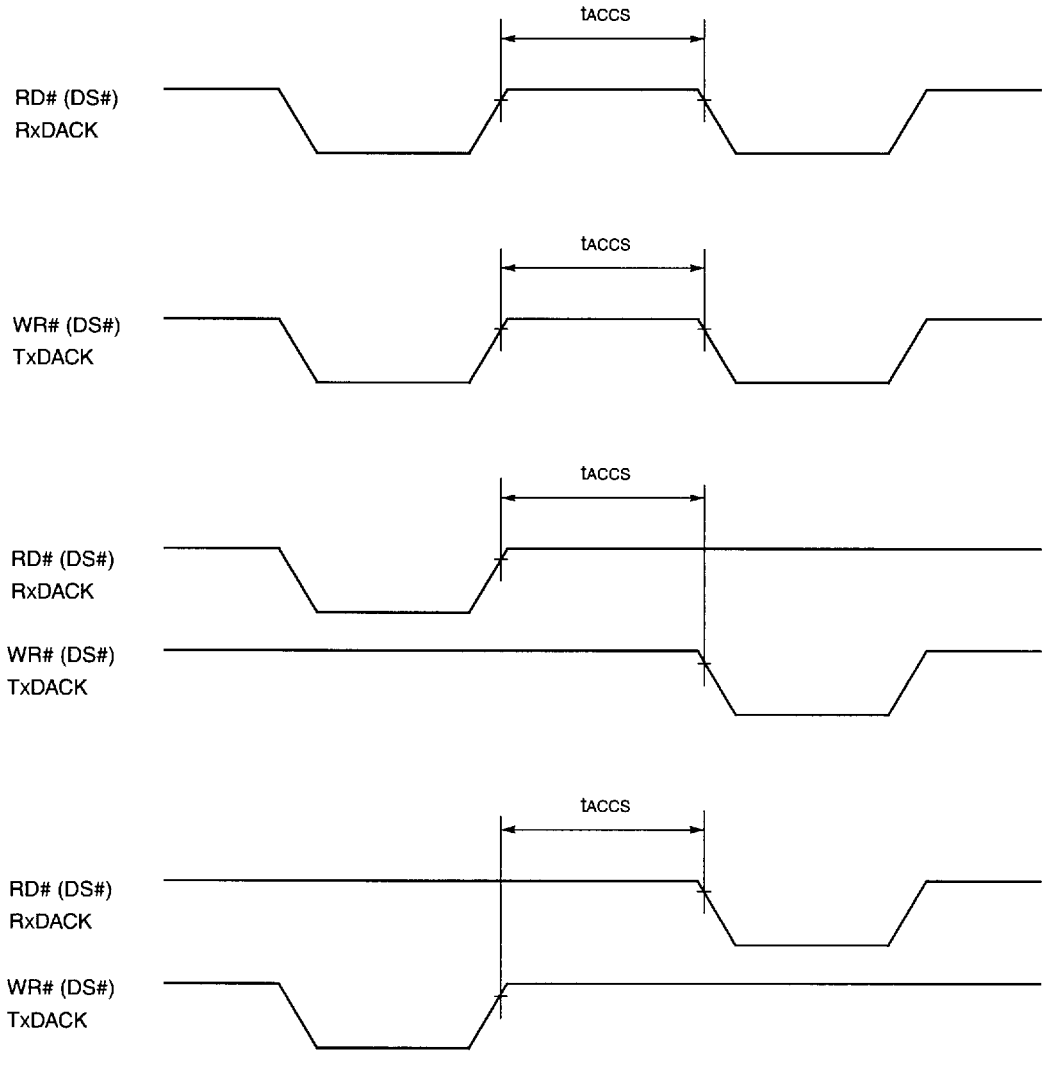


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(5) Data Access Recovery Time

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter		Symbol	Min.	Max.	Unit
Recovery time during data access	RD# ↑ WR# ↑ DS# ↑	t_{ACCS}	3t_{CK} +20	—	ns
	TxDACK ↓ RxDACK ↓				

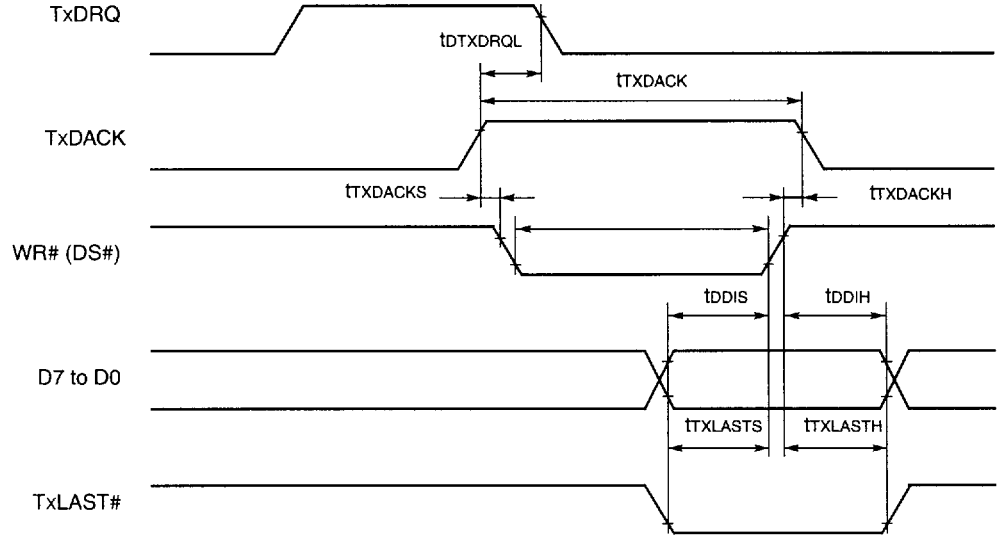


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(6) DMA Timing 1

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
TxDACK pulse width	t_{TXDACK}	1t_{CK} + 20	—	ns
TxDACK setup time (WR#, DS# ↓)	$t_{TXDACKS}$	0	—	
TxDACK hold time (WR#, DS# ↑)	$t_{TXDACKH}$	0	—	
TxDRQ delay (WR#, DACK# ↑)	$t_{DTXDRQL}$	—	60	
Data setup time (WR#, DS# ↑)	t_{DDIS}	60	—	
Data hold time (WR#, DS# ↑)	t_{DDIH}	0	—	
TxLAST# setup time (WR#, DS# ↑)	$t_{TXLASTS}$	60	—	
TxLAST# hold time (WR#, DS# ↑)	$t_{TXLASTH}$	0	—	

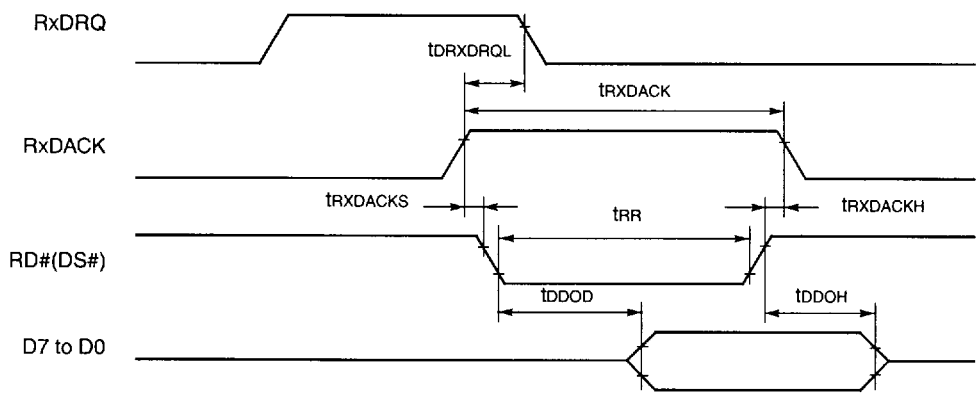


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(7) DMA Timing 2

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
RxDACK pulse width	t_{RXDACK}	$1t_{CK}$ + 20	—	ns
RxDACK setup time (RD#, DS# ↓)	$t_{RXDACKS}$	0	—	
RxDACK hold time (RD#, DS# ↑)	$t_{RXDACKH}$	0	—	
RxDRQ ↓ delay (RxDACK↑)	$t_{DRXDRQL}$	—	60	
Data delay(RD#, DS# ↓)	t_{DDOD}	—	90	
Data hold time (RD#, DS# ↑)	t_{DDOH}	10	60	

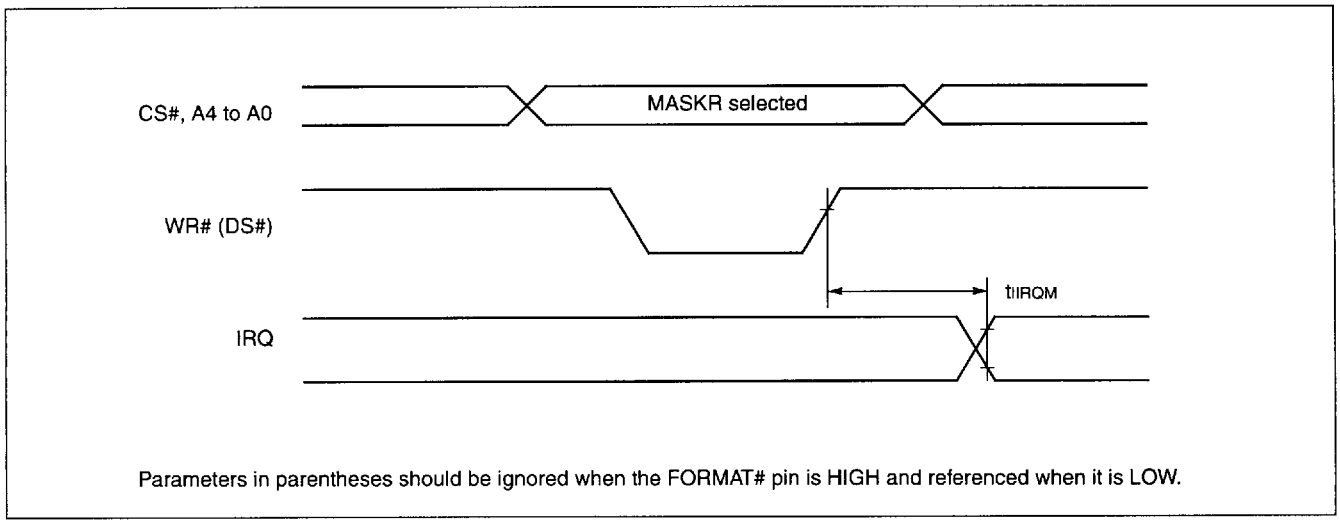


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(8) IRQ Masking

(Vcc = +5 V ±10%, Vss = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ ↑ delay (WR#, DS# ↑)	t_{IIRQM}	—	3tCK	ns



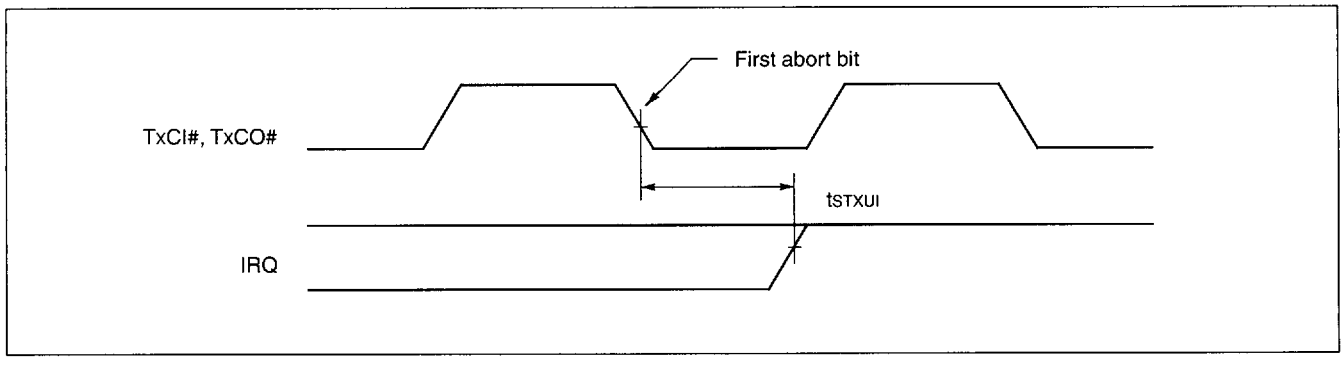
Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(9) Interrupt by Underrun

(Vcc = +5 V ±10%, Vss = 0 V, Ta = 0°C to +70°C)

Parameter		Symbol	Min.	Max.	Unit
IRQ ↑ delay (Tx,C# ↓)	(Note)	t_{STXUI}	—	3tCK	ns

Note: TxC# denotes TxCI# or TxCO#; RxC# denotes RxCI# or RxCO#.

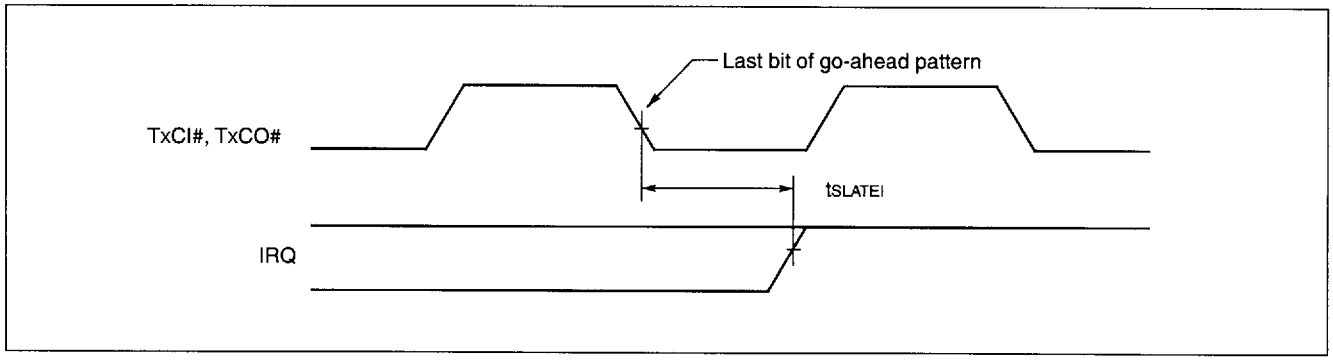


(10) Interrupt by LOOP Transmit Data Delay

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter		Symbol	Min.	Max.	Unit
IRQ ↑ delay (TxC# ↓)	(Note)	t_{SLATEI}	—	4t_{CK}	ns

Note: TxC# denotes TxCI# or TxCO#; RxC# denotes RxCI# or RxCO#.

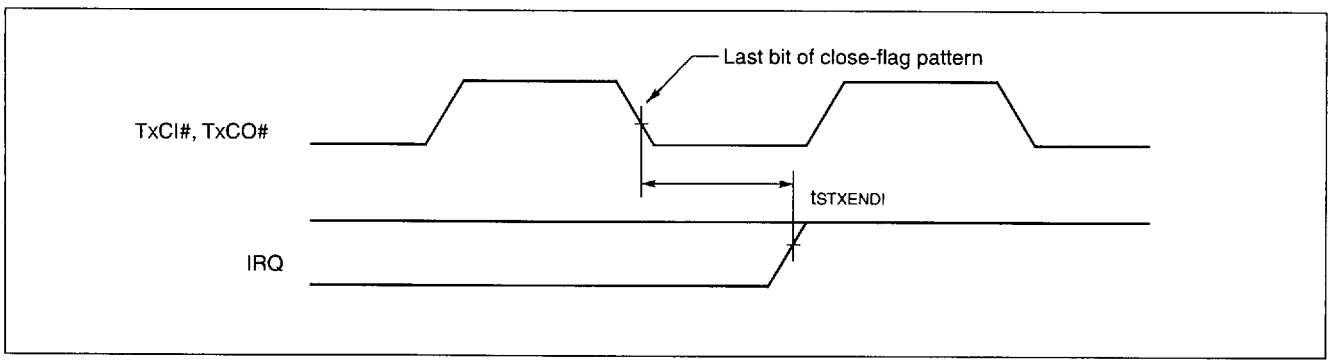


(11) Interrupt by Frame Termination

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter		Symbol	Min.	Max.	Unit
IRQ ↑ delay (TxC# ↓)	(Note)	$t_{STXENDI}$	—	3t_{CK}	ns

Note: TxC# denotes TxCI# or TxCO#; RxC# denotes RxCI# or RxCO#.

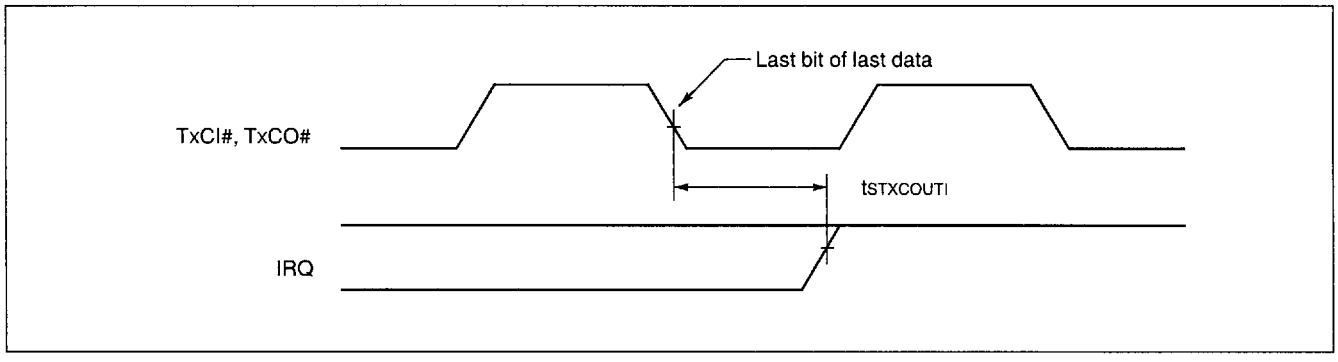


(12) Interrupt by Transmit Byte Counter

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter		Symbol	Min.	Max.	Unit
IRQ ↑ delay (TxC# ↓)	(Note)	$t_{STXCOUTI}$	—	3t_{CK}	ns

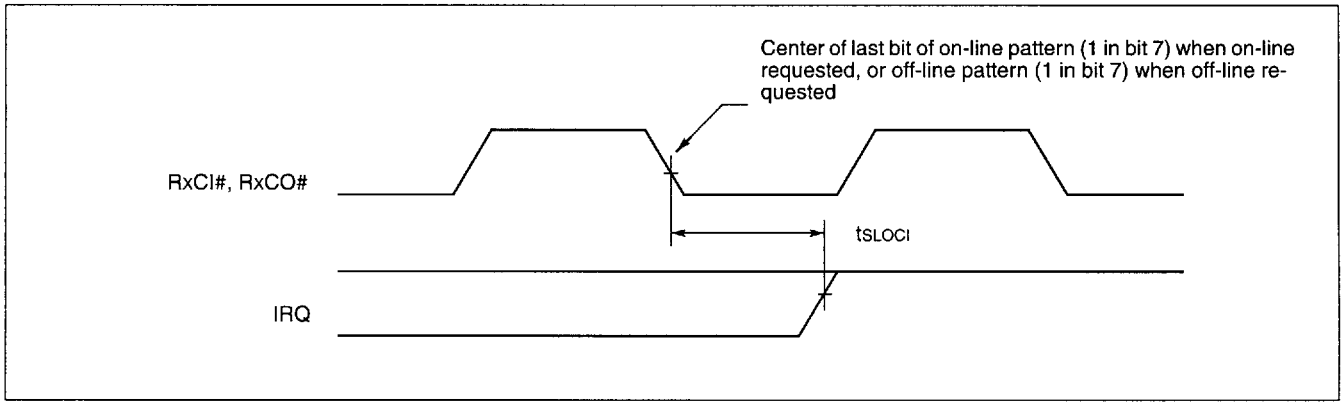
Note: TxC# denotes TxCI# or TxCO#; RxC# denotes RxCI# or RxCO#.



(13) Interrupt by Loop On-line

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

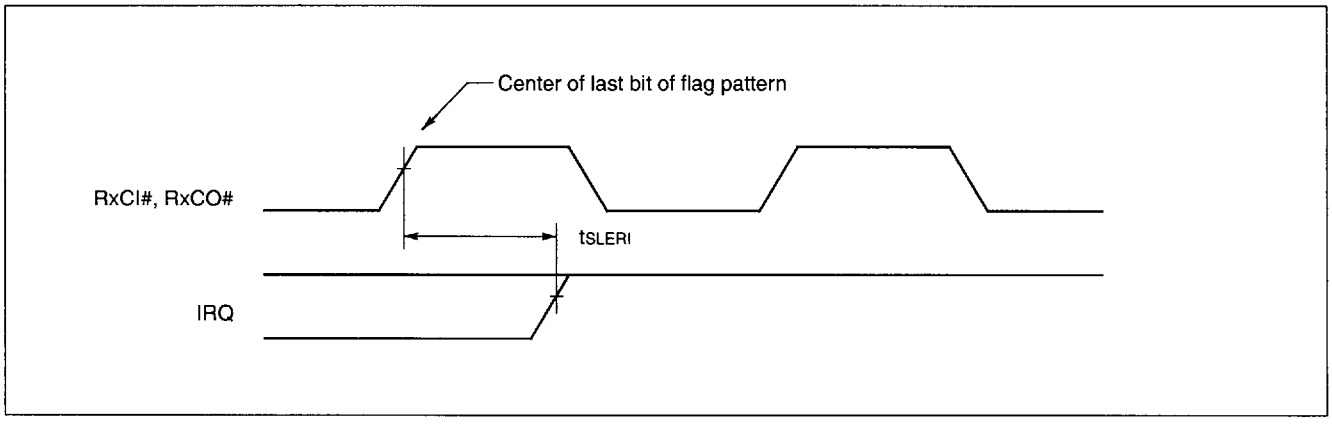
Parameter	Symbol	Min.	Max.	Unit
IRQ ↑ delay (RxC# ↑)	t_{SLOCI}	—	9t_{CK}	ns



(14) Interrupt by Loop Error

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

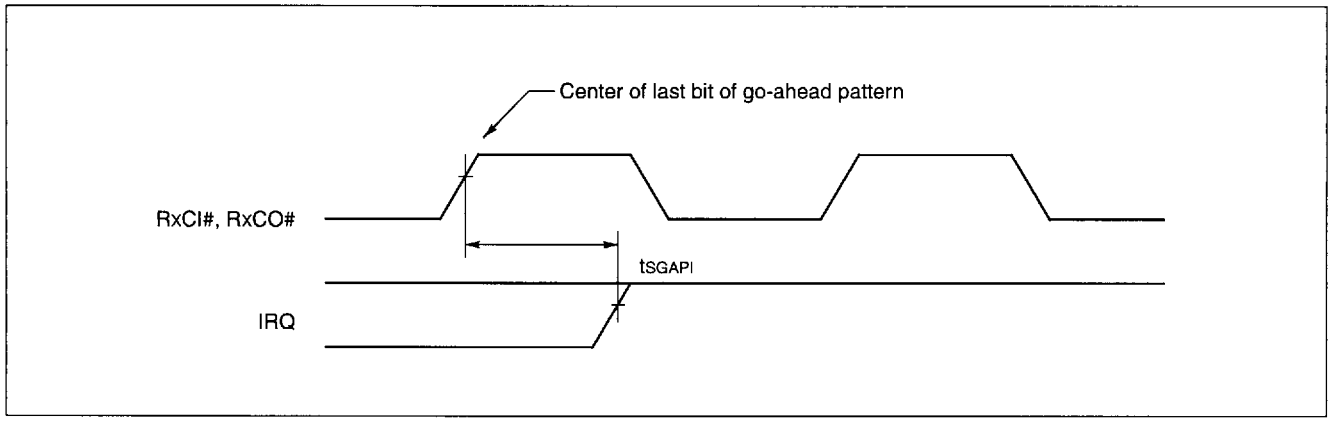
Parameter	Symbol	Min.	Max.	Unit
IRQ ↑ delay (RxC# ↑)	t_{SLERI}	—	5t_{CK}	ns



(15) Interrupt by Detection of Go-agead Pattern

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

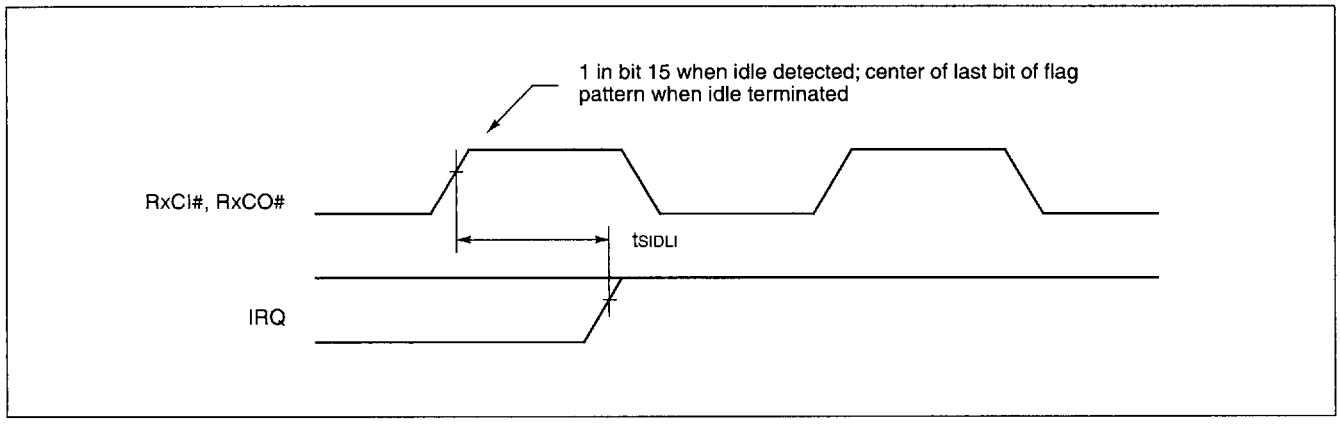
Parameter	Symbol	Min.	Max.	Unit
IRQ ↑ delay (RxC# ↑)	t_{SGAPI}	—	3t_{CK}	ns



(16) Interrupt by Idle Detection/Idle Termination

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

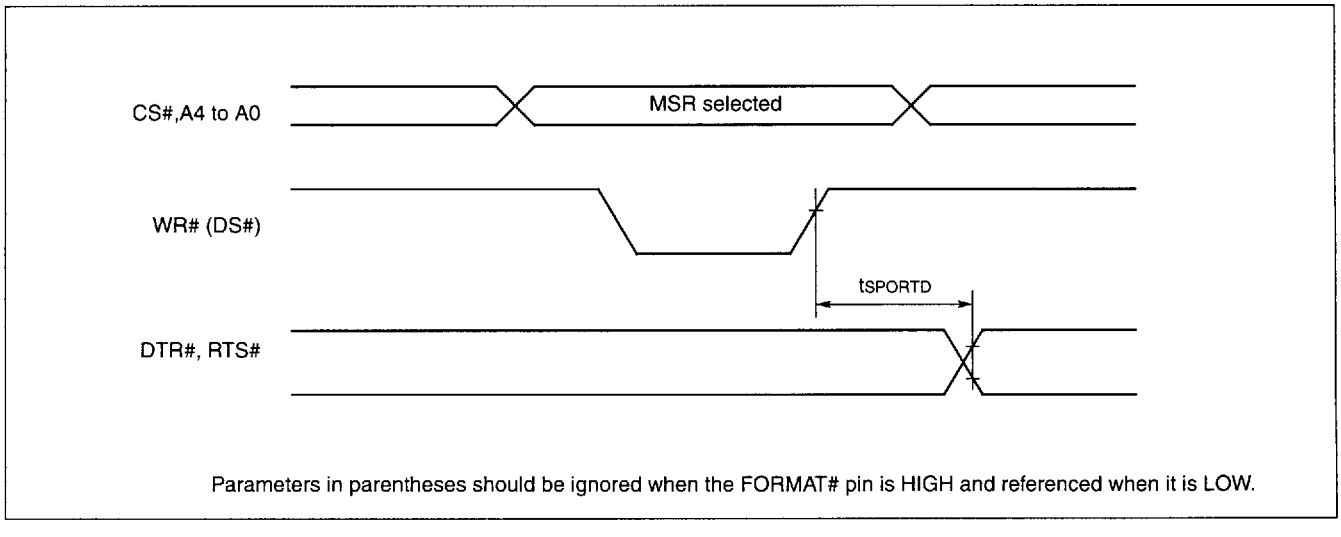
Parameter	Symbol	Min.	Max.	Unit
IRQ ↑ delay (RxC# ↑)	t_{SIDLI}	—	4t_{CK}	ns



(17) Output Modem Control Signal

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
Port output delay (WR#, DS# ↑)	t_{SPORTD}	—	2t_{CK} + 60	ns

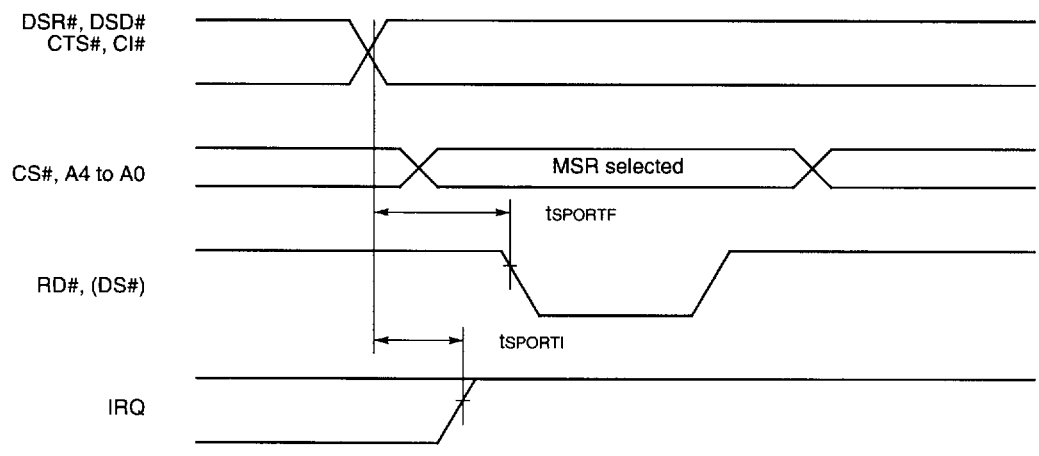


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(18) Input Modem Control Signal 1

(Vcc = +5 V ±10%, Vss = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ ↑ delay (Port ↓ ↑)	tSPORTI	—	4tCK	ns
Port input setting (RD#, DS# ↓)	tSPORTF	—	1tCK + tCKH + 60	

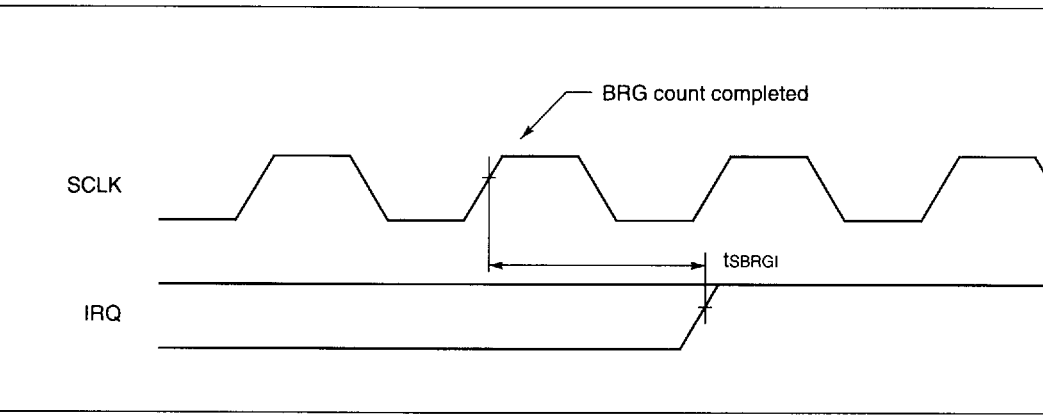


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(19) Input Modem Control Signal2

(Vcc = +5 V ±10%, Vss = 0 V, Ta = 0°C to +70°C)

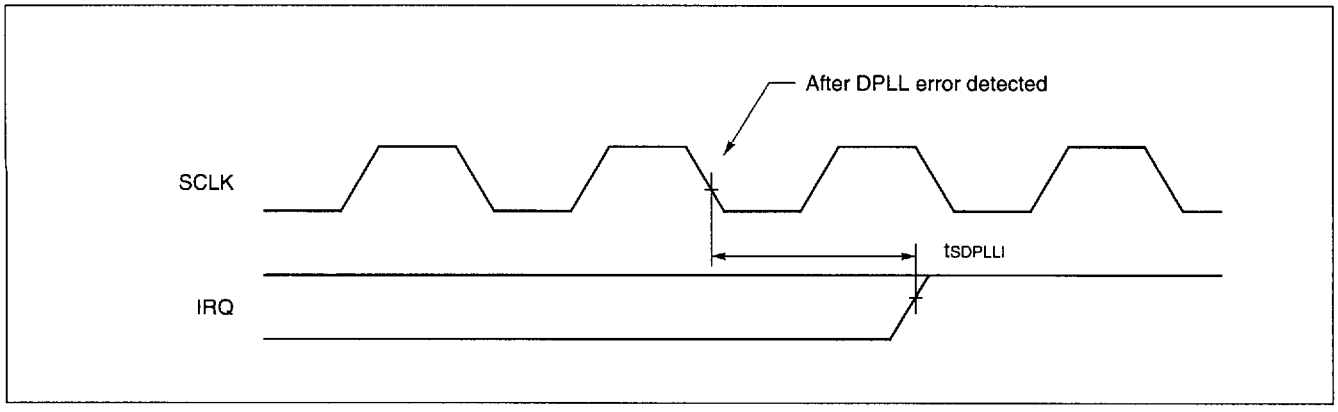
Parameter	Symbol	Min.	Max.	Unit
IRQ ↑ delay (SCLK ↓)	tSBRGI	—	5tCK + 250	ns



(20) Input Modem Control Signal 3

(Vcc = +5 V ±10%, Vss = 0 V, Ta = 0°C to +70°C)

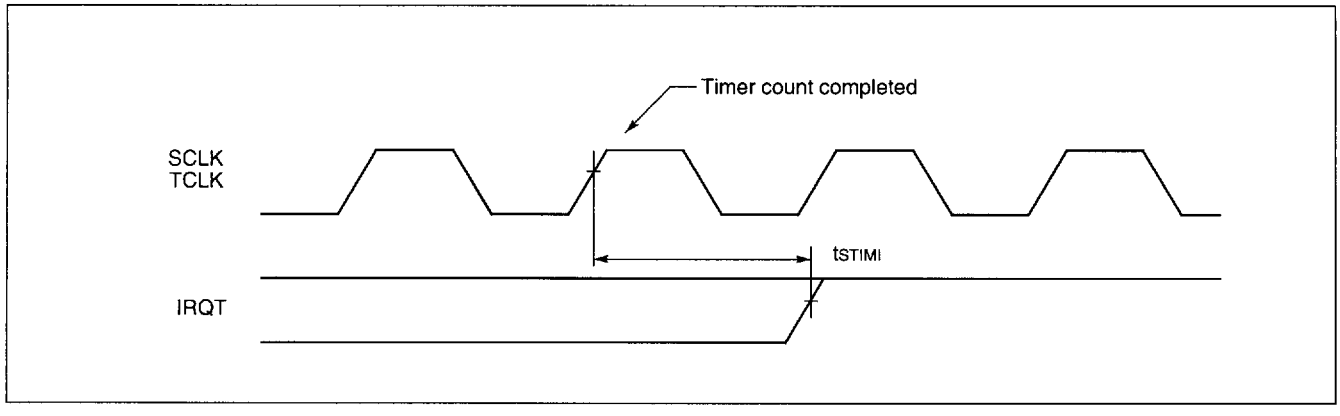
Parameter	Symbol	Min.	Max.	Unit
IRQ ↑ delay (SCLK ↓)	tSDPLLI	—	5tCK + 250	ns



(21) Input Modem Control Signal 4

(Vcc = +5 V ±10%, Vss = 0 V, Ta = 0°C to +70°C)

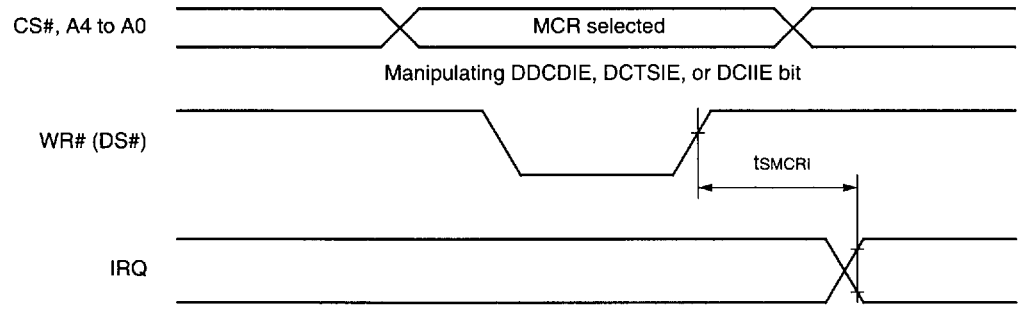
Parameter	Symbol	Min.	Max.	Unit
IRQT ↑ delay (SCLK, TCLK ↑)	tSTIMI	—	5tCK + 250	ns



(22) Interrupt Request Signal 1 by Manipulation of Each Interrupt Cause

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ delay (WR#, DS# ↑ – MCR)	t_{SMCRI}	—	3t_{CK}	ns

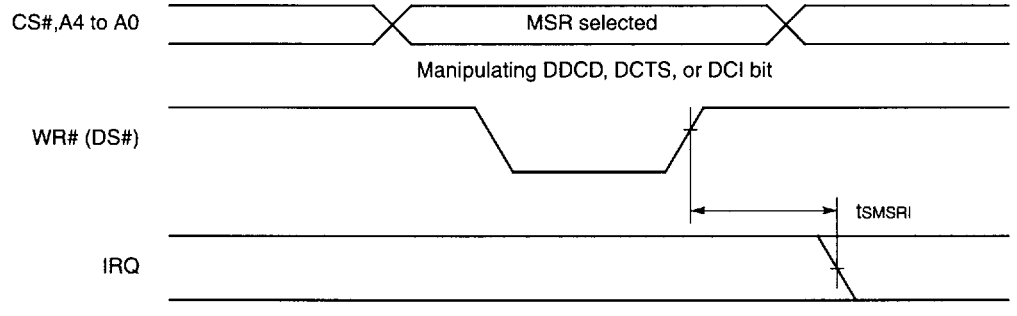


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(23) Interrupt Request Signal 2 by Manipulation of Each Interrupt Cause

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ ↓ delay (WR#, DS# ↑ – MSR)	t_{SMSRI}	—	3t_{CK}	ns

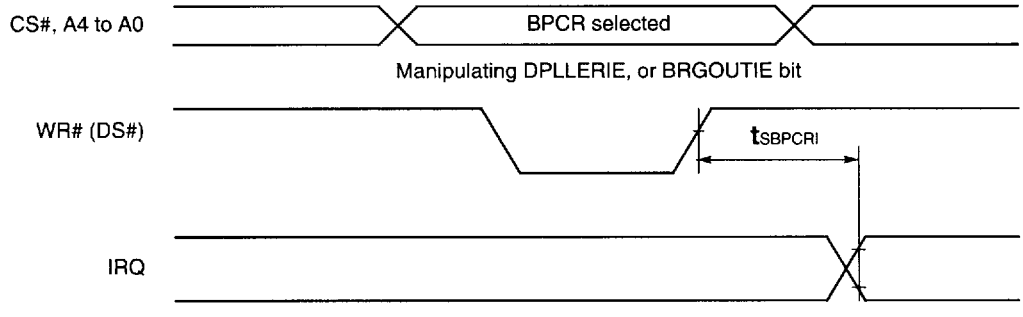


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(24) Interrupt Request Signal 3 by Manipulation of Each Interrupt Cause

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ delay (WR#, DS# ↑ –BPCR)	t_{SBPCRI}	—	3tCK	ns

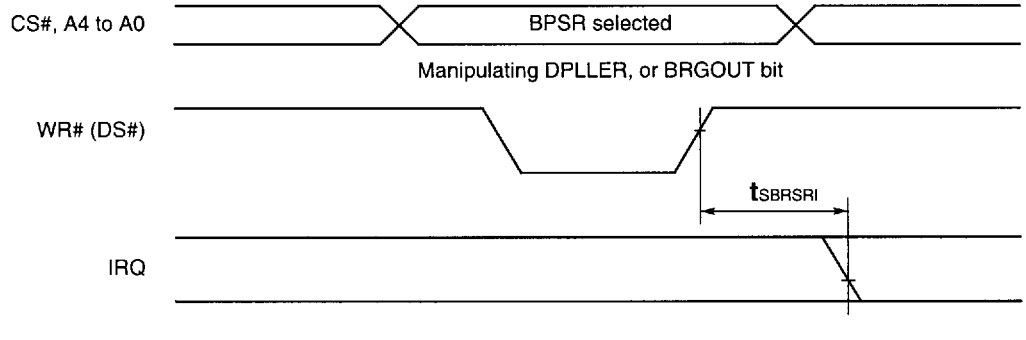


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(25) Interrupt Request Signal 4 by Manipulation of Each Interrupt Cause

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ ↓ delay (WR#, DS# ↑ –BPSR)	t_{SBPSRI}	—	3tCK	ns

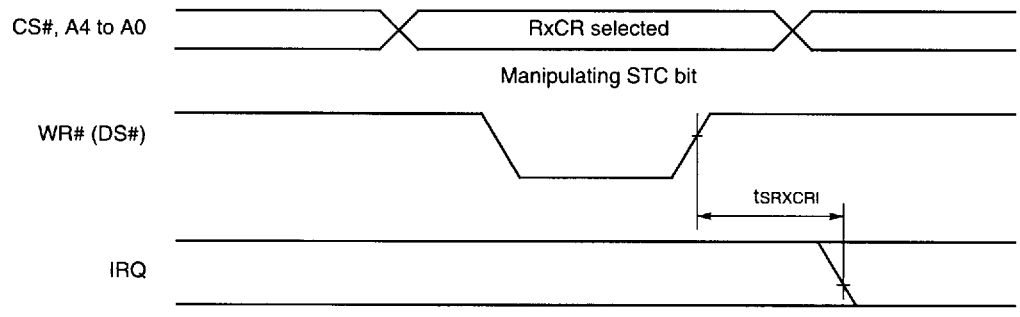


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(26) Interrupt Request Signal 5 by Manipulation of Each Interrupt Cause

(Vcc = +5 V ±10%, Vss = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ ↓ delay (WR#, DS# ↑ –RxCR)	tSRXCRI	—	4tCK	ns

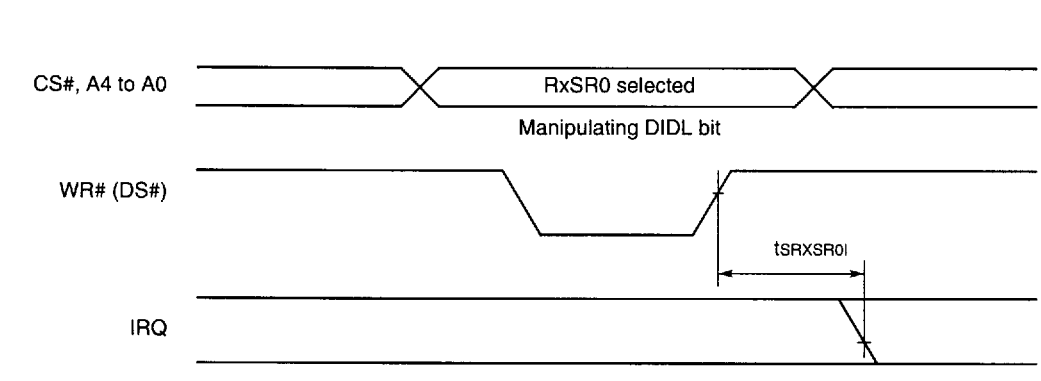


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(27) Interrupt Request Signal 6 by Manipulation of Each Interrupt Cause

(Vcc = +5 V ±10%, Vss = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ ↓ delay (WR#, DS# ↑ –RxSR0)	tSRXSR0I	—	3tCK	ns

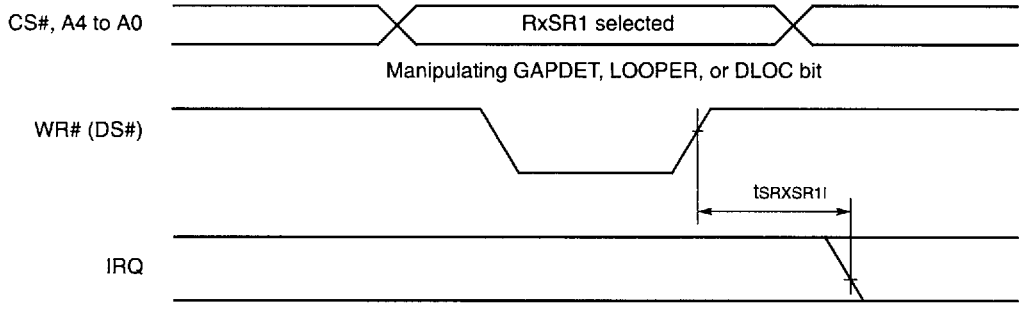


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(28) Interrupt Request Signal 7 by Manipulation of Each Interrupt Cause

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ ↓ delay (WR# DS# ↑ –RxSR1)	$t_{SRXSRXI}$	—	3tCK	ns

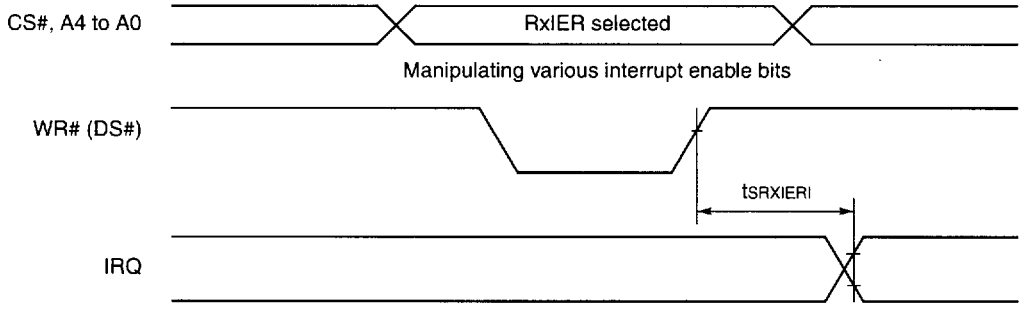


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(29) Interrupt Request Signal 8 by Manipulation of Each Interrupt Cause

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ delay (WR#, DS# ↑ –RxIER)	$t_{SRXIERI}$	—	3tCK	ns

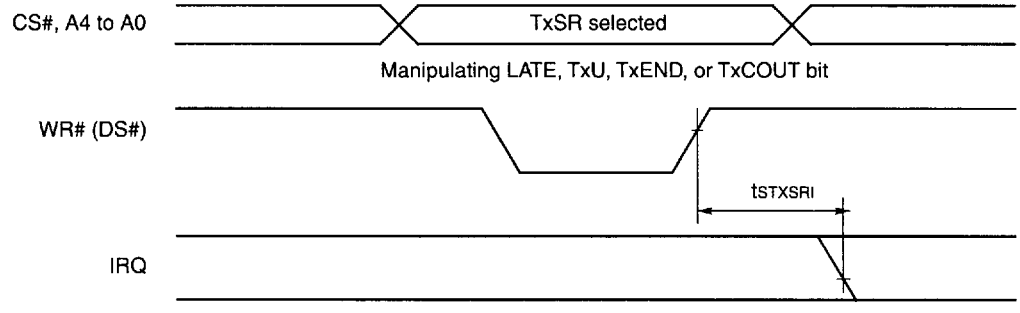


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(30) Interrupt Request Signal 9 by Manipulation of Each Interrupt Cause

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ ↓ delay (WR#, DS# ↑ –TxSR)	t_{STXSRI}	—	3tCK	ns

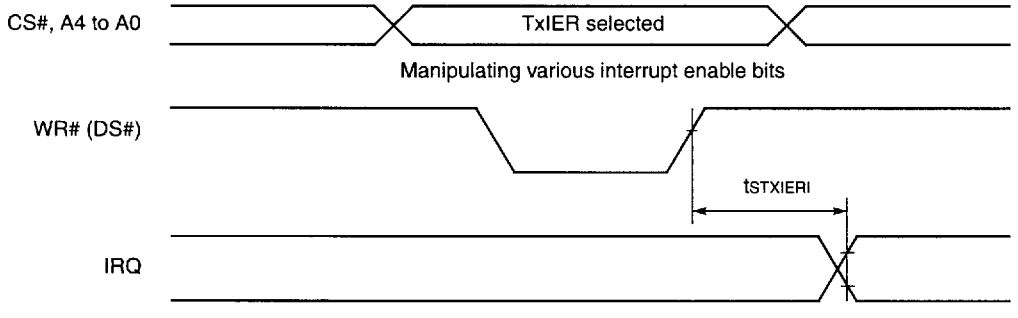


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(31) Interrupt Request Signal 10 by Manipulation of Each Interrupt Cause

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ delay (WR#, DS# ↑ –TxIER)	$t_{STXIERI}$	—	3tCK	ns

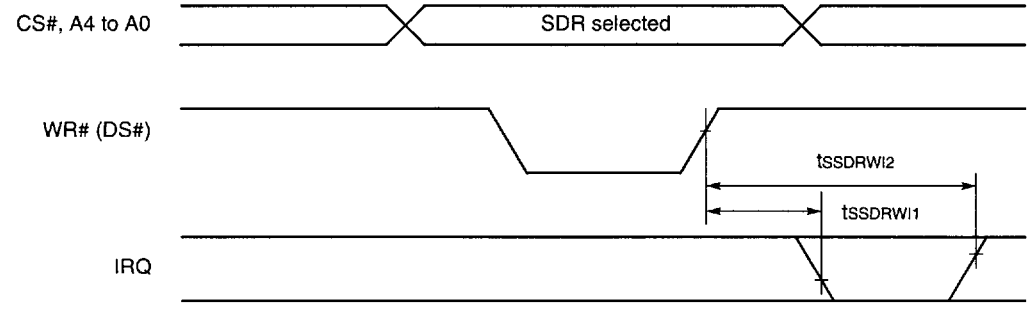


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(32) Interrupt Request Signal 11 by Manipulation of Each Interrupt

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ ↓ delay (WR#, DS# ↑ –SDR)	$t_{SSDRWI1}$	—	4tCK	ns
IRQ ↓ delay (WR#, DS# ↑ –SDR)	$t_{SSDRWI2}$	—	5tCK	

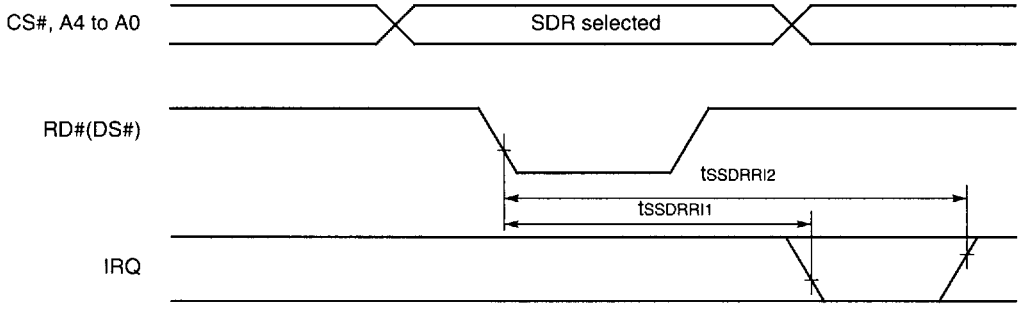


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(33) Interrupt Request Signal 12 by Manipulation of Each Interrupt Cause

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ ↓ delay (WR#, DS# –SDR) ↓	$t_{SSDRRI1}$	—	4tCK	ns
IRQ ↓ delay (WR#, DS# –SDR) ↓	$t_{SSDRRI2}$	—	5tCK	

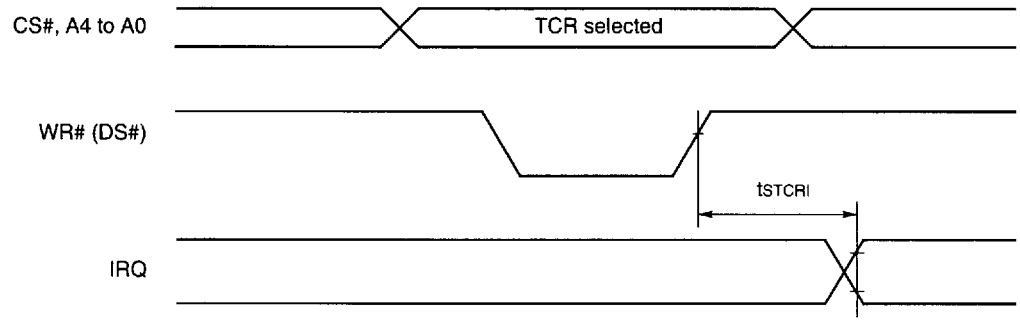


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(34) Interrupt Request Signal 13 by Manipulation of Each Interrupt Cause

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ delay (WR#, DS# ↑ –TCR)	t_{STCRI}	—	3t_{CK}	ns

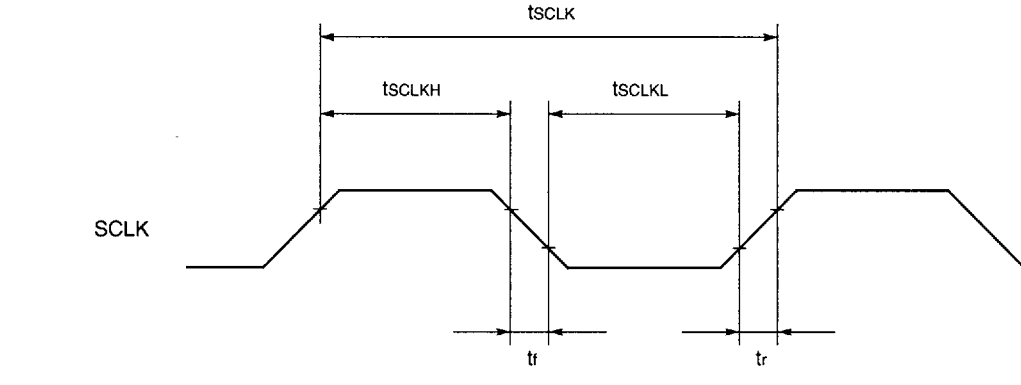


Parameters in parentheses should be ignored when the FORMAT# pin is HIGH and referenced when it is LOW.

(35) SCLK Input

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

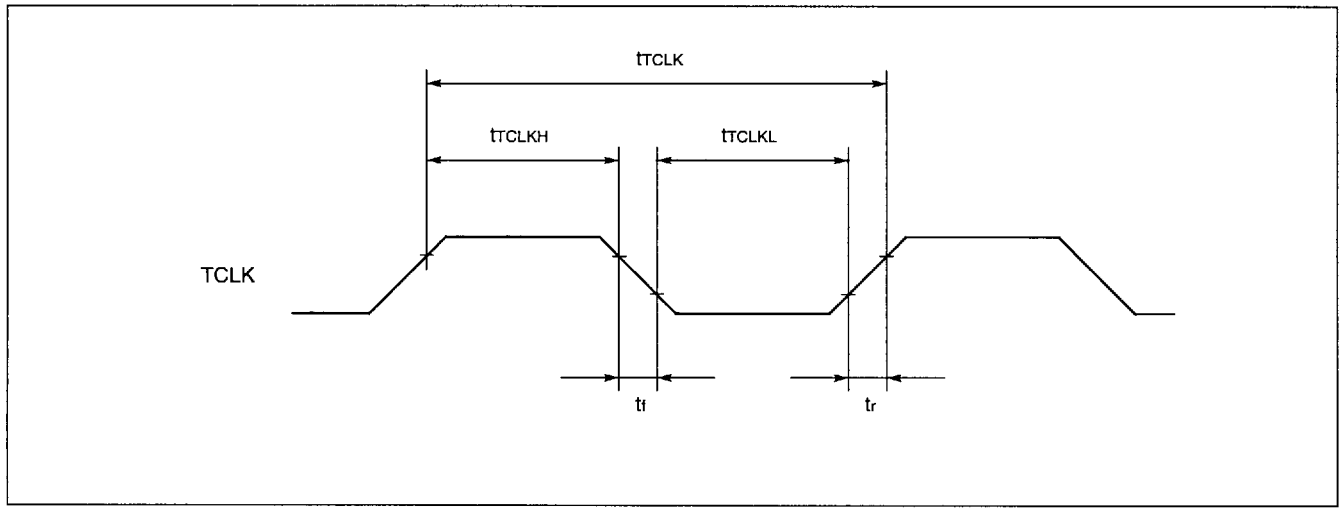
Parameter	Symbol	Min.	Max.	Unit
External clock period	t_{SCLK}	100	—	ns
LOW-level external clock pulse duration	t_{SCLKL}	40	—	
HIGH-level external clock pulse duration	t_{SCLKH}	40	—	



(36) TCLK Input

(Vcc = +5 V ±10%, Vss = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
Timer clock period	t_{TCLK}	100	—	ns
LOW-level timer clock pulse duration	t_{TCLKL}	40	—	
HIGH-level timer clock pulse duration	t_{TCLKH}	40	—	

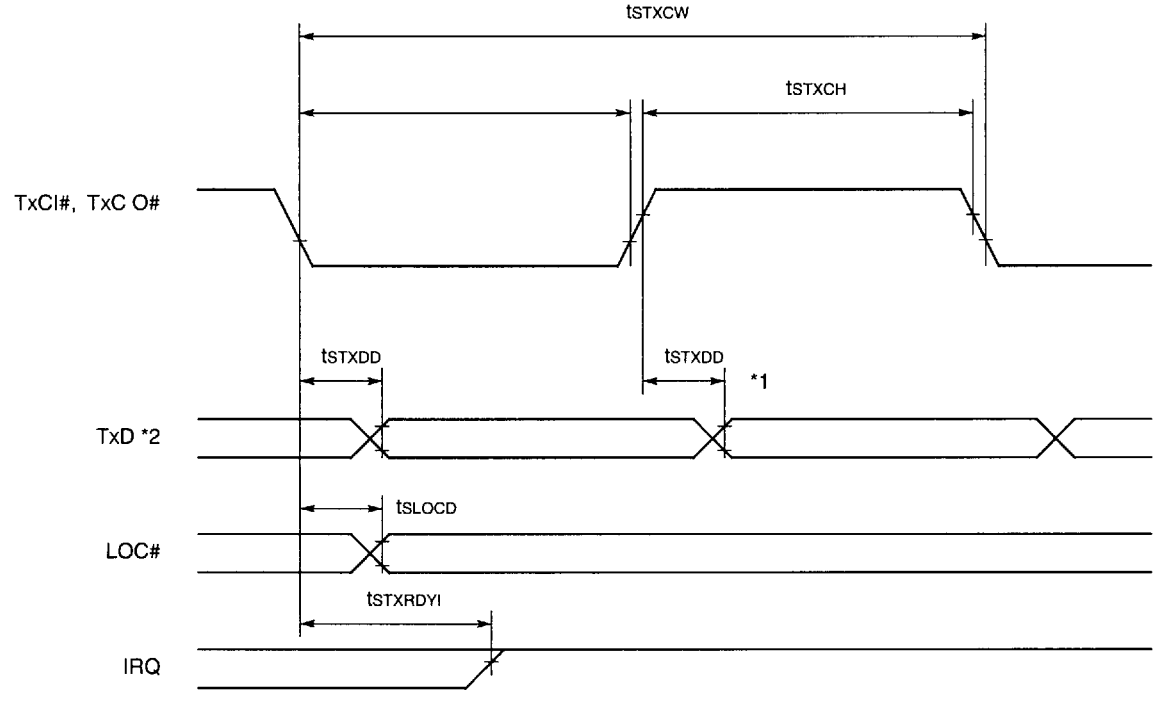


(37) Transmit Clock and Transmit Data

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ ↑ delay (TxC# ↓) (Note 1)	$t_{STXRDYL}$	—	6t_{CK}	ns
TxCI# clock period	t_{STXCW}	4t_{CK} (Note 2)	—	
LOW-level TxCI# clock pulse duration	t_{STXCL}	1t_{CK} + 40 (Note 3)	—	
HIGH-level TxCI# clock pulse duration	t_{STXCH}	1t_{CK} + 40 (Note 3)	—	
TxD delay (TxC#)	t_{STXDD}	—	100	
LOC# delay (TxC#)	t_{SLOCD}	—	100	

Notes: 1. TxC# denotes TxCI# or TxCO#; RxC# denotes RxCI# or RxCO#
2. In LOOP mode: if NRZ or NRZI code, the minimum level is 8 t_{CK}; if FM0, FM1, or Manchester code, the minimum level is 12 t_{CK}.
3. In LOOP mode: if NRZ or NRZI code, the minimum level is 3 t_{CK}+40; if FM0, FM1, or Manchester code, the minimum level is 5 t_{CK}+40.



*1: No change if NRZ or NZRI code

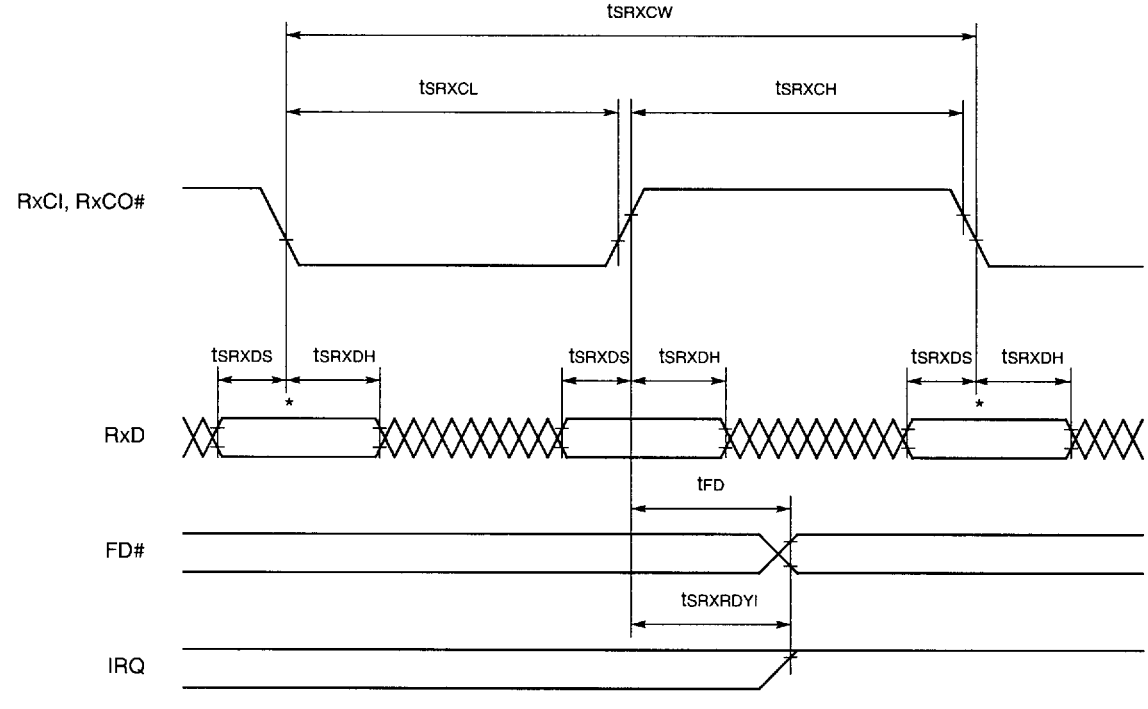
*2: When the Send High (SH) or Send Break (SB) bit of the TxCR register is enabled, output is assumed after a maximum of 3 t_{CK} from the rising edge of WR# (DS#).

(38) Receive Clock and Receive Data

(V_{CC} = +5 V ±10%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
IRQ ↑ delay (RxC# ↑) (Note 1)	$t_{SRXRDYI}$	—	4t_{CK}	ns
RxCI# clock period	t_{SRXCW}	4t_{CK} (Note 2)	—	
LOW-level RxCI# clock pulse width	t_{SRXCL}	1t_{CK} + 40 (Note 3)	—	
HIGH-level RxCI# clock pulse width	t_{SRXCH}	1t_{CK} + 40 (Note 3)	—	
RxD setup time (RxC#)	t_{SRXDS}	0	—	
RxD hold time (RxC#)	t_{SRXDH}	160	—	
FD# output delay (RxC#)	t_{FD}	—	3t_{CK}	

Notes: 1. Interrupt timing due to RxRDY bit, receive errors (CRCER, OER, SFER), frame termination (EOF, ADET)
2. In LOOP mode: if NRZ or NRZI code, the minimum level is 8 t_{CK}; if FM0, FM1, or Manchester code, the minimum level is 12 t_{CK}.
3. In LOOP mode: if NRZ or NRZI code, the minimum level is 3 t_{CK}+40; if FM0, FM1, or Manchester code, the minimum level is 5 t_{CK}+40.



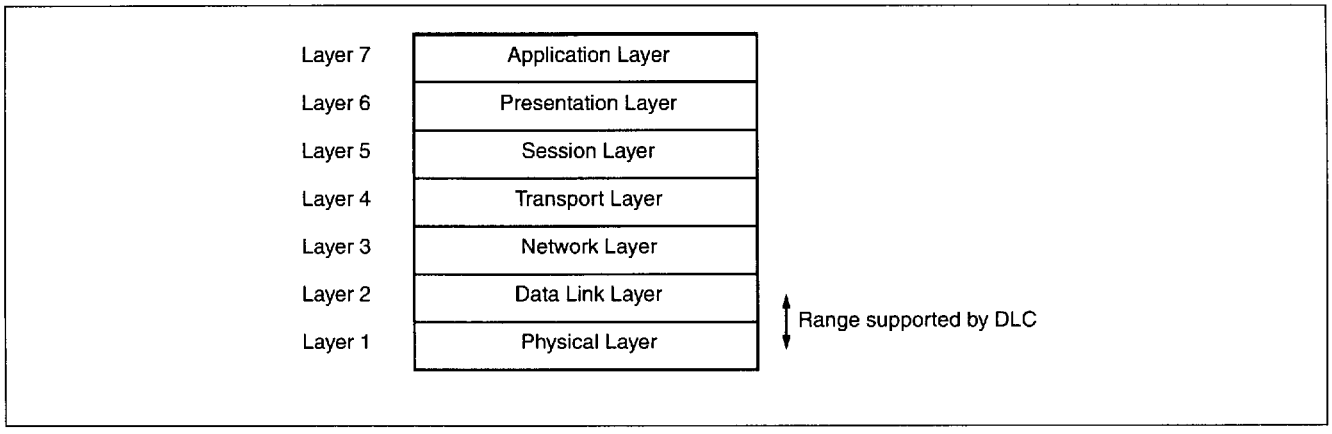
* When FM0 and FM1 code, the first value of the data bit must be defined.

■ FUNCTIONAL OVERVIEW

1. DLC Position in Systems

(1) Supported Range of OSI Models

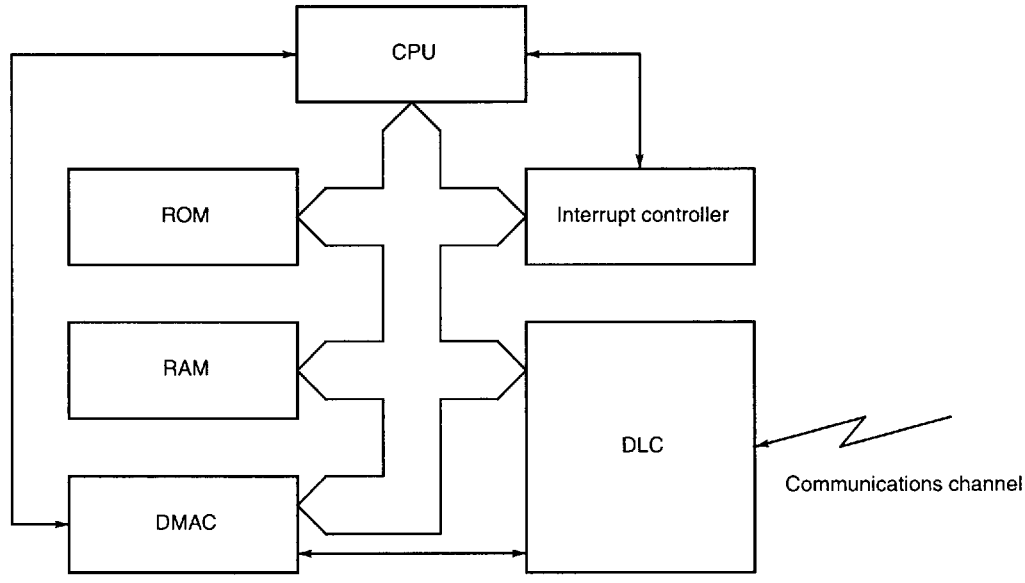
The DLC supports the HDLC-recommended frame format function for Layer 2 (Data Link Layer) of the seven layers of OSI models. It also supports the X.21 bis-recommended modem control interface for Layer 1 (Physical Layer).



(2) Typical System Configuration

Figure 1 shows a typical system configuration using the DLC.

Fig. 1 Typical System Configuration



2. Functional Description

When it is used in microcomputer systems, the DLC manages the serial communications interface by controlling the transfer of Bit Oriented Protocol (BOP) serial data in full-duplex communications.

At receiving, it compares the addresses in the HDLC frame input from the communications line, checks the Frame Check Sequence (FCS), and deletes 0s in frames.

If the addresses match, the DLC receives the frame, in which case the address is accepted as part of the received data. If the addresses do not match, the DLC ignores the frame.

When CRC is enabled, the DLC checks the FCS in the received frame and indicates the results in the status register. In this case, the FCS data is not accepted as part of the received data. When CRC is disabled, the DLC does not check the FCS, but handles it as part of the received data.

At transmitting, the DLC sends the flag pattern, generates and adds the FCS, and inserts 0s in the frame. Addresses are not sent automatically .

Address						Register Name	Abbreviation	Bit Configuration							
CS#	A4	A3	A2	A1	A0			bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	0	Protocol select	SMR0	Unused	Unused	Unused	Unused	PS3	PS2	PS1	PS0
0	0	0	0	0	1	CRC select	SMR1	Unused	Unused	Unused	PRS	CRCM1	CRCM0	Unused	Unused
0	0	0	0	1	0	Transfer mode	SMR2	TURN	CODE2	CODE1	CODE0	RXC1	RXC0	TXC1	TXC0
0	0	0	0	1	1	Character 0	CHRR0	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	1	0	0	Character 1	CHRR1	A15/D7	A14/D6	A13/D5	A12/D4	A11/D3	A10/D2	A9/D1	A8/D0
0	0	0	1	0	1	Reserved									
0	0	0	1	1	0	Modem status	MSR	Unused	DCI	DI	DSR	DDCD	DCTS	DCD	CTS
0	0	0	1	1	1	Modem control	MCR	DDCDIE	DCTSIE	DCIIE	Unused	CTSAUTO	Unused	DTR	RTS
0	0	1	0	0	0	Receive status 0	RXSR0	ADET	EOF	SFER	OER	CRCER	RXIDL	DIDL	RXRDY
0	0	1	0	0	1	Receive status 1	RXSR1	GAPDET	FDET/LOOPER	DLOC	LOC	Unused	RBL2	RBL1	RBL0
0	0	1	0	1	0	Receive control	RXCR	RXE	Unused	Unused	Unused	Unused	Unused	HUNT	STC
0	0	1	0	1	1	Receive interrupt enable	RXIER	RXD/I	GAPDETIE	LOOPERIE	DLOCIE	ENDIE	ERRIE	DIDLIE	RXRDYIE
0	0	1	1	0	0	Transmit status	TXSR	LATE	Unused	Unused	TXCOUT	TXEND	TXEMP	TXU	TXRDY
0	0	1	1	0	1	Transmit control	TXCR	TXE	SH	SB	IDLS	TXRST	SA	OFD	TXLAST
0	0	1	1	1	0	Transmit interrupt enable	TXIER	TXD/I	Unused	Unused	TXCOUTIE	TXENDIE	LATEIE	TXUIE	RXRDYIE
0	0	1	1	1	1	Serial data	SDR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	Transmit byte counter 0	TXBCR0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	Transmit byte counter 1	TXBCR1	D15	D14	D13	D12	D11	D10	D9	D8
0	1	0	0	1	0	Transmit flag 0	TXFR0	N7	N6	N5	N4	N3	N2	N1	N0
0	1	0	0	1	1	Transmit flag 1	TXFR1	FOUT	Unused	Unused	Unused	N3	N2	N1	N0
0	1	0	1	0	0	Transmit mode	SMR3	Unused	TXBRGEN	FD/DTR	NRZIM	TXCSM	TXCOUTEND	TXUEND	TXLASTEND
0	1	0	1	0	1	Port	PORTR	PI0	PI2	PI1	PI0	PO3	PO2	PO1	PO0
0	1	0	1	1	0	Request	REQR	TXDRQ	RXDRQ	Unused	Unused	Unused	IMODEM	ITX	IRX
0	1	0	1	1	1	Mask	MASKR	MTXDRQ	MRXDRQ	Unused	Unused	Unused	MMODEM	MTX	MRX
0	1	1	0	0	0	BRG1/DPLL status	B1PSR	Unused	Unused	Unused	Unused	Unused	Unused	DPLLER	BRG1OUT
0	1	1	0	0	1	BRG1/DPLL control	B1PCR	DPLLERIE	TS	BRG1OUTIE	BRG1G	N3	N2	N1	N0
0	1	1	0	1	0	BRG1 divide value	BG1DR	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0
0	1	1	0	1	1	Reserved									
0	1	1	1	0	0	BRG2 status	B2SR	Unused	Unused	Unused	Unused	Unused	Unused	Unused	BRG2OUT
0	1	1	1	0	1	BRG2 control	B2CR	BRG2CLK	BRG2OUTIE	BRG2EN	BRG2G	N3	N2	N1	N0
0	1	1	1	1	0	BRG2 divide value	BG2DR	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0
0	1	1	1	1	1	Reserved									
1	X	X	X	X	X	No Access									

0:LOW level, 1:HIGH level, X:Don't Care

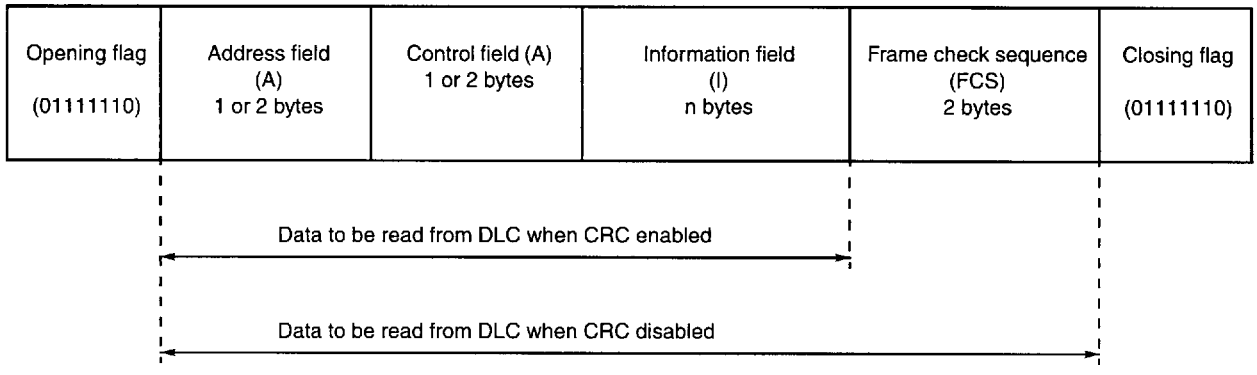
*Access (read/write) to 'reserved' register locations is inhibited. Allocating other peripheral LSI registers to these locations is also inhibited.

■ DATA FORMAT

1. Receiving

Figure 2 shows the receive data format supported by the DLC.

Fig. 2 Receive Data Format

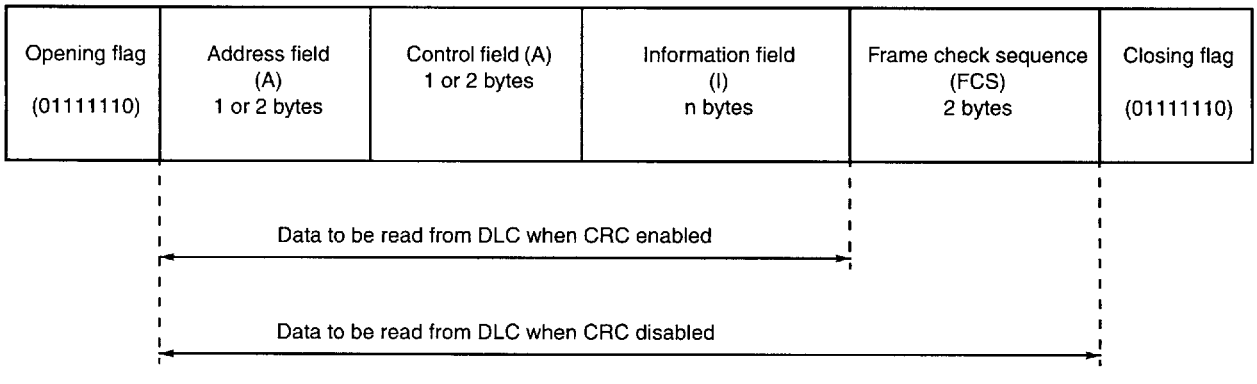


- The data in the address field is always read from the DLC regardless of whether address comparison is specified.
- When CRC is enabled, the FCS data is used only for the CRC check and is not read from the DLC.
- The data in the control and information fields can be read from the DLC.

2. Transmitting

Figure 3 shows the transmit data format supported by the DLC.

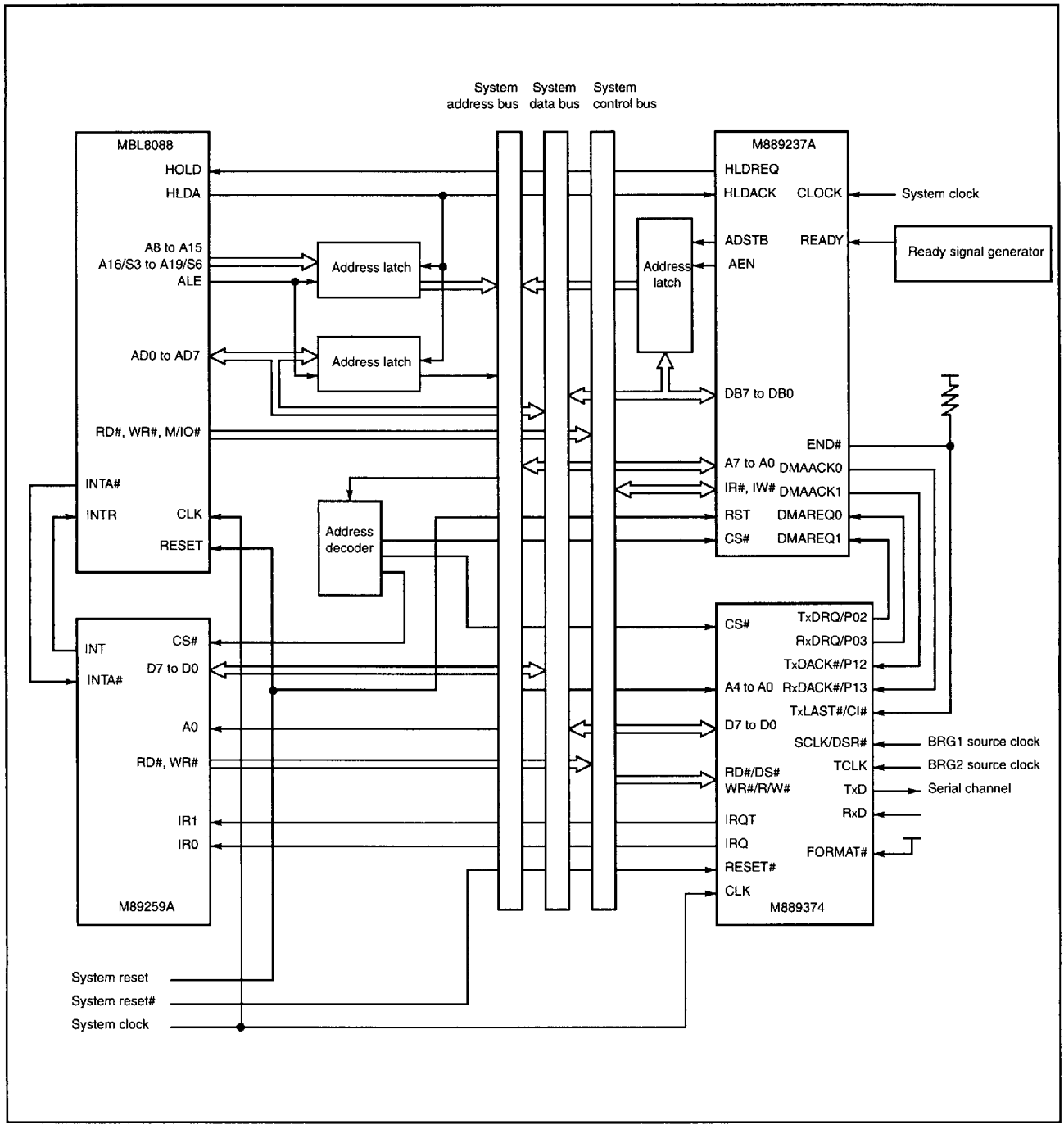
Fig. 3 Transmit Data Format



- The data in the address field is written as the transmit data to the DLC.
- When CRC is enabled, the FCS data is transmitted automatically to the DLC.
- The data in the control and information fields can be written to the DLC.

■ APPLICATION EXAMPLES

1. Example of System Configuration



2. Example of Application Software

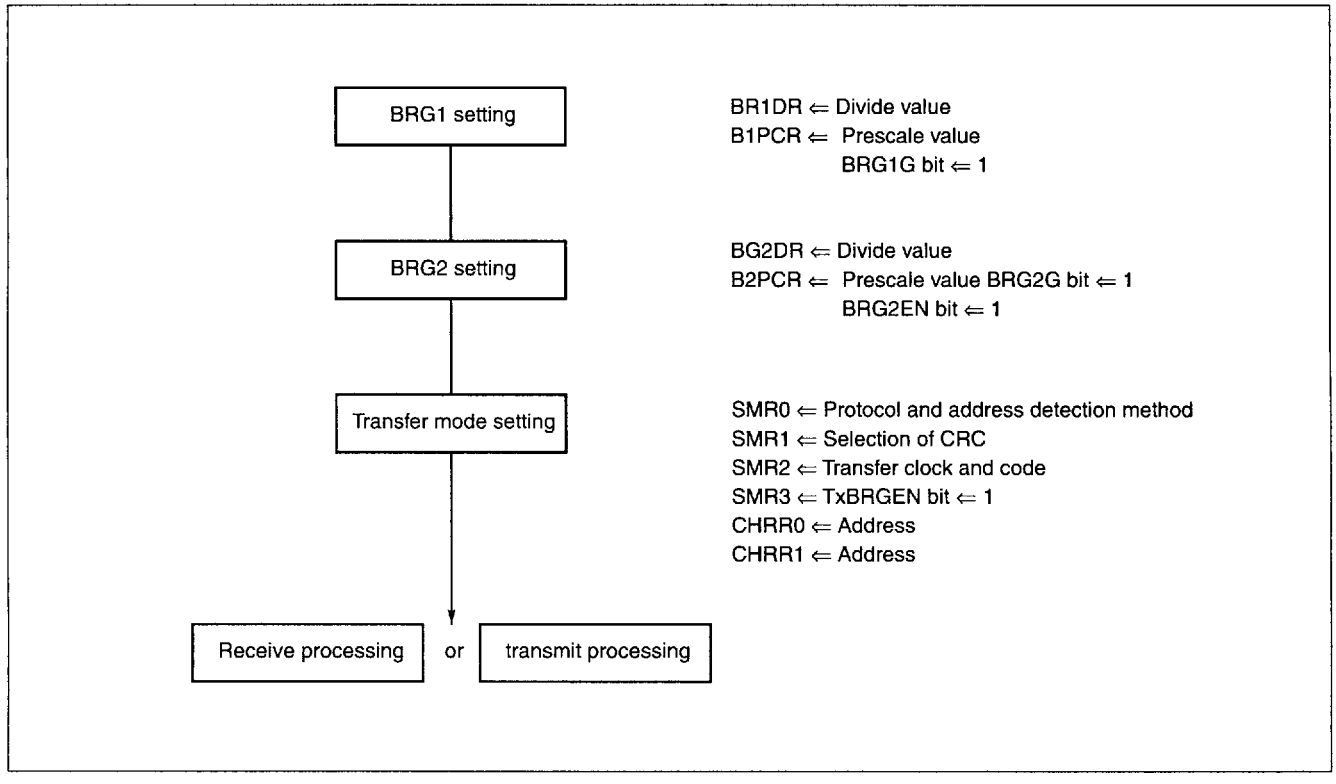
An example of how to use the DLC is shown below.

(1) Operating Conditions

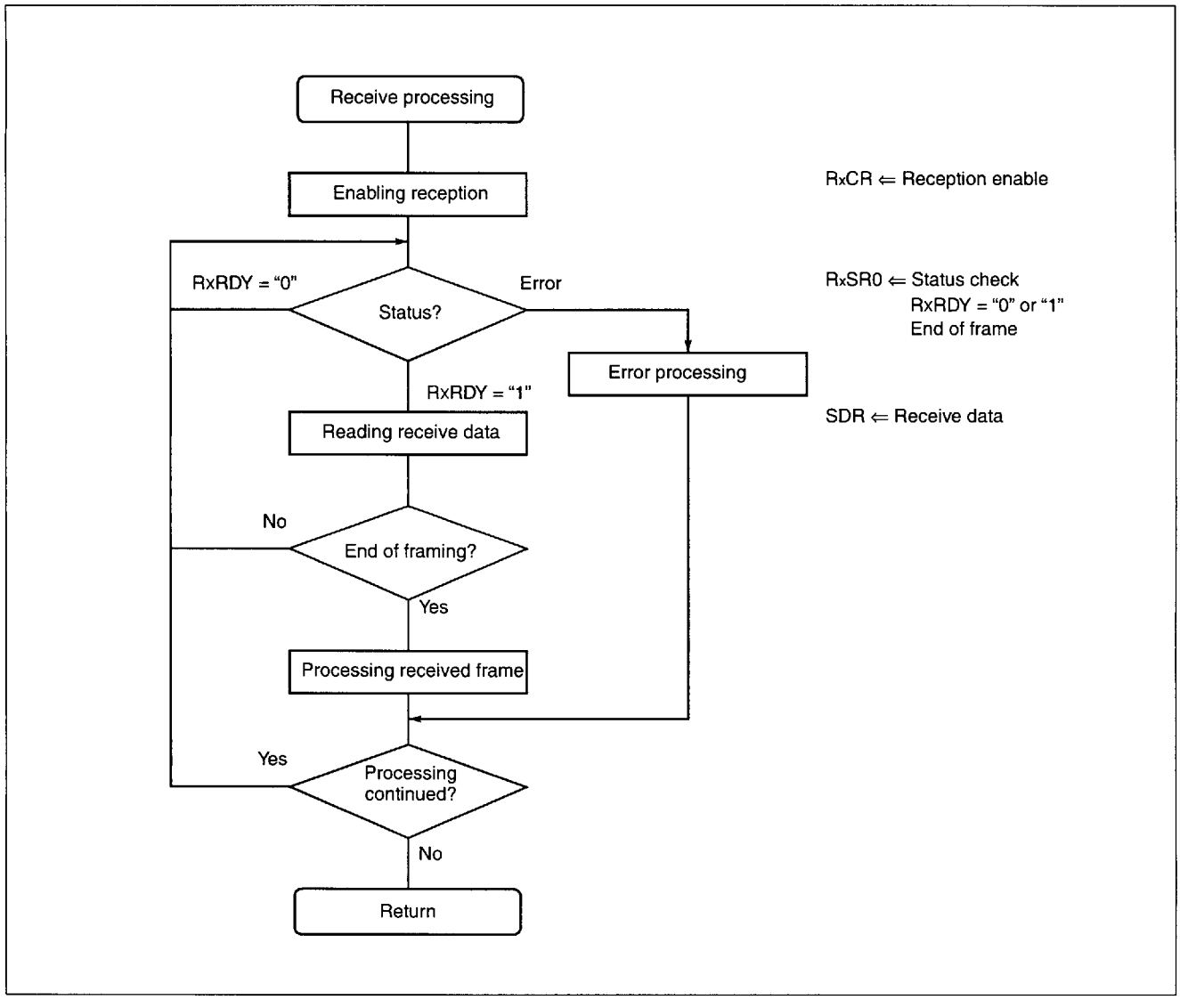
- BRG1 is used as the receive clock.
- BRG2 is used as the transmit clock.

(2) Flowchart

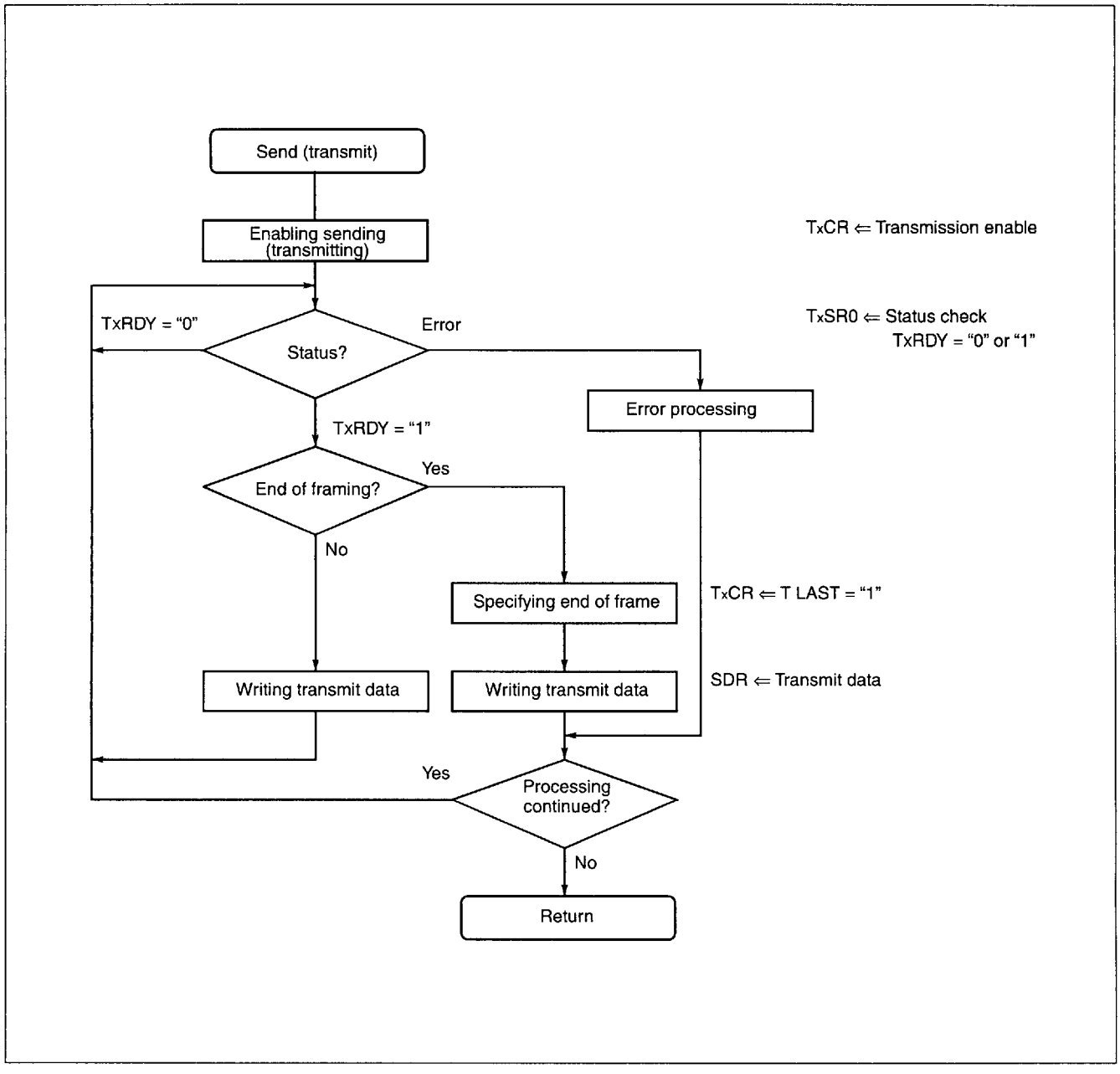
- Initial settings



- Receiving Flow



- Transmitting Flow



■ USAGE PRECAUTIONS

1. Reserved addresses in register map

Do not access reserved addresses or allocate the registers of other LSIs to these addresses.

2. Protocol select register, CRC select register, and transfer mode register

Always set these registers before enabling transmission or reception.

3. Transmit and receive interrupt enable registers

Do not enable interrupts for the TxRDY bit or RxRDY bit when making DMA requests.

4. Using BRG1 or BRG2 as interval timer

When using BRG1 or BRG2 as an interval timer, do not set 0s at all the bits of the BRG1 divide value register (BG1DR) or the BRG2 divide value register (BG2DR).

5. Using BRG as transfer clock

When using BRG as a transfer clock, always set the division value at the BRG1 or BRG2 register before setting the clock source with the transfer mode register (SMR2). For details on the setting procedure, refer to the MB89374 User's Manual.

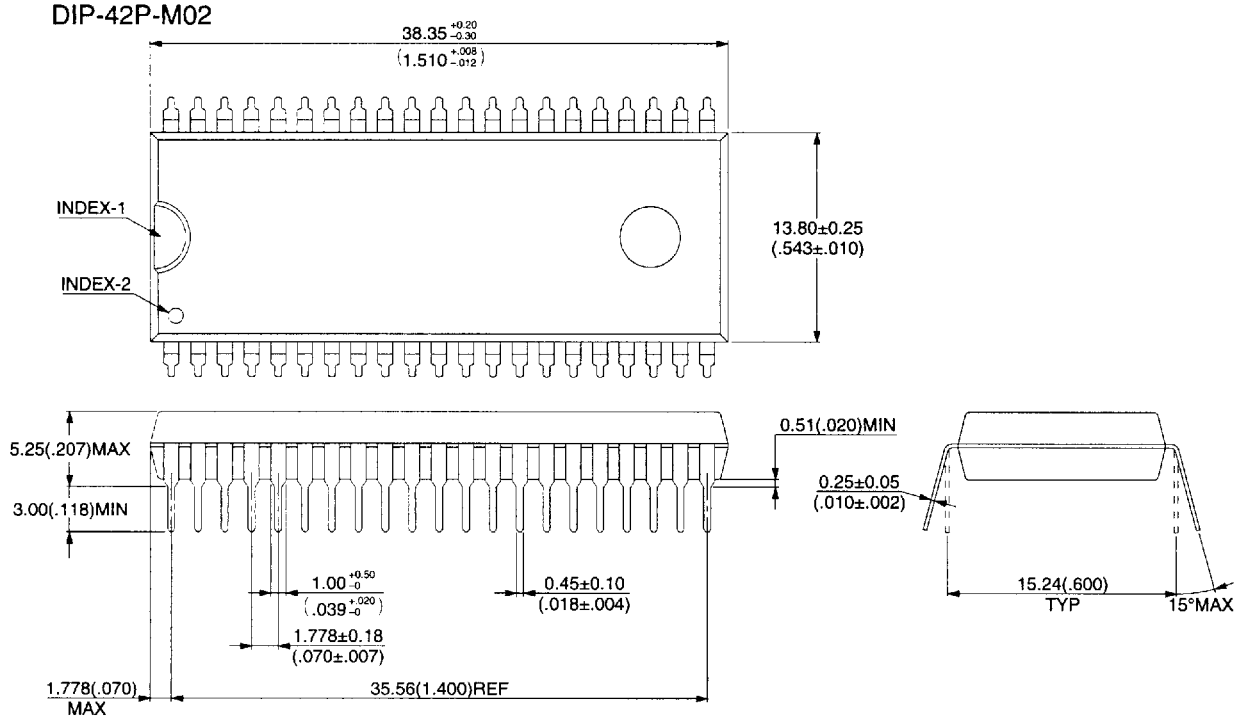
■ ORDERING INFORMATION

Part number	Package	Remarks
MB89374P-SH	42-pin plastic SH-DIP (DIP-42P-M02)	
MB89374PFQ	48-pin plastic QFP (FPT-48P-M13)	

■ PACKAGE DIMENSIONS

42 pin, Plastic SH-DIP

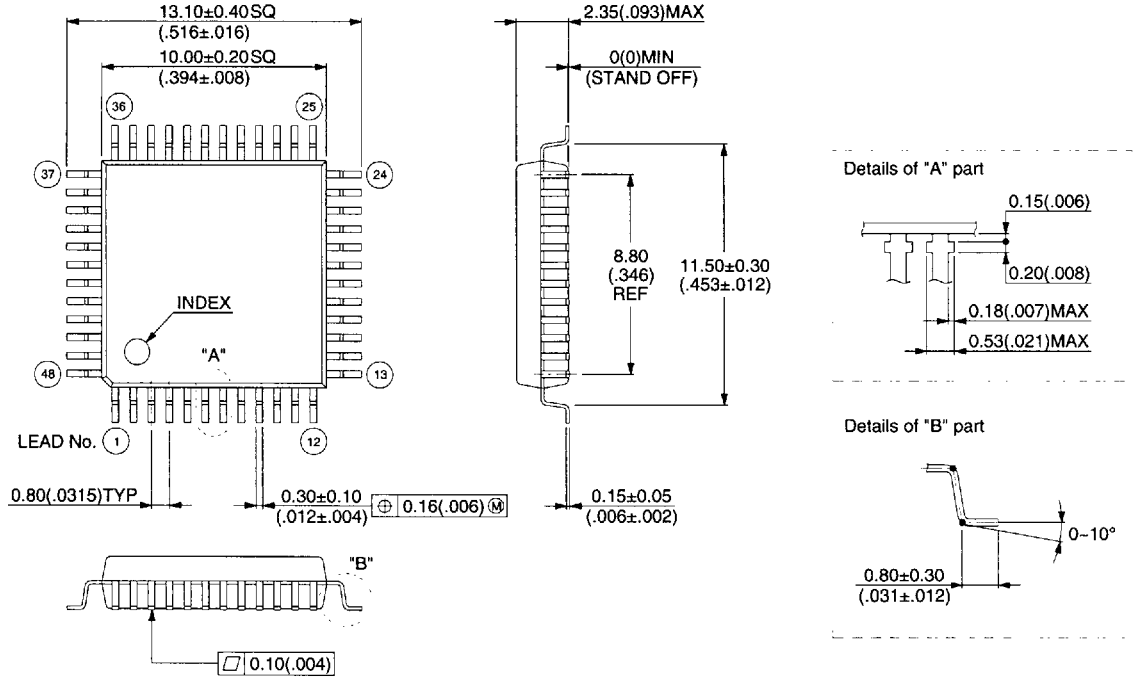
DIP-42P-M02



Dimensions in mm (inches).

(Continued)

48 pin, Plastic QFP
FPT-48P-M13



Dimensions in mm (inches).