Advance Information

MC13181/D
Rev. 0, 08/2002

Wireless Power Management Integrated Circuit

MOTOROLA
intelligence everywhere™

digital dna™

MC13181

(Scale 2:1)

Package Information
Plastic Package
Case 1307
(QFN-24)

Ordering Information

Device	Marking	Package
MC13181R2	13180	QFN-24

The MC13181 Wireless Power Management Integrated Circuit (PMIC) is a monolithic IC designed for hand-held electronics products in conjunction with the Motorola Bluetooth™ chipset (the MC13180 Bluetooth Radio and MC71000 Bluetooth Protocol Controller) or stand-alone in other products. The MC13181 is ideal for devices operating from a 3.6 V single-cell Lithium-ion battery or other energy systems in the 2.85 to 6.5 V range. The IC features three independently enabled Low Drop Out (LDO) Linear Voltage Regulators for powering baseband, audio, RF/IF, and interface circuitry. A comparator with logic-enabled hysteresis and one scaled input is provided for use as a low-battery detector to protect against destructive battery discharge; it can alternately be used for general system interfacing. A supervisory circuit is integrated to provide a reset signal to the Protocol Controller indicating valid supply. An over-temperature shutdown function is integrated to protect against excessive power dissipation. A Shutdown input line is provided to allow for disabling of all active circuitry to minimize battery loading and to provide single line master disable. Logic inputs accept V_{ih} levels from 1.5 V to V_{CC}.

Typical Applications

- Add-On Bluetooth Adaptor Cards for Cellular Phones
- Cellular Phones
- USB Dongle
- GPS or PDA
- Cordless Headsets
- Other portable devices requiring multiple independent regulators in one package

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Features

- Low-Battery Detector
- Three LDO Voltage Regulators:
  2.65 V, 65 mA for RF/IF
  1.85 V, 30 mA for Baseband
  3.0/3.3 V, 60 mA for USB, Audio CODEC, or other circuitry
  Integrated Pass Device
  Independent Enable Lines
  Optimized for Low-Cost Bypass Capacitors
- Microprocessor Supervisor Circuit
- General Purpose Inverter, OR Gate and Comparator
- Maximum V_{CC} Rated up to 7.0 V (6.5 V recommended)
- Voltage-Robust, Level Shifted Logic Inputs to V_{CC} (6.5 V)
- Seamless Integration with Motorola's Bluetooth Chipset
- Thermal Shutdown

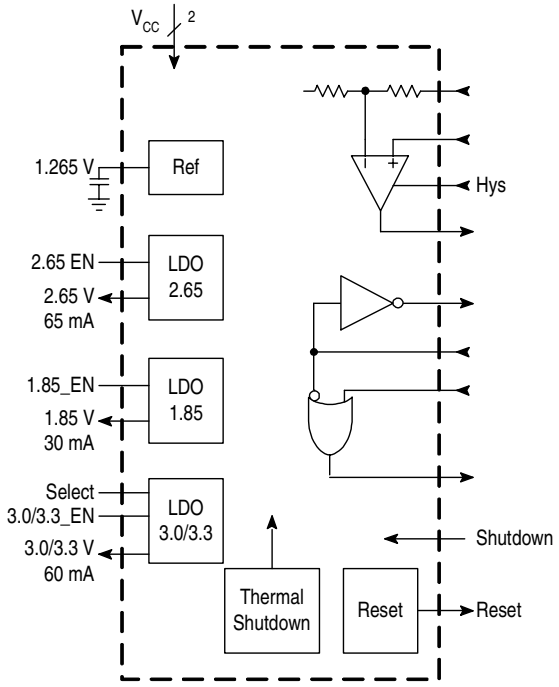


Figure 1. Simplified Block Diagram

1 Electrical Specifications

Table 1. Maximum Ratings

Ratings	Symbol	Value	Unit
Power Supply Input Voltage	V_I	0 to 7.0	V
Voltage Input	V_{in}	-0.3 to V_{CC} +0.3	V
Output Voltage	V_{out}	-0.3 to V_{CC} +0.3	V
Output Short Circuit Duration	-	Infinite	-
Thermal Resistance, Junction to Ambient	$R_{\theta ja}$	115	°C/W
Storage Temperature Range	T_{stg}	-40 to 150	°C
Operating Junction Temperature	T_J	125	°C
Lead Soldering Temperature @ 260°C	T_{solder}	10	sec

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Contact Description section.

Table 2. Maximum Package Power Dissipation

The power dissipation level at which the junction temperature reaches its maximum operating value, i.e., 125°C.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Dissipation, in air	Pd	-	-	345	mW
Power Dissipation, 4-layer board	Pd	-	-	1000	mW

Table 3. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.85	-	6.5	V
Temperature Range	T_A	-40	-	85	°C

Table 4. Electrical Characteristics

(V_{CC} = 3.6 V, C_{in} = 1.0 µF, C_{out} = 1.0 µF, T_A = 25°C for typical values, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
LDO_1.85					
Output Voltage in 1.85 V Mode	V_{out}	1.813	1.85	1.887	V
Line Regulation (V_{CC2} = 2.85 V to 6.5 V, I_{out} = 15 mA)	REG_{line}	-	1.0	10	mV
Load Regulation (I_{out} = 10 µA to 30 mA)	REG_{load}	-	15	45	mV

Table 4. Electrical Characteristics (Continued)

(V_{CC} = 3.6 V, C_{in} = 1.0 µF, C_{out} = 1.0 µF, T_A = 25°C for typical values, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Ripple Rejection (Ripple 0.5 V_{pp}, V_{CC} = 2.95 V, I_o = 15 mA) f = 1.0 kHz	PSRR	40	-	-	dB
Output Noise Voltage @ I_o = 20 mA (f = 10 kHz to 100 kHz)	V_n	-	30	-	μV_{rms}
Short Circuit Current Limit (V_{out} = 0 V)	I_{lim}	-	90	-	mA
Supply Current in ON mode (I_{out} = 0 mA)	I_{SS}	-	30	40	µA
Output Capacitor	C_{out}	1	-	-	µF
ESR of Output Capacitor	ESR	-	5.0	-	Ω
Output Voltage Transient Response (10% to 100% of I_{max})		-	1.0	-	%
Output Turn On Time from Enable to 90% of final value	T_{on}	-	20	100	µs
Output Voltage Temperature Coefficient	T_C	-	100	-	ppm / °C
LDO_2.65					
Output Voltage	V	2.60	2.65	2.70	V
Dropout Voltage	V_{CC}-V_{out}	-	1.0	-	mV/ mA
Line Regulation (V_{CC1} = 2.85 V to 6.5 V, I_{out} = 32.5 mA)	REG_{line}	-	3.0	10	mV
Load Regulation (I_{out} = 10 µA to 65 mA)	REG_{load}	-	15	45	mV
Ripple Rejection, (V_{CC} Ripple = 0.5 V_{pp}, I_o = 32.5 mA) f = 1.0 kHz f = 10 kHz f = 1 MHz	PSRR	 - - -	 60 41 34	 - - -	dB
Output Noise Voltage @ I_o = 50 mA (f = 10 kHz to 100 kHz)	V_n	-	30	-	μV_{rms}
Short Circuit Current Limit (V_{out} = 0 V)	I_{lim}	-	200	-	mA
Supply Current in ON mode (I_{out} = 0 mA)	I_{SS}	-	100	125	µA
Output Capacitor	C_{out}	1.0	-	-	µF
ESR of Output Capacitor	ESR	-	4.0	-	W
Output Voltage Transient Response (10% to 100% of I_{max})		-	1.0	-	%
Output Turn On Time from Enable to 90% of final value	T_{on}	-	20	100	µs

Table 4. Electrical Characteristics (Continued)

(V_{CC} = 3.6 V, C_{in} = 1.0 µF, C_{out} = 1.0 µF, T_A = 25°C for typical values, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage Temperature Coefficient	T_C	-	100	-	ppm / °C
LDO_3.0/3.3					
Output Voltage in 3.0 V Mode Select High	V_{out}	3.0	3.06	3.12	V
Output Voltage in 3.3 V Mode Select Low	V_{out}	3.234	3.3	3.366	V
Dropout Voltage	V_{CC}-V_{out}	-	1.0	-	mV/ mA
Line Regulation (V_{CC} = 3.5 V to 6.5 V, I_{out} = 30 mA)	REG_{line}	-	2.5	10	mV
Load Regulation (I_{out} = 10 µA to 60 mA)	REG_{load}	-	8.0	45	mV
Ripple Rejection, (Ripple 0.5 V_{pp}, V_{CC} = V_{out} + 0.6 V, I_o = 30 mA) f = 1.0 kHz	PSRR	40	-	-	dB
Output Noise Voltage @ I_o = 50 mA (f = 10 kHz to 100 kHz)	V_n	-	30	-	μV_{rms}
Short Circuit Current Limit (V_{out} = 0 V)	I_{lim}	-	200	-	mA
Supply Current in ON mode (V_{CC} = V_{out} + 0.6 V, I_{out} = 0 mA)	Iss	-	10	65	µA
Output Capacitor	C_{out}	1.0	-	-	µF
ESR of Output Capacitor	ESR	-	4.0	-	W
Output Voltage Transient Response (10% to 100% of I_{max})		-	1.0	-	%
Output Turn On Time from Enable to 90% of final value	T_{on}	-	50	100	µs
Output Voltage Temperature Coefficient	T_C	-	100	-	ppm / °C
RESETB Circuit with Programmable Delay					
ResetB Threshold	V_{TH}	1.65	1.70	1.75	V
ResetB Active Timeout period with Delay Cap = 5.6 nF with Delay Cap = 68 nF	T_{reset}	 8.0 -	 14 170	 - 300	ms
Output Voltage Low	V_{ol}	0	-	0.1	V
Output Voltage High	V_{oh}	-	$V_{LDO\_1.85}$	-	V
Output Current RESETB (source or sink)	$\|I_o\|$	1.0	-	-	mA

Table 4. Electrical Characteristics (Continued)

(V_{CC} = 3.6 V, C_{in} = 1.0 µF, C_{out} = 1.0 µF, T_A = 25°C for typical values, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Comparator with Programmable Hysteresis					
Input Offset Voltage	V_{offset}	-5.0	-	5.0	mV
Input Impedance (V_{in} + and V_{in} -)	R_{in}	-	1600		kΩ
Input Voltage Range V_{in} +	V_{in+}	1.0	-	V_{CC2} - 1V	V
Input Voltage Range V_{in} - (scaling factor of approximately 0.44)	V_{in-}	1.0	-	V_{CC2}	V
Output Voltage Low	V_{ol}	0	-	0.1	V
Output Voltage High	V_{oh}	-	$V_{LDO\_1.85}$	-	V
Slew Rate C_L = 50 pF Positive Slope Negative Slope	S_R	 - -	 100 200	 - -	V/µs
Output Current DETECT (source or sink)	$\|I_o\|$	1.0	-	-	mA
Hysteresis Voltage Pin HYS SELECT Low (hysteresis enabled)		-	30	-	mV
Voltage Reference (C_{out} = 470 nF Ceramic)					
V_{CC} Operating Range	V_{CC1}	2.2	-	6.5	V
Output Voltage	V_{ref}	1.250	1.265	1.278	V
Temperature Coefficient	TC_{Vref}	-	0.022	-	mV/°C
Line Regulation	V_{REF_LINE}	-	0.08	-	mV/V
Output Capacitor		-	470	-	nF
Startup Time	$T_{startup}$	-	1.0	-	ms
OR Gate					
V_{CC} Operating Range	V_{CC2}	2.2	-	6.5	V
Output Voltage Low	V_{ol}	-	-	0.1	V
Output Voltage High	V_{oh}	1.55	-	V_{CC2}	V
Inverter Gate					
Hysteresis Voltage		-	50	-	mV
Output Voltage Low	V_{ol}	-	-	0.1	V

Table 4. Electrical Characteristics (Continued)

(V_{CC} = 3.6 V, C_{in} = 1.0 µF, C_{out} = 1.0 µF, T_A = 25°C for typical values, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage High	V_{oh}	-	$V_{LDO\_1.85}$	-	V
Common					
Quiescent Current V_{CC1} (all LDO enables low)	I_{cq1}	-	30	42	µA
Quiescent Current V_{CC2} (all LDO enables low)	I_{cq2}	-	7.0	13	µA
Quiescent Current V_{CC} (SHUTDOWN_B low)	I_{cq} sd	-	1.8	-	µA
Input Voltage Low (enable, shutdown, Q1_B, Q2, hys sel, 3.0/3.3 select)	V_{il}	0	-	0.15	V
Input Voltage High (enable, shutdown, Q1_B, Q2, hys sel, 3.0/3.3 select)	V_{ih}	1.5	-	V_{CC2}	V
Pull Down Resistor (enable, Q2, select)	R_{pd}	-	1.0	-	MΩ
V_{CC} Differential ($V_{CC2} > V_{CC1}$)	V_{CC2}-V_{CC1}	-	0	0.3	V
V_{CC} Differential ($V_{CC1} > V_{CC2}$)	V_{CC1}-V_{CC2}	-	0	V_{CC1}	V

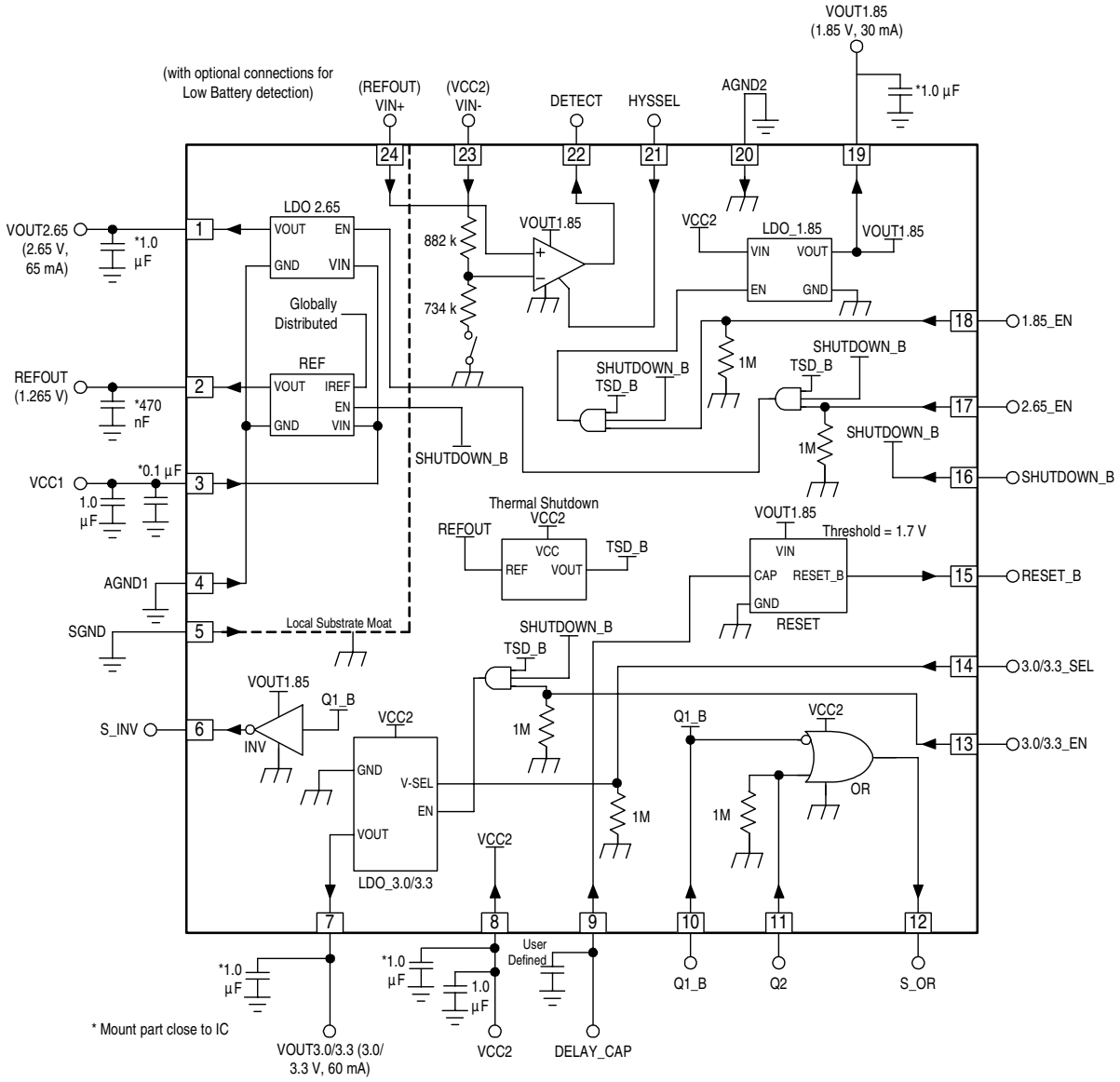
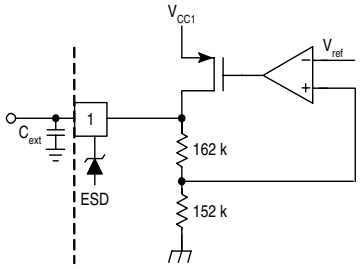
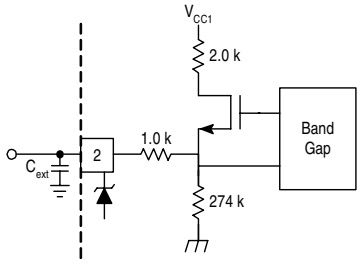
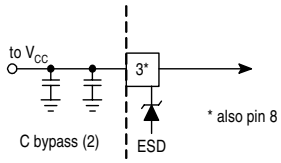
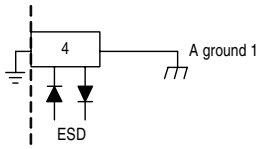
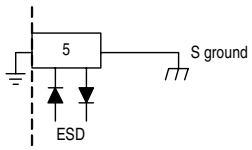
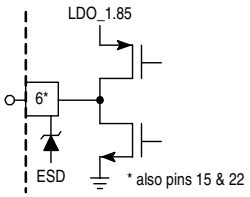


Figure 2. Simplified Functional Diagram

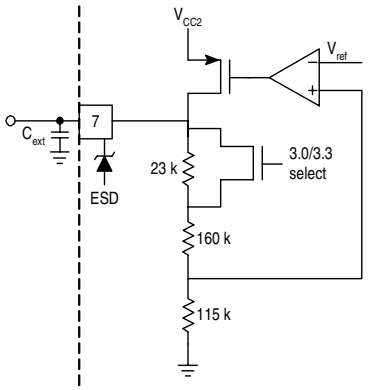
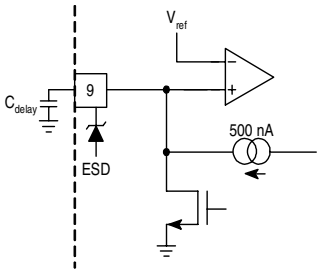
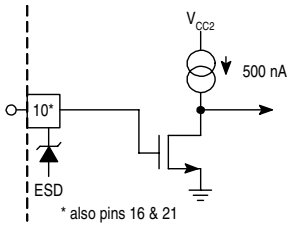
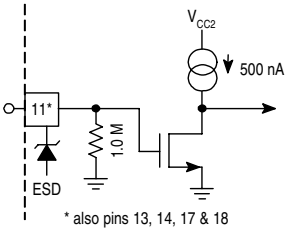
2 Pin Function Descriptions

Table 5. Pin Function Description

Pin	Symbol/ Type	Description	Equivalent Internal Circuit	Notes
1	VOUT2.65	**VOUT2.65 Regulator Output**, LDO_2.65, 2.65 V, 65 mA Output		Bypass with low ESR 1.0 µF tantalum capacitor [Note 1]
2	REFOUT	**REFOUT**,1.265 V Reference Voltage Output,		Bypass with low ESR 470 nF [Note 1]
3	VCC1	**VCC1, Positive Supply**, Power Supply Input for Reference Generation and LDO_2.65		Bypass with a 0.1 µF close to the part and a 1.0 µF low ESR.
4	AGND1	**AGND1 Ground**, Analog Ground for Reference Generation and LDO_2.65		Tie to ground
5	SGND	**SGND Ground**, Substrate for LDO_2.65 and Reference Generator		Tie to ground
6	S_INV	**S_INV**, Inverter Output		referenced to $V_{LDO\_1.85}$

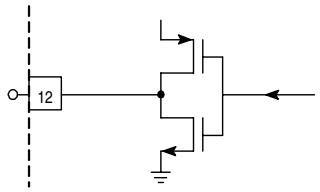
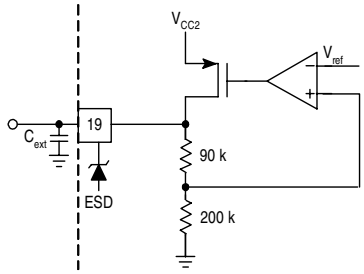
NOTES: 1. All capacitors are assumed to be low ESR tantalum. De-rating factor on capacitance value is assumed to be -20% to 10% over all cases of tolerance and temperature.
2. Contact assignments are subject to change.

Table 5. Pin Function Description (Continued)

Pin	Symbol/ Type	Description	Equivalent Internal Circuit	Notes
7	VOUT3.0/3.3	**VOUT3.0/3.3 Regulator**, LDO_3.0/3.3, 60 mA Output		Bypass with low ESR 1.0 µF tantalum capacitor [Note 1]
8	VCC2	**VCC2, Positive Supply**, Power Supply Input for non-V_{CC1} blocks	same as pin 3	Bypass with a 0.1 µF close to the part and a 1.0 µF low ESR.
9	DELAY_CAP	**DELAY_CAP**, Reset Delay Cap Input		
10	Q1_B	**Q1_B**, Input to Inverter and Complementary Input to OR Gate		can tolerate high to V_{CC}
11	Q2	**Q2**, Input to OR Input		can tolerate high to V_{CC}

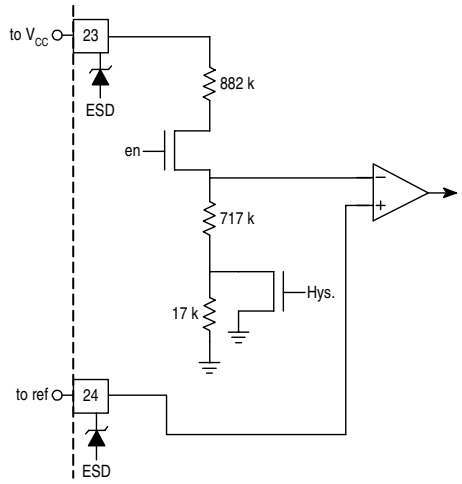
NOTES: 1. All capacitors are assumed to be low ESR tantalum. De-rating factor on capacitance value is assumed to be -20% to 10% over all cases of tolerance and temperature.
2. Contact assignments are subject to change.

Table 5. Pin Function Description (Continued)

Pin	Symbol/ Type	Description	Equivalent Internal Circuit	Notes
12	S_OR	**S_OR**, OR Output		referenced to V_{CC2}
13	3.0/3.3_EN	**3.0/3.3_EN**, LDO_3.0/ 3.3 Enable	same as pin 11	high = enable
14	3.0/3.3_SEL	**3.0/3.3_SEL**, Input logic control for 3.0 or 3.3 V from LDO_3.0/3.3	same as pin 11	high = 3.0 V, low = 3.3 V
15	RESET_B	**RESET_B**, Reset Push-Pull Output	same as pin 6	referenced to $V_{LDO\_1.85}$
16	SHUTDOWN _B	**SHUTDOWN_B**, Single Pin Master Disable	same as pin 10	Low = IC Shutdown
17	2.65_EN	**2.65_EN**, LDO_2.65 Enable	same as pin 11	high = enable
18	1.85_EN	**1.85_EN**, LDO_1.85 Enable	same as pin 11	high = enable
19	VOUT1.85	**VOUT1.85 Regulator**, LDO_1.85, 1.85 V, 30 mA Output,		Bypass with low ESR 1.0 µF tantalum capacitor [Note 1]
20	AGND2	**AGND2 Ground**, Analog Ground	Ground	Tie to ground
21	HYSSEL	**HYSSEL**, Input logic control for Comparator Hysteresis	same as pin 10	Low = hysteresis enabled, High = hysteresis disabled
22	DETECT	**DETECT**, Comparator Push-Pull Output	same as pin 6	referenced to $V_{LDO\_1.85}$

NOTES: 1. All capacitors are assumed to be low ESR tantalum. De-rating factor on capacitance value is assumed to be -20% to 10% over all cases of tolerance and temperature.
2. Contact assignments are subject to change.

Table 5. Pin Function Description (Continued)

Pin	Symbol/ Type	Description	Equivalent Internal Circuit	Notes
23	VIN-	**VIN-**, Inverting Input to Comparator through divider string		Typically, VIN- will be connected to V_{CC} and VIN+ to the reference to detect low battery.
24	VIN+	**VIN+**, Non-inverting Input to Comparator		

NOTES: 1. All capacitors are assumed to be low ESR tantalum. De-rating factor on capacitance value is assumed to be -20% to 10% over all cases of tolerance and temperature.
2. Contact assignments are subject to change.

3 Circuit Features

3.1 Low Drop Out Regulators (LDO)

All three regulators are designed for use with low-value, low-cost bypass capacitors. Low ESR tantalum capacitors are recommended (high performance ceramic capacitors with extremely low ESR, «1Ω, should be avoided at regulator outputs to ensure stability, see Table 4 (Electrical Characteristics) for allowable ESR range for each regulator). The output capacitors should be 1.0 µF minimum and should be mounted close to the IC. Better transient performance can be achieved with a larger output capacitor. In general turn-on and turn-off time will increase in proportion to the capacitor value. the regulators may not meet specified turn-on time with a larger capacitor.

Table 6. LDO Regulators

LDO	Voltage (V)	Current (mA)	SEL	C_{out} (µF)
LDO_1.85	1.85	30	-	1.0
LDO_2.65	2.65	65	-	1.0
LDO_3.0/3.3	3.0	60	high	1.0
LDO_3.0/3.3	3.3	60	low	1.0

Additional filter capacitors should be placed across each V_{CC} input. A 0.1 µF ceramic close to the IC and a 1.0 µF tantalum (placement is less critical) are recommended.

All three regulators are designed for high Power Supply Rejection Ratio, low standby current, good line and load regulation, and fast turn on.

The first regulator, LDO_1.85, supplies 1.85V. It is capable of a nominal output current of 30 mA. This regulator is ideal for powering low-voltage digital or baseband circuitry.

The second regulator, LDO_2.65, supplies 2.65 V at up to 65 mA. This regulator is intended to supply power for RF/IF circuitry. This regulator is optimized for slightly better close-in PSRR performance, and derives its power from the VCC1 input pin. The input to the MC13180, which this LDC supplies current, requires at least 2.55 V. The additional voltage of LDO_2.65 allows for a series resistor, shunt capacitor filter into incorporate to further improve PSRR on that line. The resistor must be 0.220 Ω minimum, and the capacitor 1.0 to 2.2 µF. The maximum resistor value should be chosen so that maximum current will result in a voltage drop of 0.1 V or less.

The third regulator, LDO_3.0/3.3, can be set to either 3.0 V out to 3.3 V out through a single select line. This output can source 60 mA. This regulator can be used to supply USB power or power an audio CODEC or some other peripheral as needed. If the input voltage drops below the overhead needed for regulation, the output of this regulator will track the input down to 2.7 V.

The LDO_1.85 and LDO_3.0/3.3 regulators derive their power from the VCC2 input pin. This allows filtering to be tailored for the load circuitry, and to isolate the noisy digital (1.85 V) peripheral (3.0/3.3 V) from the RF (2.65 V) and reference of the IC.

Each regulator has an independent, active-high enable line. This line can accept a “high” (to turn on the regulator) input of 1.5 V up to either V_{CC}, and can be tied directly to V_{CC} if the enable function is not to be used (shutdown will still function). If a given regulator is not needed in the application, the appropriate enable input can be tied low (<1.5 V) and the output capacitor eliminated. Care should be taken if the enable pin is to be driven from a processor powered by the corresponding regulator.

3.2 Reference Regulator

The Reference Regulator supplies a precise 1.265 V for use by the other on-chip regulators. To maintain spectral purity on the LDO regulators, this internal reference is not intended for external loading. A pin is provided for an off-chip 0.47 µF capacitor for bypassing.

The reference regulator derives its power from the VCC1 pin. Since the reference regulator supplies reference to the other regulators, power should not be applied to V_{CC2} if V_{CC1} is unpowered.

3.3 Shutdown

The active-low shutdown input disables all regulators and logic. In the shutdown state, the total IC current consumption is 2.0 µA. Shutdown also disconnects the input resistor of the divider on the VIN- input to the comparator. As this would typically be connected to V_{CC} for battery voltage detection. Shutting down MC13181 removes this approximately 5.0 µA current.

Care should be taken if this pin is to be driven from a processor operating on a voltage supplied by MC13181.

3.4 Reset Circuit

The RESET_B output goes high after a delay, based on the delay capacitor. It is initiated when $V_{LDO\_1.85}$ rises above the reset threshold of 1.70 V. When $V_{LDO\_1.85}$ falls below the reset threshold, RESET_B goes low with no delay.

To calculate the value of the delay capacitor needed for a given delay, the formula C/I = dV/dT can be used. At the start of the delay, the capacitor is shorted nearly to 0 V, and then charged with a 500 nA current source until its voltage reaches the reference voltage, 1.265 V.

T delay = C * V / I, simplifies to

T delay (ms) ~= 2.53 x C (nF)

or,

C (nF) ~= T / 2.53 (T in ms)

Note: The threshold voltage, resistance of the shorting FET and the current source will vary with temperature and V_{CC2}, so the resulting delay will vary by 2:1 or more.

3.5 Comparator with Programmable Hysteresis

The MC13181 includes a general purpose comparator. The IC's VIN- input incorporates internal resistors scaling (by a factor of approximately 0.44) the voltage to the minus input of the comparator. The IC's VIN+ input is directly connected to the plus input of the comparator. A typical application connects the VIN- input to V_{CC2} and VIN+ to the reference output for Under-Voltage Detection. The scaling resistors thereby set the threshold to 2.88 V with no additional components required.

Hysteresis, of typically 30 mV, can be enabled or disabled via the HYSSEL pin (low is enable), allowing versatility for general purpose applications.

The comparator may be used for general purpose applications, if the fixed divider ratio is accounted for. The inputs should not go lower than 1.0 V. The plus input should not exceed V_{CC2} - 1.0 V and the minus input should not exceed V_{CC2}.

The output of the comparator is push-pull, referenced to $V_{LDO\_1.85}$.

3.6 OR Gate & Inverter

The IC incorporates a general purpose inverter and OR gate. The Q1_B input is the input to the inverter and one of the OR gate inputs. The S_INV output will be the logical inversion of the input. The S_OR output will be the logical OR of the inverse of Q1_B and Q2. Q2 has an internal pull-down. See Figure 3. A truth table of this function is shown in Table 7:

Table 7. Inverter/OR Logic Truth Table

Q1_B	Q2	S_OR	S_INV
0	0	1	1
0	1	1	1
1	0	0	0
1	1	1	0

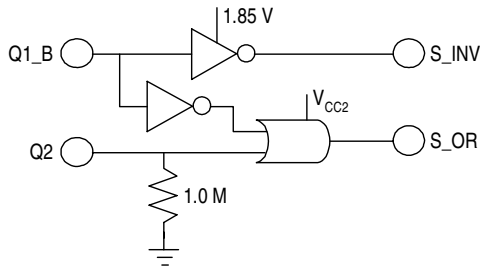


Figure 3. Inverter/OR Logic Block Diagram

Both inputs feature voltage robust level shifting and a Vih may range from 1.5 V through V_{CC2}.

The inverter output is referenced to $V_{LDO\_1.85}$. The OR gate output is referenced to V_{CC2}.

3.7 Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC and the system in the event that the maximum junction temperature is exceeded. When activated (typical threshold is set at 150°C), the three LDO regulators turn off until they are reactivated. This feature is provided to prevent failures from inadvertent overheating. Hysteresis allows stable thermal recovery.

Care should be taken in design to ensure that regulator loading and ambient thermal conditions are managed to avoid excessive power dissipation and thermal shutdown in normal operation.

PC board layout should include connection to exposed thermal pad on IC and ensure adequate heat dissipation.

4 Packaging

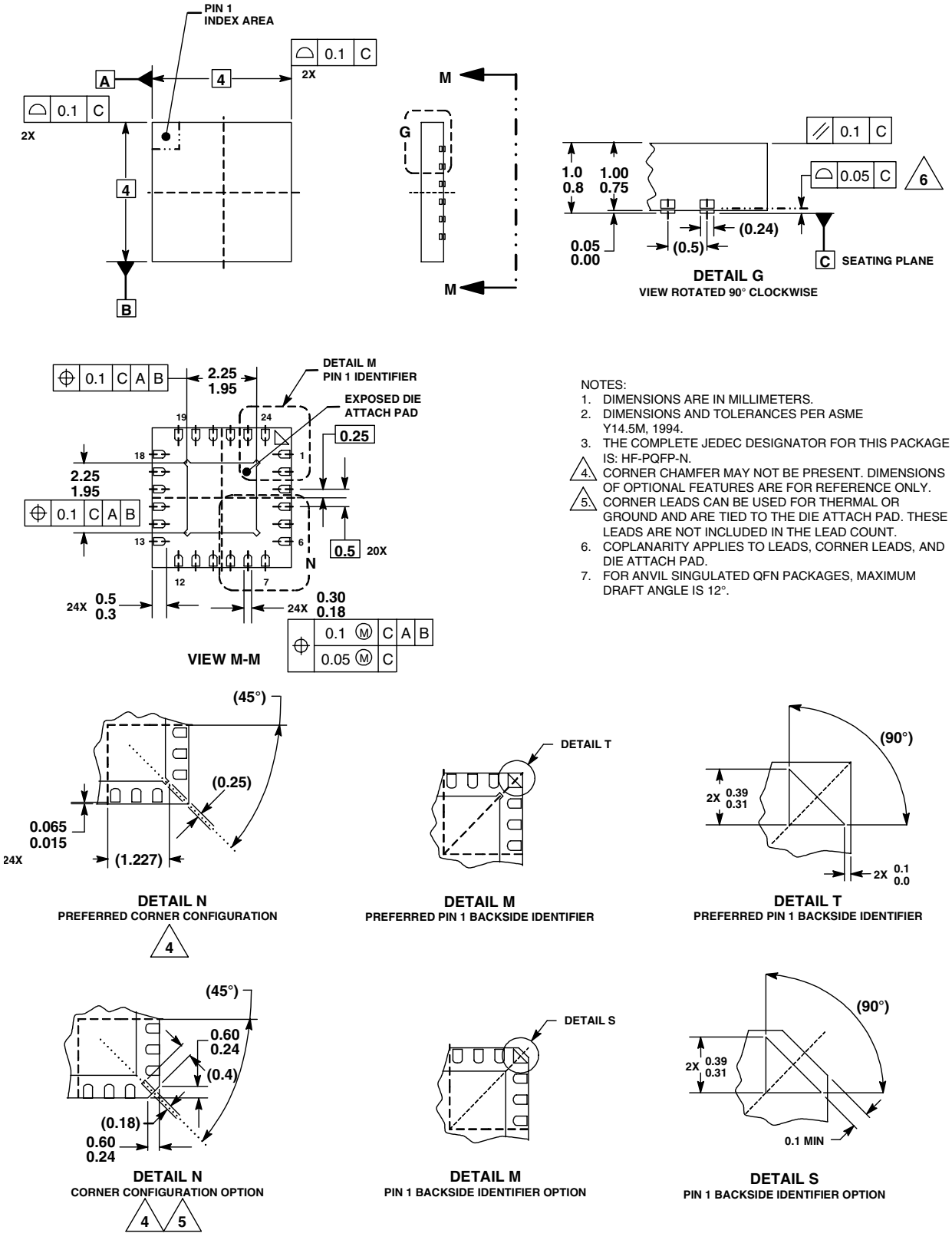


Figure 4. Outline Dimensions for QFN-24 (Case 1307-01, Issue B)

NOTES

HOW TO REACH US:

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MC13181/D