CY7C53120L8
CY7C53150L

3.3V Neuron® Chip Network Processor

Features

- **3.3V operation**
- **Three 8-bit pipelined processors for concurrent processing of application code and network traffic**
- **Hardware UART/SPI interface**
- **Eleven-pin I/O port programmable in 38 modes for fast application program development. I/O port is 5V input tolerant**
- **Two 16-bit timer/counters for measuring and generating I/O device waveforms**
- **Five-pin communication port that supports direct connect and network transceiver interfaces, and operates at 3.3V or 5V**
- **Programmable pull-ups on IO4–IO7 and 20-mA sink current on IO0–IO3**
- **Unique 48-bit Neuron ID number in every device to facilitate network installation and management**
- **0.35-μm Flash process technology**
- **On-chip LVD circuit with programmable trip point and digital filter settings**
- **Programmable Pulse Stretching reset**
- **4,096 bytes of SRAM for buffering network data, system, and application data storage**
- **2.75 KBytes (CY7C53150L), 8KBytes (CY7C53120L8) of Flash memory with on-chip charge pump for flexible storage of configuration data and application code**
- **Addresses up to 56 KBytes of external memory (CY7C53150L)**
- **16 KBytes (CY7C53120L8) of ROM containing LonTalk® network protocol firmware**
- **Maximum input clock operation of 20MHz over –40°C to 85°C[1] temperature range**
- **64-pin TQFP package (CY7C53150L)**
- **32-pin SOIC or 44-pin TQFP package (CY7C53120L8)**

Functional Description

The 3.3V Neuron® chip (CY7C53120L8/3150L) is a low-power version of the 5V Neuron chip with a number of feature enhancements. The CY7C53120L8/3150L Neuron chip implements a device for LonWorks® distributed intelligent control networks. It incorporates, on a single chip, the necessary communication and control functions, both in hardware and firmware, that facilitate the design of a LonWorks device.

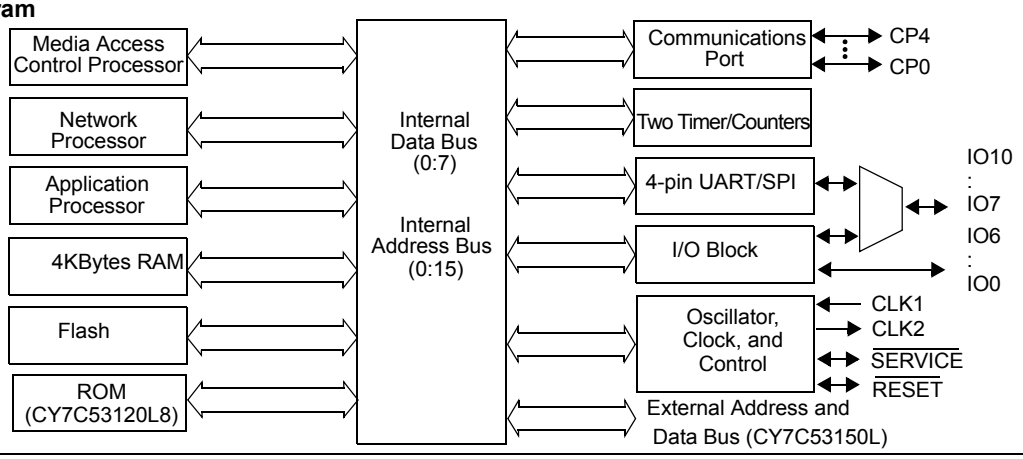
The CY7C53120L8/3150L supports all the functionality of the 5V CY7C531x0 Neuron chip. Additionally it features 4KBytes of RAM, 8KBytes of Flash memory (CY7C53120L8), and hardware UART/SPI. The CY7C53120L8/3150L has an 11-pin configurable I/O block. The I/Os are all 5V-tolerant to allow interfacing to TTL Compatible 5V components and microcontrollers.

The CY7C53120L8/3150L contains a very flexible five-pin communication port that can be configured to interface with a wide variety of media transceivers at a wide range of data rates. The communication port can operate at either 3.3V or 5V. In 5V mode the communication port is completely backward compatible with existing 5V transceivers. The most common transceiver types are twisted-pair, powerline, RF, IR, fiber-optics, and coaxial.

The CY7C53150L incorporates an external memory interface that can address up to 56KBytes with 8KBytes of the address space mapped internally. LonWorks devices that require large application programs can take advantage of this external memory capability.

Services at every layer of the OSI networking reference model are implemented in the LonTalk firmware-based protocol stored in 16KBytes ROM (CY7C53120L8), or off-chip memory (CY7C53150L). The firmware also contains 38 preprogrammed I/O drivers, simplifying application programming. The application program is stored in the Flash memory (CY7C53120L8) and/or off-chip memory (CY7C53150L), and may be updated by downloading over the network.

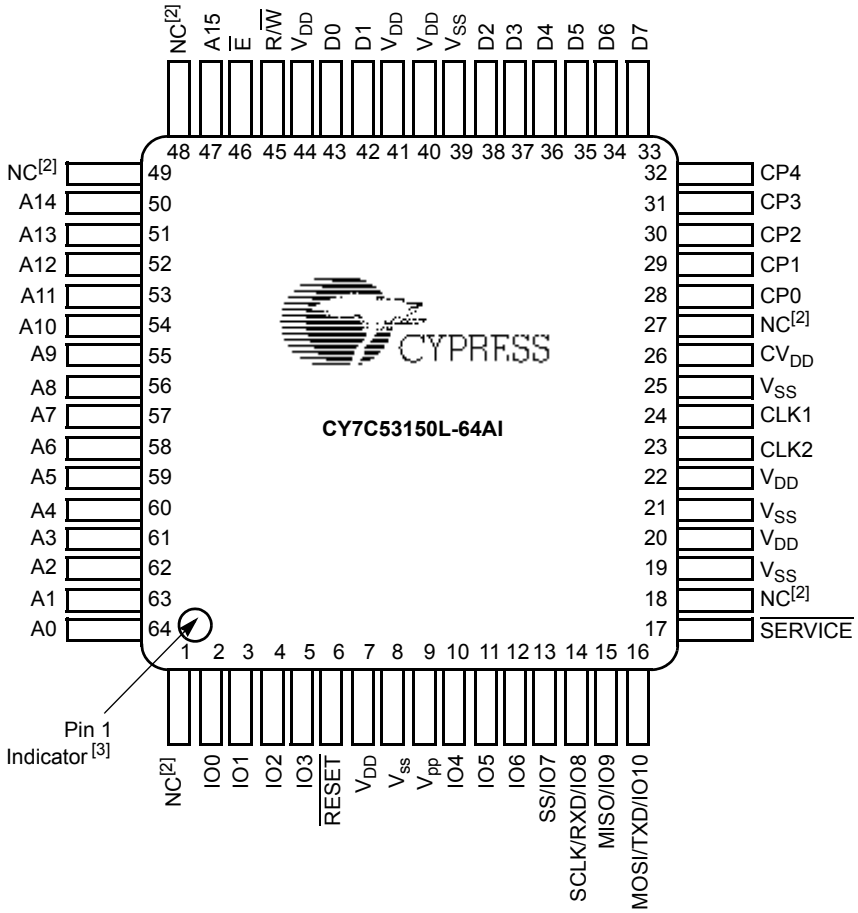
Logic Block Diagram



Note:
1. Maximum junction temperature is 105°C. $T_{Junction} = T_{Ambient} + V \bullet I \bullet \theta_{JA}$. 32-pin SOIC θ_{JA} = 61.07°C/W. 44-pin TQFP θ_{JA} = 69.5°C/W. 64-pin TQFP θ_{JA} = 56.15°C/W.

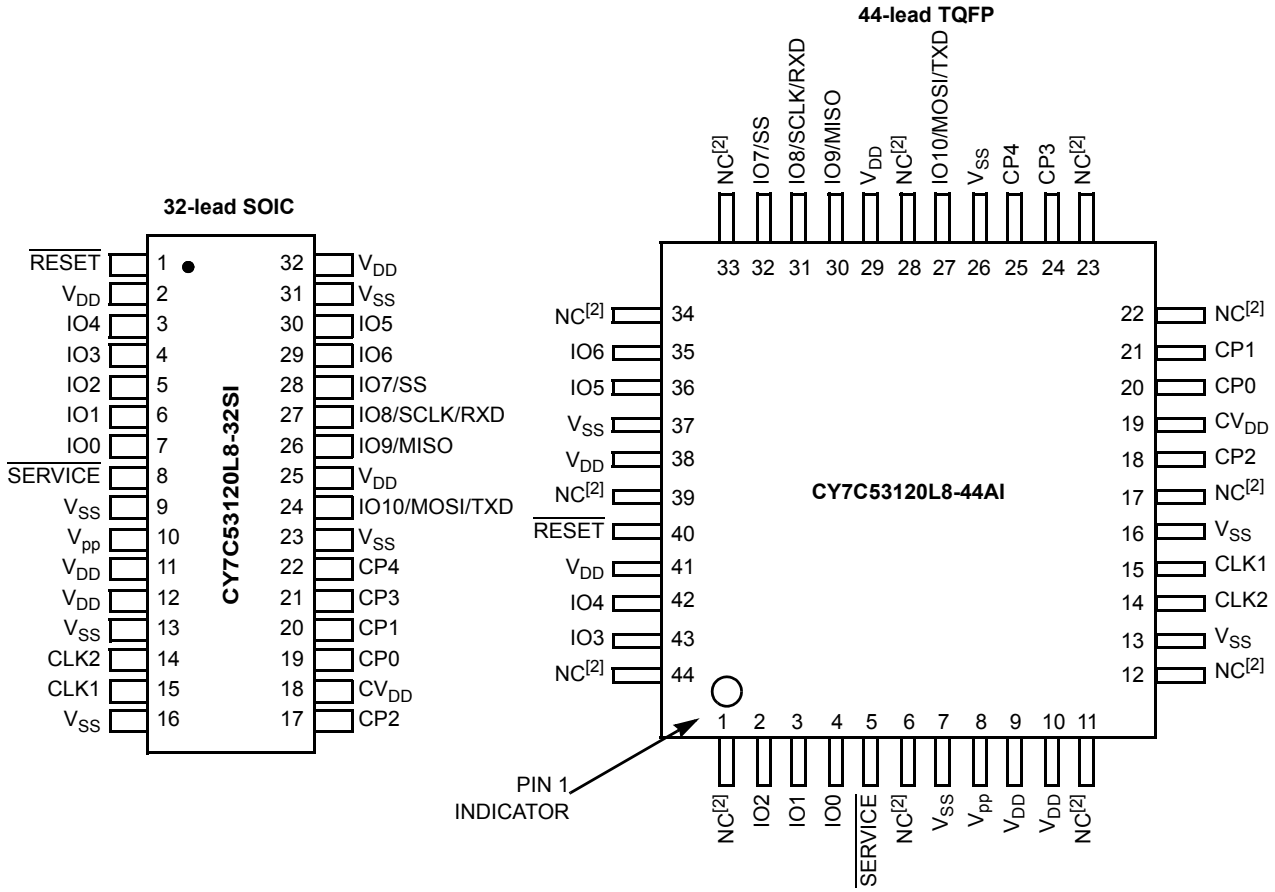
Pin Configurations

CY7C53150L
64-lead Thin Quad Flat Pack



Notes:
2. No Connect (NC) — should not be used. (These pins may be used for internal testing.)
3. The smaller dimple at the bottom left of the marking indicates pin 1.

Pin Configurations (continued)



Pin Definitions

Pin Name	I/O	Pin Function	CY7C53150L TQFP-64 Pin No.	CY7C53120L8 SOIC-32 Pin No.	CY7C53120L 8 TQFP-44 Pin No.
CLK1	Input (5V tolerant)	**Oscillator connection or external clock input**.	24	15	15
CLK2	Output	**Oscillator connection**. Leave open when external clock is input to CLK1. Maximum of one external load.	23	14	14
$\overline{\text{RESET}}$	I/O (Built-In Pull-up)	**Reset pin (active LOW)**. Note. The allowable external capacitance connected to the RESET pin is 100–1000 pF.	6	1	40
$\overline{\text{SERVICE}}$	I/O (Built-In Configurable Pull-up)	**Service pin (active LOW)**. Alternates between input and output at a 76-Hz rate.	17	8	5
IO0–IO3	I/O	**Large current-sink capacity (20mA)**. General I/O port. The output of timer/ counter 1 may be routed to IO0. The output of timer/counter 2 may be routed to IO1.	2, 3, 4, 5	7, 6, 5, 4	4, 3, 2, 43
IO4–IO7	I/O (Built-In Configurable Pull-ups)	**General I/O port**. The input to timer/counter 1 may be derived from one of IO4–IO7. The input to timer/counter 2 may be derived from IO4.	10, 11, 12, 13	3, 30, 29, 28	42, 36, 35, 32
IO8–IO10	I/O	**General I/O port**. May be used for serial communication under firmware control.	14, 15, 16	27, 26, 24	31, 30, 27
SS	Input	**Slave Select**. Muxed with IO7.	13	28	32

Pin Definitions (continued)

Pin Name	I/O	Pin Function	CY7C53150L TQFP-64 Pin No.	CY7C53120L8 SOIC-32 Pin No.	CY7C53120L 8 TQFP-44 Pin No.
SCLK/RXD	I/O	**SPI Clock or UART RXD**. Muxed with IO8. Can be configured as Open Drain Output.	14	27	31
MISO	I/O	**SPI Master In/Slave Out (MISO) Muxed with IO9**. Can be configured as Open Drain Output.	15	26	30
MOSI/TXD	I/O	**SPI Master out/Slave In (MOSI) or UART TXD. Muxed with IO10**. Can be configured as Open Drain Output.	16	24	27
D0–D7	I/O	**Bidirectional memory data bus**.	43, 42, 38, 37, 36, 35, 34, 33	N/A	N/A
R/$\overline{W}$	Output	**Read/write control output for external memory**.	45	N/A	N/A
$\overline{E}$	Output	**Enable clock control output for external memory**.	46	N/A	N/A
A0–A15	Output	**Memory address output port**.	64, 63, 62, 61, 60, 59, 58, 57, 56, 55, 54, 53, 52, 51, 50, 47	N/A	N/A
V_{DD}	Input	**Power input (3.3V nom.)**. All V_{DD} pins must be connected together externally.	7, 20, 22, 40, 41, 44	2, 11, 12, 25, 32	9, 10, 29, 38, 41
V_{SS}	Input	**Power input (0V, GND)**. All V_{SS} pins must be connected together externally.	8,19, 21, 25, 39	9, 13, 16, 23, 31	7,13, 16, 26, 37
CV_{DD} [4]	Input	**Power input, 5V or 3.3V depending on Communications Port Voltage**.	26	18	19
V_{PP}	Input	**In-circuit test mode control**. If V_{PP} is high when $\overline{RESET}$ is asserted, the I/O, address and data buses become Hi-Z.	9	10	8
CP0–CP4	Communication Network Interface	**Bidirectional port supporting communications in three modes**.	28, 29, 30, 31, 32	19, 20, 17, 21, 22	20, 21, 18, 24, 25
NC	–	**No connect**. Must not be connected on the user's PC board, since they may be connected internal to the chip.	1, 18, 27, 48, 49	–	1, 6, 11, 12, 17, 22, 23, 28, 33, 34, 39, 44

Memory Usage

All Neuron chips require system firmware to be present when they are powered up. In the case of the CY7C53120L8, this firmware is preprogrammed in the factory in an on-chip ROM. In the case of the CY7C53150L, the system firmware must be present in the first 16KBytes of an off-chip nonvolatile memory such as Flash, EPROM, EEPROM, or NVRAM. Because the system firmware implements the network protocol, it cannot itself be downloaded over the network.

For the CY7C53120L8, the user application program is stored in on-chip Flash memory. It may be programmed using a device programmer before board assembly, or may be programmed in-circuit after board assembly through a proprietary 11-pin programming interface or over the LonTalk network from an external network management tool.

For the CY7C53150L, the user application program is stored in on-chip Flash Memory and also in off-chip memory. The user program may initially be programmed into the off-chip memory device using a device programmer.

Flash Memory Retention and Endurance

Data and code stored in Flash Memory is guaranteed to be retained for at least ten years for programming temperature range of –40°C to 85°C.

The Flash memory can typically be written 100,000 times without any data loss[5]. An erase/write cycle takes 20 ms. The system firmware extends the effective endurance of the Flash memory in two ways. If the data being written to a byte of Flash memory is the same as the data already present in that byte, the firmware does not perform the physical write. So for example, an application that sets its own address in Flash memory after every reset will not use up any write cycles if the address has not changed. In addition, system firmware version 15 or higher is

Notes:
4. Power supply sequencing is required. Power must be applied such that, V_{DD} (3.3V) supply must not trail CV_{DD} (3.3V/5V) supply on power-up by more than 1V until V_{DD} reaches its normal operating voltage. Ramps can be simultaneous as long as the above condition is maintained.
5. For detailed information about data retention after 100K cycles, please see Cypress qualification report.

able to aggregate writes to eight successive address locations into a single write for CY7C53120L8 devices. For example, if 8KBytes of code is downloaded over the network, the firmware would execute only 1024 writes rather than 8,192.

Manufacturer ID

The manufacturer ID is 0x02 for both the CY7C53150L and CY7C53120L8. The major model ID is 0x02 for the CY7C53150L and 0x10 for the CY7C53120L8. The minor model ID is 0x08 for both ICs.

Low-Voltage Inhibit (LVI) Operation

The on-chip Low-voltage Inhibit circuit trips the Neuron chip reset circuit whenever the V_{DD} input drops below a set value. The default value of the LVI trip point is 2.77V, with a variation of ±100mV across process and temperature. Every time power is reapplied to the chip, the LVI trip point gets set to this default value. Through the application code, the trip point can be programmed to be one of 16 points between 2.77V and 3.19V.

The purpose of the LVI circuit is to prevent the corruption of nonvolatile memory during voltage drops. A lower value of trip point voltage decreases the likelihood of the LVI tripping due to noise on V_{DD}. A lower setting is therefore recommended for circuits with a lot of noise on the power supply. In circuits that do not have excessive noise it is recommended that the LVI trip point be increased which results in better flash protection in case of real power loss scenarios.

Internal circuitry is provided to ensure that in a power loss scenario, writes to non-volatile memory that have already started get completed. To ensure proper functioning of this circuitry, the V_{DD} droop time (during power down or power loss) should be at least 10ms from the time LVI circuit trips and voltage reaches 2.77V.

The LVI also features a programmable digital filter used to filter out V_{DD} noise. This is another method of decreasing the possibility of the LVI being triggered by the noise as opposed to true power loss events. The digital filter is programmable to a value between 16 and 128 clock cycles. The value chosen depends on the frequency of the V_{DD} noise where the digital filter period should slightly exceed the minimum frequency noise seen on V_{DD}. The LVI digital filter defaults to 128 clock cycles.

Reset Stretching

At Power-on, the CY7C53120L8/3150L provides internal Reset Stretching of 25ms at 20MHz clock frequency. Power-on Reset Stretch time scales with frequency. After Power-on, Reset Stretch is 50ms independent of frequency of operation.

At Power-on the CY7C53120L8/3150L defaults to Reset Stretch enabled. The Reset Stretch can either be left enabled or disabled through software. Reset Stretching eliminates the need for an external pulse stretching LVI which is required when using the CY7C53150 with an external Flash memory.

5V-Tolerant Reset

$\overline{\text{RESET}}$ is an Input/Output pin. It is a 5V-tolerant input pin. It can provide 5V-compatible levels when output if an external resistor is connected between pin and 5V supply.

Hardware Serial Communication Engine

The CY7C53120L8/3150L features a hardware Serial Communication Engine. The hardware engine is capable of performing high-speed communications in either SPI or UART mode.

Serial Peripheral Interface (SPI) Mode

SPI mode is 4-pin synchronous serial communications interface that can be set as either a Master or a Slave[6].

SPI Pin	Description
IO7	Slave Select (SS)
IO8	Hardware SPI Serial Clock (SPSCK)
IO9	Master Input/Slave Output (MISO)
IO10	Master Output/Slave Input (MOSI)

SPI communication is a point-to-point or point-to-multi-point interface that can be configured as master/slave, single-master/multiple-slaves or multiple-masters/single-slave. The master initiates all communication between slave and master. The master drives the SPSCK signal, which is a clock used to synchronize all data communication between master and slave.

Slave Select (SS) is an input to the Neuron chip in both the Master and the Slave modes. In Slave mode, SS is active low with the Slave communicating only when SS is low. In Master mode, the SPI engine functions only when the SS signal is held high. SS can be hard wired high or low or it can be wired to signals being generated from other sources. The Neuron Chip can use IO0 through IO6 for selecting between multiple slaves when acting as a master.

MOSI and MISO are used to send and receive data over SPI. MOSI is a data output in Master mode and is an input in Slave mode. MISO is an input in Master mode and is an output in Slave mode. The phase and polarity of the data relative to the clock signal is programmable and can be configured in four possible modes.

The SPI interface can communicate at a maximum of 5Mbps data rate with a 20-MHz input clock frequency. The maximum data rate scales with frequency. The data rate is programmable and can be scaled by selecting the desired divisor ranging from 2 to 256 in multiples of 2.

Serial Communication Interface (UART) Mode

UART mode provides a full-duplex asynchronous NRZ format serial interface for communicating with other devices with either an UART or UART interface. The UART interface is optimized to provide industry standard UART baud rates from the CY7C53120L8/3150L crystal clock rates.

UART Pin	Description
IO8	Receive Data (RXD)
IO10	Transmit Data (TXD)

Note:
6. Please see document Errata for CY7C53150L and CY7C53120L8 - 3.3V Neuron Chip (38-17019) for details.

RXD is used to receive serial data at the specified baud rate. TXD is used to transmit data serially at the specified baud rate. The idle state of the TXD and RXD lines is high. All data bytes begin with a start bit which is a '0'; this is followed by eight or nine bits of data, LSB first, and end with a stop bit which is a return to the idle state of '1.' The number of bits transmitted or received is programmable between eight or nine bits. The ninth bit can be used as a parity bit or as a second stop bit.

The maximum baud rate for the UART engine is 921.6 Kbaud with 20-MHz input clock frequency and scales with frequency. The UART can be programmed to run at most of the standard UART baud rates.

Communications Port

The Neuron chip includes a versatile 5-pin communications port that can be configured in three different ways. The Communications port can operate at either 3.3V or 5V. The Communication port can be made backward-compatible with existing 5V transceivers by supplying a 5V supply to the CV_{DD} pin.

In Single-ended Mode, pin CP0 is used for receiving serial data, pin CP1 for transmitting serial data, and pin CP2 enables an external transceiver. Data is communicated using Differential Manchester encoding.

In Special Purpose Mode, pin CP0 is used for receiving serial data, pin CP1 for transmitting serial data, pin CP2 transmits a bit clock, and pin CP4 transmits a frame clock for use by an external intelligent transceiver. In this mode, the external transceiver is responsible for encoding and decoding the data stream.

In Differential Mode, pins CP0 and CP1 form a differential receiver with built-in programmable hysteresis and low-pass filtering. Pins CP2 and CP3 form a differential driver. Serial data is communicated using Differential Manchester encoding.

The following tables describe the communications port when used in Differential Mode.

Operating the Communications Port at 5V

The 3.3V Neuron device has a 5V compatible communications port. In order to operate the Communications port at 5V, CV_{DD} has to be supplied with 5V. In this case CLK2 output will still be at 3.3V but a buffered copy of CLK2 can be obtained on CP3 pin of the communications port. When the comm port is in Single-ended Mode and the CV_{DD} is at 5V, there will be a buffered 5V version of CLK2 and the CP3 pin.

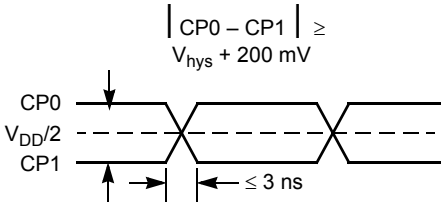


Figure 1. Receiver Input Waveform

Programmable Hysteresis Values (3.3V) (Expressed as differential peak-to-peak voltages in terms of V_{DD})

Hysteresis[7]	V_{hys} Min.	V_{hys} Typ.	V_{hys} Max.
0	0.019 V_{DD}	0.027 V_{DD}	0.035 V_{DD}
1	0.038 V_{DD}	0.054 V_{DD}	0.070 V_{DD}
2	0.057 V_{DD}	0.081 V_{DD}	0.105 V_{DD}
3	0.076 V_{DD}	0.108 V_{DD}	0.140 V_{DD}
4	0.095 V_{DD}	0.135 V_{DD}	0.175 V_{DD}
5	0.114 V_{DD}	0.162 V_{DD}	0.210 V_{DD}
6	0.133 V_{DD}	0.189 V_{DD}	0.245 V_{DD}
7	0.152 V_{DD}	0.216 V_{DD}	0.280 V_{DD}

Programmable Hysteresis Values (5V) (Expressed as differential peak-to-peak voltages in terms of V_{DD})

Hysteresis[7]	V_{hys} Min.	V_{hys} Typ.	V_{hys} Max.
0	0.019 V_{DD}	0.027 V_{DD}	0.035 V_{DD}
1	0.040 V_{DD}	0.054 V_{DD}	0.068 V_{DD}
2	0.061 V_{DD}	0.081 V_{DD}	0.101 V_{DD}
3	0.081 V_{DD}	0.108 V_{DD}	0.135 V_{DD}
4	0.101 V_{DD}	0.135 V_{DD}	0.169 V_{DD}
5	0.121 V_{DD}	0.162 V_{DD}	0.203 V_{DD}
6	0.142 V_{DD}	0.189 V_{DD}	0.236 V_{DD}
7	0.162 V_{DD}	0.216 V_{DD}	0.270 V_{DD}

Programmable Glitch Filter Values[8] (Receiver (end-to-end) filter values expressed as transient pulse suppression times)

Filter (F)	Min.	Typ.	Max.	Unit
0	10	75	140	ns
1	120	410	700	ns
2	240	800	1350	ns
3	480	1500	2600	ns

Receiver[9] **(End-to-End) Absolute Asymmetry** (Worst-case across hysteresis)

Filter (F)	Max ($\lvert t_{PLH} - t_{PHL} \rvert$)	Unit
0	35	ns
1	150	ns
2	250	ns
3	400	ns

Differential Receiver (End-to-End) Absolute Symmetry[10, 11]

Filter (F)	Hysteresis (H)	Max ($\lvert t_{PLH} - t_{PHL} \rvert$)	Unit
0	0	24	ns

Notes:
7. Hysteresis values are on the condition that the input signal swing is 200 mV greater than the programmed value.
8. The maximum data rate for the differential transceiver is 1.25 Mbps.
9. Receiver input, $V_D = V_{CP0} - V_{CP1}$, at least 200 mV greater than hysteresis levels. See *Figure 1*.
10. CP0 and CP1 inputs each 0.60 Vp – p, 1.25 MHz sine wave 180° out of phase with each other as shown in *Figure 8* V_{DD} = 5V, Figure 9 V_{DD} = 3.3V.
11. t_{PLH}: Time from input switching states from low to high to output switching states. t_{PHL}: Time from input switching states from high to low to output switching states.

Electrical Characteristics (V_{DD} = 3.0V–3.6V)

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
CV_{DD}(3.3V)	Power Supply Voltage	3.0	3.3	3.6	V
CV_{DD} (5V)	Power Supply Voltage	4.75	5	5.25	V
V_{IL}	Input Low Voltage IO0–IO10, CP0, CP3, CP4, $\overline{\text{SERVICE}}$, D0-D7, $\overline{\text{RESET}}$ CP0, CP1 (Differential)	 — —	 — —	 0.8 Programmable	V
V_{IH}	Input High Voltage IO0–IO10, CP0, CP3, CP4, $\overline{\text{SERVICE}}$, D0-D7,$\overline{\text{RESET}}$ CP0, CP1 (Differential)	 2.0 Programmable	 — —	 — —	V
V_{OL}	Low-Level Output Voltage I_{out} < 20 μA Standard Outputs (I_{OL} = 1.4mA)[12] High Sink (IO0–IO3), $\overline{\text{SERVICE}}$, $\overline{\text{RESET}}$ (I_{OL} = 20mA) High Sink (IO0–IO3), $\overline{\text{SERVICE}}$, $\overline{\text{RESET}}$ (I_{OL} = 10mA) Maximum Sink (CP2, CP3) (I_{OL} = 40mA) Maximum Sink (CP2, CP3) (I_{OL} = 15mA)	 — — — — — —	 — — — — — —	 0.1 0.4 0.8 0.4 1.0 0.4	V
V_{OH}	High-Level Output Voltage I_{out} < 20 μA Standard Outputs (I_{OH} = –1.4mA)[12] High Sink (IO0 – IO3), $\overline{\text{SERVICE}}$ (I_{OH} = –1.4mA) Maximum Source (CP2, CP3) (I_{OH} = –40mA) Maximum Source (CP2, CP3) (I_{OH} = –15mA)	 V_{DD} – 0.1 V_{DD} – 0.4 V_{DD} – 0.4 V_{DD} – 1.0 V_{DD} – 0.4	 — — — — —	 — — — — —	V
V_{hys}	Hysteresis (Excluding CLK1)	175	—	—	mV
I_{in}	Input Current (Excluding Pull-Ups) (V_{SS} to V_{DD})[13]	—	—	±10	μA
I_{pu}	Pull-Up Source Current (V_{out} = 0 V, Output = High-Z)[13]	60	—	260	μA
I_{DD}	Operating Mode Supply Current[14] 20-MHz Clock 10-MHz Clock 5-MHz Clock 2.5-MHz Clock 1.25-MHz Clock 0.625-MHz Clock[15]	 — — — — — —	 — — — — — —	 21 13 8 5 3.3 2	mA
$I_{DDsleep}$	Sleep Mode Supply Current[14]	—	6	10	μA

LVI Trip Point (V_{DD})

Part Number	Unit
CY7C53120L8, and CY7C53150L	Programmable between 2.77V and 3.19V

Notes:

12. Standard outputs are IO4–IO10, CP0, CP1, and CP4. ($\overline{\text{RESET}}$ is an open drain input/output. CLK2 must have ≤ 15 pF load.) For CY7C53150L, standard outputs also include A0–A15, D0–D7, E, and R/W.
13. IO4–IO7 and SERVICE have configurable pull-ups. $\overline{\text{RESET}}$ has a permanent pull-up.
14. Supply current measurement conditions: V_{DD} = 3.3V, all outputs under no-load conditions, all inputs ≤ 0.2V or ≥ (V_{DD} – 0.2V), configurable pull-ups off, crystal oscillator clock input, differential receiver disabled. The differential receiver adds approximately 200 μA typical and 600 μA maximum (at 5V) when enabled. It is enabled on either of the following conditions:
    - Neuron Chip in Operating mode **and** Comm Port in Differential mode.
    - Neuron Chip in Sleep mode **and** Comm Port in Differential mode **and** Comm Port Wake-up not masked.
15. Supported through an external oscillator only.

External Memory Interface Timing — CY7C53150L, V_{DD} ± 10% (V_{DD} = 3.0V to 3.6 V, T_A = –40°C to+ 85°C[1])

Parameter	Description	Min.	Max.	Unit
t_{cyc}	Memory Cycle Time (System Clock Period)[16]	100	3200	ns
PW_{EH}	Pulse Width, $\overline{E}$ High[17]	$t_{cyc}/2 – 5$	$t_{cyc}/2 + 5$	ns
PW_{EL}	Pulse Width, $\overline{E}$ Low[17]	$t_{cyc}/2 – 5$	$t_{cyc}/2 + 5$	ns
t_{AD}	Delay, $\overline{E}$ High to Address Valid	—	35	ns
t_{AH}	Address Hold Time After $\overline{E}$ High	10	—	ns
t_{RD}	Delay, $\overline{E}$ High to R/$\overline{W}$ Valid Read	—	25	ns
t_{RH}	R/$\overline{W}$ Hold Time Read After $\overline{E}$ High	5	—	ns
t_{WR}	Delay, $\overline{E}$ High to R/$\overline{W}$ Valid Write	—	25	ns
t_{WH}	R/$\overline{W}$ Hold Time Write After $\overline{E}$ High	5	—	ns
t_{DSR}	Read Data Setup Time to $\overline{E}$ High	15	—	ns
t_{DHR}	Data Hold Time Read After $\overline{E}$ High	0	—	ns
t_{DHW}	Data Hold Time Write After $\overline{E}$ High[18, 19]	10	—	ns
t_{DDW}	Delay, $\overline{E}$ Low to Data Valid	—	12	ns
t_{DHZ}	Data Three State Hold Time After $\overline{E}$ Low[20]	0	—	ns
t_{DDZ}	Delay, $\overline{E}$ High to Data Three-State[19]	—	42	ns
t_{acc}	External Memory Access Time ($t_{acc} = t_{cyc} – t_{AD} – t_{DSR}$) at 20-MHz input clock	50	—	ns

Differential Transceiver Electrical Characteristics

Characteristic at 3.3V	Min.	Max.	Unit
Receiver Common Mode Voltage Range to maintain hysteresis[21]	0.6	$V_{DD} – 1.5$	V
Receiver Common Mode Range to operate with unspecified hysteresis	0.4	$V_{DD} – 1.3$	V
Input Offset Voltage	$–0.05V_{hys} – 35$	$0.05V_{hys} + 35$	mV
Propagation Delay (F = 0, $V_{ID} = V_{hys}/2 + 200$ mV)	—	230 ns	ns
Input Resistance	5	—	MΩ
Wake-up Time	—	10	μs
Differential Output Impedance for CP2 and CP3[22]		35	Ω

Characteristic at 5V	Min.	Max.	Unit
Receiver Common Mode Voltage Range to maintain hysteresis[21]	1.2	$V_{DD} – 2.2$	V
Receiver Common Mode Range to operate with unspecified hysteresis	0.9	$V_{DD} – 1.75$	V
Input Offset Voltage	$–0.05V_{hys} – 35$	$0.05V_{hys} + 35$	mV
Propagation Delay (F = 0, $V_{ID} = V_{hys}/2 + 200$ mV)	—	230 ns	ns
Input Resistance	5	—	MΩ
Wake-up Time	—	10	μs
Differential Output Impedance for CP2 and CP3[22]		35	Ω

Notes:
16. t_{cyc} = 2(1/f), where f is the input clock (CLK1) frequency (20, 10, 5, 2.5, 1.25, or 0.625 MHz).
17. Refer to *Figure 3* for detailed measurement information.
18. The data hold parameter, t_{DHW}, is measured to the disable levels shown in *Figure 4*, rather than to the traditional data invalid levels.
19. Refer to *Figure 5* and *Figure 4* for detailed measurement information.
20. The three-state condition is when the device is not actively driving data. Refer to *Figure 2* and *Figure 5* for detailed measurement information.
21. Common mode voltage is defined as the average value of the waveform at each input at the time switching occurs.
22. Z_0 = {Sum of DC drop across CP2 and CP3 pads @40mA current} / 40mA for CVdd +/-5%.

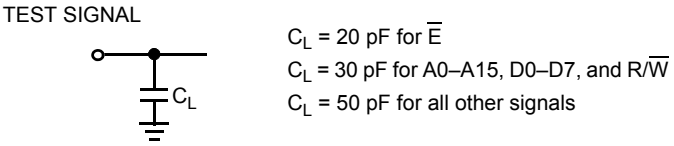


Figure 2. Signal Loading for Timing Specifications Unless Otherwise Specified

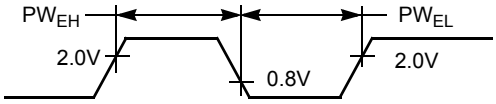
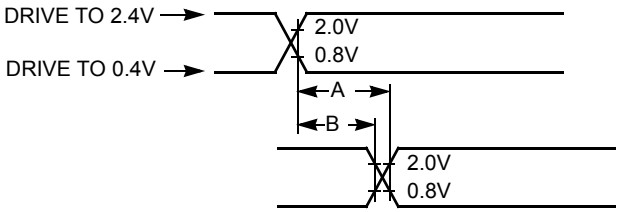
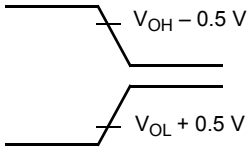


Figure 3. Test Point Levels for $\overline{E}$ Pulse Width Measurements



A — Signal valid-to-signal valid specification (maximum or minimum)
B — Signal valid-to-signal invalid specification (maximum or minimum)

Figure 4. Drive Levels and Test Point Levels for Timing Specifications Unless Otherwise Specified



V_{OH} – Measured high output drive level
V_{OL} – Measured low output drive level

Figure 5. Test Point Levels for Driven-to-Three-State Time Measurements

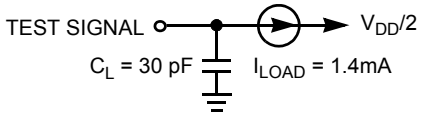


Figure 6. Signal Loading for Driven-to-Three-State Time Measurements

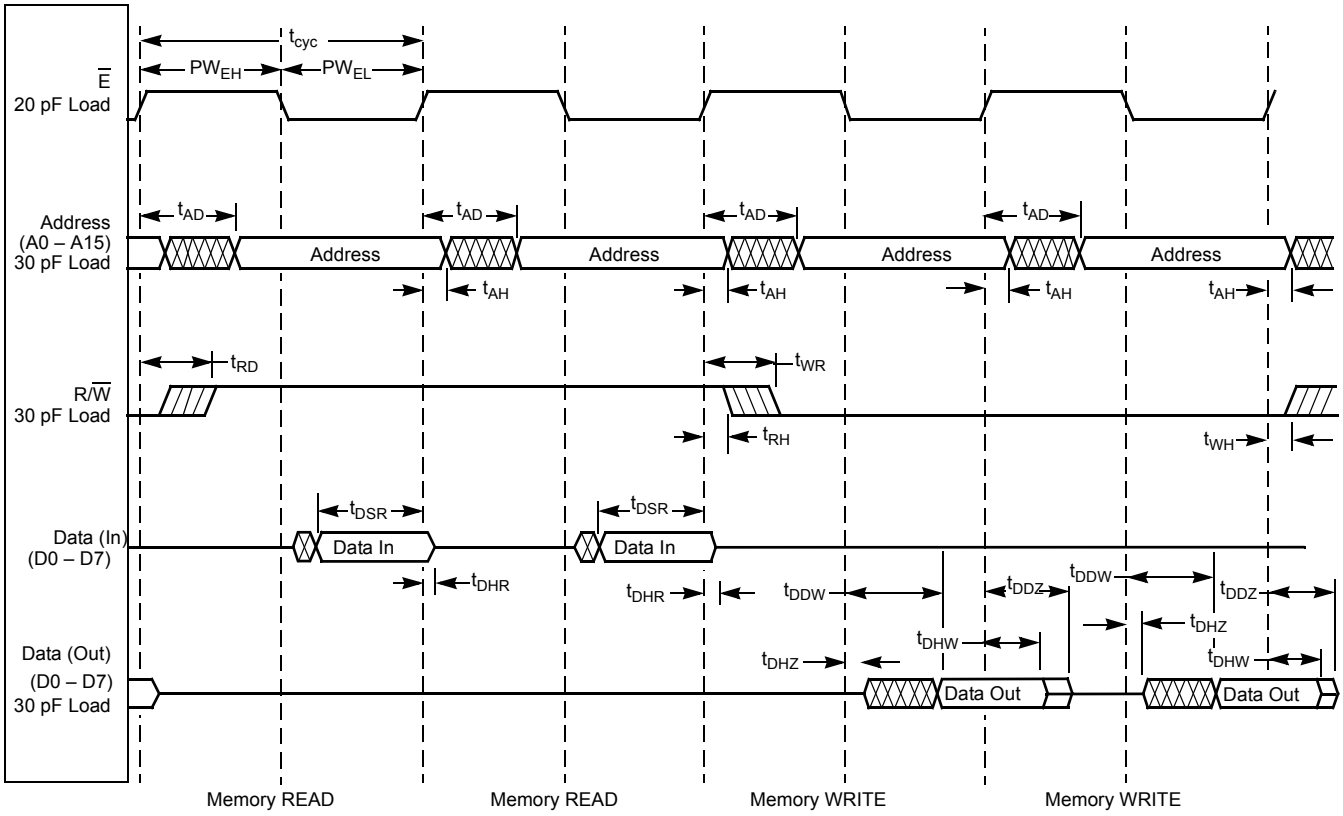
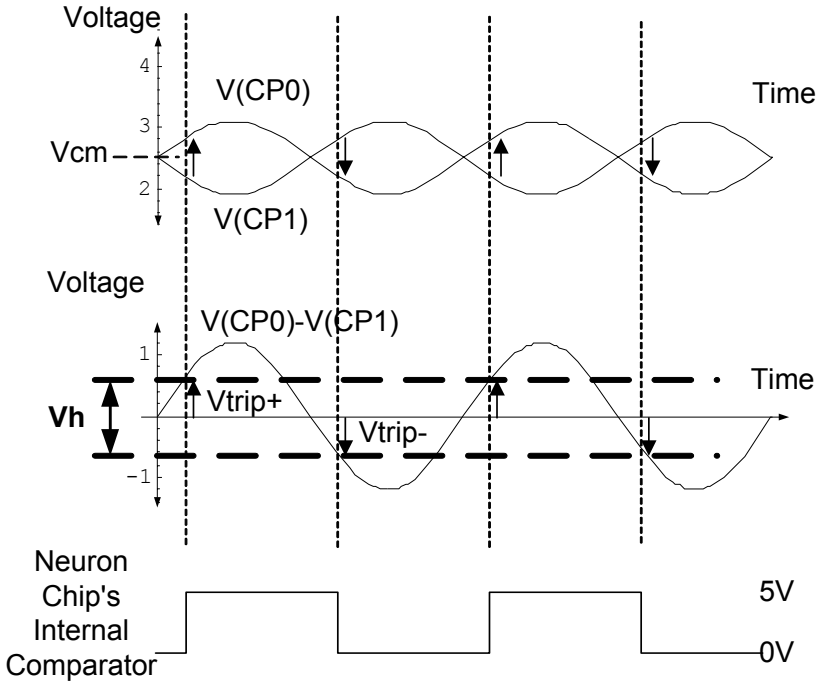
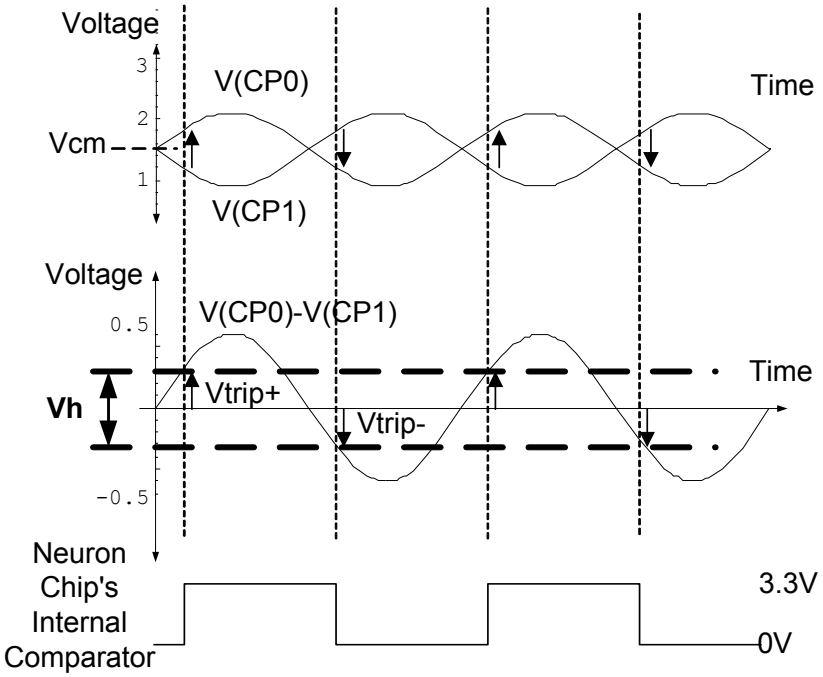


Figure 7. External Memory Interface Timing Diagram



Common-Mode voltage: Vcm = (V(CP0) + V(CP1)) / 2
Hysteresis Voltage: Vh = [Vtrip+] - [Vtrip-]

Figure 8. Differential Receiver Input Hysteresis Voltage Measurement Waveforms for 5V Operation



Common-Mode voltage: Vcm = (V(CP0) + V(CP1)) / 2
Hysteresis Voltage: Vh = [Vtrip+] - [Vtrip-]

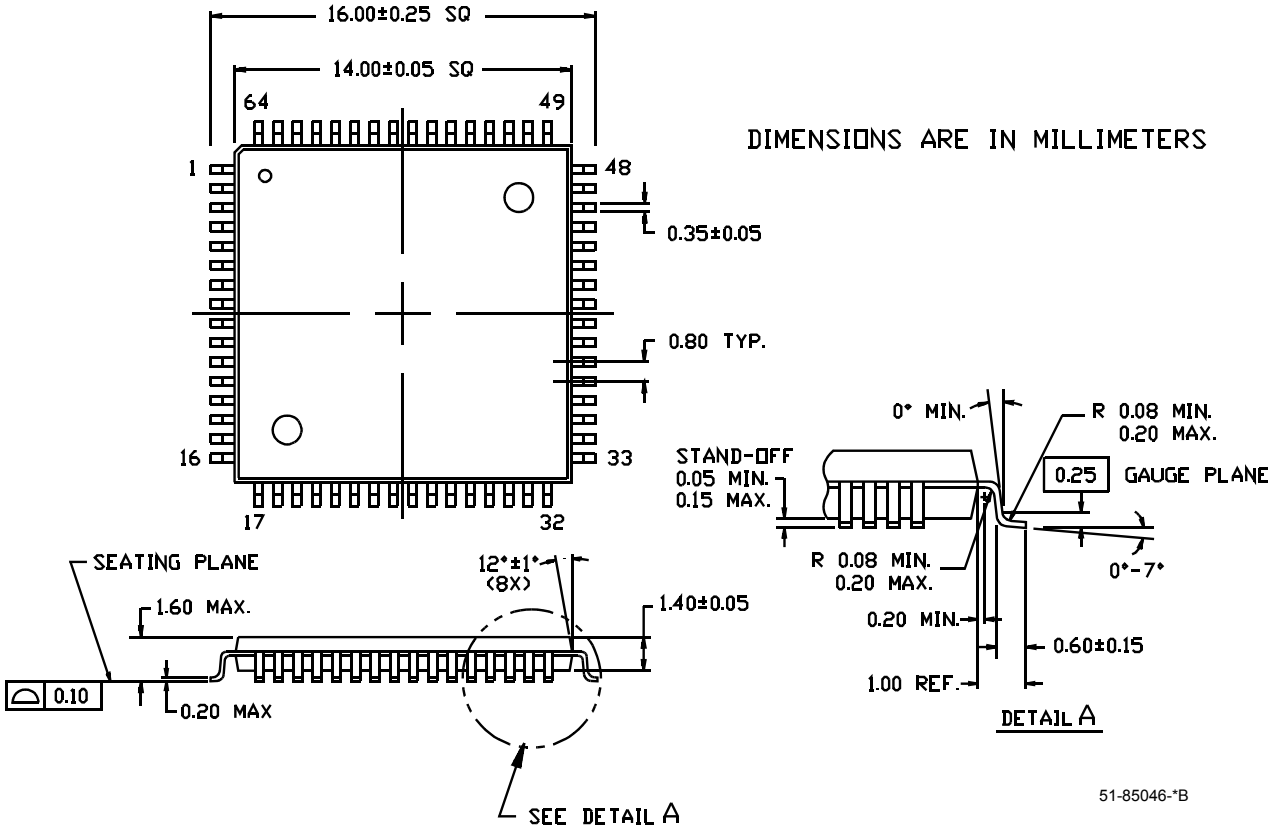
Figure 9. Differential Receiver Input Hysteresis Voltage Measurement Waveforms for 3.3V Operation

Ordering Information

Part Number	Flash (KBytes)	ROM (KBytes)	SRAM (KBytes)	Max. Input Clock (MHz)	Package Name	Package Type
CY7C53150L-64AI	2.75	0	4	10	A65	64-lead Thin Plastic Quad Flat Pack
CY7C53120L8-32SI	8	16	4	20	S34	32-lead (450 mil) Molded SOIC
CY7C53120L8-44AI	8	16	4	20	A44	44-lead Thin Plastic Quad Flat Pack

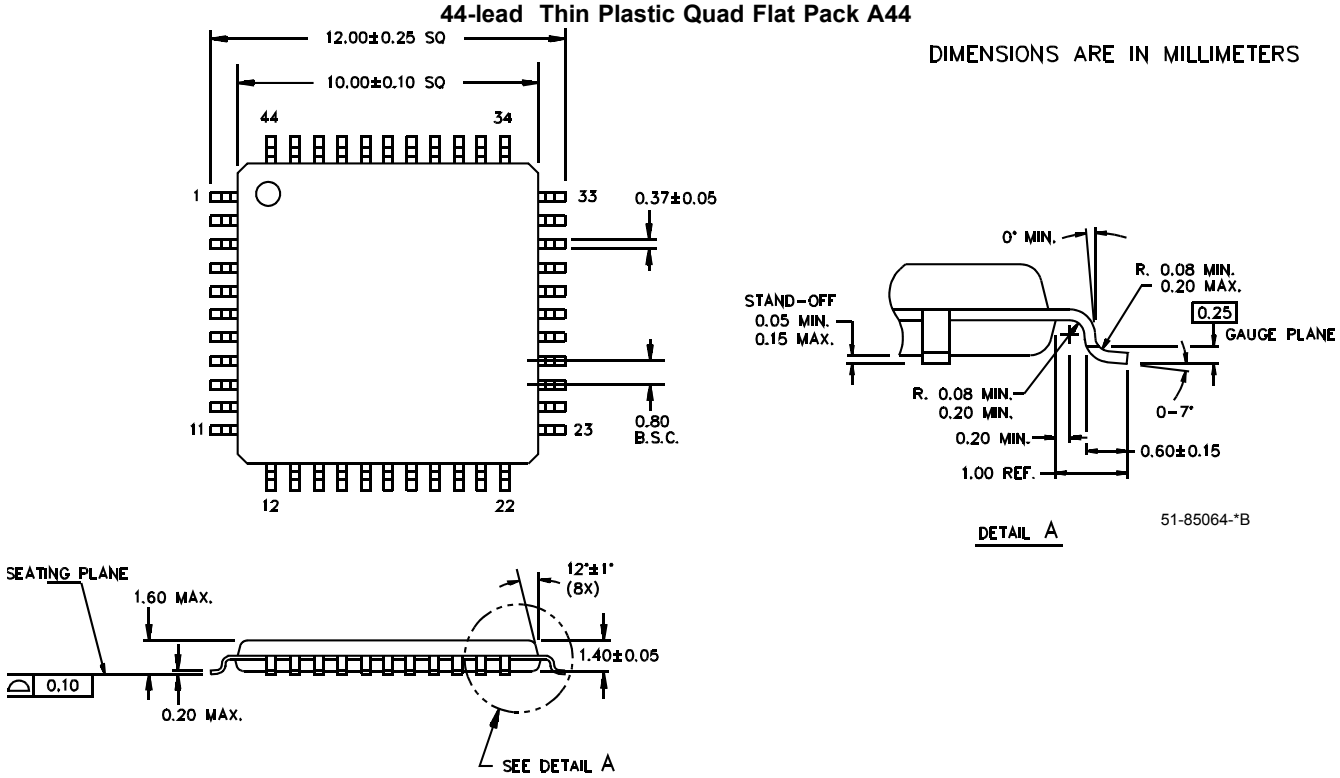
Package Diagrams

64-lead Thin Plastic Quad Flat Pack (14 × 14 × 1.4 mm) A65

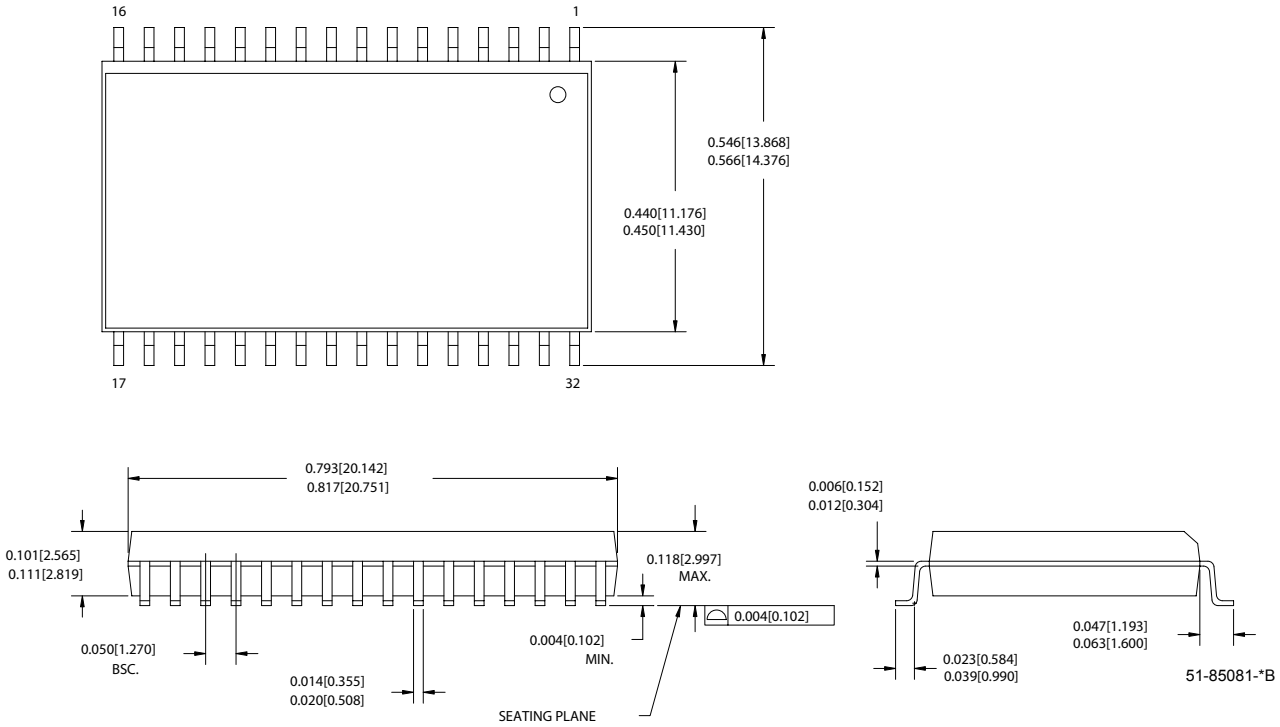


Package Diagrams (continued)

44-lead Thin Plastic Quad Flat Pack A44



32-Lead (450 MIL) Molded SOIC S34



Document History Page

Document Title: CY7C53150L/CY7C53120L8 3.3V Neuron® Chip Network Processor Document Number: 38-10002				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	121963	12/12/02	PVO	New data sheet
*A	123762	03/03/03	PVO	Changed Advance Information to Preliminary Added information on LVI, UART/SPI, Reset Stretching Corrected values of ROM, Hysteresis, and I_{PU} Added 100-pin TQFP pin definitions Made minor corrections to grammar and formatting
*B	125311	03/21/03	KBO	Add information on Power Sequence Corrected values of ROM Added default values of LVI, LVI filter and SPI divisor. Corrected I_{pu} Current limit values Clarified Reset Stretch times Corrected pin definitions (pins 10 to 14) on 100pin TQFP diagram Added Theta-JA value for the 100-pin TQFP package Changed part numbers to CY7C53120L8 / CY7C53150L Added ordering information table
*C	130922	12/31/03	TGE	Add footnote #4 on Power supply considerations Corrected Theta-JA values for all packages Added information on LVI limitations Added information on Reset operation at 5V Added information on Communication Port operation at 5V Added information on Manufacturer ID
*D	210068	See ECN	TGE	Removed 100-pin package
*E	283876	See ECN	TGE	Added SPI Slave Mode Errata Note