Hitachi 16-Bit Single-Chip Microcomputer

H8S/2319, H8S/2318 Series, H8S/2319 F-ZTAT™, H8S/2318 F-ZTAT™, H8S/2315 F-ZTAT™

H8S/2319	HD64F2319
H8S/2318	HD6432318, HD64F2318
H8S/2317	HD6432317
H8S/2316	HD6432316
H8S/2315	HD64F2315
H8S/2313	HD6432313
H8S/2312	HD6412312
H8S/2311	HD6432311
H8S/2310	HD6412310

Reference Manual

— Individual Product Specifications —

HITACHI

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Hitachi semiconductor

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Main Revisions and Additions in this Edition

Page	Item	Revisions (See Manual for Details)
All	Whole sections	Amendment due to the addition of the H8S/2319 F-ZTAT, H8S/2315 F-ZTAT, H8S/2316, and H8S/2313 to the product lineup.
5	1.1 Overview	Table 1.1 Overview The product lineup added.
6	1.2 Block Diagram	Figure 1.1 Block Diagram Note 1 amended due to the addition of $\overline{\text{WDTOVF}}$ (FWE, EMLE).
7	1.3 Pin Arrangement	Figure 1.2 Pin Arrangement Note amended due to the addition of $\overline{\text{WDTOVF}}$ (FWE, EMLE).
8		Figure 1.3 Pin Arrangement Note amended due to the addition of $\overline{\text{WDTOVF}}$ (FWE, EMLE).
10	1.4 Pin Functions in Each Operating Mode	Table 1.2 Pin Functions in Each Operating Mode Functions for pins 32 to 39, 41 to 48, and 50 to 52 (TFP-100B) in flash memory programmer mode amended. Function for pin 60 (TFP-100B) amended
12		Note 3 amended.
15	1.5 Pin Functions	Table 1.3 Pin Functions EMLE pin added.
19		Note 4 added.
20	1.6 Product Lineup	Note 2 added.
32	2.5 Memory Map in Each Operating Mode	Figure 2.1 H8S/2319 F-ZTAT Memory Map in Each Operating Mode added.
33 to 36, 42		Figures 2.2, 2.3, and 2.7 Memory Map in Each Operating Mode Note on reserved area added.
37		Figure 2.4 H8S/2316 Memory Map in Each Operating Mode added.
38 to 40		Figure 2.5 H8S/2315 F-ZTAT Memory Map in Each Operating Mode added.
41		Figure 2.6 H8S/2313 Memory Map in Each Operating Mode added.
—	2.6 H8S/2318 Series Operating Modes (F-ZTAT Version)	Deleted (see the hardware manual).

Page	Item	Revisions (See Manual for Details)
51	3.3.3 Interrupt Exception Vector Table	Table 3.3 Interrupt Sources, Vector Addresses, and Interrupt Priorities Names for SCI interrupts RXI0 and RXI1 amended.
54	3.5 Interrupt Response Times	Table 3.8 Interrupt Response Times Number of wait states until execution instruction ends amended.
73	4.2.5 Bus Control Register L (BCRL)	Description of bit 5 H8S/2319, H8S/2316, H8S/2315, and H8S/2313 added
177	5.13 Pin States	Table 5.23 I/O Port States in Each Processing State LWROD and DAOEn added to Legend.
200	5.14.11 Port G	Figure 5.35(a) Port G Block Diagram (Pin PG0) Amended.
225	6.11 ROM	Amended due to the addition of the H8S/2319 F-ZTAT to the product lineup.
252	7.1.4 A/D Conversion Characteristics	Table 7.8 A/D Conversion Characteristics Nonlinearity error, offset error, full-scale error, quantization error, and absolute accuracy amended.
254 to 262	7.2 Electrical Characteristics of Mask ROM Version (H8S/2318, H8S/2317) in Low-Voltage Operation	Added.
263	7.3 Electrical Characteristics of F-ZTAT Version (H8S/2318)	Table 7.19 Absolute Maximum Ratings Conditions A and B added. Note amended.
264 to 267	7.3.2 DC Characteristics	Tables 7.20 (a) and (b) DC Characteristics Maximum value of input leakage current, typical and maximum values of current dissipation, typical and maximum values of analog power supply voltage, typical and maximum values of reference power supply voltage, and equation in note 4 amended.
—	7.3.3 AC Characteristics	Table 7.25 Timing of On-Chip Supporting Modules WDT overflow output delay time deleted.
275	7.3.4 A/D Conversion Characteristics	Table 7.26 A/D Conversion Characteristics Nonlinearity error, offset error, full-scale error, quantization error, and absolute accuracy amended.

Page	Item	Revisions (See Manual for Details)
277 to 280	7.3.6 Flash Memory Characteristics	Tables 7.28 (a) and (b) Flash Memory Characteristics Completely replaced.
281 to 298	7.4 Electrical Characteristics of F-ZTAT Version (H8S/2315)	Added.
—		7.3.1 Notes when Converting the F-ZTAT Application Software to the Mask-ROM Versions (in the 1st Edition) Deleted (see the hardware manual).
305	8.1 List of Registers (Address Order)	H'FFC8: FLMCR1 H'FFC9: FLMCR2 H'FFCB: EBR2 Amended.
345	8.3 Functions	H'FED5: BCRL Description of bit 5 amended.
351		H'FF37: DTVECR Description of bit 7 amended.
402, 403		H'FFC8: FLMCR1 Amended.
404, 405		H'FFC9: FLMCR2 Amended.
406		H'FFCB: EBR2 Amended.

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Organization of H8S/2319, H8S/2318 Series Reference Manual

The following manuals are available for H8S/2319, H8S/2318 Series.

Table 1 Manuals

Title	Document Code
H8S/2600 Series, H8S/2000 Series Programming Manual	ADE-602-083A
H8S/2339 Series, H8S/2338 Series, H8S/2329 Series, H8S/2328 Series, H8S/2319 Series, H8S/2318 Series Hardware Manual	ADE-602-171A (in preparation)
H8S/2319, H8S/2318 Series, H8S/2319 F-ZTAT™, H8S/2318 F-ZTAT™, H8S/2315 F-ZTAT™ Reference Manual	ADE-602-188A

The H8S/2600 Series, H8S/2000 Series Programming Manual gives a detailed description of the architecture and instruction set of the H8S/2000 CPU.

The H8S/2339 Series, H8S/2338 Series, H8S/2329 Series, H8S/2328 Series, H8S/2319 Series, H8S/2318 Series Hardware Manual describes the operation of on-chip functions, and gives a detailed description of the related registers.

The H8S/2319, H8S/2318 Series, H8S/2319 F-ZTAT™, H8S/2318 F-ZTAT™, H8S/2315 F-ZTAT™ Reference Manual mainly covers information specific to H8S/2319, H8S/2318 Series and H8S/2318 F-ZTAT™ products, including pin arrangement, I/O ports, MCU operating modes (address maps), interrupt vectors, bus control, and electrical characteristics, and also includes a brief description of all I/O registers for the convenience of the user.

The contents of H8S/2339 Series, H8S/2338 Series, H8S/2329 Series, H8S/2328 Series, H8S/2319 Series, H8S/2318 Series Hardware Manual and the H8S/2319, H8S/2318 Series, H8S/2319 F-ZTAT™, H8S/2318 F-ZTAT™, H8S/2315 F-ZTAT™ Reference Manual are summarized in table 2.

Table 2 Contents of Hardware Manual and Reference Manual

No.	Item	Hardware Manual	Reference Manual
1	Overview	○	○ (including pin arrangement)
2	MCU operating modes (including address maps)	—	◎
3	Exception handling	○	○
4	Interrupt controller	◎	○
5	Bus controller	◎	◎
6	DMA controller (DMAC)	◎	—
7	Data transfer controller (DTC)	◎	—
8	16-bit timer pulse unit (TPU)	◎	—
9	Programmable pulse generator (PPG)	◎	—
10	8-bit timers	◎	—
11	Watchdog timer	◎	—
12	Serial communication interface (SCI)	◎	—
13	Smart card interface	◎	—
14	A/D converter	◎	—
15	D/A converter	◎	—
16	RAM	◎	—
17	ROM (flash memory)	◎	—
18	Clock pulse generator	◎	—
19	Power-down modes	◎	—
20	I/O ports (including port block diagrams)	—	◎
21	Electrical characteristics	—	○
22	Register reference chart (in address order, with function summary)	—	○
23	Instruction set	○	—
24	Package dimension diagrams	—	○

○: Included

◎: Included (with detailed register descriptions)

—: Not included

The following chart shows where to find various kinds of information for different purposes.

For product evaluation information, or comparative specification information for current users of Hitachi products

For product specifications

Overview	1.1 Overview
Pin arrangement diagram	1.3 Pin Arrangement
Block diagrams of function modules	Section 6 Peripheral Block Diagrams
Pin functions	1.5 Pin Functions
Electrical characteristics	Section 7 Electrical Characteristics

For detailed information on functions

For details of operation of modules

I/O port information	Section 5 I/O Ports
Interrupts and exception handling	Section 3 Exception Handling and Interrupt Controller
Information on other modules	H8S/2339 Series, H8S/2338 Series, H8S/2329 Series, H8S/2328 Series, H8S/2319 Series, H8S/2318 Series Hardware Manual
Pin functions	1.5 Pin Functions

For information on operating modes

List	1.4 Pin Functions in Each Operating Mode
Detailed descriptions	Section 2 MCU Operating Modes

For use as design material

For information on registers

List	Section 8 registers
To find a register from its address	8.1 List of Registers (Address Order)
To find register information by function	8.2 List of Registers (By Module)
Setting procedure and notes	H8S/2339 Series, H8S/2338 Series, H8S/2329 Series, H8S/2328 Series, H8S/2319 Series, H8S/2318 Series Hardware Manual

For information on instructions

List	
Operation description and notes	H8S/2600 Series, H8S/2000 Series Programming Manual
Program examples	

The H8S/2339 Series, H8S/2338 Series, H8S/2329 Series, H8S/2328 Series, H8S/2319 Series, and H8S/2318 Series have the on-chip modules shown below

Table 3 H8S/2339, H8S/2338, H8S/2329, H8S/2328, H8S/2319, and H8S/2318 Series On-Chip Modules

On-Chip Module	H8S/2339 Series, H8S/2338 Series	H8S/2329 Series, H8S/2328 Series	H8S/2319 Series, H8S/2318 Series
CPU	○	○	○
Bus controller (BUSC)	○	○	○
DRAM controller	○	○	×
DMA controller (DMAC)	○	○	×
Data transfer controller (DTC)	○	○	○
16-bit timer pulse unit (TPU)	○ (6 channels)	○ (6 channels)	○ (6 channels)
Programable pulse generator (PPG)	○	○	×
8-bit timer	○ (2 channels)	○ (2 channels)	○ (2 channels)
Watchdog timer	○	○	○
Serial communication interface (SCI)	○ (3 channels)	○ (3 channels)	○ (2 channels)
A/D converter	○ (12 channels)	○ (8 channels)	○ (8 channels)
D/A converter	○ (4 channels)	○ (2 channels)	○ (2 channels)
Interrupt controller (INTC)	○	○	○

Memory*	Product Code	ROM (kbytes)	RAM (kbytes)	Product Code	ROM (kbytes)	RAM (kbytes)	Product Code	ROM (kbytes)	RAM (kbytes)
	H8S/2339	384	32	H8S/2329	384	32	H8S/2319	512	8
	H8S/2338	256	8	H8S/2328	256	8	H8S/2318	256	8
	H8S/2337	128	8	H8s/2327	128	8	H8S/2317	128	8
	H8S/2332	—	8	H8S/2324	—	32	H8S/2316	64	8
				H8S/2323	32	8	H8S/2315	384	8
				H8S/2322R	—	8	H8S/2313	64	2
				H8S/2320	—	4	H8S/2312	—	8
							H8S/2311	32	2
							H8S/2310	—	2

○: On-chip

×: Not on-chip

Note: * See the reference manual of each series for details.

Contents

Section 1 Overview

1.1 Overview

The H8S/2319 and H8S/2318 Series are series of microcomputers (MCUs: microcomputer units), built around the H8S/2000 CPU, employing Hitachi's proprietary architecture, and equipped with peripheral functions on-chip.

The H8S/2000 CPU has an internal 32-bit architecture, is provided with sixteen 16-bit general registers and a concise, optimized instruction set designed for high-speed operation, and can address a 16-Mbyte linear address space. The instruction set is upward-compatible with H8/300 and H8/300H CPU instructions at the object-code level, facilitating migration from the H8/300, H8/300L, or H8/300H Series.

On-chip peripheral functions required for system configuration include data transfer controller (DTC) bus master, ROM and RAM memory, a 16-bit timer pulse unit (TPU), 8-bit timer, watchdog timer (WDT), serial communication interface (SCI), A/D converter, D/A converter, and I/O ports.

Single-power-supply flash memory (F-ZTAT™*) and mask ROM versions are available, providing a quick and flexible response to conditions from ramp-up through full-scale volume production, even for applications with frequently changing specifications. ROM is connected to the CPU via a 16-bit data bus, enabling both byte and word data to be accessed in one state. Instruction fetching is thus speeded up, and processing speed increased.

The features of the H8S/2319 and H8S/2318 Series are shown in table 1.1.

Note: * F-ZTAT is a trademark of Hitachi, Ltd.

Table 1.1 Overview

Item	Specification
CPU	• General-register machine — Sixteen 16-bit general registers (also usable as sixteen 8-bit registers or eight 32-bit registers) • High-speed operation suitable for realtime control — Maximum clock rate: 25 MHz — High-speed arithmetic operations 8/16/32-bit register-register add/subtract: 40 ns (at 25 MHz operation) 16 × 16-bit register-register multiply: 800 ns (at 25 MHz operation) 32 ÷ 16-bit register-register divide: 800 ns (at 25 MHz operation) • Instruction set suitable for high-speed operation — Sixty-five basic instructions — 8/16/32-bit data transfer, arithmetic, and logic instructions — Unsigned/signed multiply and divide instructions — Powerful bit-manipulation instructions • CPU operating mode — Advanced mode: 16-Mbyte address space
Bus controller	• Address space divided into 8 areas, with bus specifications settable independently for each area • Chip select output possible for each area • Choice of 8-bit or 16-bit access space for each area • 2-state or 3-state access space can be designated for each area • Number of program wait states can be set for each area • Burst ROM directly connectable • External bus release function
Data transfer controller (DTC)	• Can be activated by internal interrupt or software • Multiple transfers or multiple types of transfer possible for one activation source • Transfer possible in repeat mode, block transfer mode, etc. • Request can be sent to CPU for interrupt that activated DTC

Item	Specification
16-bit timer pulse unit (TPU)	• 6-channel 16-bit timer on-chip • Pulse I/O processing capability for up to 16 pins • Automatic 2-phase encoder count capability
8-bit timer, 2 channels	• 8-bit up-counter (external event count capability) • Two time constant registers • Two-channel connection possible
Watchdog timer	• Watchdog timer or interval timer selectable
Serial communication interface (SCI), 2 channels	• Asynchronous mode or synchronous mode selectable • Multiprocessor communication function • Smart card interface function
A/D converter	• Resolution: 10 bits • Input: 8 channels • 6.7 µs minimum conversion time (at 20 MHz operation) • Single or scan mode selectable • Sample-and-hold function • A/D conversion can be activated by external trigger or timer trigger
D/A converter	• Resolution: 8 bits • Output: 2 channels
I/O ports	• 71 input/output pins, 8 input-only pins
Memory	• Flash memory and mask ROM • High-speed static RAM
Interrupt controller	• Nine external interrupt pins (NMI, $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ7}}$) • 43 internal interrupt sources • Eight priority levels settable

Product Name	ROM	RAM
H8S/2319*	512 kbytes	8 kbytes
H8S/2318	256 kbytes	8 kbytes
H8S/2317	128 kbytes	8 kbytes
H8S/2316	64 kbytes	8 kbytes
H8S/2315*	384 kbytes	8 kbytes
H8S/2313	64 kbytes	2 kbytes
H8S/2312	—	8 kbytes
H8S/2311	32 kbytes	2 kbytes
H8S/2310	—	2 kbytes

Note: * Under development

Item	Specification
Power-down state	• Medium-speed mode • Sleep mode • Module stop mode • Software standby mode • Hardware standby mode • Variable clock division ratio
Operating modes	• Eight MCU operating modes (H8S/2318 F-ZTAT, H8S/2315 F-ZTAT)

Mode	CPU Operating Mode	Description	On-Chip ROM	External Data Bus	
				Initial Value	Maximum Value
0	—	—	—	—	—
1					
2					
3					
4	Advanced	Expanded mode with on-chip ROM disabled	Disabled	16 bits	16 bits
5				8 bits	16 bits
6		Expanded mode with on-chip ROM enabled	Enabled	8 bits	16 bits
7		Single-chip mode		—	—
8	—	—	—	—	—
9					
10	Advanced	Boot mode	Enabled	8 bits	16 bits
11				—	—
12	—	—	—	—	—
13					
14	Advanced	User program mode	Enabled	8 bits	16 bits
15				—	—

Item | **Specification**

Operating modes

- Four MCU operating modes (mask ROM version and ROMless version H8S/2319 F-ZTAT)

Mode	CPU Operating Mode	Description	On-Chip ROM	External Data Bus: Initial Value	External Data Bus: Maximum Value
1	—	—	—	—	—
2					
3					
4*	Advanced	Expanded mode with on-chip ROM disabled	Disabled	16 bits	16 bits
5*		Expanded mode with on-chip ROM disabled	Disabled	8 bits	16 bits
6		Expanded mode with on-chip ROM enabled	Enabled	8 bits	16 bits
7		Single-chip mode	Enabled	—	—

Note: * Only modes 4 and 5 are provided in the ROMless version.

Clock pulse generator

- Built-in duty correction circuit

Package

- 100-pin plastic TQFP (TFP-100B)
- 100-pin plastic QFP (FP-100A)

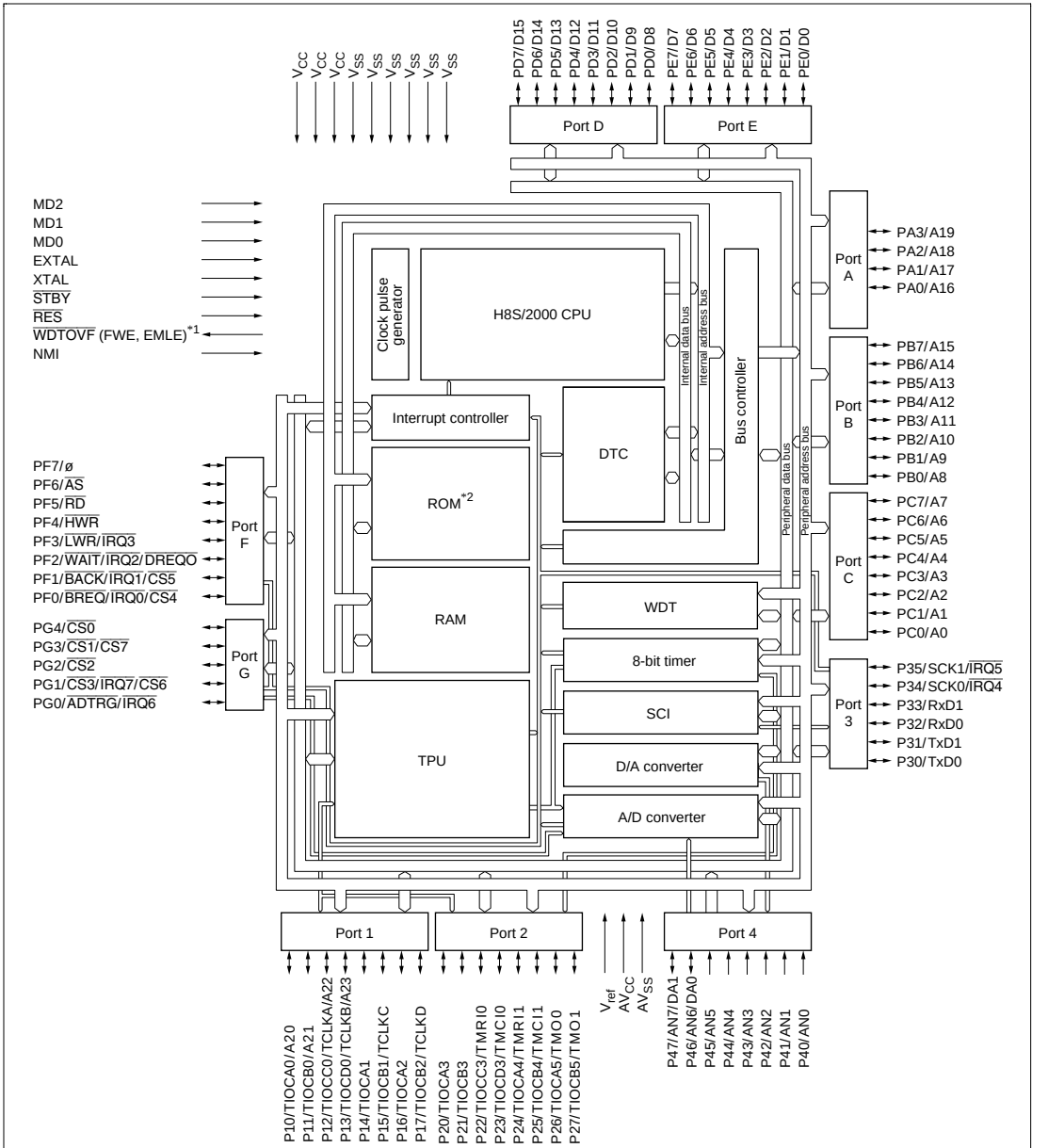
Product lineup

		Condition A	Condition B	Condition C*[1]
Operating power supply voltage		2.7 to 3.6 V	3.0 to 3.6 V	2.4 to 3.6 V
Operating frequency		2 to 20 MHz	2 to 25 MHz	2 to 14 MHz
Model	HD64F2319	*[3]	*[2]	—
	HD64F2318	*[3]	O	—
	HD6432318	O	O	O
	HD6432317	O	O	O
	HD6432316	O	O	*[2]
	HD64F2315	*[3]	*[2]	—
	HD6432313	O	O	*[2]
	HD6412312	O	O	—
	HD6432311	O	O	—
	HD6412310	O	O	—

O: Products in the current lineup

Notes: 1. T_a = –40°C to 85°C (wide-range specifications) is not available for condition C.
2. Under development
3. In planning stage

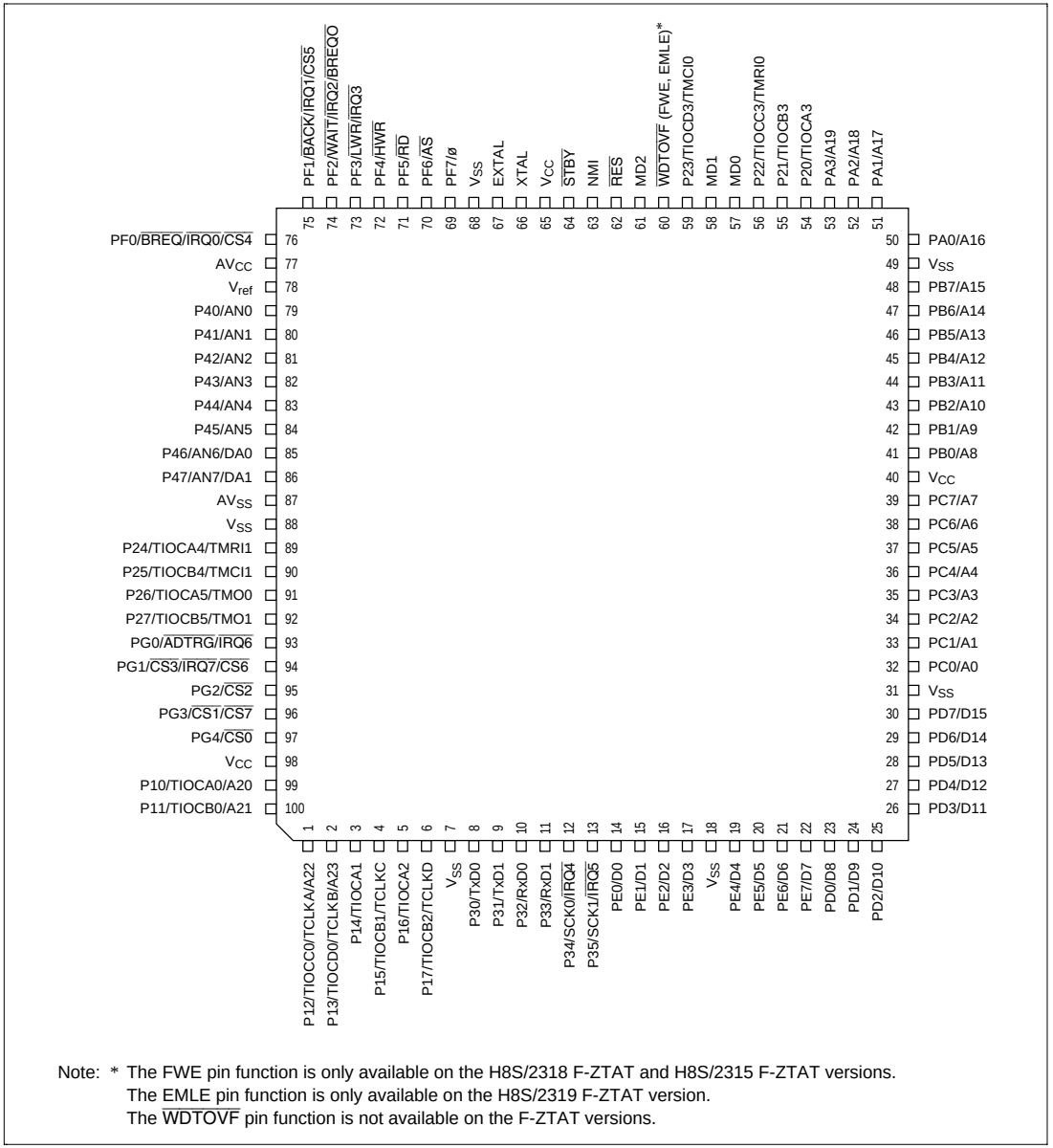
1.2 Block Diagram



Notes: 1. The FWE pin function is only available on the H8S/2318 F-ZTAT and H8S/2315 F-ZTAT versions.
The EMLE pin function is only available on the H8S/2319 F-ZTAT version.
The WDTOVF pin function is not available on the F-ZTAT versions.
2. ROM is not supported on the ROMless version.

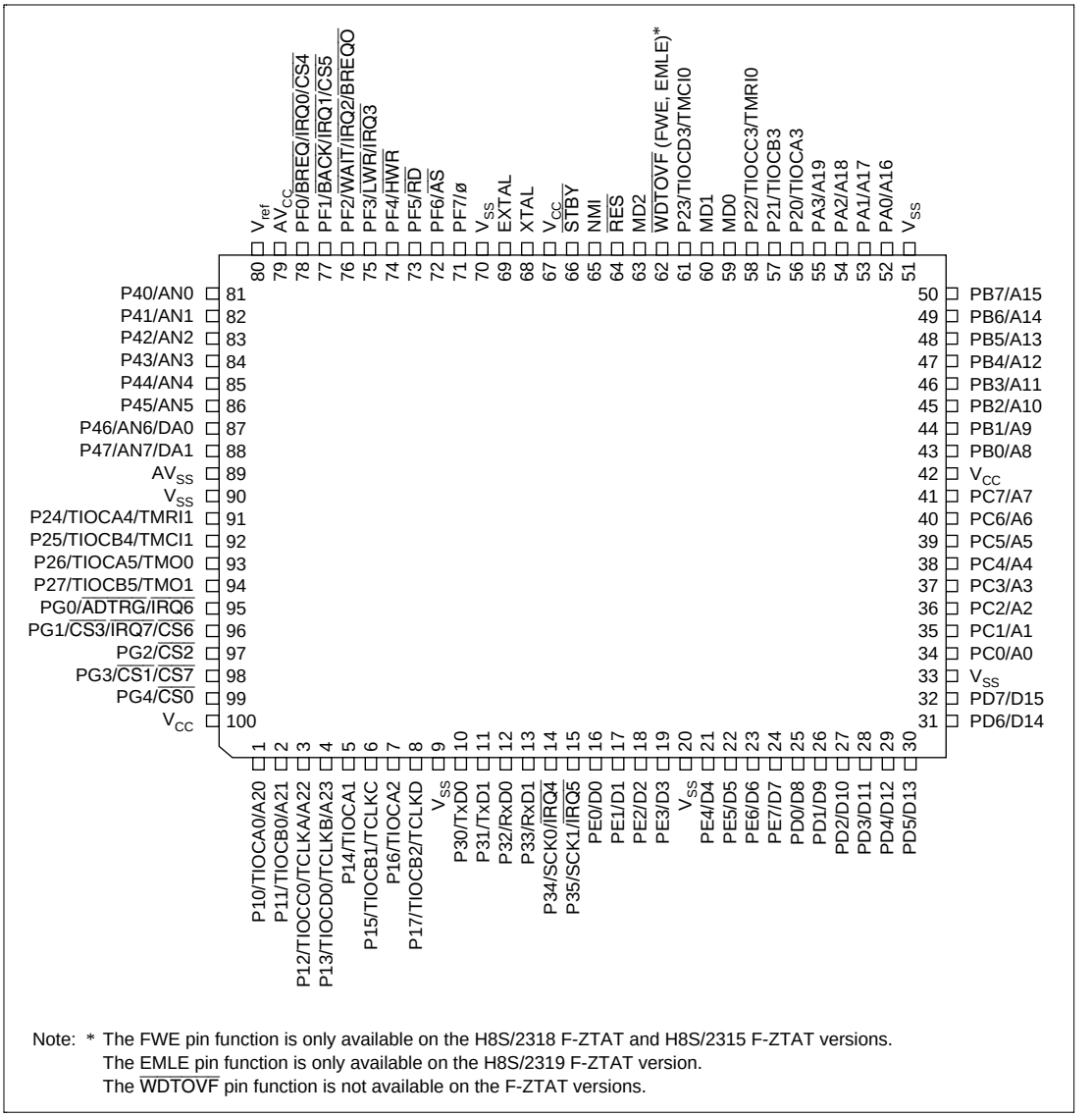
Figure 1.1 Block Diagram

1.3 Pin Arrangement



Note: * The FWE pin function is only available on the H8S/2318 F-ZTAT and H8S/2315 F-ZTAT versions.
The EMLE pin function is only available on the H8S/2319 F-ZTAT version.
The WDTOVF pin function is not available on the F-ZTAT versions.

Figure 1.2 Pin Arrangement (TFP-100B: Top View)



Note: * The FWE pin function is only available on the H8S/2318 F-ZTAT and H8S/2315 F-ZTAT versions.
The EMLE pin function is only available on the H8S/2319 F-ZTAT version.
The WDTOVF pin function is not available on the F-ZTAT versions.

Figure 1.3 Pin Arrangement (FP-100A: Top View)

1.4 Pin Functions in Each Operating Mode

Table 1.2 shows the pin functions in each of the operating modes.

Table 1.2 Pin Functions in Each Operating Mode

Pin No.		Pin Name				
TFP-100B	FP-100A	Mode 4	Mode 5	Mode 6*1	Mode 7*1	Flash Memory Programmer Mode*2
1	3	P12/TIOCC0/ TCLKA/A22	P12/TIOCC0/ TCLKA/A22	P12/TIOCC0/ TCLKA/A22	P12/TIOCC0/ TCLKA	NC
2	4	P13/TIOCD0/ TCLKB/A23	P13/TIOCD0/ TCLKB/A23	P13/TIOCD0/ TCLKB/A23	P13/TIOCD0/ TCLKB	NC
3	5	P14/TIOCA1	P14/TIOCA1	P14/TIOCA1	P14/TIOCA1	NC
4	6	P15/TIOCB1/ TCLKC	P15/TIOCB1/ TCLKC	P15/TIOCB1/ TCLKC	P15/TIOCB1/ TCLKC	NC
5	7	P16/TIOCA2	P16/TIOCA2	P16/TIOCA2	P16/TIOCA2	NC
6	8	P17/TIOCB2/ TCLKD	P17/TIOCB2/ TCLKD	P17/TIOCB2/ TCLKD	P17/TIOCB2/ TCLKD	NC
7	9	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
8	10	P30/TxD0	P30/TxD0	P30/TxD0	P30/TxD0	NC
9	11	P31/TxD1	P31/TxD1	P31/TxD1	P31/TxD1	NC
10	12	P32/RxD0	P32/RxD0	P32/RxD0	P32/RxD0	NC
11	13	P33/RxD1	P33/RxD1	P33/RxD1	P33/RxD1	NC
12	14	P34/SCK0/$\overline{IRQ4}$	P34/SCK0/$\overline{IRQ4}$	P34/SCK0/$\overline{IRQ4}$	P34/SCK0/$\overline{IRQ4}$	NC
13	15	P35/SCK1/$\overline{IRQ5}$	P35/SCK1/$\overline{IRQ5}$	P35/SCK1/$\overline{IRQ5}$	P35/SCK1/$\overline{IRQ5}$	NC
14	16	PE0/D0	PE0/D0	PE0/D0	PE0	NC
15	17	PE1/D1	PE1/D1	PE1/D1	PE1	NC
16	18	PE2/D2	PE2/D2	PE2/D2	PE2	NC
17	19	PE3/D3	PE3/D3	PE3/D3	PE3	NC
18	20	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
19	21	PE4/D4	PE4/D4	PE4/D4	PE4	NC
20	22	PE5/D5	PE5/D5	PE5/D5	PE5	NC
21	23	PE6/D6	PE6/D6	PE6/D6	PE6	NC
22	24	PE7/D7	PE7/D7	PE7/D7	PE7	NC
23	25	D8	D8	D8	PD0	FO0
24	26	D9	D9	D9	PD1	FO1
25	27	D10	D10	D10	PD2	FO2

Pin No.		Pin Name				
TFP-100B	FP-100A	Mode 4	Mode 5	Mode 6*1	Mode 7*1	Flash Memory Programmer Mode*2
26	28	D11	D11	D11	PD3	FO3
27	29	D12	D12	D12	PD4	FO4
28	30	D13	D13	D13	PD5	FO5
29	31	D14	D14	D14	PD6	FO6
30	32	D15	D15	D15	PD7	FO7
31	33	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
32	34	A0	A0	PC0/A0	PC0	A0
33	35	A1	A1	PC1/A1	PC1	A1
34	36	A2	A2	PC2/A2	PC2	A2
35	37	A3	A3	PC3/A3	PC3	A3
36	38	A4	A4	PC4/A4	PC4	A4
37	39	A5	A5	PC5/A5	PC5	A5
38	40	A6	A6	PC6/A6	PC6	A6
39	41	A7	A7	PC7/A7	PC7	A7
40	42	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
41	43	A8	A8	PB0/A8	PB0	A8
42	44	A9	A9	PB1/A9	PB1	A9
43	45	A10	A10	PB2/A10	PB2	A10
44	46	A11	A11	PB3/A11	PB3	A11
45	47	A12	A12	PB4/A12	PB4	A12
46	48	A13	A13	PB5/A13	PB5	A13
47	49	A14	A14	PB6/A14	PB6	A14
48	50	A15	A15	PB7/A15	PB7	A15
49	51	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
50	52	A16	A16	PA0/A16	PA0	A16
51	53	A17	A17	PA1/A17	PA1	A17
52	54	A18	A18	PA2/A18	PA2	A18
53	55	A19	A19	PA3/A19	PA3	NC
54	56	P20/TIOCA3	P20/TIOCA3	P20/TIOCA3	P20/TIOCA3	$\overline{OE}$
55	57	P21/TIOCB3	P21/TIOCB3	P21/TIOCB3	P21/TIOCB3	$\overline{CE}$
56	58	P22/TIOCC3/ TMRI0	P22/TIOCC3/ TMRI0	P22/TIOCC3/ TMRI0	P22/TIOCC3/ TMRI0	$\overline{WE}$
57	59	MD0	MD0	MD0	MD0	V_{SS}
58	60	MD1	MD1	MD1	MD1	V_{SS}
59	61	P23/TIOCD3/ TMCI0	P23/TIOCD3/ TMCI0	P23/TIOCD3/ TMCI0	P23/TIOCD3/ TMCI0	V_{CC}
60	62	$\overline{WDTOVF}$ (FWE, EMLE)*3	$\overline{WDTOVF}$ (FWE, EMLE)*3	$\overline{WDTOVF}$ (FWE, EMLE)*3	$\overline{WDTOVF}$ (FWE, EMLE)*3	FWE

Pin No.		Pin Name				
TFP-100B	FP-100A	Mode 4	Mode 5	Mode 6*1	Mode 7*1	Flash Memory Programmer Mode*2
61	63	MD2	MD2	MD2	MD2	V_{SS}
62	64	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$
63	65	NMI	NMI	NMI	NMI	V_{CC}
64	66	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	V_{CC}
65	67	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
66	68	XTAL	XTAL	XTAL	XTAL	XTAL
67	69	EXTAL	EXTAL	EXTAL	EXTAL	EXTAL
68	70	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
69	71	PF7/ø	PF7/ø	PF7/ø	PF7/ø	NC
70	72	PF6/$\overline{AS}$	PF6/$\overline{AS}$	PF6/$\overline{AS}$	PF6	NC
71	73	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	PF5	NC
72	74	$\overline{HWR}$	$\overline{HWR}$	$\overline{HWR}$	PF4	NC
73	75	PF3/$\overline{LWR}$/$\overline{IRQ3}$	PF3/$\overline{LWR}$/$\overline{IRQ3}$	PF3/$\overline{LWR}$/$\overline{IRQ3}$	PF3/$\overline{IRQ3}$	NC
74	76	PF2/$\overline{WAIT}$/ $\overline{IRQ2}$/$\overline{DREQO}$	PF2/$\overline{WAIT}$/ $\overline{IRQ2}$/$\overline{DREQO}$	PF2/$\overline{WAIT}$/ $\overline{IRQ2}$/$\overline{DREQO}$	PF2/$\overline{IRQ2}$	V_{CC}
75	77	PF1/$\overline{BACK}$/ $\overline{IRQ1}$/$\overline{CS5}$	PF1/$\overline{BACK}$/ $\overline{IRQ1}$/$\overline{CS5}$	PF1/$\overline{BACK}$/ $\overline{IRQ1}$/$\overline{CS5}$	PF1/$\overline{IRQ1}$	V_{SS}
76	78	PF0/$\overline{BREQ}$/ $\overline{IRQ0}$/$\overline{CS4}$	PF0/$\overline{BREQ}$/ $\overline{IRQ0}$/$\overline{CS4}$	PF0/$\overline{BREQ}$/ $\overline{IRQ0}$/$\overline{CS4}$	PF0/$\overline{IRQ0}$	V_{SS}
77	79	AV_{CC}	AV_{CC}	AV_{CC}	AV_{CC}	V_{CC}
78	80	V_{ref}	V_{ref}	V_{ref}	V_{ref}	V_{CC}
79	81	P40/AN0	P40/AN0	P40/AN0	P40/AN0	NC
80	82	P41/AN1	P41/AN1	P41/AN1	P41/AN1	NC
81	83	P42/AN2	P42/AN2	P42/AN2	P42/AN2	NC
82	84	P43/AN3	P43/AN3	P43/AN3	P43/AN3	NC
83	85	P44/AN4	P44/AN4	P44/AN4	P44/AN4	NC
84	86	P45/AN5	P45/AN5	P45/AN5	P45/AN5	NC
85	87	P46/AN6/DA0	P46/AN6/DA0	P46/AN6/DA0	P46/AN6/DA0	NC
86	88	P47/AN7/DA1	P47/AN7/DA1	P47/AN7/DA1	P47/AN7/DA1	NC
87	89	AV_{SS}	AV_{SS}	AV_{SS}	AV_{SS}	V_{SS}
88	90	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
89	91	P24/TIOCA4/ TMRI1	P24/TIOCA4/ TMRI1	P24/TIOCA4/ TMRI1	P24/TIOCA4/ TMRI1	NC
90	92	P25/TIOCB4/ TMCI1	P25/TIOCB4/ TMCI1	P25/TIOCB4/ TMCI1	P25/TIOCB4/ TMCI1	V_{SS}

Pin No.		Pin Name				
TFP-100B	**FP-100A**	**Mode 4**	**Mode 5**	**Mode 6**[*1]	**Mode 7**[*1]	**Flash Memory Programmer Mode**[*2]
91	93	P26/TIOCA5/ TMO0	P26/TIOCA5/ TMO0	P26/TIOCA5/ TMO0	P26/TIOCA5/ TMO0	NC
92	94	P27/TIOCB5/ TMO1	P27/TIOCB5/ TMO1	P27/TIOCB5/ TMO1	P27/TIOCB5/ TMO1	NC
93	95	PG0/$\overline{\text{IRQ6}}$/ $\overline{\text{ADTRG}}$	PG0/$\overline{\text{IRQ6}}$/ $\overline{\text{ADTRG}}$	PG0/$\overline{\text{IRQ6}}$/ $\overline{\text{ADTRG}}$	PG0/$\overline{\text{IRQ6}}$/ $\overline{\text{ADTRG}}$	NC
94	96	PG1/$\overline{\text{CS3}}$/ $\overline{\text{IRQ7}}$/$\overline{\text{CS6}}$	PG1/$\overline{\text{CS3}}$/ $\overline{\text{IRQ7}}$/$\overline{\text{CS6}}$	PG1/$\overline{\text{CS3}}$/ $\overline{\text{IRQ7}}$/$\overline{\text{CS6}}$	PG1/$\overline{\text{IRQ7}}$	NC
95	97	PG2/$\overline{\text{CS2}}$	PG2/$\overline{\text{CS2}}$	PG2/$\overline{\text{CS2}}$	PG2	NC
96	98	PG3/$\overline{\text{CS1}}$/$\overline{\text{CS7}}$	PG3/$\overline{\text{CS1}}$/$\overline{\text{CS7}}$	PG3/$\overline{\text{CS1}}$/$\overline{\text{CS7}}$	PG3	NC
97	99	PG4/$\overline{\text{CS0}}$	PG4/$\overline{\text{CS0}}$	PG4/$\overline{\text{CS0}}$	PG4	NC
98	100	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
99	1	P10/TIOCA0/A20	P10/TIOCA0/A20	P10/TIOCA0/A20	P10/TIOCA0	NC
100	2	P11/TIOCB0/A21	P11/TIOCB0/A21	P11/TIOCB0/A21	P11/TIOCB0	NC

Notes: 1. Only modes 4 and 5 are available on the ROMless version.

2. Flash memory programmer mode information is preliminary.

3. The FWE pin function is only available on the H8S/2318 F-ZTAT and H8S/2315 F-ZTAT versions.
The EMLE pin function is only available on the H8S/2319 F-ZTAT version.
It cannot be used as a $\overline{\text{WDTOVF}}$ pin on the F-ZTAT version.

1.5 Pin Functions

Table 1.3 Pin Functions

Type	Symbol	Pin No. TFP-100B	Pin No. FP-100A	I/O	Name and Function
Power	V_{CC}	40, 65, 98	42, 67, 100	Input	Power supply: For connection to the power supply. All V_{CC} pins should be connected to the system power supply.
	V_{SS}	7, 18, 31, 49, 68, 88	9, 20, 33, 51, 70, 90	Input	Ground: For connection to ground (0 V). All V_{SS} pins should be connected to the system power supply (0 V).
Clock	XTAL	66	68	Input	Connects to a crystal oscillator. See section 18, in the Hardware Manual, Clock Pulse Generator, for typical connection diagrams for a crystal oscillator and external clock input.
	EXTAL	67	69	Input	Connects to a crystal oscillator. The EXTAL pin can also input an external clock. See section 18, in the Hardware Manual, Clock Pulse Generator, for typical connection diagrams for a crystal oscillator and external clock input.
	ø	69	71	Output	System clock: Supplies the system clock to an external device.

Type	Symbol	Pin No. TFP-100B	Pin No. FP-100A	I/O	Name and Function
Operating mode control	MD2 to MD0	61, 58, 57	63, 60, 59	Input	Mode pins: These pins set the operating mode. The relation between the settings of pins MD2 to MD0 and the operating mode is shown below. These pins should not be changed while the H8S/2318 Series is operating.

- H8S/2318 F-ZTAT,
  H8S/2315 F-ZTAT versions

FWE	MD2	MD1	MD0	Operating Mode
0	0	0	0	—
			1	—
		1	0	—
			1	—
	1	0	0	Mode 4
			1	Mode 5
		1	0	Mode 6
			1	Mode 7
1	0	0	0	—
			1	—
		1	0	Mode 10
			1	Mode 11
	1	0	0	—
			1	—
		1	0	Mode 14
			1	Mode 15

Type	Symbol	Pin No. TFP-100B	Pin No. FP-100A	I/O	Name and Function
Operating mode control	MD2 to MD0	61, 58, 57	63, 60, 59	Input	• Mask ROM and ROMless versions, and H8S/2319 F-ZTAT version

MD2	MD1	MD0	Operating Mode
0	0	0	—
		1	—
	1	0	—
		1	—
1	0	0	Mode 4
		1	Mode 5
	1	0	Mode 6*
		1	Mode 7*

Note: * Not used on ROMless version.

Type	Symbol	Pin No. TFP-100B	Pin No. FP-100A	I/O	Name and Function
System control	$\overline{\text{RES}}$	62	64	Input	Reset input: When this pin is driven low, the chip is reset.
	$\overline{\text{STBY}}$	64	66	Input	Standby: When this pin is driven low, a transition is made to hardware standby mode.
	$\overline{\text{BREQ}}$	76	78	Input	Bus request: Used by an external bus master to issue a bus request to the H8S/2318 Series.
	$\overline{\text{BREQO}}$	74	76	Output	Bus request output: External bus request signal used when an internal bus master accesses external space in the external-bus-released state.
	$\overline{\text{BACK}}$	75	77	Output	Bus request acknowledge: Indicates that the bus has been released to an external bus master.
	FWE*[1]	60	62	Input	Flash write enable: Enables or disables writing to flash memory.
	EMLE*[2]	60	62	Input	Emulator enable: For connection to ground (0 V).

Type	Symbol	Pin No. TFP-100B	Pin No. FP-100A	I/O	Name and Function
Interrupts	NMI	63	65	Input	Nonmaskable interrupt: Requests a nonmaskable interrupt. When this pin is not used, it should be fixed high.
	$\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$	94, 93, 13, 12, 73 to 76	96, 95, 15, 14, 75 to 78	Input	Interrupt request 7 to 0: These pins request a maskable interrupt.
Address bus	A23 to A0	2, 1, 100, 99, 53 to 50, 48 to 41, 39 to 32	4 to 1, 55 to 52, 50 to 43, 41 to 34	Output	Address bus: These pins output an address.
Data bus	D15 to D0	30 to 19, 17 to 14	32 to 21, 19 to 16	I/O	Data bus: These pins constitute a bidirectional data bus.
Bus control	$\overline{\text{CS7}}$ to $\overline{\text{CS0}}$	94 to 97 75, 76	96 to 99 77, 78	Output	Chip select: Signals for selecting areas 7 to 0.
	$\overline{\text{AS}}$	70	72	Output	Address strobe: When this pin is low, it indicates that address output on the address bus is enabled.
	$\overline{\text{RD}}$	71	73	Output	Read: When this pin is low, it indicates that the external address space can be read.
	$\overline{\text{HWR}}$	72	74	Output	High write: A strobe signal that writes to external space and indicates that the upper half (D15 to D8) of the data bus is enabled.
	$\overline{\text{LWR}}$	73	75	Output	Low write: A strobe signal that writes to external space and indicates that the lower half (D7 to D0) of the data bus is enabled.
	$\overline{\text{WAIT}}$	74	76	Input	Wait: Requests insertion of a wait state in the bus cycle when accessing external 3-state address space.

Type	Symbol	Pin No. TFP-100B	Pin No. FP-100A	I/O	Name and Function
16-bit timer-pulse unit (TPU)	TCLKD to TCLKA	6, 4, 2, 1	8, 6, 4, 3	Input	Clock input D to A: These pins input an external clock.
	TIOCA0, TIOCB0, TIOCC0, TIOCD0	99, 100, 1, 2	1 to 4	I/O	Input capture/ output compare match A0 to D0: The TGR0A to TGR0D input capture input or output compare output, or PWM output pins.
	TIOCA1, TIOCB1	3, 4	5, 6	I/O	Input capture/ output compare match A1 and B1: The TGR1A and TGR1B input capture input or output compare output, or PWM output pins.
	TIOCA2, TIOCB2	5, 6	7, 8	I/O	Input capture/ output compare match A2 and B2: The TGR2A and TGR2B input capture input or output compare output, or PWM output pins.
	TIOCA3, TIOCB3, TIOCC3, TIOCD3	54 to 56, 59	56 to 58, 61	I/O	Input capture/ output compare match A3 to D3: The TGR3A to TGR3D input capture input or output compare output, or PWM output pins.
	TIOCA4, TIOCB4	89, 90	91, 92	I/O	Input capture/ output compare match A4 and B4: The TGR4A and TGR4B input capture input or output compare output, or PWM output pins.
	TIOCA5, TIOCB5	91, 92	93, 94	I/O	Input capture/ output compare match A5 and B5: The TGR5A and TGR5B input capture input or output compare output, or PWM output pins.
8-bit timer	TMO0, TMO1	91, 92	93, 94	Output	Compare match output: The compare match output pins.
	TMCI0, TMCI1	59, 90	61, 92	Input	Counter external clock input: Input pins for the external clock input to the counter.
	TMRI0, TMRI1	56, 89	58, 91	Input	Counter external reset input: The counter reset input pins.
Watchdog timer (WDT)	$\overline{\text{WDTOVF}}$*3	60	62	Output	Watchdog timer overflows: The counter overflows signal output pin in watchdog timer mode.

Type	Symbol	Pin No. TFP-100B	Pin No. FP-100A	I/O	Name and Function
Serial communication interface (SCI) Smart Card interface	TxD1, TxD0	9, 8	11, 10	Output	Transmit data (channel 0, 1): Data output pins.
	RxD1, RxD0	11, 10	13, 12	Input	Receive data (channel 0, 1): Data input pins.
	SCK1 SCK0	13, 12	15, 14	I/O	Serial clock (channel 0, 1): Clock I/O pins.
A/D converter	AN7 to AN0	86 to 79	88 to 81	Input	Analog 7 to 0: Analog input pins.
	$\overline{\text{ADTRG}}$	93	95	Input	A/D conversion external trigger input: Pin for input of an external trigger to start A/D conversion.
D/A converter	DA1, DA0	86, 85	88, 87	Output	Analog output: D/A converter analog output pins.
A/D converter and D/A converters	AV_{CC}	77	79	Input	This is the power supply pin for the A/D converter and D/A converter. When the A/D converter and D/A converter are not used, this pin should be connected to the system power supply (V_{CC}).
	AV_{SS}	87	89	Input	This is the ground pin for the A/D converter and D/A converter. This pin should be connected to the system power supply (0 V).
	V_{ref}	78	80	Input	This is the reference voltage input pin for the A/D converter and D/A converter. When the A/D converter and D/A converter are not used, this pin should be connected to the system power supply (V_{CC}).
I/O ports	P17 to P10	6 to 1, 100, 99	8 to 1	I/O	Port 1: An 8-bit I/O port. Input or output can be designated for each bit by means of the port 1 data direction register (P1DDR).
	P27 to P20	92 to 89, 59, 56 to 54	94 to 91, 61, 58 to 56	I/O	Port 2: An 8-bit I/O port. Input or output can be designated for each bit by means of the port 2 data direction register (P2DDR).

Type	Symbol	Pin No. TFP-100B	Pin No. FP-100A	I/O	Name and Function
I/O ports	P35 to P30	13 to 8	15 to 10	I/O	Port 3: A 6-bit I/O port. Input or output can be designated for each bit by means of the port 3 data direction register (P3DDR).
	P47 to P40	86 to 79	88 to 81	Input	Port 4: An 8-bit input port.
	PA3 to PA0	53 to 50	55 to 52	I/O	Port A*[4]: A 4-bit I/O port. Input or output can be designated for each bit by means of the port A data direction register (PADDR).
	PB7 to PB0	48 to 41	50 to 43	I/O	Port B*[4]: An 8-bit I/O port. Input or output can be designated for each bit by means of the port B data direction register (PBDDR).
	PC7 to PC0	39 to 32	41 to 34	I/O	Port C*[4]: An 8-bit I/O port. Input or output can be designated for each bit by means of the port C data direction register (PCDDR).
	PD7 to PD0	30 to 23	32 to 25	I/O	Port D*[4]: An 8-bit I/O port. Input or output can be designated for each bit by means of the port D data direction register (PDDDR).
	PE7 to PE0	22 to 19, 17 to 14	24 to 21, 19 to 16	I/O	Port E: An 8-bit I/O port. Input or output can be designated for each bit by means of the port E data direction register (PEDDR).
	PF7 to PF0	69 to 76	71 to 78	I/O	Port F: An 8-bit I/O port. Input or output can be designated for each bit by means of the port F data direction register (PFDDR).
	PG4 to PG0	97 to 93	99 to 95	I/O	Port G: A 5-bit I/O port. Input or output can be designated for each bit by means of the port G data direction register (PGDDR).

Notes: 1. Applies to the H8S/2318 F-ZTAT and H8S/2315 F-ZTAT versions only.
2. Applies to the H8S/2319 F-ZTAT version only.
3. Applies to mask ROM and ROMless versions only.
4. Cannot be used as an I/O port on the ROMless versions.

1.6 Product Lineup

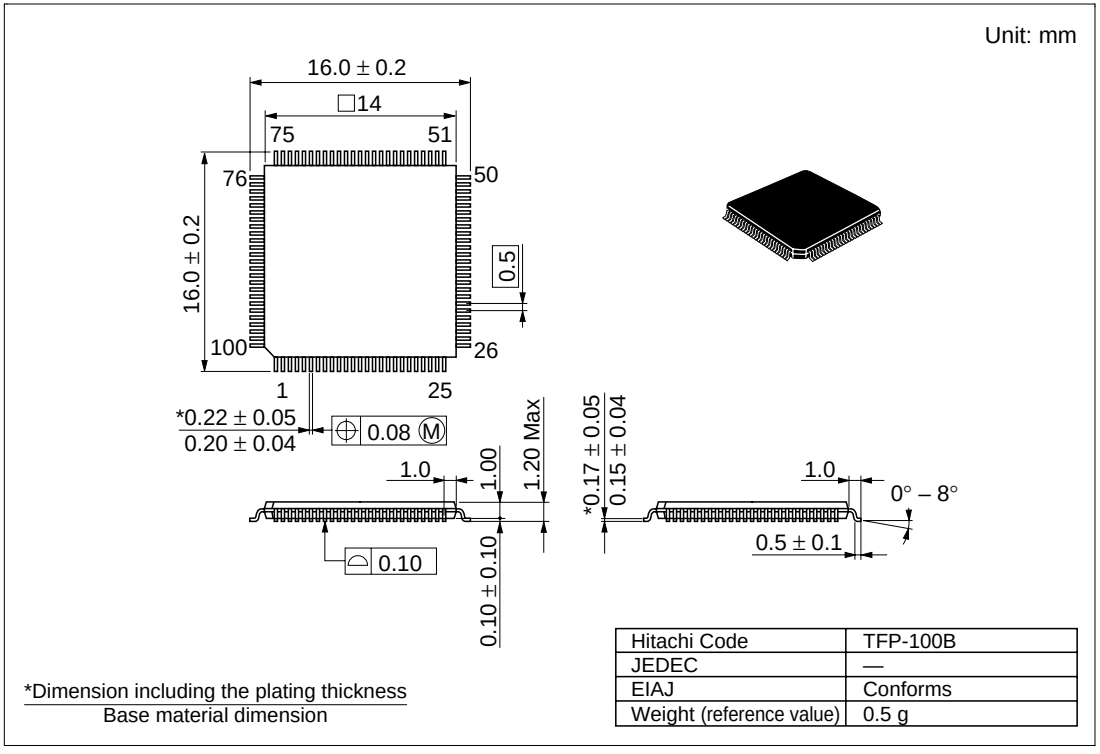
Table 1.4 H8S/2319, H8S/2318 Series Product Lineup

Product Type		Model	Marking	Package (Hitachi Package Code)
H8S/2319*[1]	F-ZTAT version	HD64F2319	HD64F2319VTE	100-pin TQFP (TFP-100B)
			HD64F2319VF	100-pin QFP (FP-100A)
H8S/2318	Mask ROM version	HD6432318*[2]	HD6432318TE	100-pin TQFP (TFP-100B)
			HD6432318F	100-pin QFP (FP-100A)
	F-ZTAT version	HD64F2318	HD64F2318VTE	100-pin TQFP (TFP-100B)
			HD64F2318VF	100-pin QFP (FP-100A)
H8S/2317	Mask ROM version	HD6432317*[2]	HD6432317TE	100-pin TQFP (TFP-100B)
			HD6432317F	100-pin QFP (FP-100A)
H8S/2316*[1]	Mask ROM version	HD6432316	HD6432316TE	100-pin TQFP (TFP-100B)
			HD6432316F	100-pin QFP (FP-100A)
H8S/2315*[1]	F-ZTAT version	HD64F2315	HD64F2315VTE	100-pin TQFP (TFP-100B)
			HD64F2315VF	100-pin QFP (FP-100A)
H8S/2313*[1]	Mask ROM version	HD6432313	HD6432313TE	100-pin TQFP (TFP-100B)
			HD6432313F	100-pin QFP (FP-100A)
H8S/2312	ROMless version	HD6412312	HD6412312VTE	100-pin TQFP (TFP-100B)
			HD6412312VF	100-pin QFP (FP-100A)
H8S/2311	Mask ROM version	HD6432311	HD6432311TE	100-pin TQFP (TFP-100B)
			HD6432311F	100-pin QFP (FP-100A)
H8S/2310	ROMless version	HD6412310	HD6412310VTE	100-pin TQFP (TFP-100B)
			HD6412310VF	100-pin QFP (FP-100A)

Notes: 1. Under development

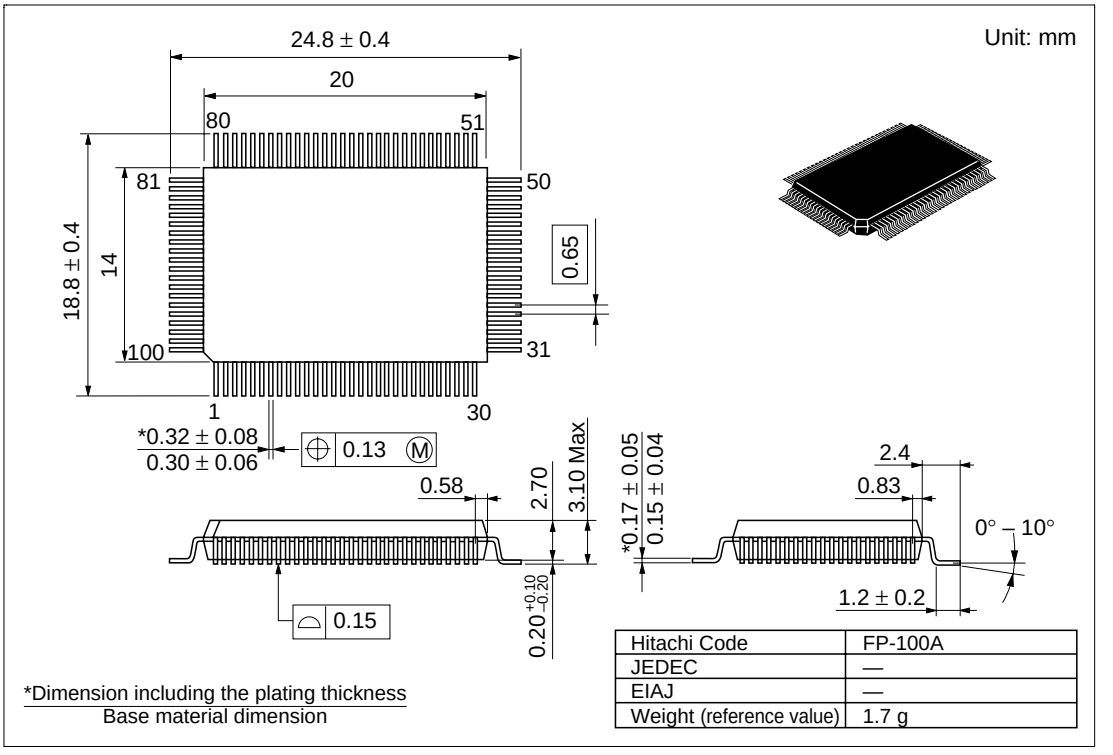
2. The HD6432318 and HD6432317 include products for V_{CC} = 2.4 V to 3.6 V (low-voltage operation) as well as for V_{CC} = 2.7 V to 3.6 V and V_{CC} = 3.0 V to 3.6 V.
   For details, see section 7, Electrical Characteristics.

1.7 Package Dimensions



Hitachi Code	TFP-100B
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.5 g

Figure 1.4 TFP-100B Package Dimensions



Hitachi Code	FP-100A
JEDEC	—
EIAJ	—
Weight (reference value)	1.7 g

Figure 1.5 FP-100A Package Dimensions

Section 2 MCU Operating Modes

2.1 Overview

2.1.1 Operating Mode Selection (H8S/2318 F-ZTAT and H8S/2315 F-ZTAT Versions)

The H8S/2318 Series has eight operating modes (modes 4 to 7, 10, 11, 14 and 15). These modes are determined by the mode pin (MD2 to MD0) and flash write enable pin (FWE) settings. The CPU operating mode and initial bus width can be selected as shown in table 2.1.

Table 2.1 lists the MCU operating modes.

Table 2.1 MCU Operating Mode Selection (H8S/2318 F-ZTAT and H8S/2315 F-ZTAT Versions)

MCU Operating Mode	FWE	MD2	MD1	MD0	CPU Operating Mode	Description	On-Chip ROM	External Data Bus	
								Initial Value	Max. Value
0	0	0	0	0	—	—	—	—	—
1				1					
2			1	0					
3				1					
4		1	0	0	Advanced	Expanded mode with on-chip ROM disabled	Disabled	16 bits	16 bits
5				1				8 bits	16 bits
6			1	0		Expanded mode with on-chip ROM enabled	Enabled	8 bits	16 bits
7				1		Single-chip mode		—	—
8	1	0	0	0	—	—	—	—	—
9				1					
10			1	0	Advanced	Boot mode	Enabled	8 bits	16 bits
11				1				—	—
12		1	0	0	—	—	—	—	—
13				1					
14			1	0	Advanced	User program mode	Enabled	8 bits	16 bits
15				1				—	—

The CPU's architecture allows for 4 Gbytes of address space, but the H8S/2318 Series actually accesses a maximum of 16 Mbytes.

Modes 4 to 6 are externally expanded modes that allow access to external memory and peripheral devices.

The external expansion modes allow switching between 8-bit and 16-bit bus modes. After program execution starts, an 8-bit or 16-bit address space can be set for each area, depending on the bus controller setting. If 16-bit access is selected for any one area, 16-bit bus mode is set; if 8-bit access is selected for all areas, 8-bit bus mode is set. Note that the functions of each pin depend on the operating mode.

Modes 10, 11, 14, and 15 are boot modes and user program modes in which the flash memory can be programmed and erased. For details, see section 17, ROM, in the Hardware Manual

The H8S/2318 Series can only be used in modes 4 to 7, 10, 11, 14, and 15. This means that the flash write enable pin and mode pins must be set to select one of these modes.

Do not change the inputs at the mode pins during operation.

2.1.2 Operating Mode Selection (Mask ROM, ROMless, and H8S/2319 F-ZTAT Versions)

The H8S/2319 and H8S/2318 Series have four operating modes (modes 4 to 7). The operating mode is determined by the mode pins (MD2 to MD0). The CPU operating mode, enabling or disabling of on-chip ROM, and the initial bus width setting can be selected as shown in table 2.2.

Table 2.2 lists the MCU operating modes.

Table 2.2 MCU Operating Mode Selection (Mask ROM, ROMless, and H8S/2319 F-ZTAT Versions)

MCU Operating Mode	MD2	MD1	MD0	CPU Operating Mode	Description	On-Chip ROM	External Data Bus Initial Value	External Data Bus Max. Value
0	0	0	0	—	—	—	—	—
1			1					
2		1	0					
3			1					
4*	1	0	0	Advanced	Expanded mode with on-chip ROM disabled	Disabled	16 bits	16 bits
5*			1				8 bits	16 bits
6		1	0		Expanded mode with on-chip ROM enabled	Enabled	8 bits	16 bits
7			1		Single-chip mode		—	—

Note: * Only modes 4 and 5 are provided in the ROMless version.

The CPU's architecture allows for 4 Gbytes of address space, but the H8S/2319 and H8S/2318 Series actually access a maximum of 16 Mbytes.

Modes 4 to 6 are externally expanded modes that allow access to external memory and peripheral devices.

The external expansion modes allow switching between 8-bit and 16-bit bus modes. After program execution starts, an 8-bit or 16-bit address space can be set for each area, depending on the bus controller setting. If 16-bit access is selected for any one area, 16-bit bus mode is set; if 8-bit access is selected for all areas, 8-bit bus mode is set. Note that the functions of each pin depend on the operating mode.

The H8S/2319 and H8S/2318 Series can only be used in modes 4 to 7. This means that the mode pins must be set to select one of these modes. However, note that only mode 4 or 5 can be set for the ROMless version.

Do not change the inputs at the mode pins during operation.

2.1.3 Register Configuration

The H8S/2319 and H8S/2318 Series have a mode control register (MDCR) that indicates the inputs at the mode pins (MD2 to MD0), and a system control register (SYSCR) and system control register 2 (SYSCR2)*[2] that control the operation of the chip. Table 2.3 summarizes these registers.

Table 2.3 Registers

Name	Abbreviation	R/W	Initial Value	Address*[1]
Mode control register	MDCR	R	Undefined	H'FF3B
System control register	SYSCR	R/W	H'01	H'FF39
System control register 2*[2]	SYSCR2	R/W	H'00	H'FF42

Notes: 1. Lower 16 bits of the address.
2. The SYSCR2 register can only be used in the F-ZTAT version. In the mask ROM and ROMless versions this register will return an undefined value if read, and cannot be modified.

2.2 Register Descriptions

2.2.1 Mode Control Register (MDCR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	—	MDS2	MDS1	MDS0
Initial value	:	1	0	0	0	0	—*	—*	—*
R/W	:	—	—	—	—	—	R	R	R

Note: * Determined by pins MD2 to MD0.

MDCR is an 8-bit read-only register that indicates the current operating mode of the H8S/2318 Series chip.

Bit 7—Reserved: This bit is always read as 1, and cannot be modified.

Bits 6 to 3—Reserved: These bits are always read as 0, and cannot be modified.

Bits 2 to 0—Mode Select 2 to 0 (MDS2 to MDS0): These bits indicate the input levels at pins MD2 to MD0 (the current operating mode). Bits MDS2 to MDS0 correspond to pins MD2 to MD0. MDS2 to MDS0 are read-only bits, and cannot be written to. The mode pin (MD2 to MD0) input levels are latched into these bits when MDCR is read. These latches are canceled by a reset.

2.2.2 System Control Register (SYSCR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	INTM1	INTM0	NMIEG	LWROD	—	RAME
Initial value	:	0	0	0	0	0	0	0	1
R/W	:	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7—Reserved: Only 0 should be written to this bit.

Bit 6—Reserved: This bit is always read as 0, and cannot be modified.

Bits 5 and 4—Interrupt Control Mode 1 and 0 (INTM1, INTM0): These bits select the control mode of the interrupt controller. For details of the interrupt control modes, see section 3.4.1, Interrupt Control Modes and Interrupt Operation, in the Hardware Manual.

Bit 5 INTM1	Bit 4 INTM0	Interrupt Control Mode	Description	
0	0	0	Control of interrupts by I bit	(Initial value)
	1	—	Setting prohibited	
1	0	2	Control of interrupts by I2 to I0 bits and IPR	
	1	—	Setting prohibited	

Bit 3—NMI Edge Select (NMIEG): Selects the valid edge of the NMI interrupt input.

Bit 3 NMIEG	Description	
0	An interrupt is requested at the falling edge of NMI input	(Initial value)
1	An interrupt is requested at the rising edge of NMI input	

Bit 2—LWR Output Disable (LWROD): Enables or disables $\overline{\text{LWR}}$ output.

Bit 2 LWROD	Description	
0	PF3 is designated as $\overline{\text{LWR}}$ output pin	(Initial value)
1	PF3 is designated as I/O port, and does not function as $\overline{\text{LWR}}$ output pin	

Bit 1—Reserved: Only 0 should be written to this bit.

Bit 0—RAM Enable (RAME): Enables or disables the on-chip RAM. The RAME bit is initialized when the reset state is released. It is not initialized in software standby mode.

Bit 0 RAME	Description	
0	On-chip RAM is disabled	
1	On-chip RAM is enabled	(Initial value)

2.2.3 System Control Register 2 (SYSCR2) (F-ZTAT Version Only)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	FLSHE	—	—	—
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	—	—	—	—	R/W	—	—	—

SYSCR2 is an 8-bit readable/writable register that performs on-chip flash memory control.

SYSCR2 is initialized to H'00 by a reset, and in hardware standby mode.

Bits 7 to 4—Reserved: These bits are always read as 0, and cannot be modified.

Bit 3—Flash Memory Control Register Enable (FLSHE): Controls CPU access to the flash memory control registers (FLMCR1, FLMCR2, EBR1, and EBR2). For details, see section 17, ROM, in the Hardware Manual.

Bit 3 FLSHE	Description
0	Flash control registers are not selected for addresses H'FFFFC8 to H'FFFFCB (Initial value)
1	Flash control registers are selected for addresses H'FFFFC8 to H'FFFFCB

Bits 2 to 0—Reserved: These bits are always read as 0, and cannot be modified.

2.3 Operating Mode Descriptions

2.3.1 Modes 1 to 3

Modes 1 to 3 are not supported in the H8S/2319 and H8S/2318 Series, and must not be set.

2.3.2 Mode 4 (Expanded Mode with On-Chip ROM Disabled)

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is disabled.

Pins P13 to P10, ports A, B, and C function as an address bus, ports D and E functions as a data bus, and part of port F carries bus control signals.

Pins P13 to P10 function as input ports immediately after a reset. These pins can be set to output addresse by setting the corresponding data direction register (DDR) bits and A23E to A20E in PFCR1 to 1.

The initial bus mode after a reset is 16 bits, with 16-bit access to all areas. However, note that if 8-bit access is designated by the bus controller for all areas, the bus mode switches to 8 bits.

2.3.3 Mode 5 (Expanded Mode with On-Chip ROM Disabled)

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is disabled.

Pins P13 to P10, ports A, B and C function as an address bus, port D functions as a data bus, and part of port F carries bus control signals.

Pins P13 to P10 function as input ports immediately after a reset. These pins can be set to output addresses by setting the corresponding data direction register (DDR) bits and A23E to A20E in PFCR1 to 1.

The initial bus mode after a reset is 8 bits, with 8-bit access to all areas. However, note that if at least one area is designated for 16-bit access by the bus controller, the bus mode switches to 16 bits and port E becomes a data bus.

2.3.4 Mode 6 (Expanded Mode with On-Chip ROM Enabled)

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is enabled.

Pins P13 to P10, ports A, B, and C function as input ports immediately after a reset. These pins can be set to output addresses by setting the corresponding data direction register (DDR) bits and A23E to A20E in PFCR1 to 1. Port D functions as a data bus, and part of port F carries bus control signals.

The initial bus mode after a reset is 8 bits, with 8-bit access to all areas. However, note that if at least one area is designated for 16-bit access by the bus controller, the bus mode switches to 16 bits and port E becomes a data bus.

2.3.5 Mode 7 (Single-Chip Mode)

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is enabled, but external addresses cannot be accessed.

All I/O ports are available for use as input/output ports.

2.3.6 Modes 8 and 9 (H8S/2318 F-ZTAT and H8S/2315 F-ZTAT Versions Only)

Modes 8 and 9 are not supported in the H8S/2319 and H8S/2318 Series, and must not be set.

2.3.7 Mode 10 (H8S/2318 F-ZTAT and H8S/2315 F-ZTAT Versions Only)

This is a flash memory boot mode. For details, see section 17, ROM, in the Hardware Manual.

Except for the fact that flash memory programming and erasing can be performed, operation in this mode is the same as in advanced expanded mode with on-chip ROM enabled.

2.3.8 Mode 11 (H8S/2318 F-ZTAT and H8S/2315 F-ZTAT Versions Only)

This is a flash memory boot mode. For details, see section 17, ROM, in the Hardware Manual.

Except for the fact that flash memory programming and erasing can be performed, operation in this mode is the same as in advanced single-chip mode.

2.3.9 Modes 12 and 13 (H8S/2318 F-ZTAT and H8S/2315 F-ZTAT Versions Only)

Modes 12 and 13 are not supported in the H8S/2319 and H8S/2318 Series, and must not be set.

2.3.10 Mode 14 (H8S/2318 F-ZTAT and H8S/2315 F-ZTAT Versions Only)

This is a flash memory user program mode. For details, see section 17, ROM, in the Hardware Manual.

Except for the fact that flash memory programming and erasing can be performed, operation in this mode is the same as in advanced expanded mode with on-chip ROM enabled.

2.3.11 Mode 15 (H8S/2318 F-ZTAT and H8S/2315 F-ZTAT Versions Only)

This is a flash memory user program mode. For details, see section 17, ROM, in the Hardware Manual.

Except for the fact that flash memory programming and erasing can be performed, operation in this mode is the same as in advanced single-chip mode.

2.4 Pin Functions in Each Operating Mode

The pin functions of ports 1 and A to F vary depending on the operating mode. Table 2.4 shows their functions in each operating mode.

Table 2.4 Pin Functions in Each Mode

Port		Mode 4	Mode 5	Mode 6*2 Mode 10*3 Mode 14*3	Mode 7*2 Mode 11*3 Mode 15*3
Port 1	P13 to P10	P*1/T/A	P*1/T/A	P*1/T/A	P*1/T
Port A	PA3 to PA0	A	A	P*1/A	P
Port B		A	A	P*1/A	P
Port C		A	A	P*1/A	P
Port D		D	D	D	P
Port E		P/D*1	P*1/D	P*1/D	P
Port F	PF7	P/C*1	P/C*1	P/C*1	P*1/C
	PF6, PF3	P/C*1	P/C*1	P/C*1	P
	PF5, PF4	C	C	C	
	PF2 to PF0	P*1/C	P*1/C	P*1/C	

Legend

P: I/O port
T: Timer I/O
A: Address bus output
D: Data bus I/O
C: Control signals, clock I/O

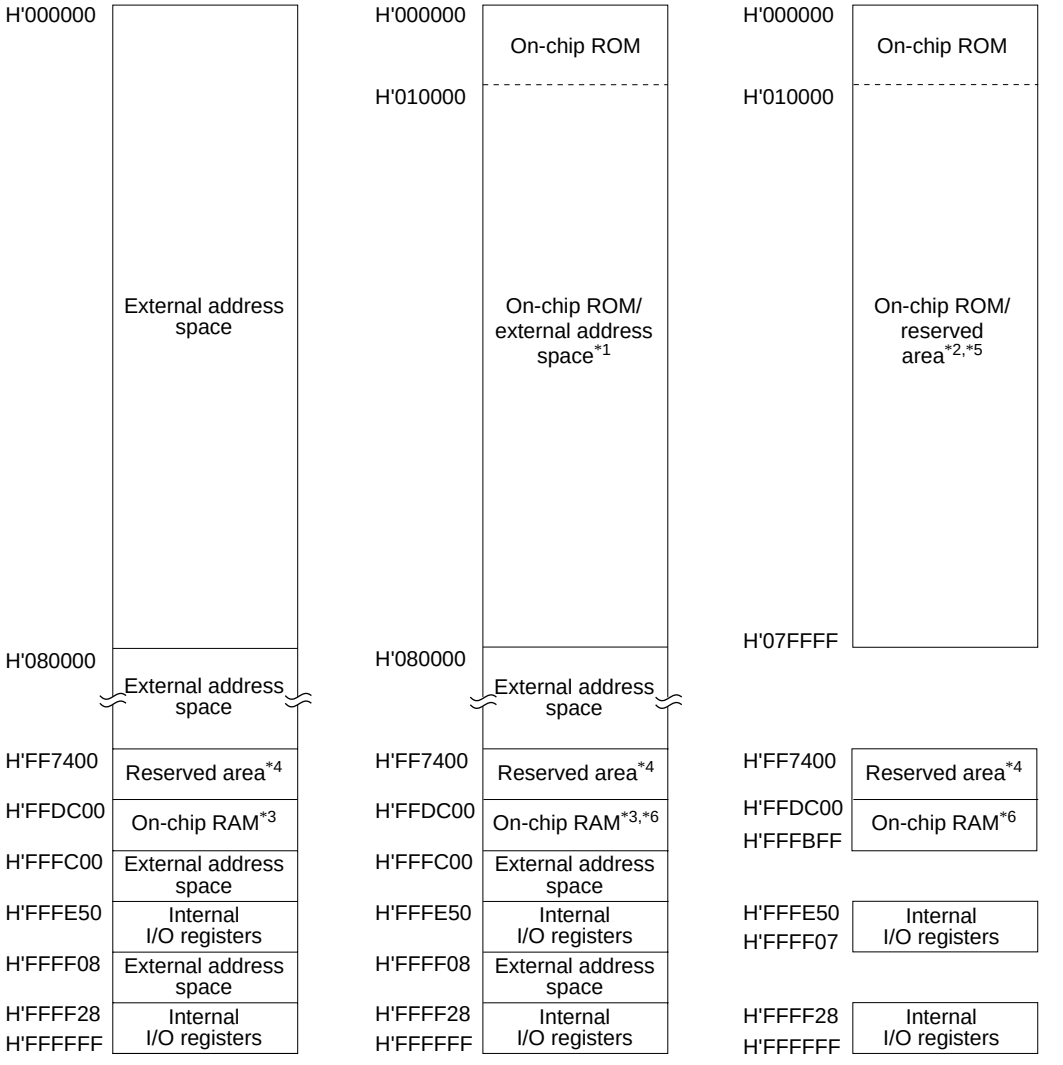
Notes: 1. After reset
2. Not used on ROMless version.
3. Applies to H8S/2318 F-ZTAT and H8S/2315 F-ZTAT versions only.

2.5 Memory Map in Each Operating Mode

Figures 2.1 to 2.7 show memory maps for each of the operating modes.

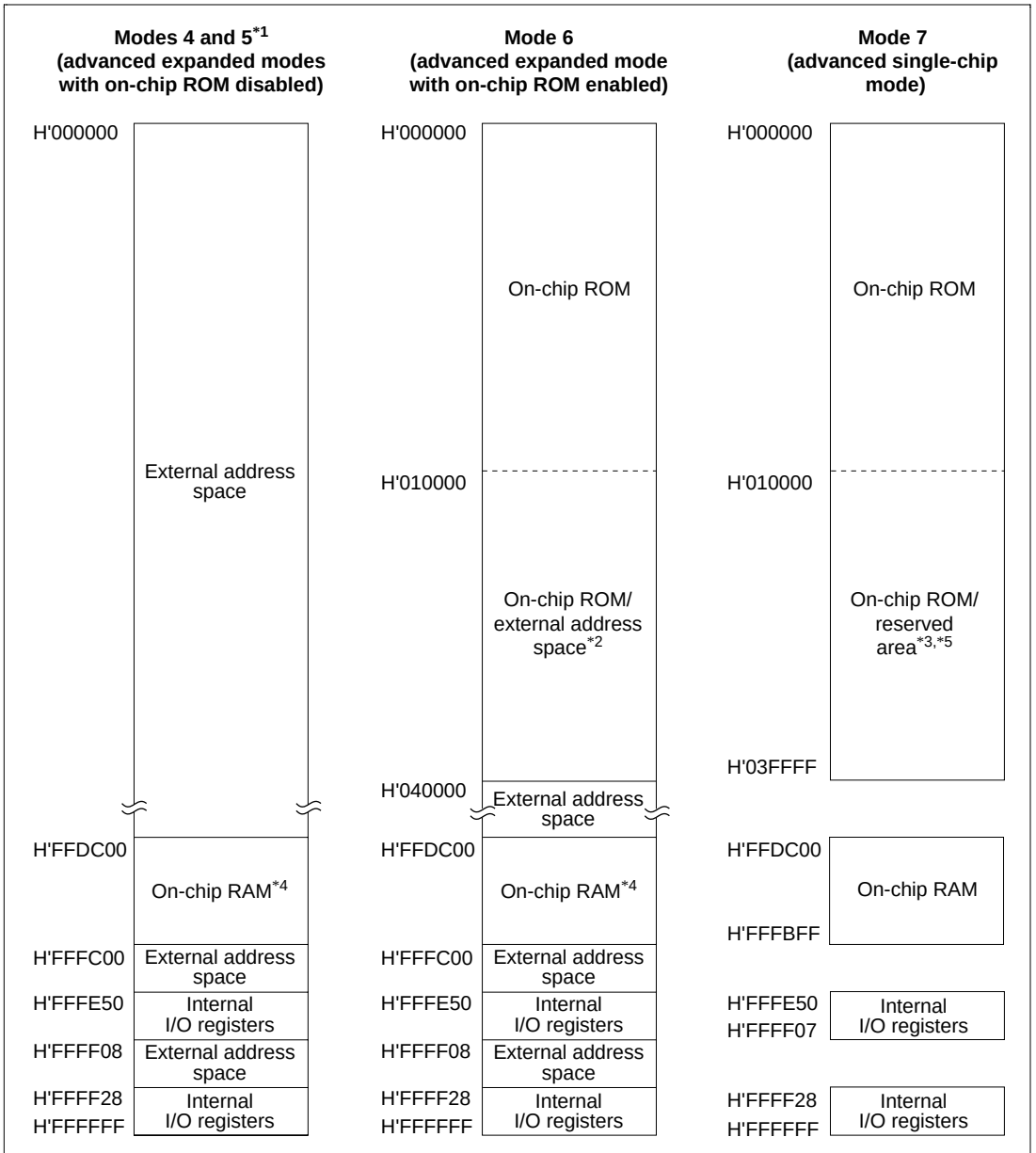
The address space is 16 Mbytes.

The address space is divided into eight areas.



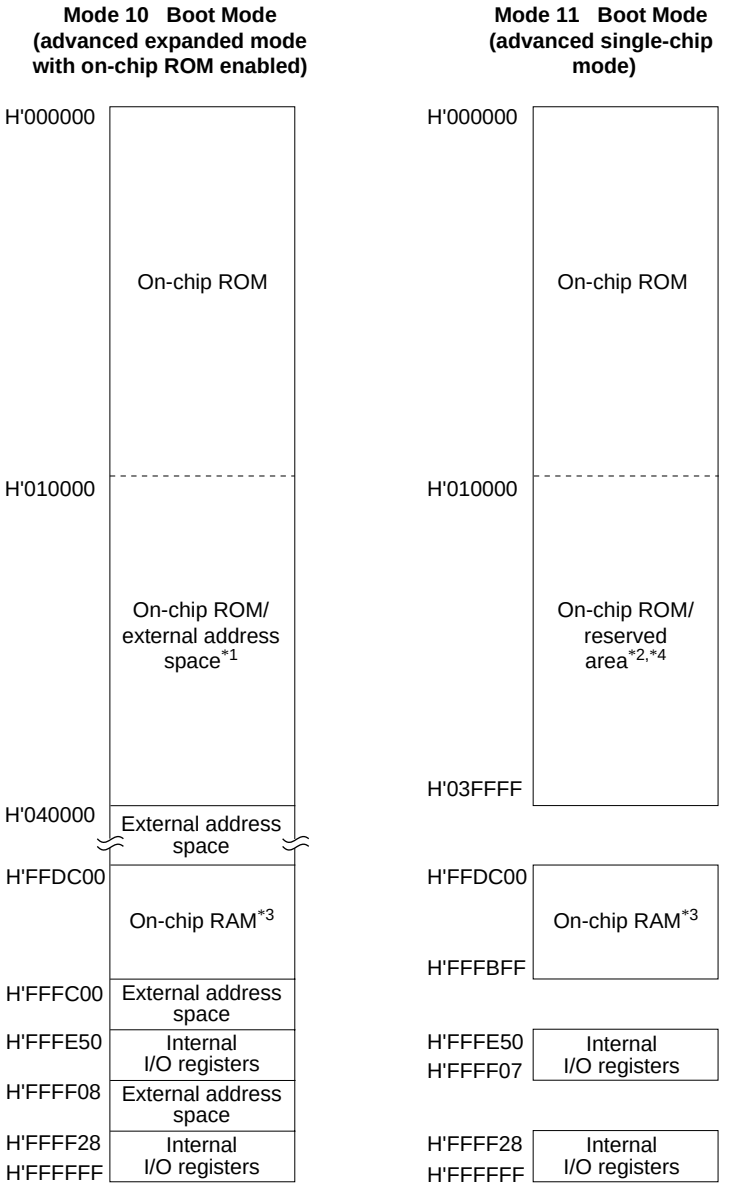
Notes: 1. External addresses when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
2. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
3. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
4. Do not access the reserved area in addresses H'FF7400 to H'FFDBFF.
5. Do not access the reserved areas.
6. When writing to the flash memory, do not clear the RAME bit in SYSCR to 0 because the on-chip RAM is used in the writing procedure.

Figure 2.1 H8S/2319 F-ZTAT Memory Map in Each Operating Mode



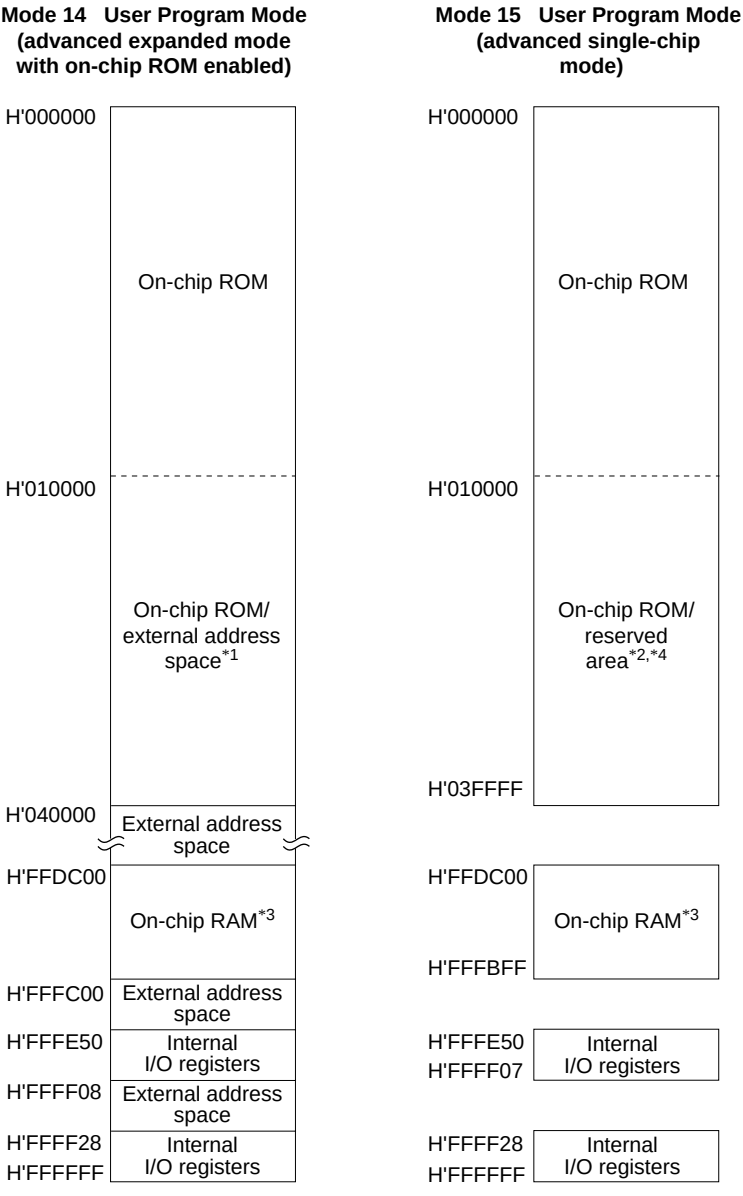
Notes: 1. Only modes 4 and 5 are provided in the ROMless version (H8S/2312).
2. External addresses when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
3. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
4. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
5. Do not access the reserved areas.

Figure 2.2 (a) H8S/2318 and H8S/2312 Memory Map in Each Operating Mode



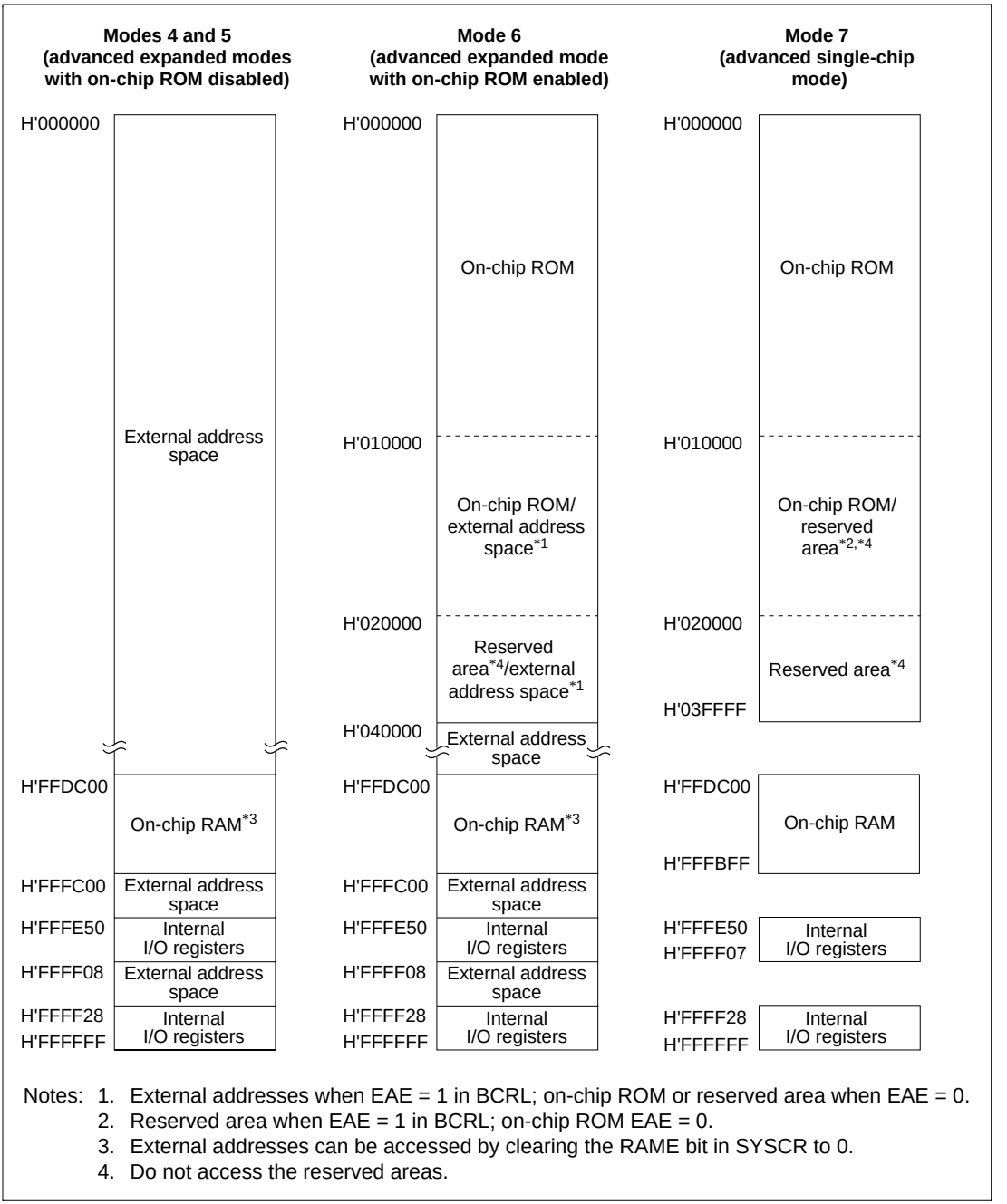
Notes: 1. External addresses when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
2. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
3. On-chip RAM is used for flash memory programming. Do not clear the RAME bit in SYSCR to 0.
4. Do not access the reserved areas.

Figure 2.2 (b) H8S/2318 Memory Map in Each Operating Mode (F-ZTAT Version Only)



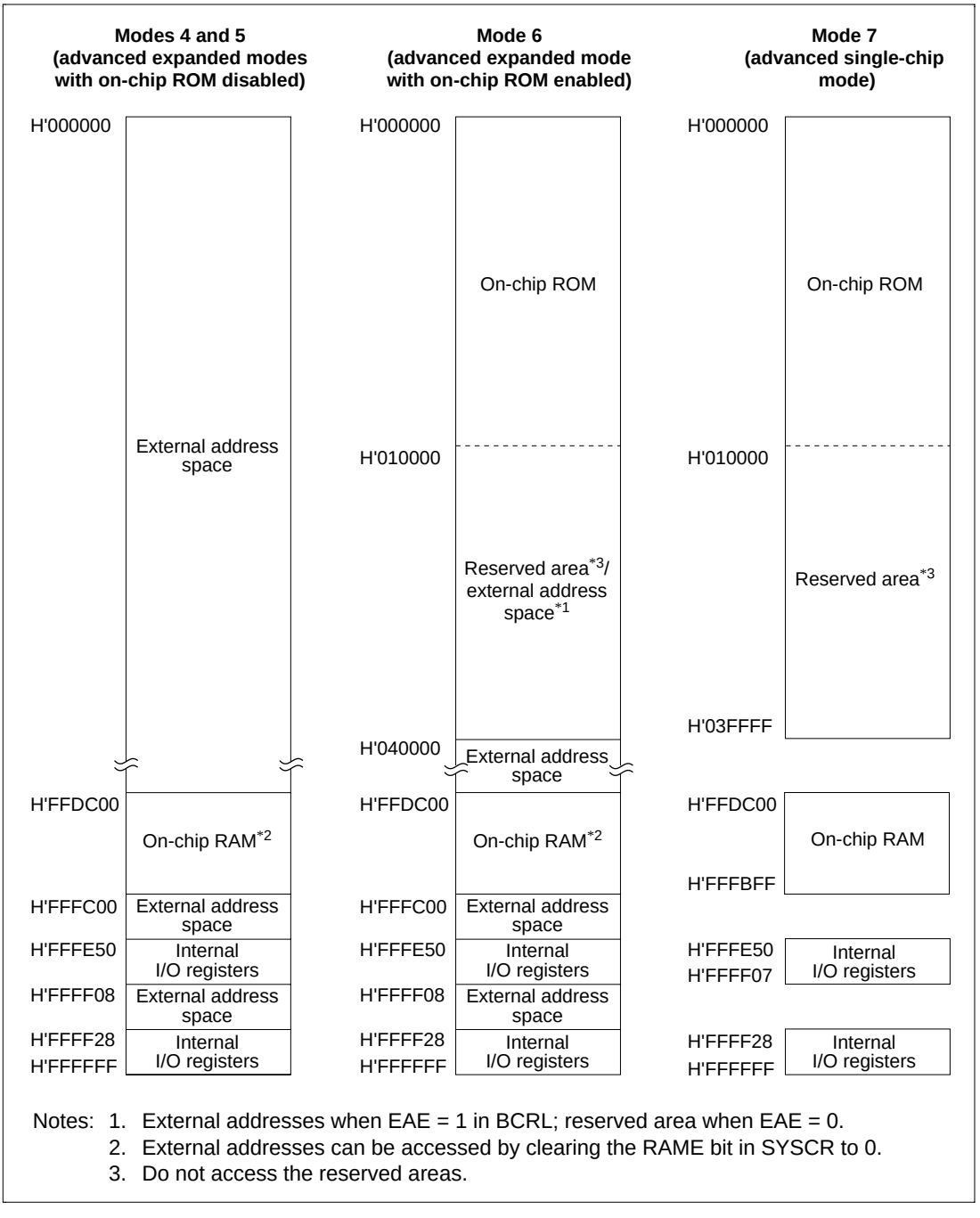
Notes: 1. External addresses when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
2. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
3. On-chip RAM is used for flash memory programming. Do not clear the RAME bit in SYSCR to 0.
4. Do not access the reserved areas.

Figure 2.2 (c) H8S/2318 Memory Map in Each Operating Mode (F-ZTAT Version Only)



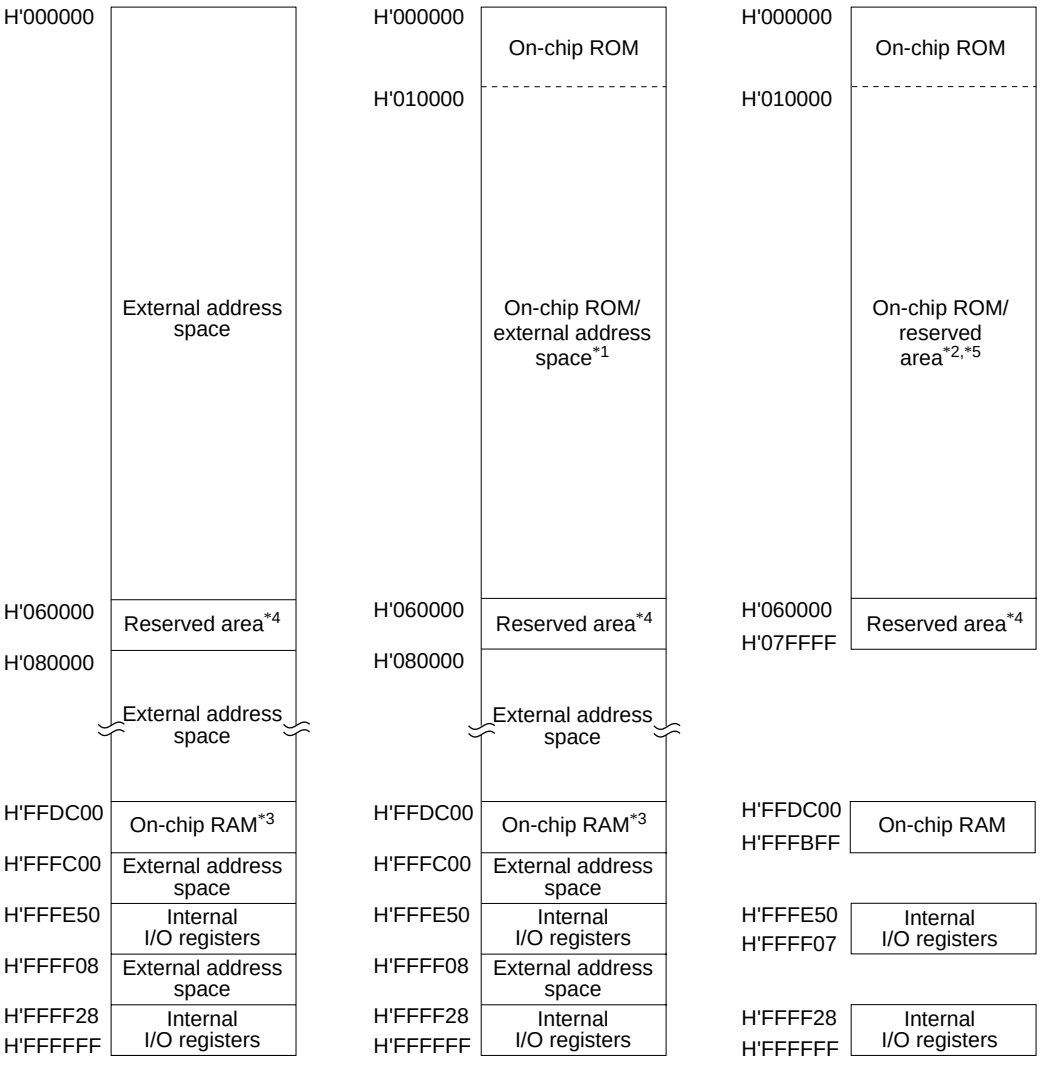
Notes: 1. External addresses when EAE = 1 in BCRL; on-chip ROM or reserved area when EAE = 0.
2. Reserved area when EAE = 1 in BCRL; on-chip ROM EAE = 0.
3. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
4. Do not access the reserved areas.

Figure 2.3 H8S/2317 Memory Map in Each Operating Mode



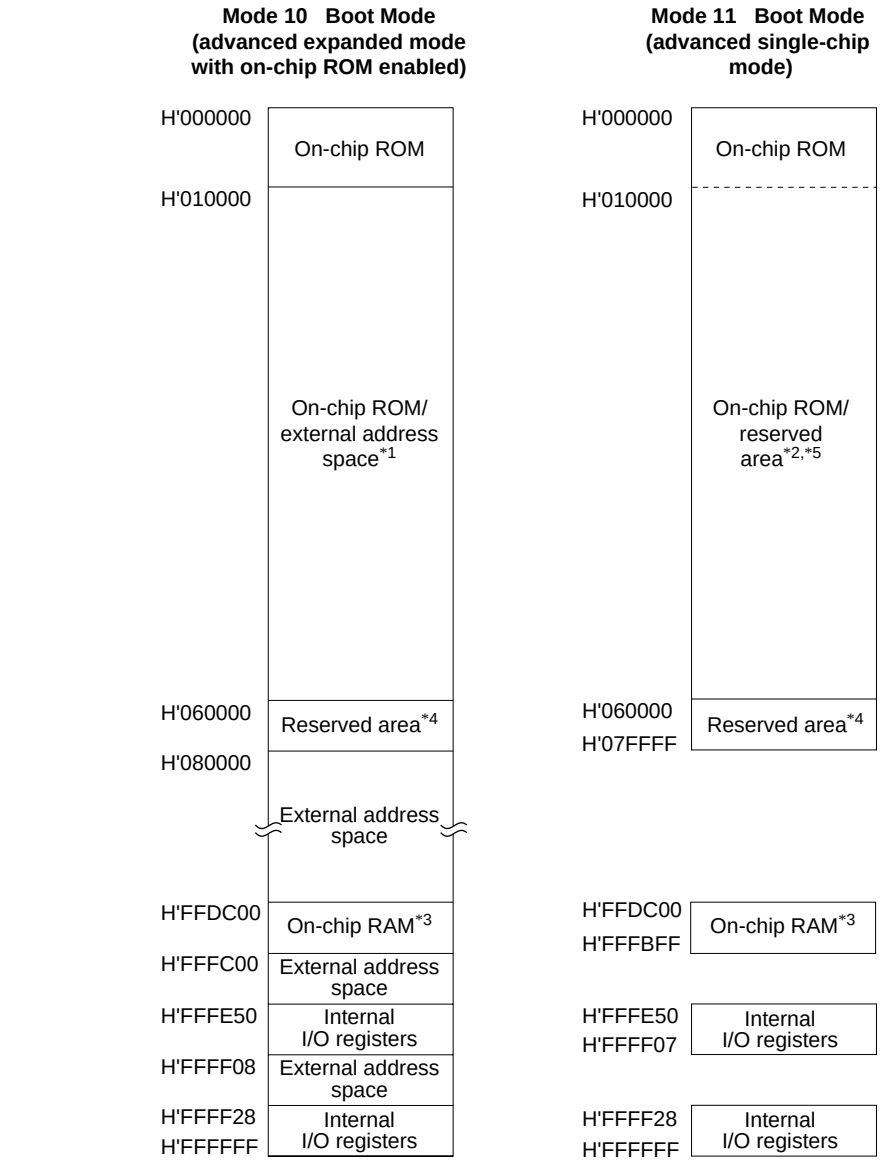
Notes: 1. External addresses when EAE = 1 in BCRL; reserved area when EAE = 0.
2. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
3. Do not access the reserved areas.

Figure 2.4 H8S/2316 Memory Map in Each Operating Mode



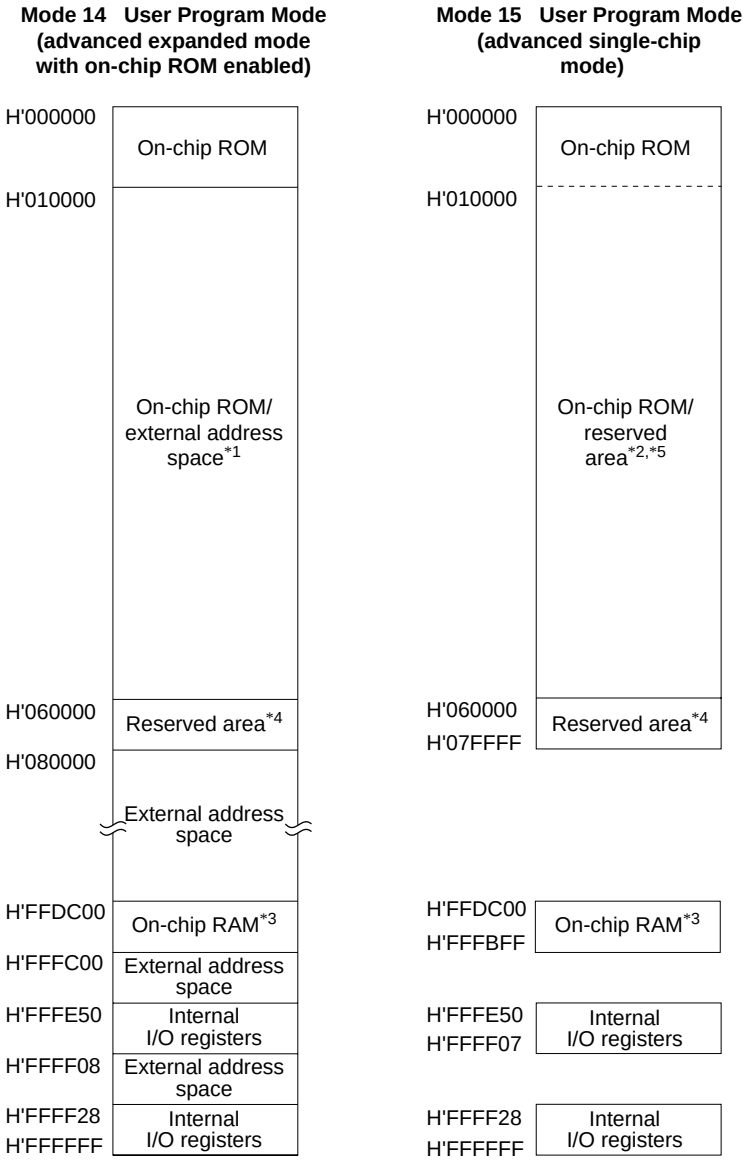
Notes: 1. External addresses when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
2. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
3. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
4. Do not access the reserved area in addresses H'060000 to H'07FFFF.
5. Do not access the reserved areas.

Figure 2.5 (a) H8S/2315 F-ZTAT Memory Map in Each Operating Mode



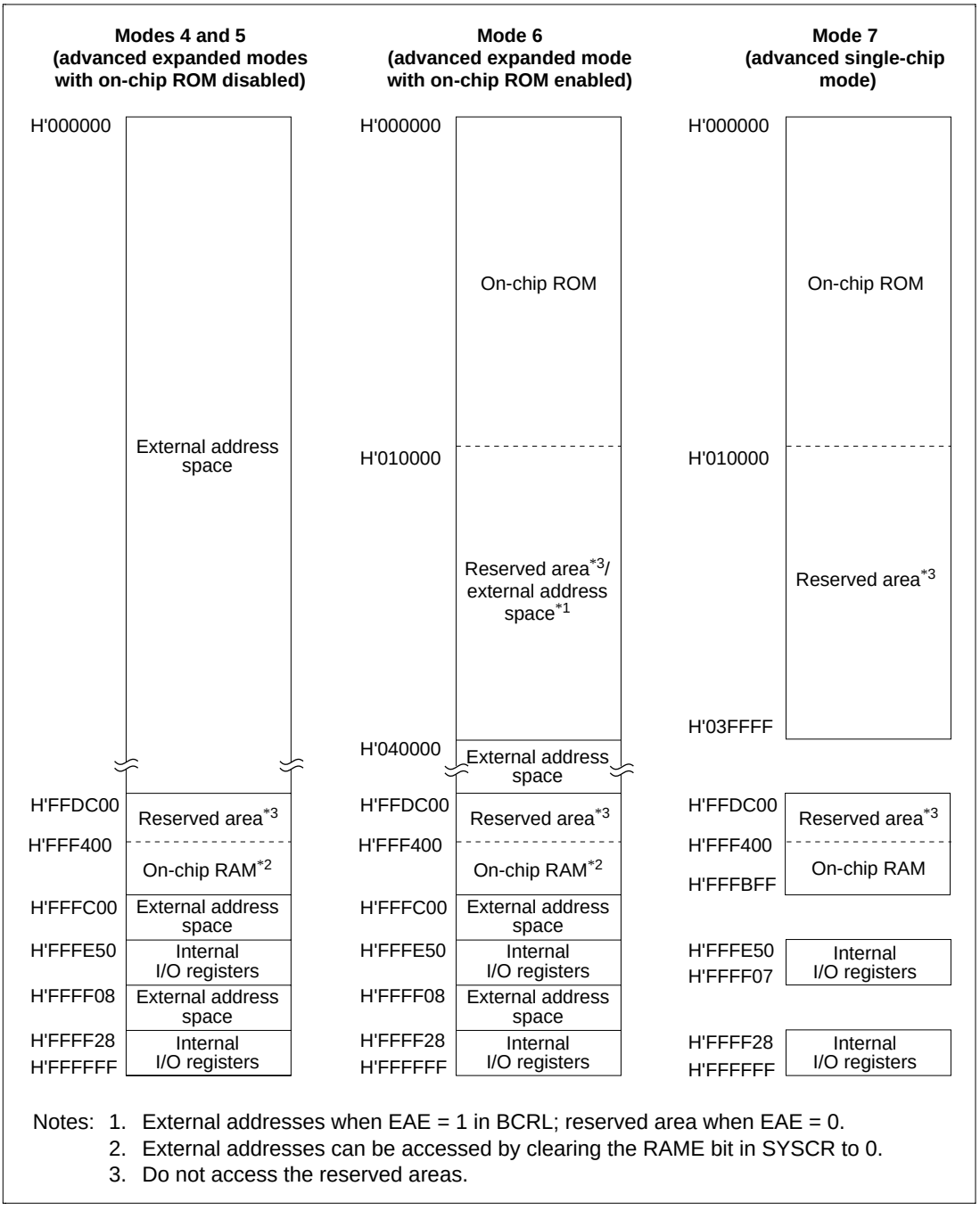
Notes: 1. External addresses when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
2. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
3. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
4. Do not access the reserved area in addresses H'060000 to H'07FFFF.
5. Do not access the reserved areas.

Figure 2.5 (b) H8S/2315 F-ZTAT Memory Map in Each Operating Mode



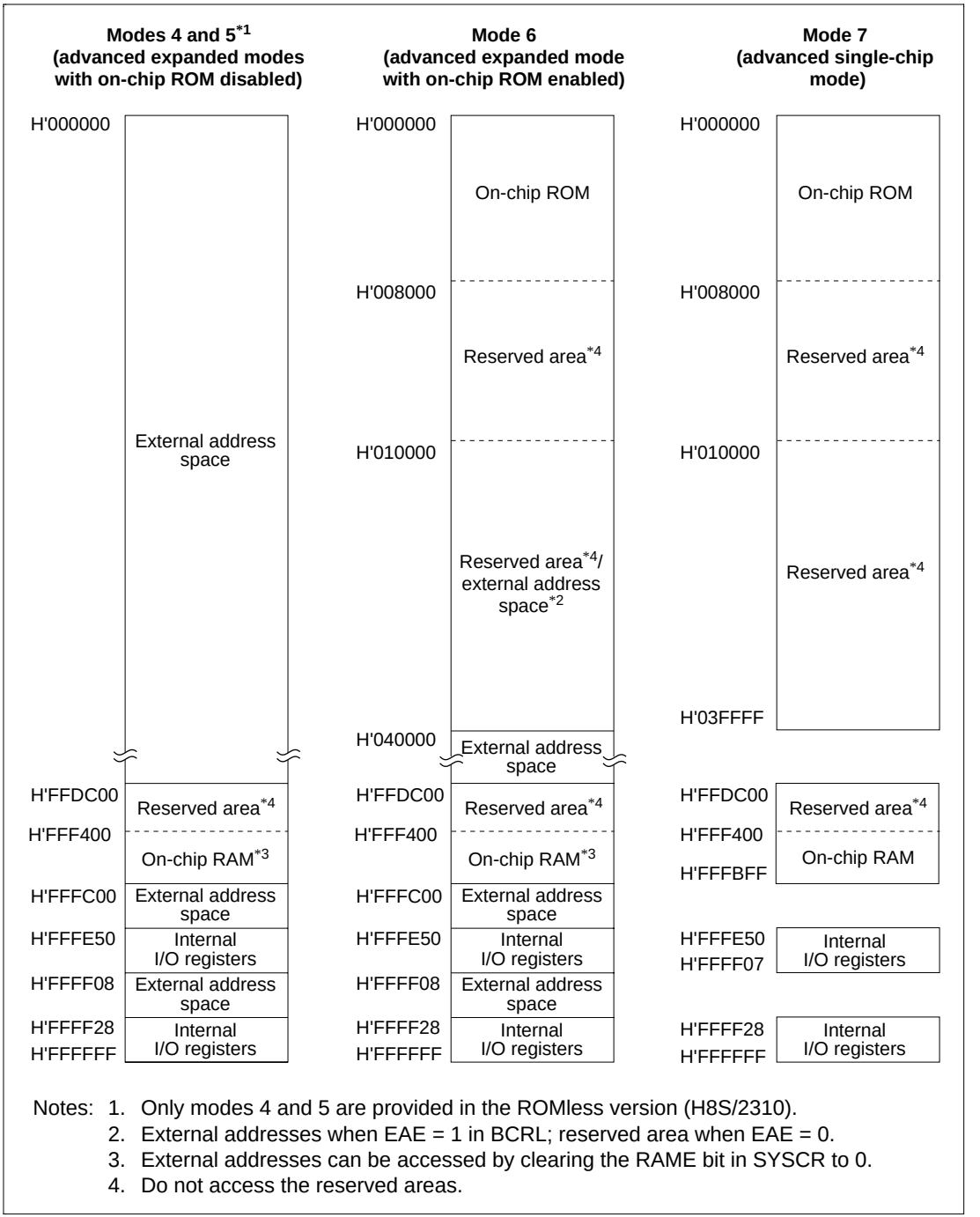
Notes: 1. External addresses when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
2. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
3. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
4. Do not access the reserved area in addresses H'060000 to H'07FFFF.
5. Do not access the reserved areas.

Figure 2.5 (c) H8S/2315 F-ZTAT Memory Map in Each Operating Mode



Notes: 1. External addresses when EAE = 1 in BCRL; reserved area when EAE = 0.
2. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
3. Do not access the reserved areas.

Figure 2.6 H8S/2313 Memory Map in Each Operating Mode



Notes: 1. Only modes 4 and 5 are provided in the ROMless version (H8S/2310).
2. External addresses when EAE = 1 in BCRL; reserved area when EAE = 0.
3. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
4. Do not access the reserved areas.

Figure 2.7 H8S/2311 and H8S/2310 Memory Map in Each Operating Mode

Section 3 Exception Handling and Interrupt Controller

3.1 Overview

3.1.1 Exception Handling Types and Priority

As table 3.1 indicates, exception handling may be caused by a reset, trap instruction, or interrupt. Exception handling is prioritized as shown in table 3.1. If two or more exceptions occur simultaneously, they are accepted and processed in order of priority. Trap instruction exceptions are accepted at all times in the program execution state.

Exception handling sources, the stack structure, and the operation of the CPU vary depending on the interrupt control mode set by the INTM0 and INTM1 bits in SYSCR.

For details of exception handling and the interrupt controller, see section 2, Exception Handling, and section 3, Interrupt Controller, in the Hardware Manual.

Table 3.1 Exception Types and Priority

Priority	Exception Type	Start of Exception Handling
High	Reset	Starts after a low-to-high transition at the $\overline{\text{RES}}$ pin, or when the watchdog timer overflows
	Trace*[1]	Starts when execution of the current instruction or exception handling ends, if the trace (T) bit is set to 1
	Interrupt	Starts when execution of the current instruction or exception handling ends, if an interrupt request has been issued*[2]
Low	Trap instruction*[3] (TRAPA)	Started by execution of a trap instruction (TRAPA)

Notes: 1. Traces are enabled only in interrupt control mode 2. Trace exception handling is not executed after execution of an RTE instruction.
2. Interrupt detection is not performed on completion of ANDC, ORC, XORC, or LDC instruction execution, or on completion of reset exception handling.
3. Trap instruction exception handling requests are accepted at all times in the program execution state.

3.2 Interrupt Controller

3.2.1 Interrupt Controller Features

- Two interrupt control modes
  - — Either of two interrupt control modes can be set by means of the INTM1 and INTM0 bits in the system control register (SYSCR).
- Priorities settable with IPRs
  - — Interrupt priority registers (IPRs) are provided for setting interrupt priorities. Eight priority levels can be set for each module for all interrupts except NMI.
  - — NMI is assigned the highest priority level of 8, and can be accepted at all times.
- Independent vector addresses
  - — All interrupt sources are assigned independent vector addresses, making it unnecessary for the source to be identified in the interrupt handling routine.
- Nine external interrupt pins
  - — NMI is the highest-priority interrupt, and is accepted at all times. Rising edge or falling edge can be selected for NMI.
  - — Falling edge, rising edge, or both edge detection, or level sensing, can be selected independently for IRQ7 to IRQ0.
- DTC control
  - — DTC activation is controlled by means of interrupts.

3.2.2 Pin Configuration

Table 3.2 Interrupt Controller Pins

Name	Symbol	I/O	Function
Nonmaskable interrupt	NMI	Input	Nonmaskable external interrupt; rising or falling edge can be selected
External interrupt requests 7 to 0	$\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$	Input	Maskable external interrupts; rising, falling, or both edges, or level sensing, can be selected

3.3 Interrupt Sources

Interrupt sources comprise external interrupts (NMI and IRQ7 to IRQ0) and internal interrupts (43 sources).

3.3.1 External Interrupts

There are nine external interrupts: NMI and IRQ7 to IRQ0. NMI and IRQ7 to IRQ0 can be used to restore the chip from software standby mode. (IRQ7 to IRQ3 can be used as software standby mode clearing sources by setting the IRQ37S bit in SBYCR to 1.)

NMI Interrupt: NMI is the highest-priority interrupt, and is always accepted by the CPU regardless of the status of the CPU interrupt mask bits. The NMIEG bit in SYSCR can be used to select whether an interrupt is requested at a rising edge or a falling edge on the NMI pin.

The vector number for NMI interrupt exception handling is 7.

Interrupts IRQ7 to IRQ0: Interrupts IRQ7 to IRQ0 are requested by an input signal at pins $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$. Interrupts IRQ7 to IRQ0 have the following features:

- Using ISCR, it is possible to select whether an interrupt is generated by a low level, falling edge, rising edge, or both edges, at pins $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$.
- Enabling or disabling of interrupt requests IRQ7 to IRQ0 can be selected with IER.
- The interrupt priority level can be set with the IPR registers.
- The status of interrupt requests IRQ7 to IRQ0 is indicated in ISR. ISR flags can be cleared to 0 by software.

A block diagram of interrupts IRQ7 to IRQ0 is shown in figure 3.1.

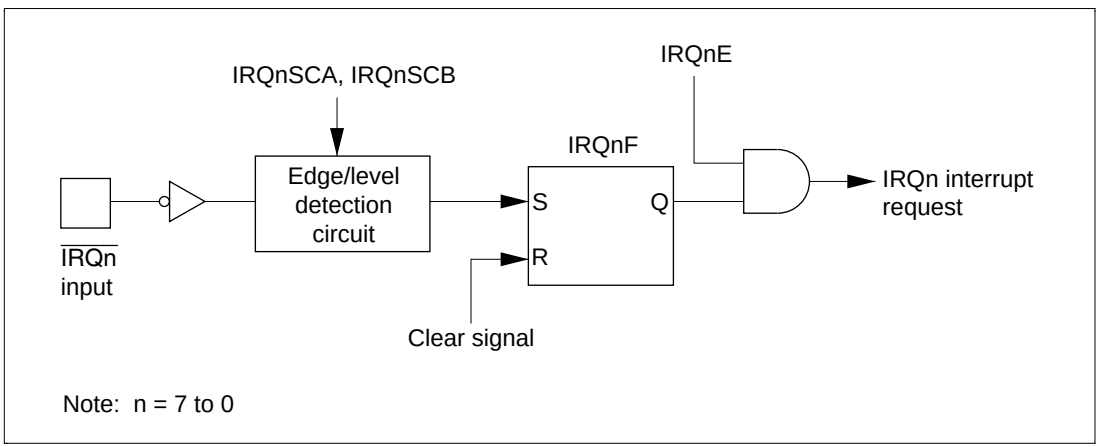


Figure 3.1 Block Diagram of Interrupts IRQ7 to IRQ0

Figure 3.2 shows the timing of IRQnF setting.

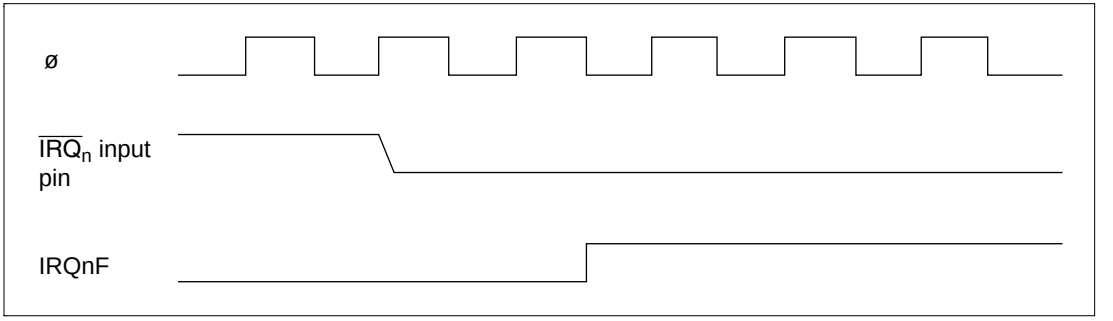


Figure 3.2 Timing of IRQnF Setting

The vector numbers for IRQ7 to IRQ0 interrupt exception handling are 23 to 16.

Detection of IRQ7 to IRQ0 interrupts does not depend on whether the relevant pin has been set for input or output. When a pin is used as an external interrupt input pin, clear the corresponding DDR bit to 0 and do not use the pin as an I/O pin for another function.

3.3.2 Internal Interrupts

There are 43 sources for internal interrupts from on-chip supporting modules.

1. For each on-chip supporting module there are flags that indicate the interrupt request status, and enable bits that select enabling or disabling of these interrupts. If any one of these is set to 1, an interrupt request is issued to the interrupt controller.
2. The interrupt priority level can be set by means of the IPR registers.
3. The DTC can be activated by a TPU, SCI, or other interrupt request. When the DTC is activated by an interrupt, the interrupt control mode and interrupt mask bits have no effect.

3.3.3 Interrupt Exception Vector Table

Table 3.3 shows interrupt sources, vector addresses, and interrupt priorities. For default priorities, the lower the vector number, the higher the priority. The DTC can be activated by an interrupt request.

Priorities among modules can be set by means of the IPR registers. The situation when two or more modules are set to the same priority, and priorities within a module, are fixed as shown in table 3.3.

Table 3.3 Interrupt Sources, Vector Addresses, and Interrupt Priorities

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*	IPR	Priority	DTC Activation
Power-on reset		0	H'0000	—	High	—
Reserved		1	H'0004			
Reserved for system use		2	H'0008			
		3	H'000C			
		4	H'0010			
Trace		5	H'0014			
Reserved for system use		6	H'0018			
NMI	External pin	7	H'001C			
Trap instruction (4 sources)		8	H'0020			
		9	H'0024			
		10	H'0028			
		11	H'002C			
Reserved for system use		12	H'0030			
		13	H'0034			
		14	H'0038			
		15	H'003C			
IRQ0	External pin	16	H'0040	IPRA6 to IPRA4		○
IRQ1		17	H'0044	IPRA2 to IPRA0		○
IRQ2		18	H'0048	IPRB6 to IPRB4		○
IRQ3		19	H'004C			○
IRQ4		20	H'0050	IPRB2 to IPRB0		○
IRQ5		21	H'0054			○
IRQ6		22	H'0058	IPRC6 to IPRC4		○
IRQ7		23	H'005C		Low	○

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*	IPR	Priority	DTC Activation
SWDTEND (software-activated data transfer end)	DTC	24	H'0060	IPRC2 to IPRC0	High	○
WOVI (interval timer)	Watchdog timer	25	H'0064	IPRD6 to IPRD4		—
Reserved	—	26	H'0068	IPRD2 to IPRD0		—
Reserved	—	27	H'006C	IPRE6 to IPRE4		—
ADI (A/D conversion end)	A/D	28	H'0070	IPRE2 to IPRE0		○
Reserved	—	29	H'0074			—
		30	H'0078			
		31	H'007C			
TGI0A (TGR0A input capture/compare match)	TPU channel 0	32	H'0080	IPRF6 to IPRF4		○
TGI0B (TGR0B input capture/compare match)		33	H'0084			○
TGI0C (TGR0C input capture/compare match)		34	H'0088			○
TGI0D (TGR0D input capture/compare match)		35	H'008C			○
TCI0V (overflow 0)		36	H'0090			—
Reserved	—	37	H'0094			—
		38	H'0098			
		39	H'009C		Low	

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*	IPR	Priority	DTC Activation
TGI1A (TGR1A input capture/compare match)	TPU channel 1	40	H'00A0	IPRF2 to IPRF0	High	○
TGI1B (TGR1B input capture/compare match)		41	H'00A4			○
TCI1V (overflow 1)		42	H'00A8			—
TCI1U (underflow 1)		43	H'00AC			—
TGI2A (TGR2A input capture/compare match)	TPU channel 2	44	H'00B0	IPRG6 to IPRG4		○
TGI2B (TGR2B input capture/compare match)		45	H'00B4			○
TCI2V (overflow 2)		46	H'00B8			—
TCI2U (underflow 2)		47	H'00BC			—
TGI3A (TGR3A input capture/compare match)	TPU channel 3	48	H'00C0	IPRG2 to IPRG0		○
TGI3B (TGR3B input capture/compare match)		49	H'00C4			○
TGI3C (TGR3C input capture/compare match)		50	H'00C8			○
TGI3D (TGR3D input capture/compare match)		51	H'00CC			○
TCI3V (overflow 3)		52	H'00D0			—
Reserved	—	53	H'00D4			—
		54	H'00D8			
		55	H'00DC		Low	

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*	IPR	Priority	DTC Activation
TGI4A (TGR4A input capture/compare match)	TPU channel 4	56	H'00E0	IPRH6 to IPRH4	High	○
TGI4B (TGR4B input capture/compare match)		57	H'00E4			○
TCI4V (overflow 4)		58	H'00E8			—
TCI4U (underflow 4)		59	H'00EC			—
TGI5A (TGR5A input capture/compare match)	TPU channel 5	60	H'00F0	IPRH2 to IPRH0		○
TGI5B (TGR5B input capture/compare match)		61	H'00F4			○
TCI5V (overflow 5)		62	H'00F8			—
TCI5U (underflow 5)		63	H'00FC			—
CMIA0 (compare match A)	8-bit timer channel 0	64	H'0100	IPRI6 to IPRI4		○
CMIB0 (compare match B)		65	H'0104			○
OVI0 (overflow 0)		66	H'0108			—
Reserved	—	67	H'010C			—
CMIA1 (compare match A)	8-bit timer channel 1	68	H'0110	IPRI2 to IPRI0		○
CMIB1 (compare match B)		69	H'0114			○
OVI1 (overflow 1)		70	H'0118			—
Reserved	—	71	H'011C		Low	—

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*	IPR	Priority	DTC Activation
Reserved	—	72	H'0120	IPRJ6 to IPRJ4	High	—
		73	H'0124			
		74	H'0128			
		75	H'012C			
		76	H'0130			
		77	H'0134			
		78	H'0138			
		79	H'013C			
ERI0 (receive error 0)	SCI channel 0	80	H'0140	IPRJ2 to IPRJ0		—
RXI0 (receive-data-full 0)		81	H'0144			○
TXI0 (transmit-data-empty 0)		82	H'0148			○
TEI0 (transmit end 0)		83	H'014C			—
ERI1 (receive error 1)	SCI channel 1	84	H'0150	IPRK6 to IPRK4		—
RXI1 (receive-data-full 1)		85	H'0154			○
TXI1 (transmit-data-empty 1)		86	H'0158			○
TEI1 (transmit end 1)		87	H'015C			—
Reserved	—	88	H'0160	IPRK2 to IPRK0		—
		89	H'0164			
		90	H'0168			
		91	H'016C		Low	

Note: * Lower 16 bits of the start address.

3.4 Interrupt Control Modes and Interrupt Operation

Interrupt operations in the H8S/2319 and H8S/2318 Series differ depending on the interrupt control mode.

NMI interrupts are accepted at all times except in the reset state and the hardware standby state. In the case of IRQ interrupts and on-chip supporting module interrupts, an enable bit is provided for each interrupt. Clearing an enable bit to 0 disables the corresponding interrupt request. Interrupt sources for which the enable bit is set to 1 are controlled by the interrupt controller.

The interrupt control modes are shown in table 3.4, the interrupts selected in each interrupt control mode in tables 3.5 and 3.6, and operations and control signal functions in each interrupt control mode in table 3.7.

The interrupt controller performs interrupt control according to the interrupt control mode set by the INTM1 and INTM0 bits in SYSCR, the priorities set in the IPR registers, and the masking state indicated by the I bit in the CPU's CCR and bits I2 to I0 in EXR.

Table 3.4 Interrupt Control Modes

Interrupt Control Mode	INTM1	INTM0	Priority Setting Registers	Interrupt Mask Bits	Description
0	0	0	—	I	Interrupt mask control is performed by the I bit.
—		1	—	—	Setting prohibited
2	1	0	IPR	I2 to I0	8-level interrupt mask control is performed by bits I2 to I0. 8 priority levels can be set with IPR.
—		1	—	—	Setting prohibited

Table 3.5 Interrupts Selected in Each Interrupt Control Mode (1)

Interrupt Control Mode	Interrupt Mask Bits	
	I	Selected Interrupts
0	0	All interrupts
	1	NMI interrupts
2	*	All interrupts

*: Don't care

Table 3.6 Interrupts Selected in Each Interrupt Control Mode (2)

Interrupt Control Mode	Selected Interrupts
0	All interrupts
2	Highest-priority-level (IPR) interrupt with priority level greater than the mask level (IPR > I2 to I0)

Table 3.7 Operations and Control Signal Functions in Each Interrupt Control Mode

Interrupt Control Mode	Settings		Interrupt Acceptance Control		8-Level Control			Default Priority Determination	T (Trace)
	INTM1	INTM0		I		I2 to I0	IPR		
0	0	0	○	IM	x	—	—*2	○	—
2	1	0	x	—*1	○	IM	PR	○	T

Legend

○: Interrupt operation control performed

x: No operation (all interrupts enabled)

IM: Used as interrupt mask bit

PR: Sets priority

—: Not used

Notes: 1. Set to 1 when interrupt is accepted.

2. Keep the initial setting.

3.5 Interrupt Response Times

The H8S/2319 and H8S/2318 Series are capable of fast word access to on-chip memory, and the program area is provided in on-chip ROM and the stack area in on-chip RAM, enabling high-speed processing.

Table 3.8 shows interrupt response times—the interval between generation of an interrupt request and execution of the first instruction in the interrupt handling routine. The execution phase symbols used in table 3.8 are explained in table 3.9.

Table 3.8 Interrupt Response Times

		Advanced Mode	
No.	**Execution Phase**	**INTM1 = 0**	**INTM1 = 1**
1	Interrupt priority determination*[1]	3	3
2	Number of wait states until executing instruction ends*[2]	1 to (19 + 2 · S_I)	1 to (19 + 2 · S_I)
3	PC, CCR, and EXR stacking	2 · S_K	3 · S_K
4	Vector fetch	2 · S_I	2 · S_I
5	Instruction fetch*[3]	2 · S_I	2 · S_I
6	Internal processing*[4]	2	2
Total (when using on-chip memory)		12 to 32	13 to 33

Notes: 1. Two states in case of internal interrupt.
2. Refers to MULXS and DIVXS instructions.
3. Prefetch after interrupt acceptance and interrupt handling routine prefetch.
4. Internal processing after interrupt acceptance and internal processing after vector fetch.

Table 3.9 Number of States in Interrupt Handling Routine Execution Phases

	Access To				
		External Device			
		8-Bit Bus		16-Bit Bus	
Symbol	**Internal Memory**	**2-State Access**	**3-State Access**	**2-State Access**	**3-State Access**
Instruction fetch S_I	1	4	6 + 2m	2	3 + m
Branch address read S_J					
Stack manipulation S_K					

Legend
m: Number of wait states in an external device access

3.6 DTC Activation by Interrupt

3.6.1 Overview

In the H8S/2319 and H8S/2318 Series, the DTC can be activated by an interrupt. In this case, the following options are available:

1. Interrupt request to CPU
2. Activation request to DTC
3. Selection of a number of the above

See table 3.3 for the interrupt requests that can be used to activate the DTC. For details, see section 6, Data Transfer Controller, in the Hardware Manual.

3.6.2 Block Diagram

Figure 3.3 shows a block diagram of the DTC and interrupt controller.

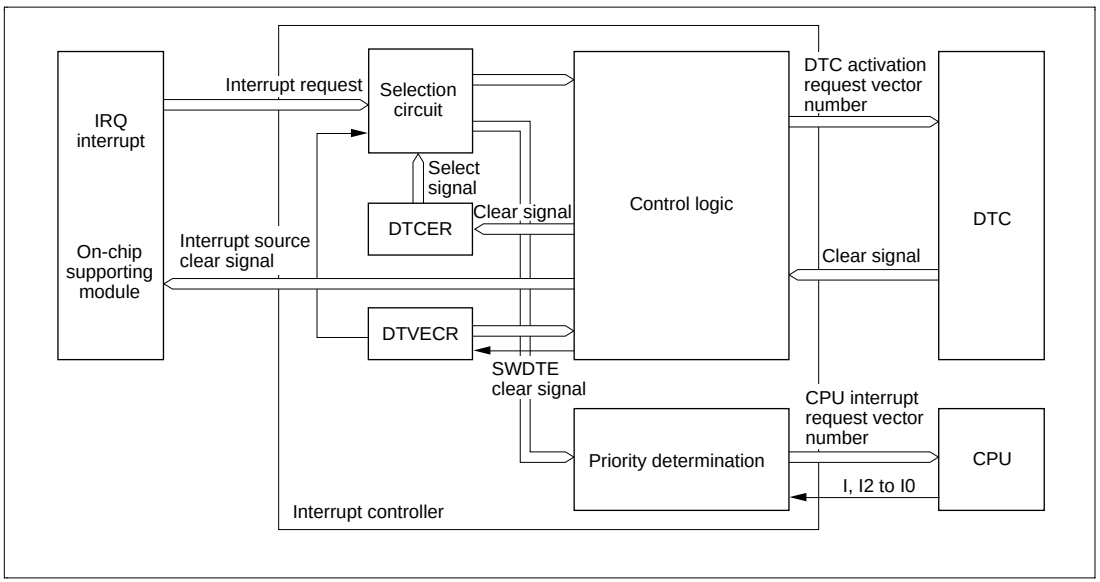


Figure 3.3 Interrupt Control for DTC

3.6.3 Operation

The interrupt controller has three main functions in DTC control, as described below.

Selection of Interrupt Source: For interrupt sources, it is possible to select DTC activation request or CPU interrupt request with the DTCE bit in DTC registers DTCERA to DTCERE.

After a DTC data transfer, the DTCE bit can be cleared to 0 and an interrupt request sent to the CPU in accordance with the specification of the DISEL bit in the DTC's MRB register.

When the DTC has performed the specified number of data transfers and the transfer counter value is 0, the DTCE bit is cleared to 0 after the DTC data transfer and an interrupt request is sent to the CPU.

Determination of Priority: The DTC activation source is selected in accordance with the default priority order, and is not affected by mask or priority levels. See table 3.10, Interrupt Sources, DTC Vector Addresses, and Corresponding DTCEs, for the respective priorities.

Table 3.10 Interrupt Sources, DTC Vector Addresses, and Corresponding DTCEs

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address	DTCE*	Priority
Write to DTVECR	Software	DTVECR	H'0400 + (DTVECR [6:0]<<1)	—	High
IRQ0	External pin	16	H'0420	DTCEA7	
IRQ1		17	H'0422	DTCEA6	
IRQ2		18	H'0424	DTCEA5	
IRQ3		19	H'0426	DTCEA4	
IRQ4		20	H'0428	DTCEA3	
IRQ5		21	H'042A	DTCEA2	
IRQ6		22	H'042C	DTCEA1	
IRQ7		23	H'042E	DTCEA0	
ADI (A/D conversion end)	A/D	28	H'0438	DTCEB6	
TGI0A (GR0A compare match/input capture)	TPU channel 0	32	H'0440	DTCEB5	
TGI0B (GR0B compare match/input capture)		33	H'0442	DTCEB4	
TGI0C (GR0C compare match/input capture)		34	H'0444	DTCEB3	
TGI0D (GR0D compare match/input capture)		35	H'0446	DTCEB2	
TGI1A (GR1A compare match/input capture)	TPU channel 1	40	H'0450	DTCEB1	
TGI1B (GR1B compare match/input capture)		41	H'0452	DTCEB0	
TGI2A (GR2A compare match/input capture)	TPU channel 2	44	H'0458	DTCEC7	
TGI2B (GR2B compare match/input capture)		45	H'045A	DTCEC6	Low

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address	DTCE*	Priority
TGI3A (GR3A compare match/input capture)	TPU channel 3	48	H'0460	DTCEC5	High
TGI3B (GR3B compare match/input capture)		49	H'0462	DTCEC4	
TGI3C (GR3C compare match/input capture)		50	H'0464	DTCEC3	
TGI3D (GR3D compare match/input capture)		51	H'0466	DTCEC2	
TGI4A (GR4A compare match/input capture)	TPU channel 4	56	H'0470	DTCEC1	
TGI4B (GR4B compare match/input capture)		57	H'0472	DTCEC0	
TGI5A (GR5A compare match/input capture)	TPU channel 5	60	H'0478	DTCED5	
TGI5B (GR5B compare match/input capture)		61	H'047A	DTCED4	
CMIA0	8-bit timer channel 0	64	H'0480	DTCED3	
CMIB0		65	H'0482	DTCED2	
CMIA1	8-bit timer channel 1	68	H'0488	DTCED1	
CMIB1		69	H'048A	DTCED0	
RXI0 (receive-data-full 0)	SCI channel 0	81	H'04A2	DTCEE3	
TXI0 (transmit-data-empty 0)		82	H'04A4	DTCEE2	
RXI1 (receive-data-full 1)	SCI channel 1	85	H'04AA	DTCEE1	
TXI1 (transmit-data-empty 1)		86	H'04AC	DTCEE0	Low

Note: * DTCE bits with no corresponding interrupt are reserved, and should be written with 0.

Operation Order: If the same interrupt is selected as a DTC activation source and a CPU interrupt source, the DTC data transfer is performed first, followed by CPU interrupt exception handling.

Table 3.11 summarizes interrupt source selection and interrupt source clearance control according to the setting of the DTCE bit of DTC registers DTCERA to DTCERE and the DISEL bit in the DTC's MRB register.

Table 3.11 Interrupt Source Selection and Clearing Control

Settings			
DTC		Interrupt Source Selection/Clearing Control	
DTCE	DISEL	DTC	CPU
0	*	X	◎
1	0	◎	X
	1	○	◎

Legend

◎: The relevant interrupt is used. Interrupt source clearing is performed.
(The CPU should clear the source flag in the interrupt handling routine.)

○: The relevant interrupt is used. The interrupt source is not cleared.

X: The relevant bit cannot be used.

*: Don't care

Usage Note: SCI and A/D converter interrupt sources are cleared when the DTC reads or writes to the prescribed register, and are not dependent on the DISEL bit.

Section 4 Bus Controller

4.1 Overview

The H8S/2319 and H8S/2318 Series have an on-chip bus controller (BSC) that manages the external address space divided into eight areas. The bus specifications, such as bus width and number of access states, can be set independently for each area, enabling multiple memories to be connected easily.

The bus controller also has a bus arbitration function, and controls the operation of the internal bus masters—the CPU and data transfer controller (DTC).

4.1.1 Features

The features of the bus controller are listed below.

- Manages external address space in area units
  - In advanced mode, manages the external space as 8 areas of 2 Mbytes
  - Bus specifications can be set independently for each area
  - Burst ROM interfaces can be set
- Basic bus interface
  - Chip select signals ($\overline{CS0}$ to $\overline{CS7}$) can be output for areas 0 to 7
  - 8-bit access or 16-bit access can be selected for each area
  - 2-state access or 3-state access can be selected for each area
  - Program wait states can be inserted for each area
- Burst ROM interface
  - Burst ROM interface can be set for area 0
  - Selection of 1- or 2-state burst access
- Idle cycle insertion
  - An idle cycle can be inserted in case of external read cycles in different areas
  - An idle cycle can be inserted in case of an external write cycle immediately after an external read cycle
- Bus arbitration function
  - Includes a bus arbiter that arbitrates bus mastership between the CPU and DTC
- Other features
  - External bus release function

4.1.2 Block Diagram

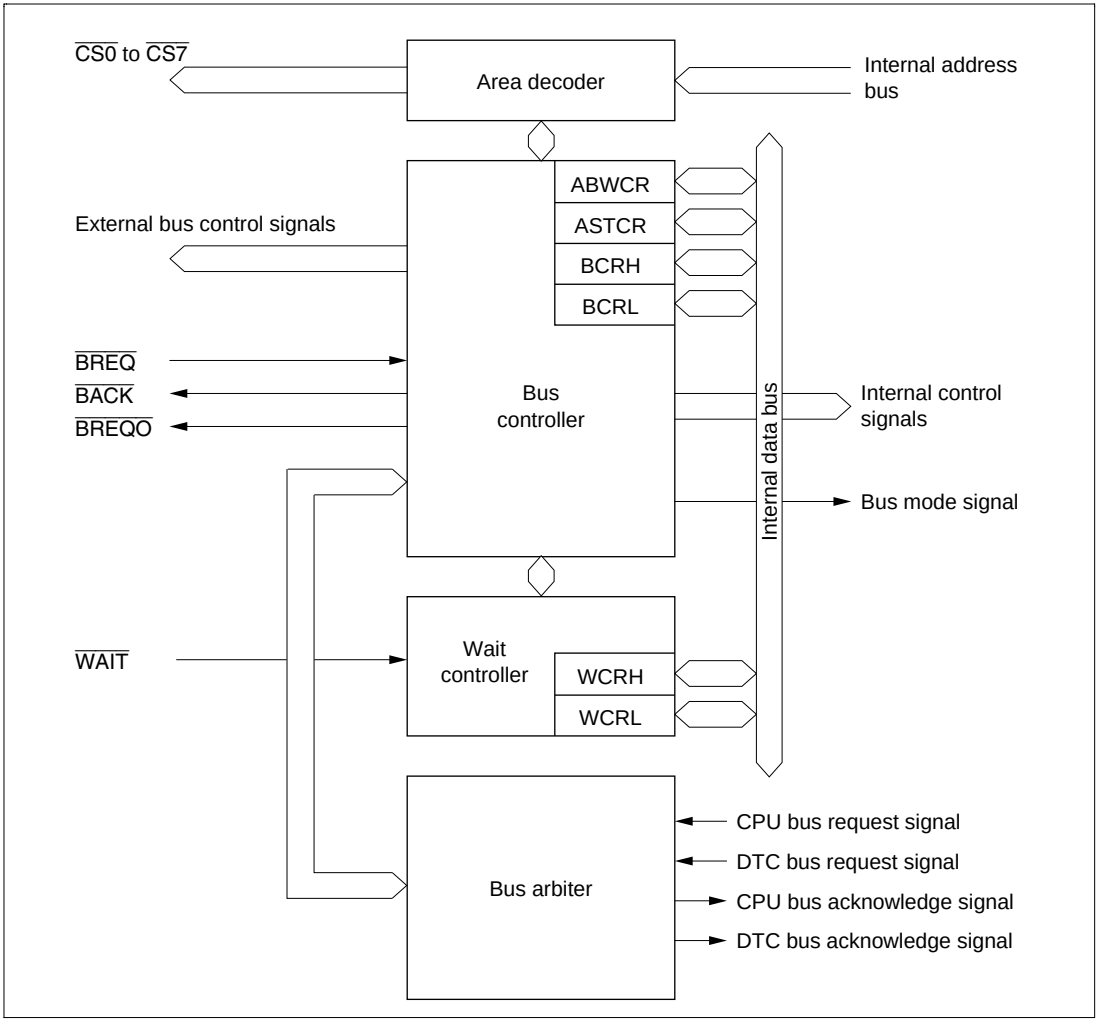


Figure 4.1 Block Diagram of Bus Controller

4.1.3 Pin Configuration

Table 4.1 summarizes the pins of the bus controller.

Table 4.1 Bus Controller Pins

Name	Symbol	I/O	Function
Address strobe	$\overline{AS}$	Output	Strobe signal indicating that address output on address bus is enabled.
Read	$\overline{RD}$	Output	Strobe signal indicating that external space is being read.
High write	$\overline{HWR}$	Output	Strobe signal indicating that external space is to be written, and upper half (D15 to D8) of data bus is enabled.
Low write	$\overline{LWR}$	Output	Strobe signal indicating that external space is to be written, and lower half (D7 to D0) of data bus is enabled.
Chip select 0	$\overline{CS0}$	Output	Strobe signal indicating that area 0 is selected.
Chip select 1	$\overline{CS1}$	Output	Strobe signal indicating that area 1 is selected.
Chip select 2	$\overline{CS2}$	Output	Strobe signal indicating that area 2 is selected.
Chip select 3	$\overline{CS3}$	Output	Strobe signal indicating that area 3 is selected.
Chip select 4	$\overline{CS4}$	Output	Strobe signal indicating that area 4 is selected.
Chip select 5	$\overline{CS5}$	Output	Strobe signal indicating that area 5 is selected.
Chip select 6	$\overline{CS6}$	Output	Strobe signal indicating that area 6 is selected.
Chip select 7	$\overline{CS7}$	Output	Strobe signal indicating that area 7 is selected.
Wait	$\overline{WAIT}$	Input	Wait request signal when accessing external 3-state access space.
Bus request	$\overline{BREQ}$	Input	Request signal for release of bus to external device.
Bus request acknowledge	$\overline{BACK}$	Output	Acknowledge signal indicating that bus has been released.
Bus request output	$\overline{BREQO}$	Output	External bus request signal used when internal bus master accesses external space when external bus is released.

4.1.4 Register Configuration

Table 4.2 summarizes the registers of the bus controller.

Table 4.2 Bus Controller Registers

Name	Abbreviation	R/W	Initial Value Reset	Address*[1]
Bus width control register	ABWCR	R/W	H'FF/H'00*[2]	H'FED0
Access state control register	ASTCR	R/W	H'FF	H'FED1
Wait control register H	WCRH	R/W	H'FF	H'FED2
Wait control register L	WCRL	R/W	H'FF	H'FED3
Bus control register H	BCRH	R/W	H'D0	H'FED4
Bus control register L	BCRL	R/W	H'3C	H'FED5

Notes: 1. Lower 16 bits of the address.
2. Determined by the MCU operating mode.

4.2 Register Descriptions

4.2.1 Bus Width Control Register (ABWCR)

Bit	:	7	6	5	4	3	2	1	0
		ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0
Modes 5 to 7									
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Mode 4									
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ABWCR is an 8-bit readable/writable register that designates each area as either 8-bit access space or 16-bit access space.

ABWCR sets the data bus width for the external memory space. The bus width for on-chip memory and internal I/O registers is fixed regardless of the settings in ABWCR.

After a reset and in hardware standby mode, ABWCR is initialized to H'FF in modes 5 to 7*, and to H'00 in mode 4. It is not initialized in software standby mode.

Note: * Modes 6 and 7 cannot be used in the ROMless version.

Bits 7 to 0—Area 7 to 0 Bus Width Control (ABW7 to ABW0): These bits select whether the corresponding area is to be designated as 8-bit access space or 16-bit access space.

Bit n ABWn	Description
0	Area n is designated for 16-bit access
1	Area n is designated for 8-bit access

(n = 7 to 0)

4.2.2 Access State Control Register (ASTCR)

Bit	:	7	6	5	4	3	2	1	0
		AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASTCR is an 8-bit readable/writable register that designates each area as either 2-state access space or 3-state access space.

ASTCR sets the number of access states for the external memory space. The number of access states for on-chip memory and internal I/O registers is fixed regardless of the settings in ASTCR.

ASTCR is initialized to H'FF by a reset, and in hardware standby mode. It is not initialized in software standby mode.

Bits 7 to 0—Area 7 to 0 Access State Control (AST7 to AST0): These bits select whether the corresponding area is to be designated as 2-state access space or 3-state access space.

Wait state insertion is enabled or disabled at the same time.

Bit n ASTn	Description	
0	Area n is designated for 2-state access Wait state insertion in area n external space access is disabled	
1	Area n is designated for 3-state access Wait state insertion in area n external space access is enabled	(Initial value)

(n = 7 to 0)

4.2.3 Wait Control Registers H and L (WCRH, WCRL)

WCRH and WCRL are 8-bit readable/writable registers that select the number of program wait states for each area.

Program waits are not inserted in on-chip memory or internal I/O register access.

WCRH and WCRL are initialized to H'FF by a reset, and in hardware standby mode. They are not initialized in software standby mode.

WCRH

Bit	:	7	6	5	4	3	2	1	0
		W71	W70	W61	W60	W51	W50	W41	W40
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 and 6—Area 7 Wait Control 1 and 0 (W71, W70): These bits select the number of program wait states when area 7 in external space is accessed while the AST7 bit in ASTCR is set to 1.

Bit 7 W71	Bit 6 W70	Description
0	0	Program wait not inserted when external space area 7 is accessed
	1	1 program wait state inserted when external space area 7 is accessed
1	0	2 program wait states inserted when external space area 7 is accessed
	1	3 program wait states inserted when external space area 7 is accessed (Initial value)

Bits 5 and 4—Area 6 Wait Control 1 and 0 (W61, W60): These bits select the number of program wait states when area 6 in external space is accessed while the AST6 bit in ASTCR is set to 1.

Bit 5 W61	Bit 4 W60	Description
0	0	Program wait not inserted when external space area 6 is accessed
	1	1 program wait state inserted when external space area 6 is accessed
1	0	2 program wait states inserted when external space area 6 is accessed
	1	3 program wait states inserted when external space area 6 is accessed (Initial value)

Bits 3 and 2—Area 5 Wait Control 1 and 0 (W51, W50): These bits select the number of program wait states when area 5 in external space is accessed while the AST5 bit in ASTCR is set to 1.

Bit 3 W51	Bit 2 W50	Description
0	0	Program wait not inserted when external space area 5 is accessed
	1	1 program wait state inserted when external space area 5 is accessed
1	0	2 program wait states inserted when external space area 5 is accessed
	1	3 program wait states inserted when external space area 5 is accessed (Initial value)

Bits 1 and 0—Area 4 Wait Control 1 and 0 (W41, W40): These bits select the number of program wait states when area 4 in external space is accessed while the AST4 bit in ASTCR is set to 1.

Bit 1 W41	Bit 0 W40	Description
0	0	Program wait not inserted when external space area 4 is accessed
	1	1 program wait state inserted when external space area 4 is accessed
1	0	2 program wait states inserted when external space area 4 is accessed
	1	3 program wait states inserted when external space area 4 is accessed (Initial value)

WCRL

Bit	:	7	6	5	4	3	2	1	0
		W31	W30	W21	W20	W11	W10	W01	W00
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 and 6—Area 3 Wait Control 1 and 0 (W31, W30): These bits select the number of program wait states when area 3 in external space is accessed while the AST3 bit in ASTCR is set to 1.

Bit 7 W31	Bit 6 W30	Description
0	0	Program wait not inserted when external space area 3 is accessed
	1	1 program wait state inserted when external space area 3 is accessed
1	0	2 program wait states inserted when external space area 3 is accessed
	1	3 program wait states inserted when external space area 3 is accessed (Initial value)

Bits 5 and 4—Area 2 Wait Control 1 and 0 (W21, W20): These bits select the number of program wait states when area 2 in external space is accessed while the AST2 bit in ASTCR is set to 1.

Bit 5 W21	Bit 4 W20	Description
0	0	Program wait not inserted when external space area 2 is accessed
	1	1 program wait state inserted when external space area 2 is accessed
1	0	2 program wait states inserted when external space area 2 is accessed
	1	3 program wait states inserted when external space area 2 is accessed (Initial value)

Bits 3 and 2—Area 1 Wait Control 1 and 0 (W11, W10): These bits select the number of program wait states when area 1 in external space is accessed while the AST1 bit in ASTCR is set to 1.

Bit 3 W11	Bit 2 W10	Description
0	0	Program wait not inserted when external space area 1 is accessed
	1	1 program wait state inserted when external space area 1 is accessed
1	0	2 program wait states inserted when external space area 1 is accessed
	1	3 program wait states inserted when external space area 1 is accessed (Initial value)

Bits 1 and 0—Area 0 Wait Control 1 and 0 (W01, W00): These bits select the number of program wait states when area 0 in external space is accessed while the AST0 bit in ASTCR is set to 1.

Bit 1 W01	Bit 0 W00	Description
0	0	Program wait not inserted when external space area 0 is accessed
	1	1 program wait state inserted when external space area 0 is accessed
1	0	2 program wait states inserted when external space area 0 is accessed
	1	3 program wait states inserted when external space area 0 is accessed (Initial value)

4.2.4 Bus Control Register H (BCRH)

Bit	:	7	6	5	4	3	2	1	0
		ICIS1	ICIS0	BRSTRM	BRSTS1	BRSTS0	—	—	—
Initial value	:	1	1	0	1	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BCRH is an 8-bit readable/writable register that selects enabling or disabling of idle cycle insertion, and the memory interface for area 0.

BCRH is initialized to H'D0 by a reset, and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—Idle Cycle Insert 1 (ICIS1): Selects whether or not one idle cycle state is to be inserted between bus cycles when successive external read cycles are performed in different areas.

Bit 7 ICIS1	Description
0	Idle cycle not inserted in case of successive external read cycles in different areas.
1	Idle cycle inserted in case of successive external read cycles in different areas. (Initial value)

Bit 6—Idle Cycle Insert 0 (ICIS0): Selects whether or not one idle cycle state is to be inserted between bus cycles when successive external read and external write cycles are performed .

Bit 6 ICIS0	Description
0	Idle cycle not inserted in case of successive external read and external write cycles.
1	Idle cycle inserted in case of successive external read and external write cycles. (Initial value)

Bit 5—Burst ROM Enable (BRSTRM): Selects whether area 0 is used as a burst ROM interface area.

Bit 5 BRSTRM	Description
0	Area 0 is basic bus interface area (Initial value)
1	Area 0 is burst ROM interface area

Bit 4—Burst Cycle Select 1 (BRSTS1): Selects the number of burst cycles for the burst ROM interface.

Bit 4 BRSTS1	Description	
0	Burst cycle comprises 1 state	
1	Burst cycle comprises 2 states	(Initial value)

Bit 3—Burst Cycle Select 0 (BRSTS0): Selects the number of words that can be accessed in a burst access on the burst ROM interface.

Bit 3 BRSTS0	Description	
0	Max. 4 words in burst access	(Initial value)
1	Max. 8 words in burst access	

Bits 2 to 0—Reserved: Only 0 should be written to these bits.

4.2.5 Bus Control Register L (BCRL)

Bit	:	7	6	5	4	3	2	1	0
		BRLE	BREQOE	EAE	—	—	—	—	WAITE
Initial value	:	0	0	1	1	1	1	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BCRL is an 8-bit readable/writable register that performs selection of the external bus-released state protocol, selection of the area partition unit, and enabling or disabling of $\overline{\text{WAIT}}$ pin input.

BCRL is initialized to H'3C by a reset, and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—Bus Release Enable (BRLE): Enables or disables external bus release.

Bit 7 BRLE	Description	
0	External bus release disabled. $\overline{\text{BREQ}}$, $\overline{\text{BACK}}$, and $\overline{\text{BREQO}}$ pins can be used as I/O ports	(Initial value)
1	External bus release enabled	

Bit 6—BREQO Pin Enable (BREQOE): Outputs a signal that requests the external bus master to drop the bus request signal ($\overline{\text{BREQ}}$) in the external bus-released state or when an internal bus master performs an external space access.

Bit 6 BREQOE	Description	
0	$\overline{\text{BREQO}}$ output disabled. $\overline{\text{BREQO}}$ pin can be used as I/O port	(Initial value)
1	$\overline{\text{BREQO}}$ output enabled	

Bit 5—External Address Enable (EAE): Designates addresses H'010000 to H'03FFFF* as either internal or external addresses.

Note: * H'010000 to H'05FFFF in the H8S/2315.
H'010000 to H'07FFFF in the H8S/2319.

	Description		
Bit 5 EAE	**H8S/2319, H8S/2318, H8S/2315**	**H8S/2317**	**H8S/2316, H8S/2313, H8S/2311**
0	On-chip ROM	Addresses H'010000 to H'01FFFF are on-chip ROM and addresses H'020000 to H'03FFFF are reserved area*[1]	Reserved area*[1]
1	Addresses H'010000 to H'03FFFF*[2] are external addresses in external expanded mode or reserved area*[1] in single-chip mode		

Notes: 1. Do not access a reserved area.
2. H'010000 to H'05FFFF in the H8S/2315.
H'010000 to H'07FFFF in the H8S/2319.

Bits 4 to 2—Reserved: Only 1 should be written to these bits.

Bit 1—Reserved: Only 0 should be written to this bit.

Bit 0—WAIT Pin Enable (WAITE): Selects enabling or disabling of wait input by the $\overline{\text{WAIT}}$ pin.

Bit 0 WAITE	Description	
0	Wait input by $\overline{\text{WAIT}}$ pin disabled. $\overline{\text{WAIT}}$ pin can be used as I/O port	(Initial value)
1	Wait input by $\overline{\text{WAIT}}$ pin enabled	

4.3 Overview of Bus Control

4.3.1 Area Partitioning

In advanced mode, the bus controller partitions the 16-Mbyte address space into eight areas, 0 to 7, in 2-Mbyte units, and performs bus control for external space in area units. Figure 4.2 shows an outline of the memory map.

Chip select signals ($\overline{CS0}$ to $\overline{CS7}$) can be output for each area.

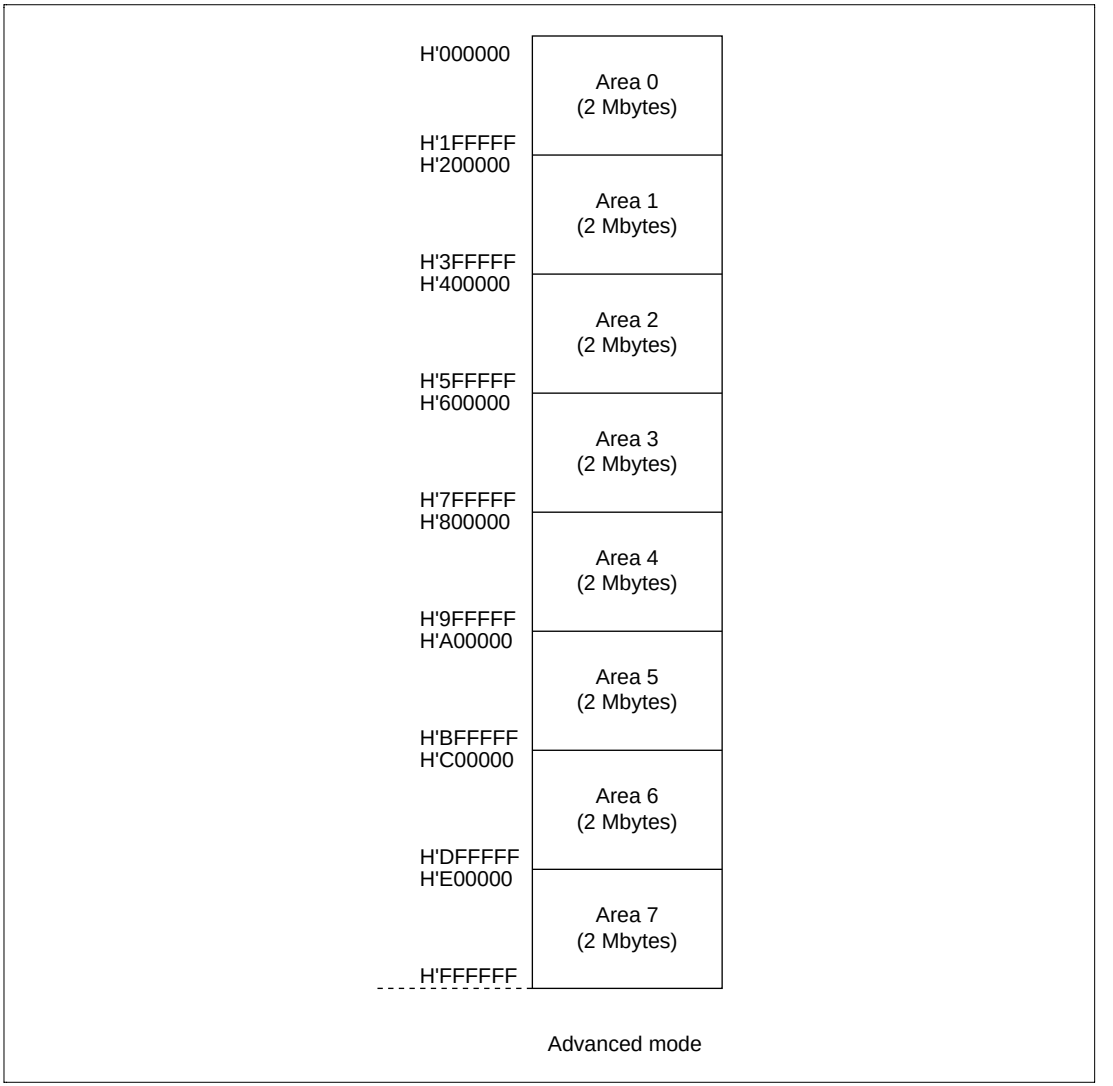


Figure 4.2 Area Partitioning

4.3.2 Bus Specifications

The external space bus specifications consist of three elements: (1) bus width, (2) number of access states, and (3) number of program wait states.

The bus width and number of access states for on-chip memory and internal I/O registers are fixed, and are not affected by the bus controller.

Bus Width: A bus width of 8 or 16 bits can be selected with ABWCR. An area for which an 8-bit bus is selected functions as an 8-bit access space, and an area for which a 16-bit bus is selected functions as a16-bit access space.

If all areas are designated for 8-bit access, 8-bit bus mode is set; if any area is designated for 16-bit access, 16-bit bus mode is always set. When the burst ROM interface is selected, 16-bit bus mode is always set.

Number of Access States: Two or three access states can be selected with ASTCR. An area for which 2-state access is selected functions as a 2-state access space, and an area for which 3-state access is selected functions as a 3-state access space.

With the burst ROM interface, the number of access states may be determined without regard to ASTCR.

When 2-state access space is designated, wait insertion is disabled.

Number of Program Wait States: When 3-state access space is designated by ASTCR, the number of program wait states to be inserted automatically is selected with WCRH and WCRL. From 0 to 3 program wait states can be selected.

Table 4.3 shows the bus specifications for each basic bus interface area.

Table 4.3 Bus Specifications for Each Area (Basic Bus Interface)

ABWCR	ASTCR	WCRH, WCRL		Bus Specifications (Basic Bus Interface)		
ABWn	ASTn	Wn1	Wn0	Bus Width	Access States	Program Wait States
0	0	—	—	16	2	0
	1	0	0		3	0
			1			1
		1	0			2
			1			3
1	0	—	—	8	2	0
	1	0	0		3	0
			1			1
		1	0			2
			1			3

4.3.3 Memory Interfaces

The memory interfaces of the H8S/2319 and H8S/2318 Series comprise a basic bus interface that allows direct connection of ROM, SRAM, and so on; and a burst ROM interface that allows direct connection of burst ROM(only area 0).

An area for which the basic bus interface is designated functions as normal space, and an area for which the burst ROM interface is designated functions as burst ROM space.

4.3.4 Advanced Mode

The initial state of each area is basic bus interface, 3-state access space. The initial bus width is selected according to the operating mode. The bus specifications described here cover basic items only, and the sections on each memory interface (4.4 and 4.5) should be referred to for further details.

Area 0: Area 0 includes on-chip ROM, and in expanded mode with on-chip ROM disabled, all of area 0 is external space. In expanded mode with on-chip ROM enabled, the space excluding on-chip ROM is external space.

When area 0 external space is accessed, the $\overline{\text{CS0}}$ signal can be output.

Either basic bus interface or burst ROM interface can be selected for area 0.

Areas 1 to 6: In external expanded mode, all of area 1 to area 6 is external space.

When area 1 to 6 external space is accessed, the $\overline{CS1}$ to $\overline{CS6}$ pin signals can be output, respectively.

Only the basic bus interface can be used for areas 1 to 6.

Area 7: Area 7 includes the on-chip RAM and internal/O registers. In external expanded mode, the space excluding the on-chip RAM and internal/O registers is external space. The on-chip RAM is enabled when the RAME bit in the system control register (SYSCR) is set to 1; when the RAME bit is cleared to 0, the on-chip RAM is disabled and the corresponding space becomes external space .

When area 7 external space is accessed, the $\overline{CS7}$ signal can be output.

Only the basic bus interface can be used for the area 7 memory interface.

4.3.5 Chip Select Signals

The chip can output chip select signals ($\overline{CS0}$ to $\overline{CS7}$) to areas 0 to 7, the signal being driven low when the corresponding external space area is accessed.

Figure 4.3 shows an example of $\overline{CSn}$ (n = 0 to 7) output timing.

Enabling or disabling of $\overline{CSn}$ signal output is performed by setting the data direction register (DDR) bit for the port corresponding to the particular $\overline{CSn}$ pin.

In expanded mode with on-chip ROM disabled, the $\overline{CS0}$ pin is placed in the output state after a reset. Pins CS1 to CS7 are placed in the input state after a reset, and so the corresponding DDR bits should be set to 1 when outputting signals $\overline{CS1}$ to $\overline{CS7}$.

In expanded mode with on-chip ROM enabled, pins $\overline{CS0}$ to $\overline{CS7}$ are all placed in the input state after a reset, and so the corresponding DDR bits should be set to 1 when outputting signals $\overline{CS0}$ to $\overline{CS7}$.

For details, see section 5, I/O Ports.

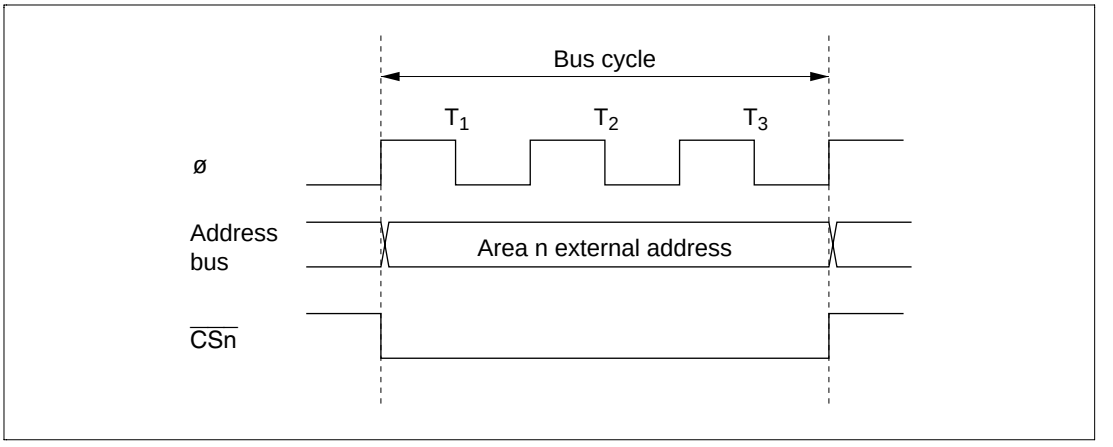


Figure 4.3 $\overline{\text{CSn}}$ Signal Output Timing (n = 0 to 7)

4.4 Basic Bus Interface

4.4.1 Overview

The basic bus interface enables direct connection of ROM, SRAM, and so on.

The bus specifications can be selected with ABWCR, ASTCR, WCRH, and WCRL. For details, see section 4.4, Basic Bus Interface, in the Hardware Manual.

4.4.2 Wait Control

When accessing external space , the chip can extend the bus cycle by inserting one or more wait states (T_w). There are two ways of inserting wait states: program wait insertion and pin wait insertion using the $\overline{\text{WAIT}}$ pin.

Program Wait Insertion: From 0 to 3 wait states can be inserted automatically between the T_2 state and T_3 state on an individual area basis in 3-state access space, according to the settings in WCRH and WCRL.

Pin Wait Insertion: Setting the WAITE bit in BCRL to 1 enables wait input by means of the $\overline{\text{WAIT}}$ pin. When external space is accessed in this state, a program wait is first inserted in accordance with the settings in WCRH and WCRL. If the $\overline{\text{WAIT}}$ pin is low at the falling edge of ø in the last T_2 or T_w state, another T_w state is inserted. If the $\overline{\text{WAIT}}$pin is held low, T_w states are inserted it goes high.

This is useful when inserting four or more T_w states, or when changing the number of T_w states for different external devices.

The WAITE bit setting applies to all areas.

Figure 4.4 shows an example of wait state insertion timing.

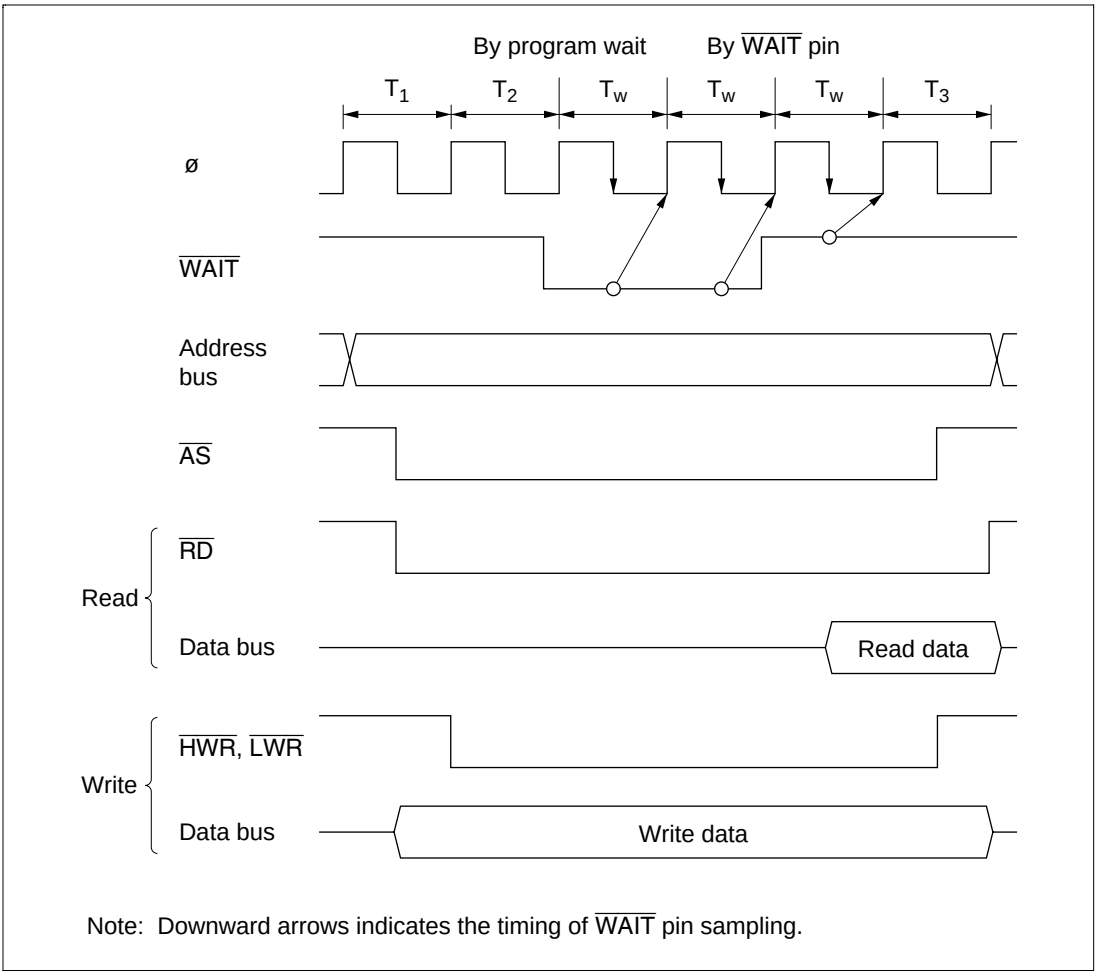


Figure 4.4 Example of Wait State Insertion Timing

The settings after a reset are: 3-state access, 3 program wait state insertion, and WAIT input disabled.

4.5 Burst ROM Interface

4.5.1 Overview

With the H8S/2319 and H8S/2318 Series, external space area 0 can be designated as burst ROM space, and burst ROM interfacing performed. The burst ROM space interface enables 16-bit ROM with burst access capability to be accessed at high speed.

Area 0 can be designated as burst ROM space by means of the BRSTRM bit in BCRH. Consecutive burst accesses of a maximum or 4 words or 8 words can be performed for CPU instruction fetches only. One or two states can be selected for burst access.

4.5.2 Basic Timing

The number of states in the initial cycle (full access) of the burst ROM interface is determined by the setting of the AST0 bit in ASTCR. When the AST0 bit is set to 1, wait state insertion is also possible. One or two states can be selected for the burst cycle, according to the setting of the BRSTS1 bit in BCRH. Wait states cannot be inserted. When area 0 is designated as burst ROM space, it functions as 16-bit access space regardless of the setting of the ABW0 bit in ABWCR.

When the BRSTS0 bit in BCRH is cleared to 0, burst access of up to 4 words is performed; when the BRSTS0 bit is set to 1, burst access of up to 8 words is performed.

The basic access timing for burst ROM space is shown in figures 4.5 (a) and (b). The timing shown in figure 4.5 (a) is for the case where the AST0 and BRSTS1 bits are both set to 1, and that in figure 4.5 (b) is for the case where both these bits are cleared to 0.

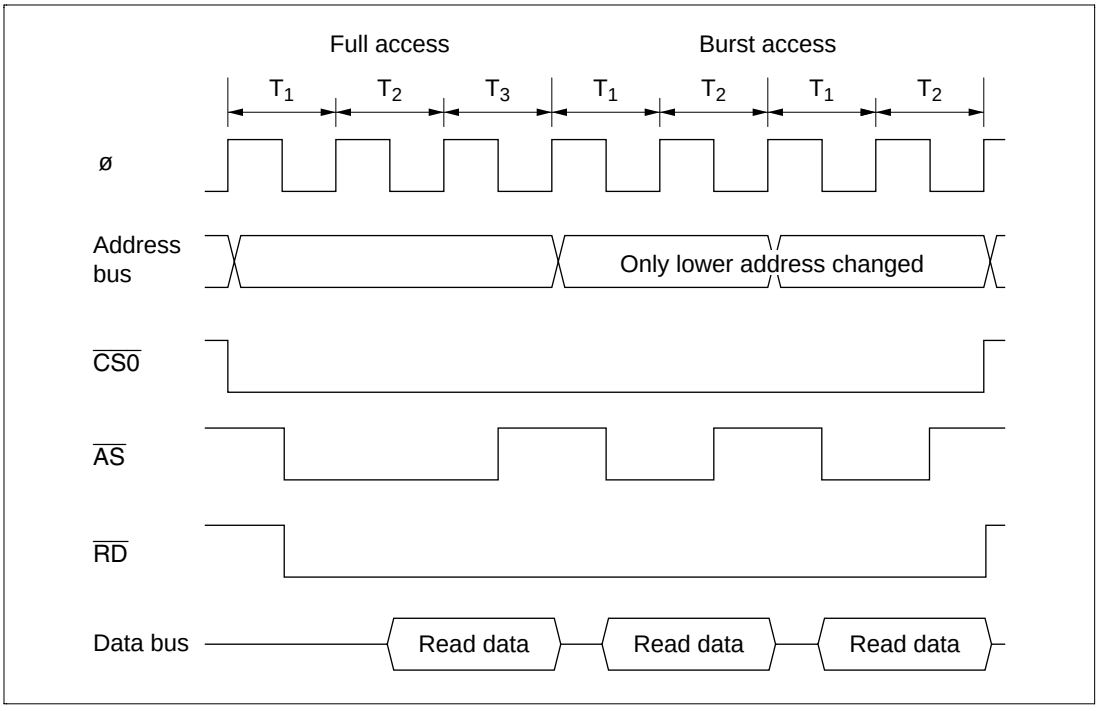


Figure 4.5 (a) Example of Burst ROM Access Timing (When AST0 = BRSTS1= 1)

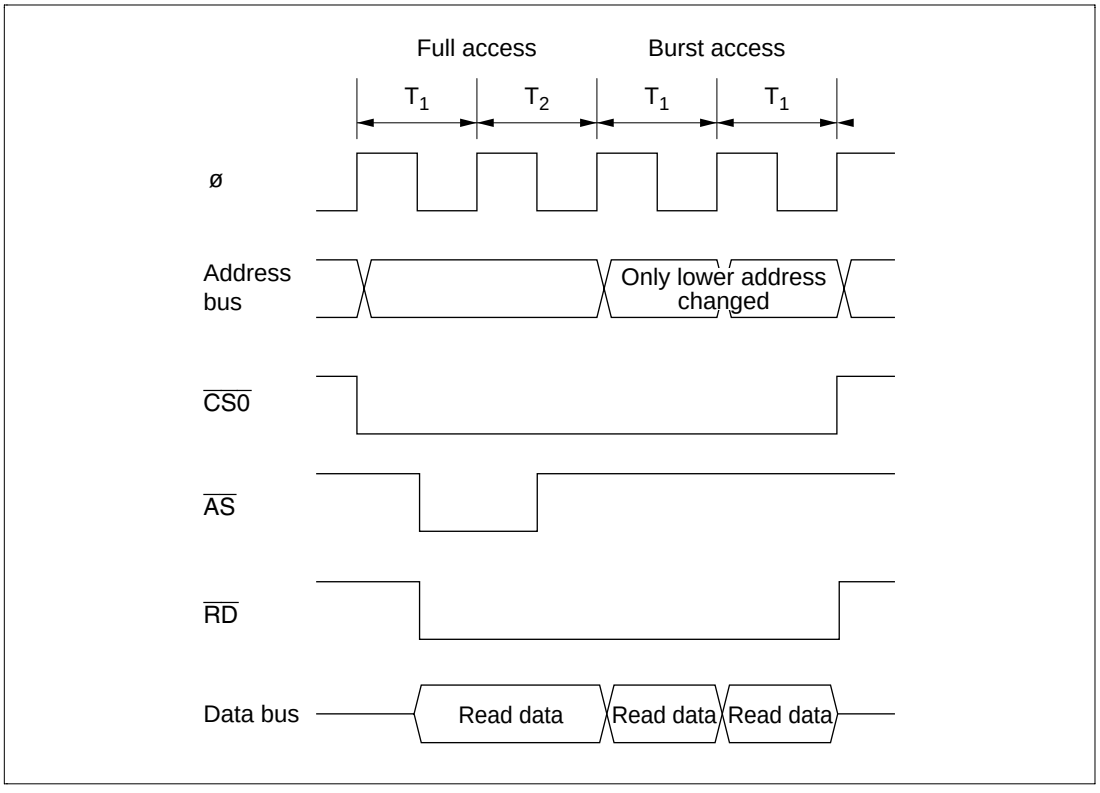


Figure 4.5 (b) Example of Burst ROM Access Timing (When AST0 = BRSTS1 = 0)

4.5.3 Wait Control

As with the basic bus interface, either program wait insertion or pin wait insertion using the $\overline{\text{WAIT}}$ pin can be used in the initial cycle (full access) on the burst ROM interface. See section 4.4.2, Wait Control.

Wait states cannot be inserted in a burst cycle.

4.6 Idle Cycle

4.6.1 Operation

When the H8S/2319 or H8S/2318 Series chip accesses external space, it can insert a 1-state idle cycle (T_I) between bus cycles in the following two cases: (1) when read accesses in different areas occur consecutively, and (2) when a write cycle occurs immediately after a read cycle. By inserting an idle cycle it is possible, for example, to avoid data collisions between ROM, etc., with a long output floating time, and high-speed memory, I/O interfaces, and so on.

Consecutive Reads in Different Areas: If consecutive reads in different areas occur while the ICIS1 bit in BCRH is set to 1, an idle cycle is inserted at the start of the second read cycle. This is enabled in advanced mode.

Figure 4.6 shows an example of the operation in this case. In this example, bus cycle A is a read cycle for ROM with a long output floating time, and bus cycle B is a read cycle for SRAM, each being located in a different area. In (a), an idle cycle is not inserted, and a collision occurs in bus cycle B between the read data from ROM and that from SRAM. In (b), an idle cycle is inserted, and a data collision is prevented.

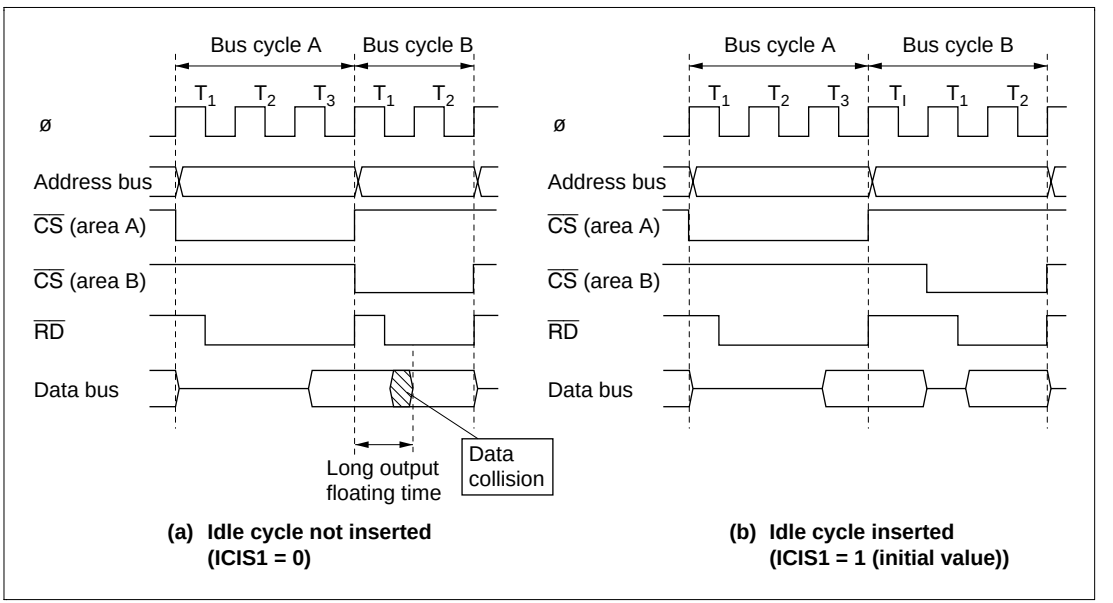


Figure 4.6 Example of Idle Cycle Operation (1)

Write after Read: If an external write occurs after an external read while the ICIS0 bit in BCRH is set to 1, an idle cycle is inserted at the start of the write cycle.

Figure 4.7 shows an example of the operation in this case. In this example, bus cycle A is a read cycle for ROM with a long output floating time, and bus cycle B is a CPU write cycle. In (a), an idle cycle is not inserted, and a collision occurs in bus cycle B between the read data from ROM and the CPU write data. In (b), an idle cycle is inserted, and a data collision is prevented.

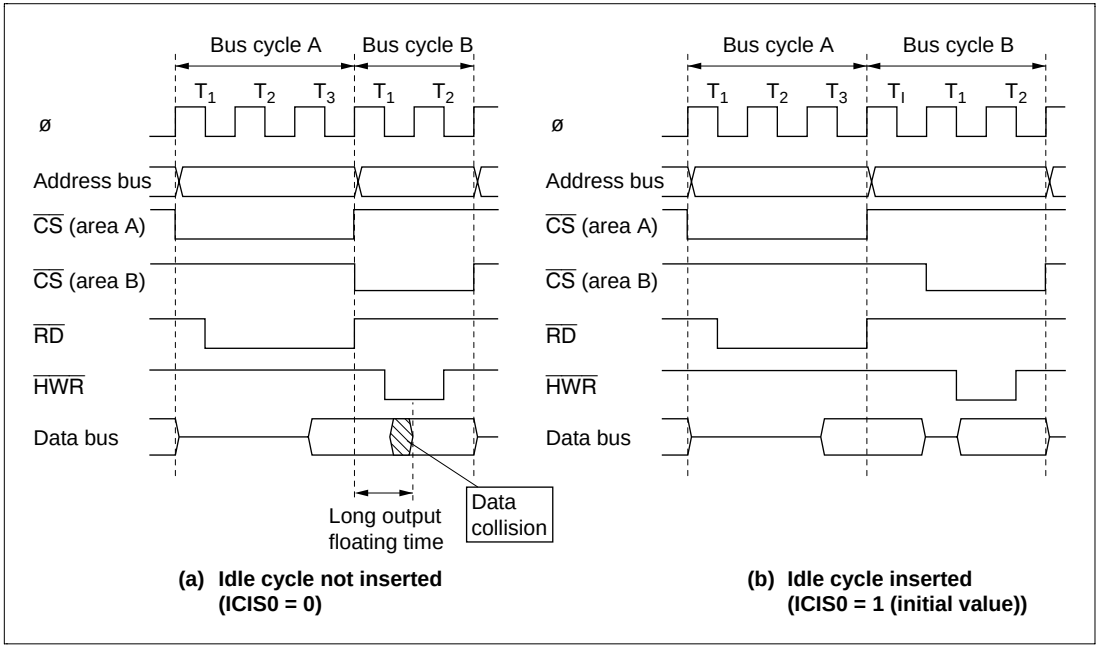


Figure 4.7 Example of Idle Cycle Operation (2)

Relationship between Chip Select ($\overline{CS}$) Signal and Read ($\overline{RD}$) Signal: Depending on the system's load conditions, the $\overline{RD}$ signal may lag behind the $\overline{CS}$ signal. An example is shown in figure 4.8.

In this case, with the setting for no idle cycle insertion (a), there may be a period of overlap between the bus cycle A $\overline{RD}$ signal and the bus cycle B $\overline{CS}$ signal.

Setting idle cycle insertion, as in (b), however, will prevent any overlap between the $\overline{RD}$ and $\overline{CS}$ signals.

In the initial state after reset release, idle cycle insertion (b) is set.

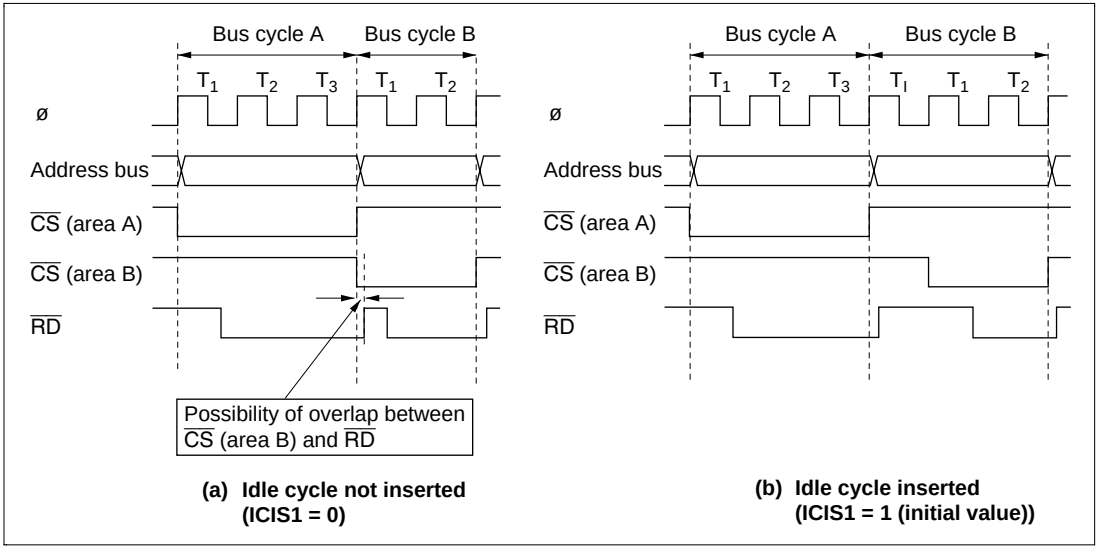


Figure 4.8 Relationship between Chip Select ($\overline{CS}$) and Read ($\overline{RD}$)

4.6.2 Pin States in Idle Cycle

Table 4.4 shows the pin states in an idle cycle.

Table 4.4 Pin States in Idle Cycle

Pins	Pin State
A23 to A0	Contents of following bus cycle
D15 to D0	High impedance
$\overline{\text{CSn}}$	High
$\overline{\text{AS}}$	High
$\overline{\text{RD}}$	High
$\overline{\text{HWR}}$	High
$\overline{\text{LWR}}$	High

4.7 Bus Release

4.7.1 Overview

The H8S/2319 and H8S/2318 Series can release the external bus in response to a bus request from an external device. In the external bus-released state, the internal bus master continues to operate as long as there is no external access.

If an internal bus master wants to make an external access in the external bus-released state, it can issue a request off-chip for the bus request to be dropped.

4.7.2 Operation

In external expanded mode, the bus can be released to an external device by setting the BRLE bit in BCRL to 1. Driving the $\overline{\text{BREQ}}$ pin low issues an external bus request to the H8S/2319 or H8S/2318 Series chip. When the $\overline{\text{BREQ}}$ pin is sampled, at the prescribed timing the $\overline{\text{BACK}}$ pin is driven low, and the address bus, data bus, and bus control signals are placed in the high-impedance state, establishing the external bus-released state.

In the external bus-released state, an internal bus master can perform accesses using the internal bus. When an internal bus master wants to make an external access, it temporarily defers activation of the bus cycle, and waits for the bus request from the external bus master to be dropped.

If the BREQOE bit in BCRL is set to 1, when an internal bus master wants to make an external access in the external bus-released state, the $\overline{\text{BREQO}}$ pin is driven low and a request can be made off-chip to drop the bus request.

When the $\overline{\text{BREQ}}$ pin goes high, the $\overline{\text{BACK}}$ pin is driven high at the prescribed timing and the external bus-released state is terminated.

If an external bus release request and external access occur simultaneously, the order of priority is as follows:

(High) External bus release > Internal bus master external access (Low)

4.7.3 Pin States in External-Bus-Released State

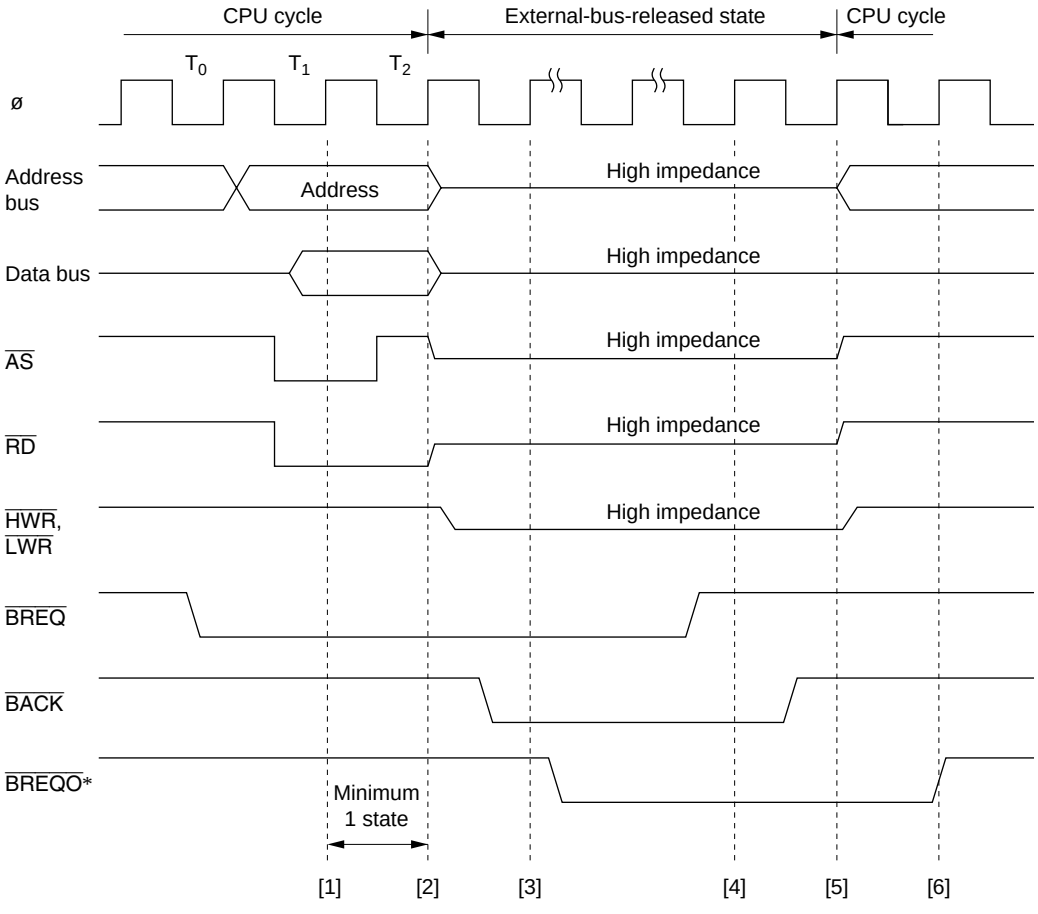
Table 4.5 shows pin states in the external-bus-released state.

Table 4.5 Pin States in Bus-Released State

Pins	Pin State
A23 to A0	High impedance
D15 to D0	High impedance
$\overline{\text{CSn}}$	High impedance
$\overline{\text{AS}}$	High impedance
$\overline{\text{RD}}$	High impedance
$\overline{\text{HWR}}$	High impedance
$\overline{\text{LWR}}$	High impedance

4.7.4 Transition Timing

Figure 4.9 shows the timing for transition to the bus-released state.



[1] Low level of $\overline{\text{BREQ}}$ pin is sampled at fall of T_2 state.
[2] $\overline{\text{BACK}}$ pin is driven low at end of CPU read cycle, releasing bus to external bus master.
[3] $\overline{\text{BREQ}}$ pin state is still sampled in external-bus-released state.
[4] High level of $\overline{\text{BREQ}}$ pin is sampled.
[5] $\overline{\text{BACK}}$ pin is driven high, ending bus release cycle.
[6] $\overline{\text{BREQO}}$ signal goes high 1.5 clocks after rise of $\overline{\text{BACK}}$ signal.

Note: * Output only when BREQOE = 1.

Figure 4.9 Bus-Released State Transition Timing

4.7.5 Usage Note

If MSTPCR is set to H'FFFF or H'EFFF and a transition is made to sleep mode, the external bus release function will halt. Therefore, these settings should not be used.

4.8 Bus Arbitration

4.8.1 Overview

The H8S/2319 and H8S/2318 Series have a bus arbiter that arbitrates bus master operations.

There are two bus masters, the CPU and DTC which perform read/write operations when they have possession of the bus. Each bus master requests the bus by means of a bus request signal. The bus arbiter determines priorities at the prescribed timing, and permits use of the bus by means of a bus request acknowledge signal. The selected bus master then takes possession of the bus and begins its operation.

4.8.2 Operation

The bus arbiter monitors the bus masters' bus request signals, and if the bus is requested, sends a bus request acknowledge signal to the bus master making the request. If there are bus requests from more than one bus master, the bus request acknowledge signal is sent to the one with the highest priority. When a bus master receives the bus request acknowledge signal, it takes possession of the bus until that signal is canceled.

The order of priority of the bus masters is as follows:

(High) DTC > CPU (Low)

An external access by an internal bus master and external bus release can be executed in parallel.

If an external bus release request and an external access by an internal bus master occur simultaneously, the order of priority is as follows:

(High) External bus release > Internal bus master external access (Low)

4.8.3 Bus Transfer Timing

Even if a bus request is received from a bus master with a higher priority than that of the bus master that has acquired the bus and is currently operating, the bus is not necessarily transferred immediately. There are specific times at which each bus master can relinquish the bus.

CPU: The CPU is the lowest-priority bus master, and if a bus request is received from the DTC, the bus arbiter transfers the bus to the bus master that issued the request. The timing for transfer of the bus is as follows:

- The bus is transferred at a break between bus cycles. However, if a bus cycle is executed in discrete operations, as in the case of a longword-size access, the bus is not transferred between the component operations. For details of times when the bus is not transferred, see appendix A.5, Bus States During Instruction Execution, in the Hardware Manual.
- If the CPU is in sleep mode, it transfers the bus immediately.

DTC: The DTC sends the bus arbiter a request for the bus when an activation request is generated.

The DTC can release the bus after a vector read, a register information read (3 states), a single data transfer, or a register information write (3 states). It does not release the bus during a register information read (3 states), a single data transfer, or a register information write (3 states).

4.8.4 Note on Use of External Bus Release

External bus release can be performed on completion of an external bus cycle. The $\overline{RD}$ signal remain low until the end of the external bus cycle. Therefore, when external bus release is performed, the $\overline{RD}$ signals may change from the low level to the high-impedance state.

4.9 Bus Controller Operation in a Reset

In a reset, the chip, including the bus controller, enters the reset state immediately, and any executing bus cycle is aborted.

Section 5 I/O Ports

5.1 Overview

The H8S/2319 and H8S/2318 Series have 10 I/O ports (ports 1, 2, 3, and A to G), and one input-only port (port 4).

Table 5.1 summarizes the port functions. The pins of each port also have other functions.

Each port includes a data direction register (DDR) that controls input/output (not provided for the input-only ports), a data register (DR) that stores output data, and a port register (PORT) used to read the pin states.

Ports A to E have a built-in MOS pull-up function, and in addition to DR and DDR, have a MOS input pull-up control register (PCR) to control the on/off state of MOS input pull-up.

Port 3 and port A include an open drain control register (ODR) that controls the on/off state of the output buffer PMOS.

Ports 1, A to F can drive a single TTL load and 50 pF capacitive load, and ports 2, 3, and G can drive a single TTL load and 30 pF capacitive load.

Ports 1, 2, and ports 34, 35 (only when used as IRQ inputs), ports F0 to F3 (only when used as IRQ inputs), ports G0 and G1 (only when used as IRQ inputs) are schmitt-triggered inputs.

Table 5.1 Port Functions

Port	Description	Pins	Mode 4	Mode 5	Mode 6*1	Mode 7*1
Port 1	• 8-bit I/O port • Schmitt-triggered input	P17/TIOCB2/TCLKD P16/TIOCA2 P15/TIOCB1/TCLKC P14/TIOCA1	8-bit I/O port also functioning as TPU I/O pins (TCLKA, TCLKB, TCLKC, TCLKD, TIOCA0, TIOCB0, TIOCC0, TIOCD0, TIOCA1, TIOCB1, TIOCA2, TIOCB2)			
		P13/TIOCD0/TCLKB/A23 P12/TIOCC0/TCLKA/A22 P11/TIOCB0/A21 P10/TIOCA0/A20	When DDR = 0: input port also functioning as TPU I/O pins (TCLKA, TCLKB, TIOCA0, TIOCB0, TIOCC0, TIOCD0) When DDR = 1 and A23E to A20E = 1: Address output When DDR = 1 and A23E to A20E = 0: DR value output			
Port 2	• 8-bit I/O port • Schmitt-triggered input	P27/TIOCB5/TMO1 P26/TIOCA5/TMO0 P25/TIOCB4/TMCI1 P24/TIOCA4/TMRI1 P23/TIOCD3/TMCI0 P22/TIOCC3/TMRI0 P21/TIOCB3 P20/TIOCA3	8-bit I/O port also functioning as TPU I/O pins (TIOCA3, TIOCB3, TIOCC3, TIOCD3, TIOCA4, TIOCB4, TIOCA5, TIOCB5), and 8-bit timer (channels 0 and 1) I/O pins (TMRI0, TMCI0, TMO0, TMRI1, TMCI1, TMO1)			
Port 3	• 6-bit I/O port • Open-drain output capability • Schmitt-triggered input ($\overline{IRQ5}$, $\overline{IRQ4}$)	P35/SCK1/$\overline{IRQ5}$ P34/SCK0/$\overline{IRQ4}$ P33/RxD1 P32/RxD0 P31/TxD1 P30/TxD0	6-bit I/O port also functioning as SCI (channels 0 and 1) I/O pins (TxD0, RxD0, SCK0, TxD1, RxD1, SCK1) and interrupt input pins ($\overline{IRQ5}$, $\overline{IRQ4}$)			

Port	Description	Pins	Mode 4	Mode 5	Mode 6*1	Mode 7*1
Port 4	• 8-bit input port	P47/AN7/DA1 P46/AN6/DA0 P45/AN5 P44/AN4 P43/AN3 P42/AN2 P41/AN1 P40/AN0	8-bit input port also functioning as A/D converter analog inputs (AN7 to AN0) and D/A converter analog outputs (DA1 and DA0)			
Port A	• 4-bit I/O port • Built-in MOS input pull-up • Open-drain output capability	PA3/A19 to PA0/A16	Address output		When DDR = 0 (after reset): input ports When DDR = 1: address output	I/O ports
Port B	• 8-bit I/O port • Built-in MOS input pull-up	PB7/A15 to PB0/A8	Address output		When DDR = 0 (after reset): input port When DDR = 1: address output	I/O port
Port C	• 8-bit I/O port • Built-in MOS input pull-up	PC7/A7 to PC0/A0	Address output		When DDR = 0 (after reset): input port When DDR = 1: address output	I/O port
Port D	• 8-bit I/O port • Built-in MOS input pull-up	PD7/D15 to PD0/D8	Data bus input/output			I/O port

Port	Description	Pins	Mode 4	Mode 5	Mode 6*1	Mode 7*1
Port E	• 8-bit I/O port • Built-in MOS input pull-up	PE7/D7 to PE0/D0	In 8-bit bus mode: I/O port In 16-bit bus mode: data bus input/output			I/O port
Port F	• 8-bit I/O port • Schmitt-triggered input ($\overline{IRQ3}$ to $\overline{IRQ0}$)	PF7/ø	When DDR = 0: input port When DDR = 1 (after reset): ø output			When DDR = 0 (after reset): input port When DDR = 1: ø output
		PF6/$\overline{AS}$	When ASOD = 1: I/O port When ASOD = 0: $\overline{AS}$ output			I/O port
		PF5/$\overline{RD}$ PF4/$\overline{HWR}$	$\overline{RD}$, $\overline{HWR}$ output			
		PF3/$\overline{LWR}$/$\overline{IRQ3}$	In 8-bit bus mode: When LWROD = 1, I/O port In 16-bit bus mode: $\overline{LWR}$ output also functioning as interrupt input pin ($\overline{IRQ3}$)			I/O port also functioning as interrupt input pins ($\overline{IRQ3}$ to $\overline{IRQ0}$)
		PF2/$\overline{WAIT}$/$\overline{IRQ2}$/$\overline{BREQO}$	When WAITE = 0, BRLE = 0, BREQOE = 0 (after reset): I/O port also functioning as interrupt input pin ($\overline{IRQ2}$)			
			When WAITE = 1: $\overline{WAIT}$ input also functioning as interrupt input pin ($\overline{IRQ2}$)			
			When WAITE = 0, BRLE = 1, BREQOE = 1: $\overline{BREQO}$ output also functioning as interrupt input pin ($\overline{IRQ2}$)			
		PF1/$\overline{BACK}$/$\overline{IRQ1}$/$\overline{CS5}$ PF0/$\overline{BREQ}$/$\overline{IRQ0}$/$\overline{CS4}$	When BRLE = 0 (after reset): I/O port also functioning as interrupt input pins ($\overline{IRQ1}$, $\overline{IRQ0}$) When CS25E = 1, PF1CS5S = 1, and DDR = 1: Also functions as $\overline{CS5}$ output When CS25E = 1, PF0CS4S = 1, and DDR = 1: Also functions as $\overline{CS4}$ output			
			When BRLE = 1: $\overline{BREQ}$ input, $\overline{BACK}$ output also functioning as interrupt input pins ($\overline{IRQ1}$, $\overline{IRQ0}$)			

Port	Description	Pins	Mode 4	Mode 5	Mode 6*1	Mode 7*1
Port G	• 5-bit I/O port • Schmitt-triggered input ($\overline{IRQ7}$, $\overline{IRQ6}$)	PG4/$\overline{CS0}$	When DDR = 0*2: input port When DDR = 1*3: $\overline{CS0}$ output			I/O port also functions as interrupt input pins ($\overline{IRQ7}$, $\overline{IRQ6}$) and A/D converter input pin ($\overline{ADTRG}$)
		PG3/$\overline{CS1}$/$\overline{CS7}$	I/O port When DDR = 1, CS167E = 1, and CSS17 = 0: Also functions as $\overline{CS1}$ output When DDR = 1, CS167E = 1, and CSS17 = 1: Also functions as $\overline{CS7}$ output			
		PG2/$\overline{CS2}$	I/O port When DDR = 1 and CS25E = 1: Also functions as $\overline{CS2}$ output			
		PG1/$\overline{CS3}$/ $\overline{IRQ7}$/$\overline{CS6}$	I/O port When DDR = 1, CS25E = 1, and CSS36 = 0: Also functions as $\overline{CS3}$ output When DDR = 1, CSS36 = 1, and CS167E = 1: Also functions as $\overline{CS6}$ output and interrupt input pin ($\overline{IRQ7}$)			
		PG0/$\overline{IRQ6}$/ $\overline{ADTRG}$	I/O port also functioning as interrupt input pin ($\overline{IRQ6}$) and A/D converter input pin ($\overline{ADTRG}$)			

Notes: 1. Modes 6 and 7 are not available on the ROMless version.
2. After a reset in mode 6
3. After a reset in mode 4 or 5

5.2 Port 1

5.2.1 Overview

Port 1 is an 8-bit I/O port. Port 1 pins also function as TPU I/O pins (TCLKA, TCLKB, TCLKC, TCLKD, TIOCA0, TIOCB0, TIOCC0, TIOCD0, TIOCA1, TIOCB1, TIOCA2, and TIOCB2) and an address bus output function. Port 1 pin functions change according to the operating mode. The address output or port output function is selected according to the settings of bits A23E to A20E in PFCR1. Port 1 pins have Schmitt-trigger inputs.

Figure 5.1 shows the port 1 pin configuration.

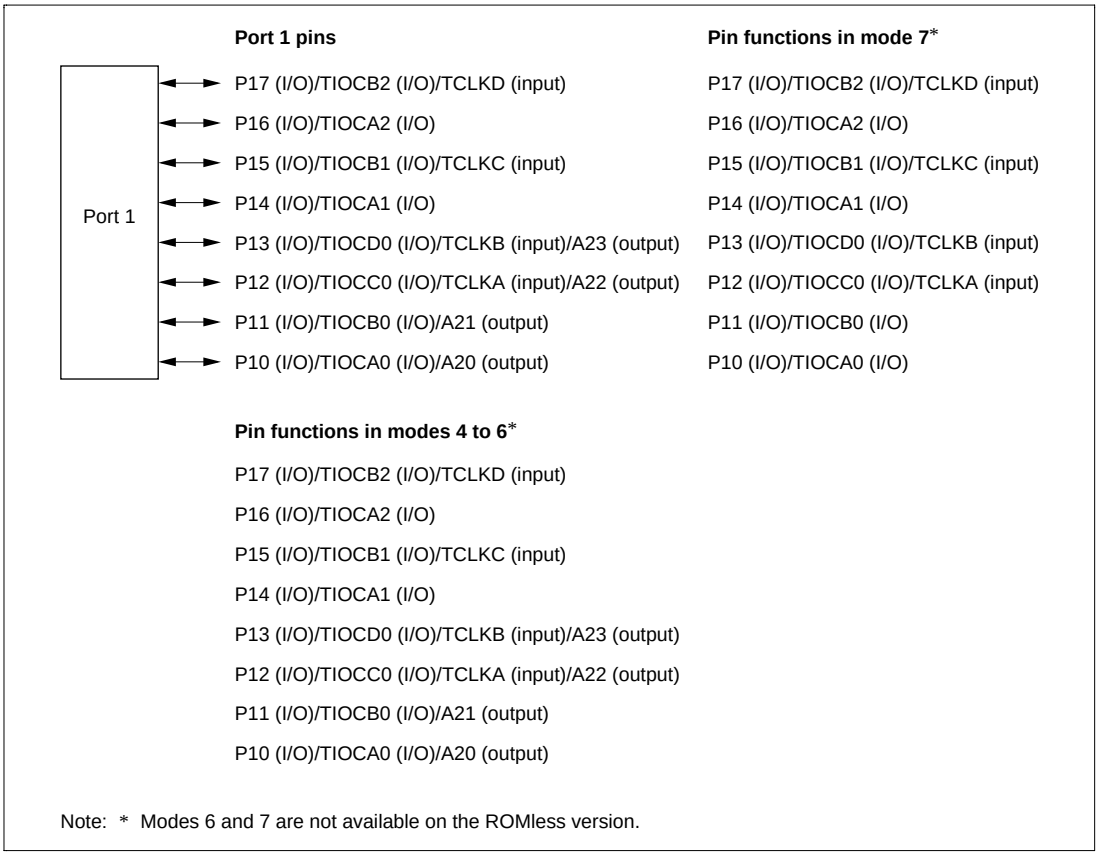


Figure 5.1 Port 1 Pin Functions

5.2.2 Register Configuration

Table 5.2 shows the port 1 register configuration.

Table 5.2 Port 1 Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port 1 data direction register	P1DDR	W	H'00	H'FEB0
Port 1 data register	P1DR	R/W	H'00	H'FF60
Port 1 register	PORT1	R	Undefined	H'FF50
Port function control register 1	PFCR1	R/W	H'0F	H'FF45

Note: * Lower 16 bits of the address.

Port 1 Data Direction Register (P1DDR)

Bit	:	7	6	5	4	3	2	1	0
		P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

P1DDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port 1. P1DDR cannot be read; if it is, an undefined value will be read.

Setting a P1DDR bit to 1 makes the corresponding port 1 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P1DDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state after in software standby mode.

Whether the address output pins maintain their output state or go to the high-impedance state in a transition to software standby mode is selected by the OPE bit in SBYCR.

Port 1 Data Register (P1DR)

Bit	:	7	6	5	4	3	2	1	0
		P17DR	P16DR	P15DR	P14DR	P13DR	P12DR	P11DR	P10DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P1DR is an 8-bit readable/writable register that stores output data for the port 1 pins (P17 to P10).

P1DR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state after in software standby mode.

Port 1 Register (PORT1)

Bit	:	7	6	5	4	3	2	1	0
		P17	P16	P15	P14	P13	P12	P11	P10
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins P17 to P10.

PORT1 is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port 1 pins (P17 to P10) must always be performed on P1DR.

If a port 1 read is performed while P1DDR bits are set to 1, the P1DR values are read. If a port 1 read is performed while P1DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT1 contents are determined by the pin states, as P1DDR and P1DR are initialized. PORT1 retains its prior state after in software standby mode.

Port Function Control Register 1 (PFCR1)

Bit	:	7	6	5	4	3	2	1	0
		CSS17	CSS36	PF1CS5S	PF0CS4S	A23E	A22E	A21E	A20E
Initial value	:	0	0	0	0	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PFCR1 is an 8-bit readable/writable register that performs I/O port control. PFCR1 is initialized to H'0F by a reset, and in hardware standby mode.

Bit 7—CS17 Select (CSS17): Selects whether $\overline{CS1}$ or $\overline{CS7}$ is output from the PG3 pin. For details see section 5.12 port G.

Bit 6—CS36 Select (CSS36): Selects whether $\overline{CS3}$ or $\overline{CS6}$ is output from the PG1 pin. For details, see section 5.12 port G.

Bit 5—Port F1 Chip Select 5 Select (PF1CS5S): Selects enabling or disabling of $\overline{CS5}$ output. For details, see section 5.11 port F.

Bit 4—Port F0 Chip Select 4 Select (PF0CS4S): Selects enabling or disabling of $\overline{CS4}$ output. For details, see section 5.11 port F.

Bit 3—Address 23 Enable (A23E): Enables or disables address output 23 (A23). This bit is valid in modes 4 to 6.

Bit 3 A23E	Description	
0	P13DR is output when P13DDR = 1	
1	A23 is output when P13DDR = 1	(Initial value)

Bit 2—Address 22 Enable (A22E): Enables or disables address output 22 (A22). This bit is valid in modes 4 to 6.

Bit 2 A22E	Description	
0	P12DR is output when P12DDR = 1	
1	A22 is output when P12DDR = 1	(Initial value)

Bit 1—Address 21 Enable (A21E): Enables or disables address output 21 (A21). This bit is valid in modes 4 to 6.

Bit 1 A21E	Description	
0	P11DR is output when P11DDR = 1	
1	A21 is output when P11DDR = 1	(Initial value)

Bit 0—Address 20 Enable (A20E): Enables or disables address output 20 (A20). This bit is valid in modes 4 to 6.

Bit 0 A20E	Description	
0	P10DR is output when P10DDR = 1	
1	A20 is output when P10DDR = 1	(Initial value)

5.2.3 Pin Functions

Port 1 pins also function as TPU I/O pins (TCLKA, TCLKB, TCLKC, TCLKD, TIOCA0, TIOCB0, TIOCC0, TIOCD0, TIOCA1, TIOCB1, TIOCA2, and TIOCB2) and address output pins (A23 to A20). Port 1 pin functions are shown in table 5.3.

Table 5.3 Port 1 Pin Functions

Pin	Selection Method and Pin Functions
P17/TIOCB2/ TCLKD	The pin function is switched as shown below according to the combination of the TPU channel 2 setting by bits MD3 to MD0 in TMDR2, bits IOB3 to IOB0 in TIOR2, bits CCLR1 and CCLR0 in TCR2, bits TPSC2 to TPSC0 in TCR0 and TCR5, and bit P17DDR.

TPU Channel 2 Setting	Table Below (1)	Table Below (2)	
P17DDR	—	0	1
Pin function	TIOCB2 output	P17 input	P17 output
		TIOCB2 input *1	
	TCLKD input *2		

TPU Channel 2 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Notes: 1. TIOCB2 input when MD3 to MD0 = B'0000 or B'01xx and IOB3 = 1.

2. TCLKD input when the setting for either TCR0 or TCR5 is: TPSC2 to TPSC0 = B'111.
TCLKD input when channels 2 and 4 are set to phase counting mode (MD3 to MD0 = B'01xx).

Pin	Selection Method and Pin Functions
P16/TIOCA2	The pin function is switched as shown below according to the combination of the TPU channel 2 setting by bits MD3 to MD0 in TMDR2, bits IOA3 to IOA0 in TIOR2, bits CCLR1 and CCLR0 in TCR2, and bit P16DDR.

TPU Channel 2 Setting	Table Below (1)	Table Below (2)	
P16DDR	—	0	1
Pin function	TIOCA2 output	P16 input	P16 output
		TIOCA2 input *1	

TPU Channel 2 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'001x	B'0011	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output function	—	Output compare output	—	PWM mode 1 output *2	PWM mode 2 output	—

x: Don't care

Notes: 1. TIOCA2 input when MD3 to MD0 = B'0000 or B'01xx and IOA3 = 1.
2. TIOCB2 output is disabled.

Pin	Selection Method and Pin Functions
P15/TIOCB1/ TCLKC	The pin function is switched as shown below according to the combination of the TPU channel 1 setting by bits MD3 to MD0 in TMDR1, bits IOB3 to IOB0 in TIOR1, bits CCLR1 and CCLR0 in TCR1, bits TPSC2 to TPSC0 in TCR0, TCR2, TCR4, and TCR5, and bit P15DDR.

TPU Channel 1 Setting	Table Below (1)	Table Below (2)	
P15DDR	—	0	1
Pin function	TIOCB1 output	P15 input	P15 output
		TIOCB1 input *1	
	TCLKC input *2		

TPU Channel 1 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Notes: 1. TIOCB1 input when MD3 to MD0 = B'0000 or B'01xx and IOB3 to IOB0 = B'10xx.

2. TCLKC input when the setting for either TCR0 or TCR2 is: TPSC2 to TPSC0 = B'110; or when the setting for either TCR4 or TCR5 is TPSC2 to TPSC0 = B'101.
TCLKC input when channels 2 and 4 are set to phase counting mode (MD3 to MD0 = B'01xx).

Pin	Selection Method and Pin Functions
P14/TIOCA1	The pin function is switched as shown below according to the combination of the TPU channel 1 setting by bits MD3 to MD0 in TMDR1, bits IOA3 to IOA0 in TIOR1, bits CCLR1 and CCLR0 in TCR1, and bit P14DDR.

TPU Channel 1 Setting	Table Below (1)	Table Below (2)	
P14DDR	—	0	1
Pin function	TIOCA1 output	P14 input	P14 output
		TIOCA1 input *[1]	

TPU Channel 1 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output function	—	Output compare output	—	PWM mode 1 output*[2]	PWM mode 2 output	—

x: Don't care

Notes: 1. TIOCA1 input when MD3 to MD0 = B'0000 or B'01xx and IOA3 to IOA0 = B'10xx.
2. TIOCB1 output is disabled.

Pin	Selection Method and Pin Functions
P13/TIOCD0/ TCLKB/A23	The pin function is switched as shown below according to the combination of the operating mode, TPU channel 0 setting (by bits MD3 to MD0 in TMDR0, bits IOD3 to IOD0 in TIOR0L, and bits CCLR2 to CCLR0 in TCR0), bits TPSC2 to TPSC0 in TCR0 to TCR2, bit A23E in PFCR1, and bit P13DDR.

Operating Mode	Mode 7*[1]			Modes 4, 5, 6*[1]					
TPU Channel 0 Setting	Table Below (1)	Table Below (2)		Table Below (1)			Table Below (2)		
P13DDR	—	0	1	0	1		0	1	
A23E	—	—	—	—	0	1	—	0	1
Pin function	TIOCD0 output	P13 input	P13 output	TIOCD0 output	TIOCD0 output	A23 output	P13 input	P13 output	A23 output
		TIOCD0 input*[2]					TIOCD0 input*[2]		
	TCLKB input*[3]								

TPU Channel 0 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOD3 to IOD0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'110	B'110
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Notes: 1. Modes 6 and 7 are not available on the ROMless version.

2. TIOCD0 input when MD3 to MD0 = B'0000 and IOD3 to IOD0 = B'10xx.

3. TCLKB input when the TCR0, TCR1, or TCR2 setting is: TPSC2 to TPSC0 = B'101.

   TCLKB input when channels 1 and 5 are set to phase counting mode (MD3 to MD0 = B'01xx).

Pin	Selection Method and Pin Functions
P12/TIOCC0/ TCLKA/A22	The pin function is switched as shown below according to the combination of the operating mode, TPU channel 0 setting (by bits MD3 to MD0 in TMDR0, bits IOC3 to IOC0 in TIOR0L, and bits CCLR2 to CCLR0 in TCR0), bits TPSC2 to TPSC0 in TCR0 to TCR5, bit A22E in PFCR1 and bit P12DDR.

Operating Mode	Mode 7*[1]			Modes 4, 5, 6*[1]					
TPU Channel 0 Setting	Table Below (1)	Table Below (2)		Table Below (1)			Table Below (2)		
P12DDR	—	0	1	0	1		0	1	
A22E	—	—	—	—	0	1	—	0	1
Pin function	TIOCC0 output	P12 input	P12 output	TIOCC0 output	TIOCC0 output	A22 output	P12 input	P12 output	A22 output
		TIOCC0 input*[2]					TIOCC0 input*[2]		
	TCLKA input*[3]								

TPU Channel 0 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000		B'001x	B'0010	B'0011	
IOC3 to IOC0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR2 to CCLR0	—	—	—	—	Other than B'101	B'101
Output function	—	Output compare output	—	PWM mode 1 output*[4]	PWM mode 2 output	—

x: Don't care

Notes: 1. Modes 6 and 7 are not available on the ROMless version.

2. TIOCC0 input when MD3 to MD0 = B'0000 and IOC3 to IOC0 = B'10xx.

3. TCLKA input when the TCR0 to TCR5 setting is: TPSC2 to TPSC0 = B'100.
   TCLKA input when channel 1 and 5 are set to phase counting mode (MD3 to MD0 = B'01xx).

4. TIOCD0 output is disabled.
   When BFA = 1 or BFB = 1 in TMDR0, output is disabled and setting (2) applies.

Pin	Selection Method and Pin Functions
P11/TIOCB0/ A21	The pin function is switched as shown below according to the combination of the operating mode, TPU channel 0 setting (by bits MD3 to MD0 in TMDR0, bits IOB3 to IOB0 in TIOR0H, and bits CCLR2 to CCLR0 in TCR0), bit A21E in PFCR1 and bit P11DDR.

Operating Mode	Mode 7*[1]			Modes 4, 5, 6*[1]					
TPU Channel 0 Setting	Table Below (1)	Table Below (2)		Table Below (1)			Table Below (2)		
P11DDR	—	0	1	0	1		0	1	
A21E	—	—	—	—	0	1	—	0	1
Pin function	TIOCB0 output	P11 input	P11 output	TIOCB0 output	TIOCB0 output	A21 output	P11 input	P11 output	A21 output
		TIOCB0 input*[2]					TIOCB0 input*[2]		
	TCLKB input*[3]								

TPU Channel 0 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'010	B'010
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Notes: 1. Modes 6 and 7 are not available on the ROMless version.
2. TIOCB0 input when MD3 to MD0 = B'0000 and IOB3 to IOB0 = B'10xx.

Pin	Selection Method and Pin Functions
P10/TIOCA0/ A20	The pin function is switched as shown below according to the combination of the operating mode, TPU channel 0 setting (by bits MD3 to MD0 in TMDR0, bits IOA3 to IOA0 in TIOR0H, and bits CCLR2 to CCLR0 in TCR0), bit A20E in PFCR1 and bit P10DDR.

Operating Mode	Mode 7*1			Modes 4, 5, 6*1					
TPU Channel 0 Setting	Table Below (1)	Table Below (2)		Table Below (1)			Table Below (2)		
P10DDR	—	0	1	0	1		0	1	
A20E	—	—	—	—	0	1	—	0	1
Pin function	TIOCA0 output	P10 input	P10 output	TIOCA0 output	TIOCA0 output	A20 output	P10 input	P10 output	A20 output
		TIOCA0 input*2					TIOCA0 input*2		

TPU Channel 0 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR2 to CCLR0	—	—	—	—	Other than B'001	B'001
Output function	—	Output compare output	—	PWM mode 1 output*3	PWM mode 2 output	—

x: Don't care

Notes: 1. Modes 6 and 7 are not available on the ROMless version.
2. TIOCA0 input when MD3 to MD0 = B'0000 and IOA3 to IOA0 = B'10xx.
3. TIOCB0 output is disabled.

5.3 Port 2

5.3.1 Overview

Port 2 is an 8-bit I/O port. Port 2 pins also function as TPU I/O pins (TIOCA3, TIOCB3, TIOCC3, TIOCD3, TIOCA4, TIOCB4, TIOCA5, and TIOCB5), and 8-bit timer I/O pins (TMRI0, TMCI0, TMO0, TMRI1, TMCI1, and TMO1). Port 2 pin functions are the same in all operating modes. Port 2 uses Schmitt-triggered input.

Figure 5.2 shows the port 2 pin configuration.

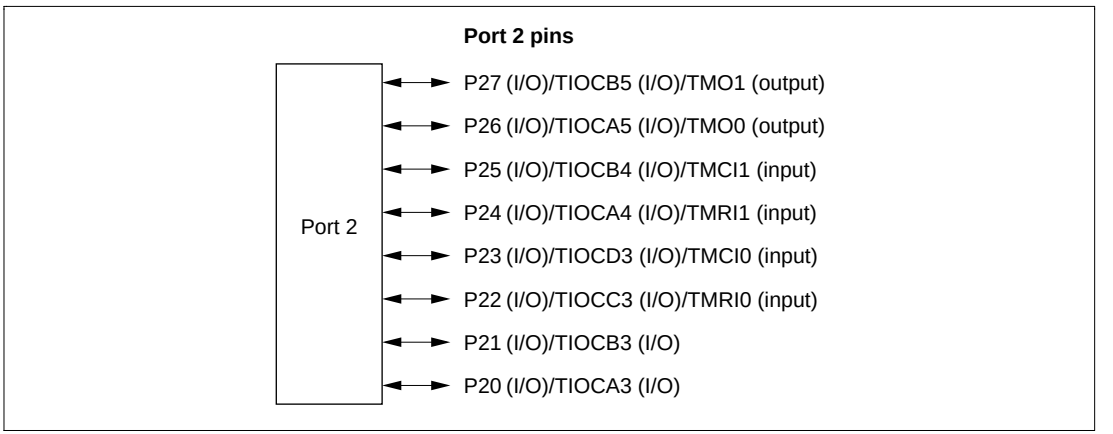


Figure 5.2 Port 2 Pin Functions

5.3.2 Register Configuration

Table 5.4 shows the port 2 register configuration.

Table 5.4 Port 2 Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port 2 data direction register	P2DDR	W	H'00	H'FEB1
Port 2 data register	P2DR	R/W	H'00	H'FF61
Port 2 register	PORT2	R	Undefined	H'FF51

Note: * Lower 16 bits of the address.

Port 2 Data Direction Register (P2DDR)

Bit	:	7	6	5	4	3	2	1	0
		P27DDR	P26DDR	P25DDR	P24DDR	P23DDR	P22DDR	P21DDR	P20DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

P2DDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port 2. P2DDR cannot be read; if it is, an undefined value will be read.

Setting a P2DDR bit to 1 makes the corresponding port 2 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P2DDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state after in software standby mode.

Port 2 Data Register (P2DR)

Bit	:	7	6	5	4	3	2	1	0
		P27DR	P26DR	P25DR	P24DR	P23DR	P22DR	P21DR	P20DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P2DR is an 8-bit readable/writable register that stores output data for the port 2 pins (P27 to P20).

P2DR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state after in software standby mode.

Port 2 Register (PORT2)

Bit	:	7	6	5	4	3	2	1	0
		P27	P26	P25	P24	P23	P22	P21	P20
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins P27 to P20.

PORT2 is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port 2 pins (P27 to P20) must always be performed on P2DR.

If a port 2 read is performed while P2DDR bits are set to 1, the P2DR values are read. If a port 2 read is performed while P2DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT2 contents are determined by the pin states, as P2DDR and P2DR are initialized. PORT2 retains its prior state after in software standby mode.

5.3.3 Pin Functions

Port 2 pins also function as TPU I/O pins (TIOCA3, TIOCB3, TIOCC3, TIOCD3, TIOCA4, TIOCB4, TIOCA5, and TIOCB5), and 8-bit timer I/O pins (TMRI0, TMCI0, TMO0, TMRI1, TMCI1, and TMO1). Port 2 pin functions are shown in table 5.5.

Table 5.5 Port 2 Pin Functions

Pin | **Selection Method and Pin Functions**

P27/TIOCB5/ TMO1

The pin function is switched as shown below according to the combination of the TPU channel 5 setting by bits MD3 to MD0 in TMDR5, bits IOB3 to IOB0 in TIOR5, bits CCLR1 and CCLR0 in TCR5, bits OS3 to OS0 in TCSR1, and bit P27DDR.

OS3 to OS0	All 0			Any 1
TPU Channel 5 Setting	Table Below (1)	Table Below (2)		—
P27DDR	—	0	1	—
Pin function	TIOCB5 output	P27 input	P27 output	TMO1 output
		TIOCB5 input *		

TPU Channel 5 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Note: * TIOCB5 input when MD3 to MD0 = B'0000 or B'01xx and IOB3 = 1.

Pin	Selection Method and Pin Functions
P26/TIOCA5/ TMO0	The pin function is switched as shown below according to the combination of the TPU channel 5 setting by bits MD3 to MD0 in TMDR5, bits IOA3 to IOA0 in TIOR5, bits CCLR1 and CCLR0 in TCR5, bits OS3 to OS0 in TCSR0, and bit P26DDR.

OS3 to OS0	All 0			Any 1
TPU Channel 5 Setting	Table Below (1)	Table Below (2)		—
P26DDR	—	0	1	—
Pin function	TIOCA5 output	P26 input	P26 output	TMO0 output
		TIOCA5 input *1		

TPU Channel 5 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output function	—	Output compare output	—	PWM mode 1 output*2	PWM mode 2 output	—

x: Don't care

Notes: 1. TIOCA5 input when MD3 to MD0 = B'0000 or B'01xx and IOA3 = 1.
2. TIOCB5 output is disabled.

Pin	Selection Method and Pin Functions
P25/TIOCB4/ TMCI1	This pin is used as the 8-bit timer external clock input pin when external clock is selected with bits CKS2 to CKS0 in TCR1. The pin function is switched as shown below according to the combination of the TPU channel 4 setting by bits MD3 to MD0 in TMDR4 and bits IOB3 to IOB0 in TIOR4, bits CCLR1 and CCLR0 in TCR4, and bit P25DDR.

TPU Channel 4 Setting	Table Below (1)	Table Below (2)	
P25DDR	—	0	1
Pin function	TIOCB4 output	P25 input	P25 output
		TIOCB4 input *	
	TMCI1 input		

TPU Channel 4 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Note: * TIOCB4 input when MD3 to MD0 = B'0000 or B'10xx and IOB3 to IOB0 = B'10xx.

Pin	Selection Method and Pin Functions
P24/TIOCA4/ TMRI1	This pin is used as the 8-bit timer counter reset pin when bits CCLR1 and CCLR0 in TCR1 are both set to 1. The pin function is switched as shown below according to the combination of the TPU channel 4 setting by bits MD3 to MD0 in TMDR4, bits IOA3 to IOA0 in TIOR4, bits CCLR1 and CCLR0 in TCR4, and bit P24DDR.

TPU Channel 4 Setting	Table Below (1)	Table Below (2)	
P24DDR	—	0	1
Pin function	TIOCA4 output	P24 input	P24 output
		TIOCA4 input *1	
	TMRI1 input		

TPU Channel 4 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output function	—	Output compare output	—	PWM mode 1 output*2	PWM mode 2 output	—

x: Don't care

Notes: 1. TIOCA4 input when MD3 to MD0 = B'0000 or B'01xx and IOA3 to IOA0 = B'10xx.
2. TIOCB4 output is disabled.

Pin	Selection Method and Pin Functions
P23/TIOCD3/ TMCI0	This pin is used as the 8-bit timer external clock input pin when external clock is selected with bits CKS2 to CKS0 in TCR0. The pin function is switched as shown below according to the combination of the TPU channel 3 setting by bits MD3 to MD0 in TMDR3, bits IOD3 to IOD0 in TIOR3L, bits CCLR2 to CCLR0 in TCR3, and bit P23DDR.

TPU Channel 3 Setting	Table Below (1)	Table Below (2)	
P23DDR	—	0	1
Pin function	TIOCD3 output	P23 input	P23 output
		TIOCD3 input *	
	TMCI0 input		

TPU Channel 3 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOD3 to IOD0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'110	B'110
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Note: * TIOCD3 input when MD3 to MD0 = B'0000 and IOD3 to IOD0 = B'10xx.

Pin	Selection Method and Pin Functions
P22/TIOCC3/ TMRI0	This pin is used as the 8-bit timer counter reset pin when bits CCLR1 and CCLR0 in TCR0 are both set to 1. The pin function is switched as shown below according to the combination of the TPU channel 3 setting by bits MD3 to MD0 in TMDR3, bits IOC3 to IOC0 in TIOR3L, bits CCLR2 to CCLR0 in TCR3, and bit P22DDR.

TPU Channel 3 Setting	Table Below (1)	Table Below (2)	
P22DDR	—	0	1
Pin function	TIOCC3 output	P22 input	P22 output
		TIOCC3 input *1	
	TMRI0 input		

TPU Channel 3 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000		B'001x	B'0010	B'0011	
IOC3 to IOC0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR2 to CCLR0	—	—	—	—	Other than B'101	B'101
Output function	—	Output compare output	—	PWM mode 1 output*2	PWM mode 2 output	—

x: Don't care

Notes: 1. TIOCC3 input when MD3 to MD0 = B'0000 and IOC3 to IOC0 = B'10xx.

2. TIOCD3 output is disabled.
When BFA = 1 or BFB = 1 in TMDR3, output is disabled and setting (2) applies.

Pin	Selection Method and Pin Functions
P21/TIOCB3	The pin function is switched as shown below according to the combination of the TPU channel 3 setting by bits MD3 to MD0 in TMDR3, bits IOB3 to IOB0 in TIOR3H, bits CCLR2 to CCLR0 in TCR3, and bit P21DDR.

TPU Channel 3 Setting	Table Below (1)	Table Below (2)	
P21DDR	—	0	1
Pin function	TIOCB3 output	P21 input	P21 output
		TIOCB3 input *	

TPU Channel 3 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'010	B'010
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Note: * TIOCB3 input when MD3 to MD0 = B'0000 and IOB3 to IOB0 = B'10xx.

Pin	Selection Method and Pin Functions
P20/TIOCA3	The pin function is switched as shown below according to the combination of the TPU channel 3 setting by bits MD3 to MD0 in TMDR3, bits IOA3 to IOA0 in TIOR3H, bits CCLR2 to CCLR0 in TCR3, and bit P20DDR.

TPU Channel 3 Setting	Table Below (1)	Table Below (2)	
P20DDR	—	0	1
Pin function	TIOCA3 output	P20 input	P20 output
		TIOCA3 input *[1]	

TPU Channel 3 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR2 to CCLR0	—	—	—	—	Other than B'001	B'001
Output function	—	Output compare output	—	PWM mode 1 output*[2]	PWM mode 2 output	—

x: Don't care

Notes: 1. TIOCA3 input when MD3 to MD0 = B'0000 and IOA3 to IOA0 = B'10xx.

2. TIOCB3 output is disabled.

5.4 Port 3

5.4.1 Overview

Port 3 is a 6-bit I/O port. Port 3 pins also function as SCI I/O pins (TxD0, RxD0, SCK0, TxD1, RxD1, and SCK1) and interrupt input pins ($\overline{IRQ4}$, $\overline{IRQ5}$). Port 3 pin functions are the same in all operating modes. The interrupt input pins ($\overline{IRQ4}$, $\overline{IRQ5}$) are Schmitt-triggered inputs.

Figure 5.3 shows the port 3 pin configuration.

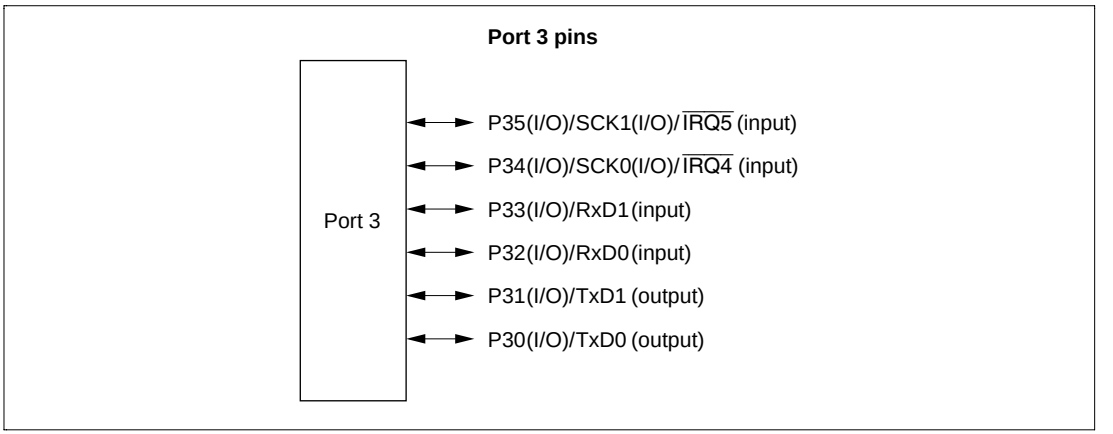


Figure 5.3 Port 3 Pin Functions

5.4.2 Register Configuration

Table 5.6 shows the port 3 register configuration.

Table 5.6 Port 3 Registers

Name	Abbreviation	R/W	Initial Value*1	Address*2
Port 3 data direction register	P3DDR	W	H'00	H'FEB2
Port 3 data register	P3DR	R/W	H'00	H'FF62
Port 3 register	PORT3	R	Undefined	H'FF52
Port 3 open drain control register	P3ODR	R/W	H'00	H'FF76

Notes: 1. Value of bits 5 to 0.
2. Lower 16 bits of the address.

Port 3 Data Direction Register (P3DDR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	P35DDR	P34DDR	P33DDR	P32DDR	P31DDR	P30DDR
Initial value	:	Undefined	Undefined	0	0	0	0	0	0
R/W	:	—	—	W	W	W	W	W	W

P3DDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port 3. Bits 7 and 6 are reserved. P3DDR cannot be read; if it is, an undefined value will be read.

Setting a P3DDR bit to 1 makes the corresponding port 3 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P3DDR is initialized to H'00 (bits 5 to 0) by a reset, and in hardware standby mode. It retains its prior state after in software standby mode. As the SCI is initialized, the pin states are determined by the P3DDR and P3DR specifications.

Port 3 Data Register (P3DR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	P35DR	P34DR	P33DR	P32DR	P31DR	P30DR
Initial value	:	Undefined	Undefined	0	0	0	0	0	0
R/W	:	—	—	R/W	R/W	R/W	R/W	R/W	R/W

P3DR is an 8-bit readable/writable register that stores output data for the port 3 pins (P35 to P30).

Bits 7 and 6 are reserved; they return an undetermined value if read, and cannot be modified.

P3DR is initialized to H'00 (bits 5 to 0) by a on reset, and in hardware standby mode. It retains its prior state after in software standby mode.

Port 3 Register (PORT3)

Bit	7	6	5	4	3	2	1	0
	—	—	P35	P34	P33	P32	P31	P30
Initial value	Undefined	Undefined	—*	—*	—*	—*	—*	—*
R/W	—	—	R	R	R	R	R	R

Note: * Determined by state of pins P35 to P30.

PORT3 is an 8-bit read-only register that shows the pin states, and cannot be modified. Writing of output data for the port 3 pins (P35 to P30) must always be performed on P3DR.

Bits 7 and 6 are reserved; they return an undetermined value if read, and cannot be modified.

If a port 3 read is performed while P3DDR bits are set to 1, the P3DR values are read. If a port 3 read is performed while P3DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT3 contents are determined by the pin states, as P3DDR and P3DR are initialized. PORT3 retains its prior state after in software standby mode.

Port 3 Open Drain Control Register (P3ODR)

Bit	7	6	5	4	3	2	1	0
	—	—	P35ODR	P34ODR	P33ODR	P32ODR	P31ODR	P30ODR
Initial value	Undefined	Undefined	0	0	0	0	0	0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W

P3ODR is an 8-bit readable/writable register that controls the PMOS on/off status for each port 3 pin (P35 to P30).

Bits 7 and 6 are reserved; they return an undetermined value if read, and cannot be modified.

Setting a P3ODR bit to 1 makes the corresponding port 3 pin an NMOS open-drain output pin, while clearing the bit to 0 makes the pin a CMOS output pin.

P3ODR is initialized to H'00 (bits 5 to 0) by a reset, and in hardware standby mode. It retains its prior state after in software standby mode.

5.4.3 Pin Functions

Port 3 pins also function as SCI I/O pins (TxD0, RxD0, SCK0, TxD1, RxD1, and SCK1) and interrupt input pins ($\overline{IRQ4}$, $\overline{IRQ5}$). Port 3 pin functions are shown in table 5.7.

Table 5.7 Port 3 Pin Functions

Pin | **Selection Method and Pin Functions**

P35/SCK1/$\overline{IRQ5}$

The pin function is switched as shown below according to the combination of bit C/$\overline{A}$ in the SCI1 SMR, bits CKE0 and CKE1 in SCR, and bit P35DDR.

CKE1	0				1
C/$\overline{A}$	0			1	—
CKE0	0		1	—	—
P35DDR	0	1	—	—	—
Pin function	P35 input pin	P35 output pin*[1]	SCK1 output pin*[1]	SCK1 output pin*[1]	SCK1 input pin
	$\overline{IRQ5}$ interrupt input pin*[2]				

Notes: 1. When P35ODR = 1, the pin becomes an NMOS open-drain output.
2. When this pin is used as an external interrupt input, it should not be used as an input/output pin with other functions.

P34/SCK0/$\overline{IRQ4}$

The pin function is switched as shown below according to the combination of bit C/$\overline{A}$ in the SCI0 SMR, bits CKE0 and CKE1 in SCR, and bit P34DDR.

CKE1	0				1
C/$\overline{A}$	0			1	—
CKE0	0		1	—	—
P34DDR	0	1	—	—	—
Pin function	P34 input pin	P34 output pin*[1]	SCK0 output pin*[1]	SCK0 output pin*[1]	SCK0 input pin
	$\overline{IRQ4}$ interrupt input pin*[2]				

Notes: 1. When P34ODR = 1, the pin becomes an NMOS open-drain output.
2. When this pin is used as an external interrupt input, it should not be used as an input/output pin with other functions.

Pin	Selection Method and Pin Functions
P33/RxD1	The pin function is switched as shown below according to the combination of bit RE in the SCI1 SCR, and bit P33DDR.

RE	0		1
P33DDR	0	1	—
Pin function	P33 input pin	P33 output pin*	RxD1 input pin

Note: * When P33ODR = 1, the pin becomes an NMOS open-drain output.

P32/RxD0 — The pin function is switched as shown below according to the combination of bit RE in the SCI0 SCR, and bit P32DDR.

RE	0		1
P32DDR	0	1	—
Pin function	P32 input pin	P32 output pin*	RxD0 input pin

Note: * When P32ODR = 1, the pin becomes an NMOS open-drain output.

P31/TxD1 — The pin function is switched as shown below according to the combination of bit TE in the SCI1 SCR, and bit P31DDR.

TE	0		1
P31DDR	0	1	—
Pin function	P31 input pin	P31 output pin*	TxD1 output pin

Note: * When P31ODR = 1, the pin becomes an NMOS open-drain output.

P30/TxD0 — The pin function is switched as shown below according to the combination of bit TE in the SCI0 SCR, and bit P30DDR.

TE	0		1
P30DDR	0	1	—
Pin function	P30 input pin	P30 output pin*	TxD0 output pin

Note: * When P30ODR = 1, the pin becomes an NMOS open-drain output.

5.5 Port 4

5.5.1 Overview

Port 4 is an 8-bit input-only port. Port 4 pins also function as A/D converter analog input pins (AN0 to AN7) and D/A converter analog output pins (DA0 and DA1). Port 4 pin functions are the same in all operating modes. Figure 5.4 shows the port 4 pin configuration.

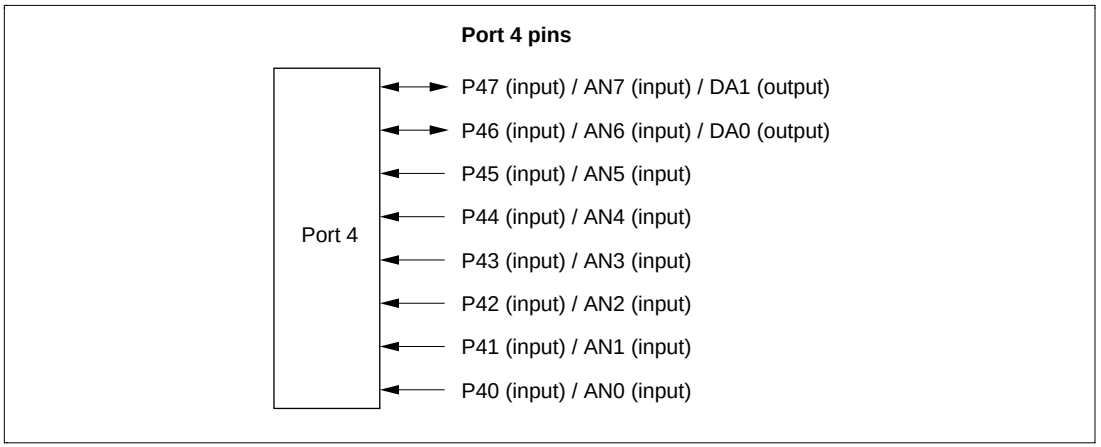


Figure 5.4 Port 4 Pin Functions

5.5.2 Register Configuration

Table 5.8 shows the port 4 register configuration. Port 4 is an input-only port, and does not have a data direction register or data register.

Table 5.8 Port 4 Register

Name	Abbreviation	R/W	Initial Value	Address*
Port 4 register	PORT4	R	Undefined	H'FF53

Note: * Lower 16 bits of the address.

Port 4 Register (PORT4): The pin states are always read when a port 4 read is performed.

Bit	:	7	6	5	4	3	2	1	0
		P47	P46	P45	P44	P43	P42	P41	P40
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins P47 to P40.

5.5.3 Pin Functions

Port 4 pins also function as A/D converter analog input pins (AN0 to AN7) and D/A converter analog output pins (DA0 and DA1).

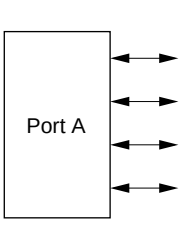
5.6 Port A

5.6.1 Overview

Port A is a 4-bit I/O port. Port A pins also function as address bus outputs. The pin functions change according to the operating mode.

Port A has a built-in MOS input pull-up function that can be controlled by software.

Figure 5.5 shows the port A pin configuration.



Port A pins	Pin functions in modes 4 and 5
PA3/A19	A19 (output)
PA2/A18	A18 (output)
PA1/A17	A17 (output)
PA0/A16	A16 (output)

Pin functions in mode 6*	Pin functions in mode 7*
PA3 (input)/A19 (output)	PA3 (I/O)
PA2 (input)/A18 (output)	PA2 (I/O)
PA1 (input)/A17 (output)	PA1 (I/O)
PA0 (input)/A16 (output)	PA0 (I/O)

Note: * Modes 6 and 7 are not available on the ROMless version.

Figure 5.5 Port A Pin Functions

5.6.2 Register Configuration

Table 5.9 shows the port A register configuration.

Table 5.9 Port A Registers

Name	Abbreviation	R/W	Initial Value*[1]	Address*[2]
Port A data direction register	PADDR	W	H'0	H'FEB9
Port A data register	PADR	R/W	H'0	H'FF69
Port A register	PORTA	R	Undefined	H'FF59
Port A MOS pull-up control register	PAPCR	R/W	H'0	H'FF70
Port A open-drain control register	PAODR	R/W	H'0	H'FF77

Notes: 1. Value of bits 3 to 0.
2. Lower 16 bits of the address.

Port A Data Direction Register (PADDR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PA3DDR	PA2DDR	PA1DDR	PA0DDR
Initial value	Undefined	Undefined	Undefined	Undefined	0	0	0	0
R/W	—	—	—	—	W	W	W	W

PADDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port A. PADDR cannot be read; if it is, an undefined value will be read. Bits 7 to 4 are reserved.

PADDR is initialized to H'0 (bits 3 to 0) by a reset and in hardware standby mode. It retains its prior state after in software standby mode. The OPE bit in SBYCR is used to select whether the address output pins retain their output state or become high-impedance when a transition is made to software standby mode.

- Modes 4 and 5

  The corresponding port A pins are address outputs irrespective of the value of bits PA3DDR to PA0DDR.

- Mode 6*

  Setting a PADDR bit to 1 makes the corresponding port A pin an address output while clearing the bit to 0 makes the pin an input port.

- Mode 7*

  Setting a PADDR bit to 1 makes the corresponding port A pin an output port, while clearing the bit to 0 makes the pin an input port.

Note: * Modes 6 and 7 are not available on the ROMless version.

Port A Data Register (PADR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	PA3DR	PA2DR	PA1DR	PA0DR
Initial value	:	Undefined	Undefined	Undefined	Undefined	0	0	0	0
R/W	:	—	—	—	—	R/W	R/W	R/W	R/W

PADR is an 8-bit readable/writable register that stores output data for the port A pins (PA3 to PA0).

Bits 7 to 4 are reserved; they return an undetermined value if read, and cannot be modified.

PADR is initialized to H'0 (bits 3 to 0) by a reset, and in hardware standby mode. It retains its prior state after in software standby mode.

Port A Register (PORTA)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	PA3	PA2	PA1	PA0
Initial value	:	Undefined	Undefined	Undefined	Undefined	—*	—*	—*	—*
R/W	:	—	—	—	—	R	R	R	R

Note: * Determined by state of pins PA3 to PA0.

PORTA is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port A pins (PA3 to PA0) must always be performed on PADR.

Bits 7 to 4 are reserved; they return an undetermined value if read, and cannot be modified.

If a port A read is performed while PADDR bits are set to 1, the PADR values are read. If a port A read is performed while PADDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTA contents are determined by the pin states, as PADDR and PADR are initialized. PORTA retains its prior state after in software standby mode.

Port A MOS Pull-Up Control Register (PAPCR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	PA3PCR	PA2PCR	PA1PCR	PA0PCR
Initial value	:	Undefined	Undefined	Undefined	Undefined	0	0	0	0
R/W	:	—	—	—	—	R/W	R/W	R/W	R/W

PAPCR is an 8-bit readable/writable register that controls the MOS input pull-up function incorporated into port A on an individual bit basis.

Bits 7 to 4 are reserved; they return an undetermined value if read, and cannot be modified.

Bits 3 to 0 are valid in modes 6 and 7*, and all the bits are invalid in modes 4 and 5. When a PADDR bit is cleared to 0 (input port setting), setting the corresponding PAPCR bit to 1 turns on the MOS input pull-up for the corresponding pin.

PAPCR is initialized to H'0 (bits 3 to 0) by a reset, and in hardware standby mode. It retains its prior state after in software standby mode.

Note: * Modes 6 and 7 are not available on the ROMless version.

Port A Open Drain Control Register (PAODR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	PA3ODR	PA2ODR	PA1ODR	PA0ODR
Initial value	:	Undefined	Undefined	Undefined	Undefined	0	0	0	0
R/W	:	—	—	—	—	R/W	R/W	R/W	R/W

PAODR is an 8-bit readable/writable register that controls whether PMOS is on or off for each port A pin (PA3 to PA0).

Bits 7 to 4 are reserved; they return an undetermined value if read, and cannot be modified.

All bits are valid in mode 7.*

Setting a PAODR bit to 1 makes the corresponding port A pin an NMOS open-drain output, while clearing the bit to 0 makes the pin a CMOS output.

PAODR is initialized to H'0 (bits 3 to 0) by a reset, and in hardware standby mode. It retains its prior state after in software standby mode.

Note: * Modes 6 and 7 are not available on the ROMless version.

5.6.3 Pin Functions

Modes 4 and 5: In modes 4 and 5, the lower 4 bits of port A are designated as address outputs automatically.

Port A pin functions in modes 4 and 5 are shown in figure 5.6.

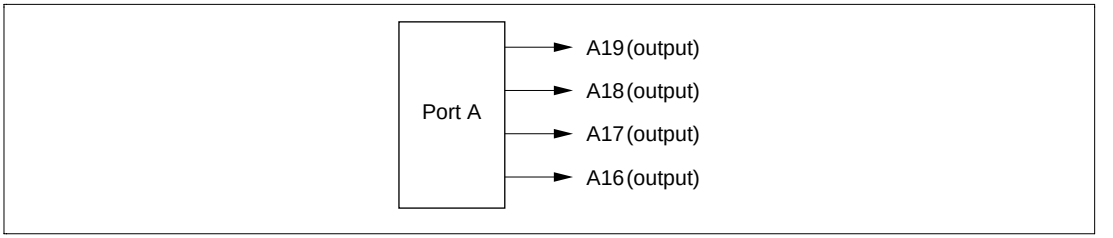


Figure 5.6 Port A Pin Functions (Modes 4 and 5)

Mode 6*: In mode 6*, port A pins function as address outputs or input ports. Input or output can be specified on an individual bit basis. Setting a PADDR bit to 1 makes the corresponding port A pin an address output, while clearing the bit to 0 makes the pin an input port.

Port A pin functions in mode 6 are shown in figure 5.7.

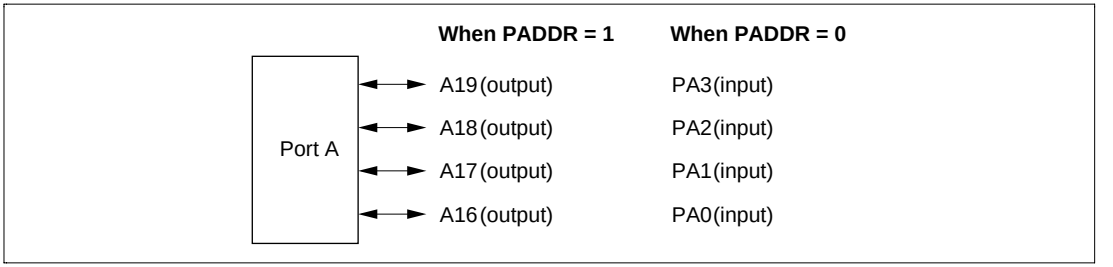


Figure 5.7 Port A Pin Functions (Mode 6)

Mode 7*: In mode 7*, port A pins function as I/O ports. Input or output can be specified for each pin on an individual bit basis. Setting a PADDR bit to 1 makes the corresponding port A pin an output port, while clearing the bit to 0 makes the pin an input port.

Port A pin functions in mode 7 are shown in figure 5.8.

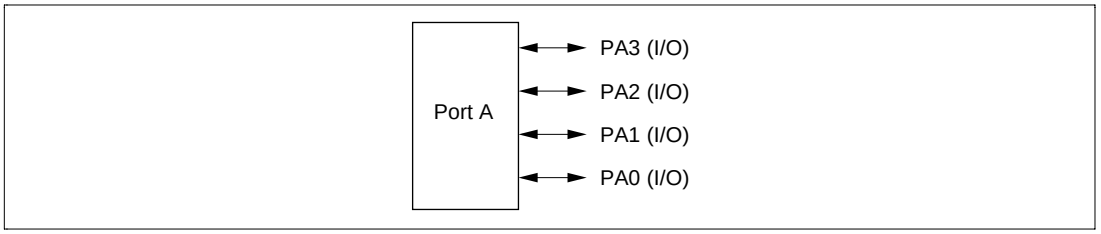


Figure 5.8 Port A Pin Functions (Mode 7)

Note: * Modes 6 and 7 are not available on the ROMless version.

5.6.4 MOS Input Pull-Up Function

Port A has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in modes 6 and 7*, and cannot be used in modes 4 and 5. MOS input pull-up can be specified as on or off on an individual bit basis.

When a PADDR bit is cleared to 0, setting the corresponding PAPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset, and in hardware standby mode. The prior state is retained after in software standby mode.

Table 5.10 summarizes the MOS input pull-up states.

Table 5.10 MOS Input Pull-Up States (Port A)

Modes		Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
6, 7*	PA3 to PA0	OFF	OFF	ON/OFF	ON/OFF
4, 5	PA3 to PA0			OFF	OFF

Legend:
OFF: MOS input pull-up is always off.
ON/OFF: On when PADDR = 0 and PAPCR = 1; otherwise off.

Note: * Modes 6 and 7 are not available on the ROMless version.

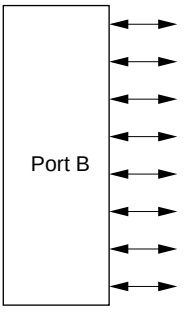
5.7 Port B

5.7.1 Overview

Port B is an 8-bit I/O port. Port B has an address bus output function, and the pin functions change according to the operating mode.

Port B has a built-in MOS input pull-up function that can be controlled by software.

Figure 5.9 shows the port B pin configuration.



Port B pins	Pin functions in modes 4 and 5
PB7 / A15	A15 (output)
PB6 / A14	A14 (output)
PB5 / A13	A13 (output)
PB4 / A12	A12 (output)
PB3 / A11	A11 (output)
PB2 / A10	A10 (output)
PB1 / A9	A9 (output)
PB0 / A8	A8 (output)

Pin functions in mode 6*	Pin functions in mode 7*
PB7 (input) / A15 (output)	PB7 (I/O)
PB6 (input) / A14 (output)	PB6 (I/O)
PB5 (input) / A13 (output)	PB5 (I/O)
PB4 (input) / A12 (output)	PB4 (I/O)
PB3 (input) / A11 (output)	PB3 (I/O)
PB2 (input) / A10 (output)	PB2 (I/O)
PB1 (input) / A9 (output)	PB1 (I/O)
PB0 (input) / A8 (output)	PB0 (I/O)

Note: * Modes 6 and 7 are not available on the ROMless version.

Figure 5.9 Port B Pin Functions

5.7.2 Register Configuration

Table 5.11 shows the port B register configuration.

Table 5.11 Port B Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port B data direction register	PBDDR	W	H'00	H'FEBA
Port B data register	PBDR	R/W	H'00	H'FF6A
Port B register	PORTB	R	Undefined	H'FF5A
Port B MOS pull-up control register	PBPCR	R/W	H'00	H'FF71

Note: * Lower 16 bits of the address.

Port B Data Direction Register (PBDDR)

Bit	:	7	6	5	4	3	2	1	0
		PB7DDR	PB6DDR	PB5DDR	PB4DDR	PB3DDR	PB2DDR	PB1DDR	PB0DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

PBDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port B. PBDDR cannot be read; if it is, an undefined value will be read.

PBDDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode. The OPE bit in SBYCR is used to select whether the address output pins retain their output state or become high-impedance when a transition is made to software standby mode.

- Modes 4 and 5
  The corresponding port B pins are address outputs irrespective of the value of the PBDDR bits.
- Mode 6*
  Setting a PBDDR bit to 1 makes the corresponding port B pin an address output, while clearing the bit to 0 makes the pin an input port.
- Mode 7*
  Setting a PBDDR bit to 1 makes the corresponding port B pin an output port, while clearing the bit to 0 makes the pin an input port.

Note: * Modes 6 and 7 are not available on the ROMless version.

Port B Data Register (PBDR)

Bit	:	7	6	5	4	3	2	1	0
		PB7DR	PB6DR	PB5DR	PB4DR	PB3DR	PB2DR	PB1DR	PB0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PBDR is an 8-bit readable/writable register that stores output data for the port B pins (PB7 to PB0). PBDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port B Register (PORTB)

Bit	:	7	6	5	4	3	2	1	0
		PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins PB7 to PB0.

PORTB is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port B pins (PB7 to PB0) must always be performed on PBDR.

If a port B read is performed while PBDDR bits are set to 1, the PBDR values are read. If a port B read is performed while PBDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTB contents are determined by the pin states, as PBDDR and PBDR are initialized. PORTB retains its prior state in software standby mode.

Port B MOS Pull-Up Control Register (PBPCR)

Bit	:	7	6	5	4	3	2	1	0
		PB7PCR	PB6PCR	PB5PCR	PB4PCR	PB3PCR	PB2PCR	PB1PCR	PB0PCR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PBPCR is an 8-bit readable/writable register that controls the MOS input pull-up function incorporated into port B on an individual bit basis.

When a PBDDR bit is cleared to 0 (input port setting) in mode 6 or 7, setting the corresponding PBPCR bit to 1 turns on the MOS input pull-up for the corresponding pin.

PBPCR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

5.7.3 Pin Functions

Modes 4 and 5: In modes 4 and 5, port B pins are automatically designated as address outputs.

Port B pin functions in modes 4 and 5 are shown in figure 5.10.

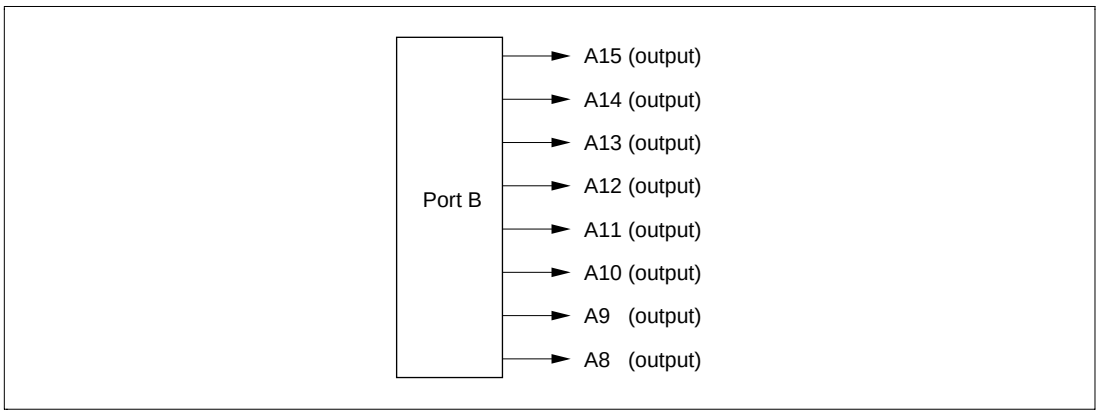


Figure 5.10 Port B Pin Functions (Modes 4 and 5)

Mode 6*: In mode 6, port B pins function as address outputs or input ports. Input or output can be specified on an individual bit basis. Setting a PBDDR bit to 1 makes the corresponding port B pin an address output, while clearing the bit to 0 makes the pin an input port.

Port B pin functions in mode 6 are shown in figure 5.11

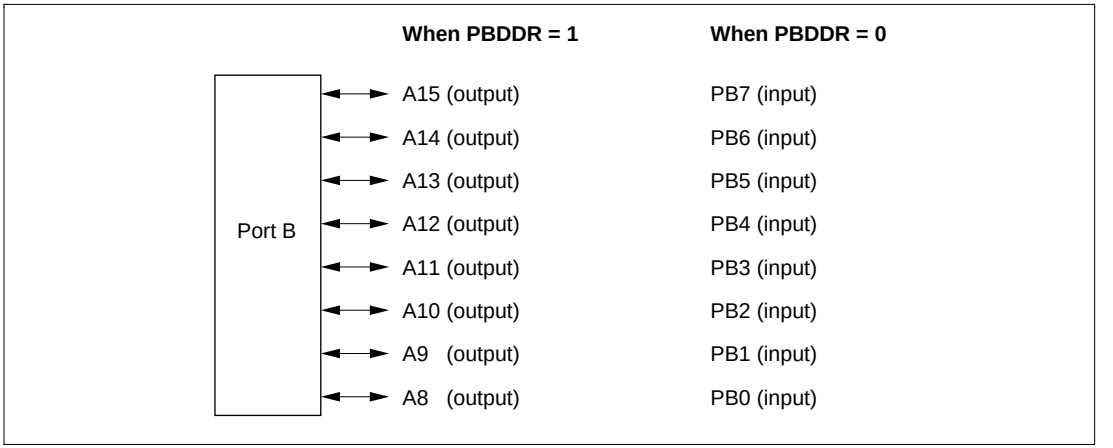


Figure 5.11 Port B Pin Functions (Mode 6)

Mode 7*: In mode 7, port B pins function as I/O ports. Input or output can be specified for each pin on an individual bit basis. Setting a PBDDR bit to 1 makes the corresponding port B pin an output port, while clearing the bit to 0 makes the pin an input port.

Port B pin functions in mode 7 are shown in figure 5.12.

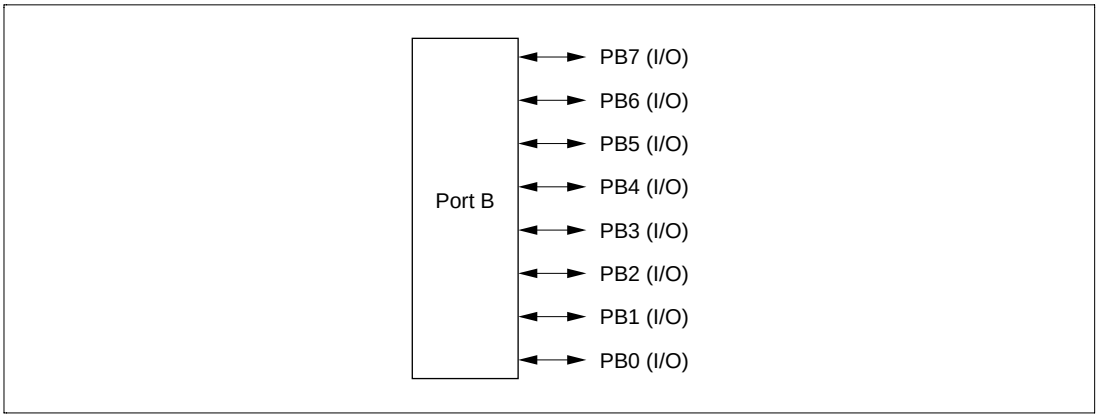


Figure 5.12 Port B Pin Functions (Mode 7)

Note: * Modes 6 and 7 are not available on the ROMless version.

5.7.4 MOS Input Pull-Up Function

Port B has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in modes 6 and 7, and can be specified as on or off on an individual bit basis.

When a PBDDR bit is cleared to 0 in mode 6 or 7, setting the corresponding PBPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset, and in hardware standby mode. The prior state is retained in software standby mode.

Table 5.12 summarizes the MOS input pull-up states.

Table 5.12 MOS Input Pull-Up States (Port B)

Modes	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
4, 5	OFF	OFF	OFF	OFF
6, 7			ON/OFF	ON/OFF

Legend

OFF: MOS input pull-up is always off.

ON/OFF: On when PBDDR = 0 and PBPCR = 1; otherwise off.

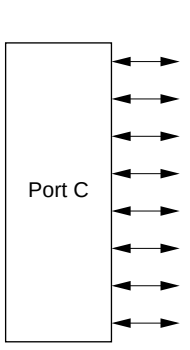
5.8 Port C

5.8.1 Overview

Port C is an 8-bit I/O port. Port C has an address bus output function, and the pin functions change according to the operating mode.

Port C has a built-in MOS input pull-up function that can be controlled by software.

Figure 5.13 shows the port C pin configuration.



Port C pins	Pin functions in modes 4 and 5
PC7 / A7	A7 (output)
PC6 / A6	A6 (output)
PC5 / A5	A5 (output)
PC4 / A4	A4 (output)
PC3 / A3	A3 (output)
PC2 / A2	A2 (output)
PC1 / A1	A1 (output)
PC0 / A0	A0 (output)

Pin functions in mode 6*	Pin functions in mode 7*
PC7 (input) / A7 (output)	PC7 (I/O)
PC6 (input) / A6 (output)	PC6 (I/O)
PC5 (input) / A5 (output)	PC5 (I/O)
PC4 (input) / A4 (output)	PC4 (I/O)
PC3 (input) / A3 (output)	PC3 (I/O)
PC2 (input) / A2 (output)	PC2 (I/O)
PC1 (input) / A1 (output)	PC1 (I/O)
PC0 (input) / A0 (output)	PC0 (I/O)

Note: * Modes 6 and 7 are not available on the ROMless version.

Figure 5.13 Port C Pin Functions

5.8.2 Register Configuration

Table 5.13 shows the port C register configuration.

Table 5.13 Port C Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port C data direction register	PCDDR	W	H'00	H'FEBB
Port C data register	PCDR	R/W	H'00	H'FF6B
Port C register	PORTC	R	Undefined	H'FF5B
Port C MOS pull-up control register	PCPCR	R/W	H'00	H'FF72

Note: * Lower 16 bits of the address.

Port C Data Direction Register (PCDDR)

Bit	:	7	6	5	4	3	2	1	0
		PC7DDR	PC6DDR	PC5DDR	PC4DDR	PC3DDR	PC2DDR	PC1DDR	PC0DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

PCDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port C. PCDDR cannot be read; if it is, an undefined value will be read.

PCDDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode. The OPE bit in SBYCR is used to select whether the address output pins retain their output state or become high-impedance when a transition is made to software standby mode.

- Modes 4 and 5

  The corresponding port C pins are address outputs irrespective of the value of the PCDDR bits.

- Mode 6*

  Setting a PCDDR bit to 1 makes the corresponding port C pin an address output, while clearing the bit to 0 makes the pin an input port.

- Mode 7*

  Setting a PCDDR bit to 1 makes the corresponding port C pin an output port, while clearing the bit to 0 makes the pin an input port.

Note: * Modes 6 and 7 are not available on the ROMless version.

Port C Data Register (PCDR)

Bit	:	7	6	5	4	3	2	1	0
		PC7DR	PC6DR	PC5DR	PC4DR	PC3DR	PC2DR	PC1DR	PC0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PCDR is an 8-bit readable/writable register that stores output data for the port C pins (PC7 to PC0).

PCDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port C Register (PORTC)

Bit	:	7	6	5	4	3	2	1	0
		PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins PC7 to PC0.

PORTC is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port C pins (PC7 to PC0) must always be performed on PCDR.

If a port C read is performed while PCDDR bits are set to 1, the PCDR values are read. If a port C read is performed while PCDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTC contents are determined by the pin states, as PCDDR and PCDR are initialized. PORTC retains its prior state in software standby mode.

Port C MOS Pull-Up Control Register (PCPCR)

Bit	:	7	6	5	4	3	2	1	0
		PC7PCR	PC6PCR	PC5PCR	PC4PCR	PC3PCR	PC2PCR	PC1PCR	PC0PCR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PCPCR is an 8-bit readable/writable register that controls the MOS input pull-up function incorporated into port C on an individual bit basis.

When a PCDDR bit is cleared to 0 (input port setting) in mode 6 or 7, setting the corresponding PCPCR bit to 1 turns on the MOS input pull-up for the corresponding pin.

PCPCR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

5.8.3 Pin Functions

Modes 4 and 5: In modes 4 and 5, port C pins are automatically designated as address outputs.

Port C pin functions in modes 4 and 5 are shown in figure 5.14.

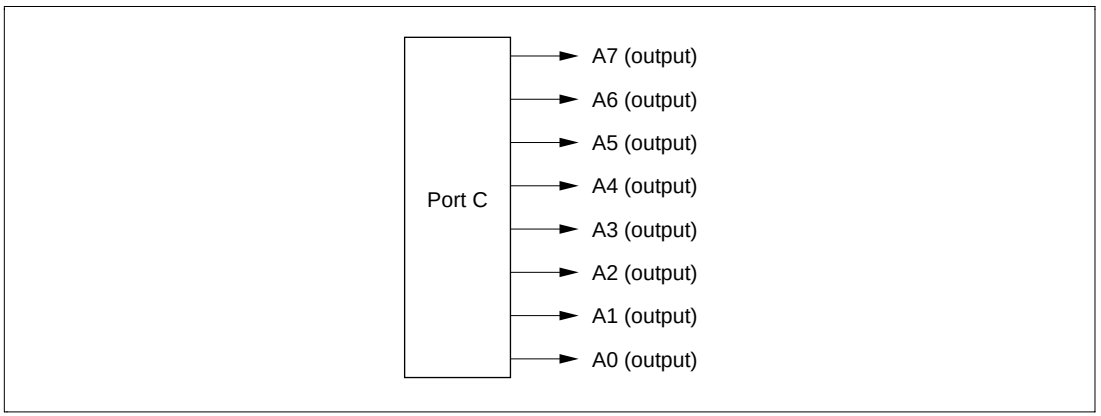


Figure 5.14 Port C Pin Functions (Modes 4 and 5)

Mode 6*: In mode 6, port C pins function as address outputs or input ports. Input or output can be specified on an individual bit basis. Setting a PCDDR bit to 1 makes the corresponding port C pin an address output, while clearing the bit to 0 makes the pin an input port.

Port C pin functions in mode 6 are shown in figure 5.15.

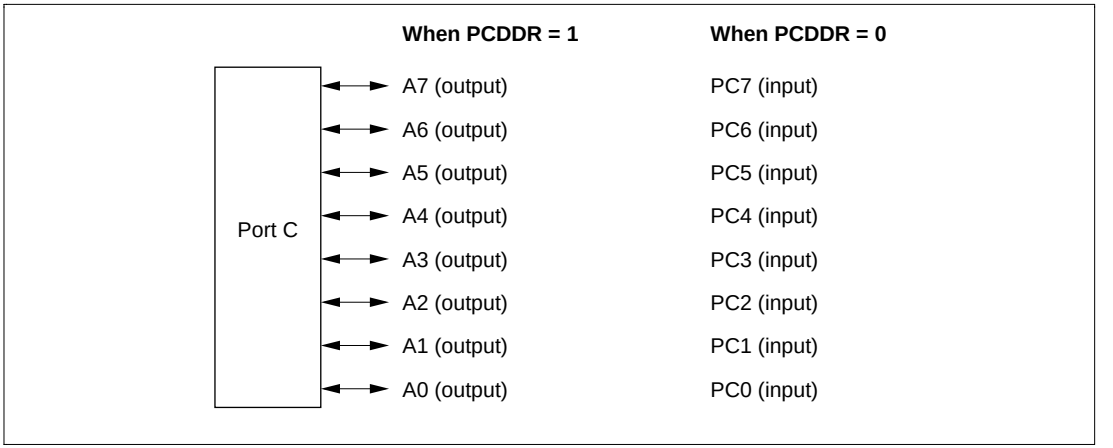


Figure 5.15 Port C Pin Functions (Mode 6)

Mode 7*: In mode 7, port C pins function as I/O ports. Input or output can be specified for each pin on an individual bit basis. Setting a PCDDR bit to 1 makes the corresponding port C pin an output port, while clearing the bit to 0 makes the pin an input port.

Port C pin functions in mode 7 are shown in figure 5.16.

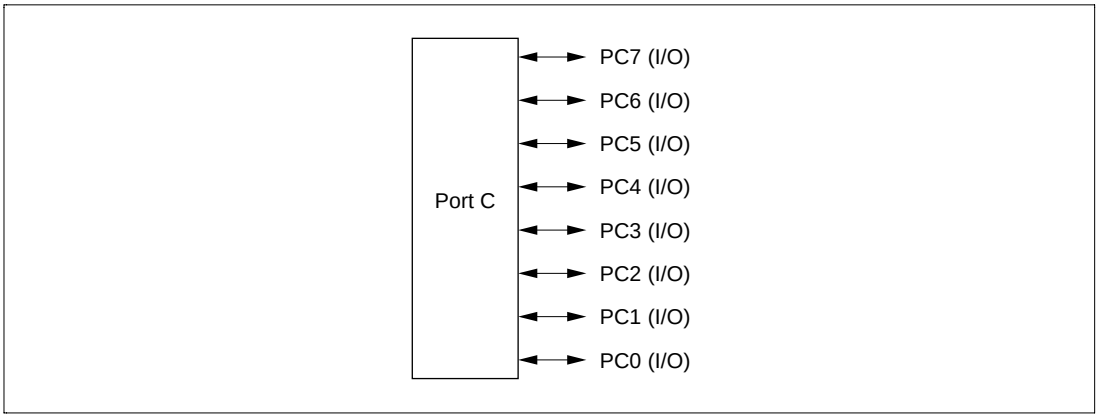


Figure 5.16 Port C Pin Functions (Mode 7)

Note: * Modes 6 and 7 are not available on the ROMless version.

5.8.4 MOS Input Pull-Up Function

Port C has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in modes 6 and 7, and can be specified as on or off on an individual bit basis.

When a PCDDR bit is cleared to 0 in mode 6 or 7, setting the corresponding PCPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset, and in hardware standby mode. The prior state is retained in software standby mode.

Table 5.14 summarizes the MOS input pull-up states.

Table 5.14 MOS Input Pull-Up States (Port C)

Modes	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
4, 5	OFF	OFF	OFF	OFF
6, 7			ON/OFF	ON/OFF

Legend

OFF: MOS input pull-up is always off.

ON/OFF: On when PCDDR = 0 and PCPCR = 1; otherwise off.

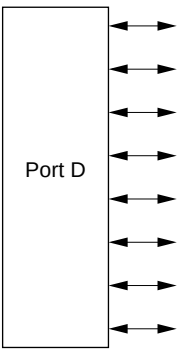
5.9 Port D

5.9.1 Overview

Port D is an 8-bit I/O port. Port D has a data bus I/O function, and the pin functions change according to the operating mode.

Port D has a built-in MOS input pull-up function that can be controlled by software.

Figure 5.17 shows the port D pin configuration.



Port D pins	Pin functions in modes 4 to 6*	Pin functions in mode 7*
PD7 / D15	D15 (I/O)	PD7 (I/O)
PD6 / D14	D14 (I/O)	PD6 (I/O)
PD5 / D13	D13 (I/O)	PD5 (I/O)
PD4 / D12	D12 (I/O)	PD4 (I/O)
PD3 / D11	D11 (I/O)	PD3 (I/O)
PD2 / D10	D10 (I/O)	PD2 (I/O)
PD1 / D9	D9 (I/O)	PD1 (I/O)
PD0 / D8	D8 (I/O)	PD0 (I/O)

Note: * Modes 6 and 7 are not available on the ROMless version.

Figure 5.17 Port D Pin Functions

5.9.2 Register Configuration

Table 5.15 shows the port D register configuration.

Table 5.15 Port D Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port D data direction register	PDDDR	W	H'00	H'FEBC
Port D data register	PDDR	R/W	H'00	H'FF6C
Port D register	PORTD	R	Undefined	H'FF5C
Port D MOS pull-up control register	PDPCR	R/W	H'00	H'FF73

Note: * Lower 16 bits of the address.

Port D Data Direction Register (PDDDR)

Bit	:	7	6	5	4	3	2	1	0
		PD7DDR	PD6DDR	PD5DDR	PD4DDR	PD3DDR	PD2DDR	PD1DDR	PD0DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

PDDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port D. PDDDR cannot be read; if it is, an undefined value will be read.

PDDDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

- Modes 4 to 6*

  The input/output direction specification by PDDDR is ignored, and port D is automatically designated for data I/O.

- Mode 7*

  Setting a PDDDR bit to 1 makes the corresponding port D pin an output port, while clearing the bit to 0 makes the pin an input port.

Note: * Modes 6 and 7 are not available on the ROMless version.

Port D Data Register (PDDR)

Bit	:	7	6	5	4	3	2	1	0
		PD7DR	PD6DR	PD5DR	PD4DR	PD3DR	PD2DR	PD1DR	PD0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDDR is an 8-bit readable/writable register that stores output data for the port D pins (PD7 to PD0).

PDDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port D Register (PORTD)

Bit	:	7	6	5	4	3	2	1	0
		PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins PD7 to PD0.

PORTD is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port D pins (PD7 to PD0) must always be performed on PDDR.

If a port D read is performed while PDDDR bits are set to 1, the PDDR values are read. If a port D read is performed while PDDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTD contents are determined by the pin states, as PDDDR and PDDR are initialized. PORTD retains its prior state in software standby mode.

Port D MOS Pull-Up Control Register (PDPCR)

Bit	:	7	6	5	4	3	2	1	0
		PD7PCR	PD6PCR	PD5PCR	PD4PCR	PD3PCR	PD2PCR	PD1PCR	PD0PCR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDPCR is an 8-bit readable/writable register that controls the MOS input pull-up function incorporated into port D on an individual bit basis.

When a PDDDR bit is cleared to 0 (input port setting) in mode 7, setting the corresponding PDPCR bit to 1 turns on the MOS input pull-up for the corresponding pin.

PDPCR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

5.9.3 Pin Functions

Modes 4 to 6*: In modes 4 to 6, port D pins are automatically designated as data I/O pins.

Port D pin functions in modes 4 to 6 are shown in figure 5.18.

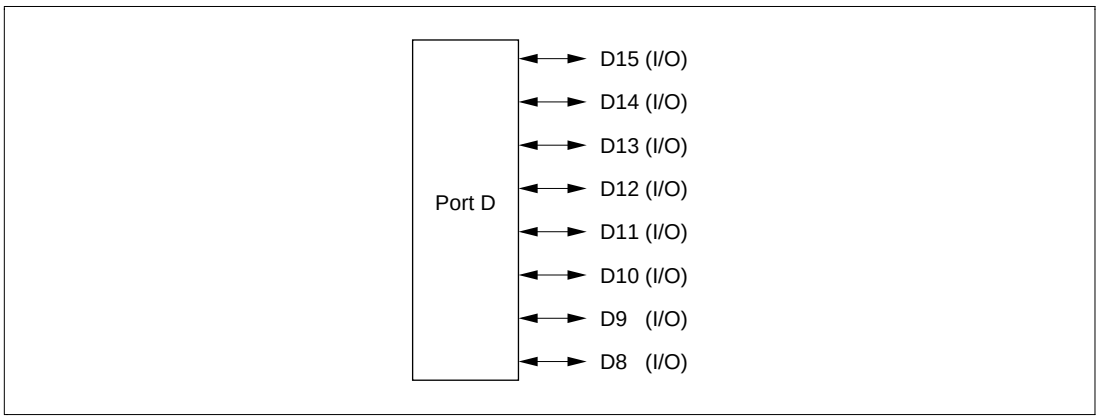


Figure 5.18 Port D Pin Functions (Modes 4 to 6)

Mode 7*: In mode 7, port D pins function as I/O ports. Input or output can be specified for each pin on an individual bit basis. Setting a PDDDR bit to 1 makes the corresponding port D pin an output port, while clearing the bit to 0 makes the pin an input port.

Port D pin functions in mode 7 are shown in figure 5.19.

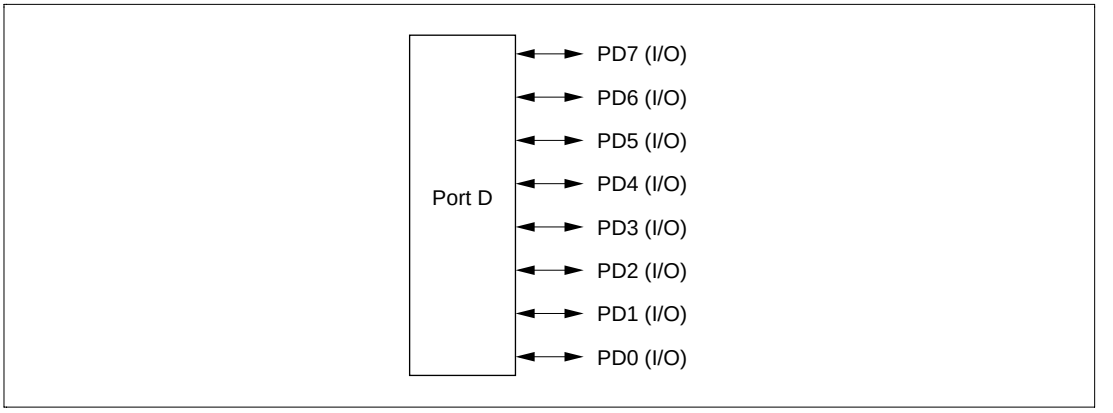


Figure 5.19 Port D Pin Functions (Mode 7)

Note: * Modes 6 and 7 are not available on the ROMless version.

5.9.4 MOS Input Pull-Up Function

Port D has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in mode 7, and can be specified as on or off on an individual bit basis.

When a PDDDR bit is cleared to 0 in mode 7, setting the corresponding PDPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset, and in hardware standby mode. The prior state is retained in software standby mode.

Table 5.16 summarizes the MOS input pull-up states.

Table 5.16 MOS Input Pull-Up States (Port D)

Modes	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
4 to 6	OFF	OFF	OFF	OFF
7			ON/OFF	ON/OFF

Legend

OFF: MOS input pull-up is always off.

ON/OFF: On when PDDDR = 0 and PDPCR = 1; otherwise off.

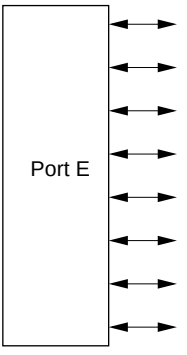
5.10 Port E

5.10.1 Overview

Port E is an 8-bit I/O port. Port E has a data bus I/O function, and the pin functions change according to the operating mode and whether 8-bit or 16-bit bus mode is selected.

Port E has a built-in MOS input pull-up function that can be controlled by software.

Figure 5.20 shows the port E pin configuration.



Port E pins	Pin functions in modes 4 to 6*	Pin functions in mode 7*
PE7 / D7	PE7 (I/O) / D7 (I/O)	PE7 (I/O)
PE6 / D6	PE6 (I/O) / D6 (I/O)	PE6 (I/O)
PE5 / D5	PE5 (I/O) / D5 (I/O)	PE5 (I/O)
PE4 / D4	PE4 (I/O) / D4 (I/O)	PE4 (I/O)
PE3 / D3	PE3 (I/O) / D3 (I/O)	PE3 (I/O)
PE2 / D2	PE2 (I/O) / D2 (I/O)	PE2 (I/O)
PE1 / D1	PE1 (I/O) / D1 (I/O)	PE1 (I/O)
PE0 / D0	PE0 (I/O) / D0 (I/O)	PE0 (I/O)

Note: * Modes 6 and 7 are not available on the ROMless version.

Figure 5.20 Port E Pin Functions

5.10.2 Register Configuration

Table 5.17 shows the port E register configuration.

Table 5.17 Port E Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port E data direction register	PEDDR	W	H'00	H'FEBD
Port E data register	PEDR	R/W	H'00	H'FF6D
Port E register	PORTE	R	Undefined	H'FF5D
Port E MOS pull-up control register	PEPCR	R/W	H'00	H'FF74

Note: * Lower 16 bits of the address.

Port E Data Direction Register (PEDDR)

Bit	:	7	6	5	4	3	2	1	0
		PE7DDR	PE6DDR	PE5DDR	PE4DDR	PE3DDR	PE2DDR	PE1DDR	PE0DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

PEDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port E. PEDDR cannot be read; if it is, an undefined value will be read.

PEDDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

- Modes 4 to 6*

  When 8-bit bus mode has been selected, port E pins function as I/O ports. Setting a PEDDR bit to 1 makes the corresponding port E pin an output port, while clearing the bit to 0 makes the pin an input port.

  When 16-bit bus mode has been selected, the input/output direction specification by PEDDR is ignored, and port E is designated for data I/O.

  For details of 8-bit and 16-bit bus modes, see section 4, Bus Controller.

- Mode 7*

  Setting a PEDDR bit to 1 makes the corresponding port E pin an output port, while clearing the bit to 0 makes the pin an input port.

Note: * Modes 6 and 7 are not available on the ROMless version.

Port E Data Register (PEDR)

Bit	:	7	6	5	4	3	2	1	0
		PE7DR	PE6DR	PE5DR	PE4DR	PE3DR	PE2DR	PE1DR	PE0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PEDR is an 8-bit readable/writable register that stores output data for the port E pins (PE7 to PE0).

PEDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port E Register (PORTE)

Bit	:	7	6	5	4	3	2	1	0
		PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins PE7 to PE0.

PORTE is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port E pins (PE7 to PE0) must always be performed on PEDR.

If a port E read is performed while PEDDR bits are set to 1, the PEDR values are read. If a port E read is performed while PEDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTE contents are determined by the pin states, as PEDDR and PEDR are initialized. PORTE retains its prior state in software standby mode.

Port E MOS Pull-Up Control Register (PEPCR)

Bit	:	7	6	5	4	3	2	1	0
		PE7PCR	PE6PCR	PE5PCR	PE4PCR	PE3PCR	PE2PCR	PE1PCR	PE0PCR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PEPCR is an 8-bit readable/writable register that controls the MOS input pull-up function incorporated into port E on an individual bit basis.

When a PEDDR bit is cleared to 0 (input port setting) in mode 4, 5, or 6 with 8-bit bus mode selected, or in mode 7, setting the corresponding PEPCR bit to 1 turns on the MOS input pull-up for the corresponding pin.

PEPCR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

5.10.3 Pin Functions

Modes 4 to 6*: In modes 4 to 6, when 8-bit access is designated and 8-bit bus mode is selected, port E pins are automatically designated as I/O ports. Setting a PEDDR bit to 1 makes the corresponding port E pin an output port, while clearing the bit to 0 makes the pin an input port.

When 16-bit bus mode is selected, the input/output direction specification by PEDDR is ignored, and port E is designated for data I/O.

Port E pin functions in modes 4 to 6 are shown in figure 5.21.

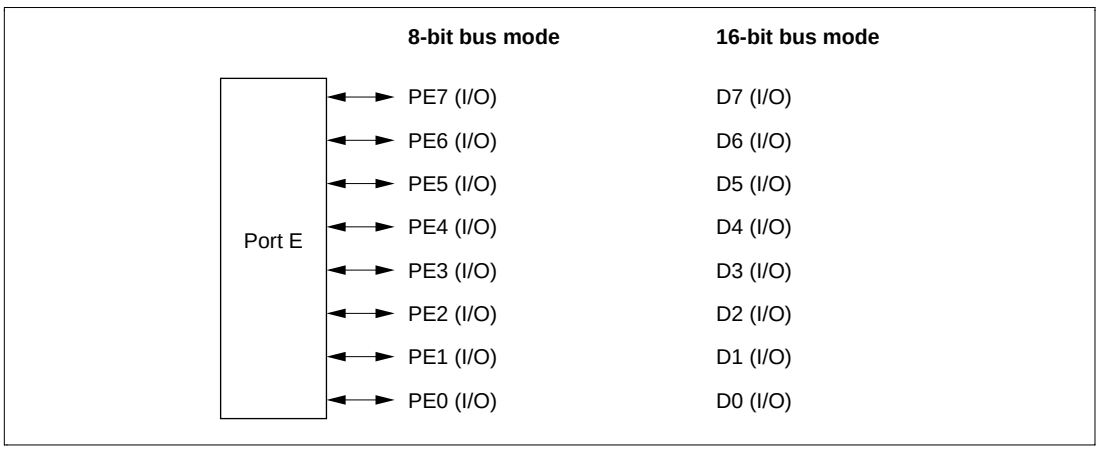


Figure 5.21 Port E Pin Functions (Modes 4 to 6)

Mode 7*: In mode 7, port E pins function as I/O ports. Input or output can be specified for each pin on a bit-by-bit basis. Setting a PEDDR bit to 1 makes the corresponding port E pin an output port, while clearing the bit to 0 makes the pin an input port.

Port E pin functions in mode 7 are shown in figure 5.22.

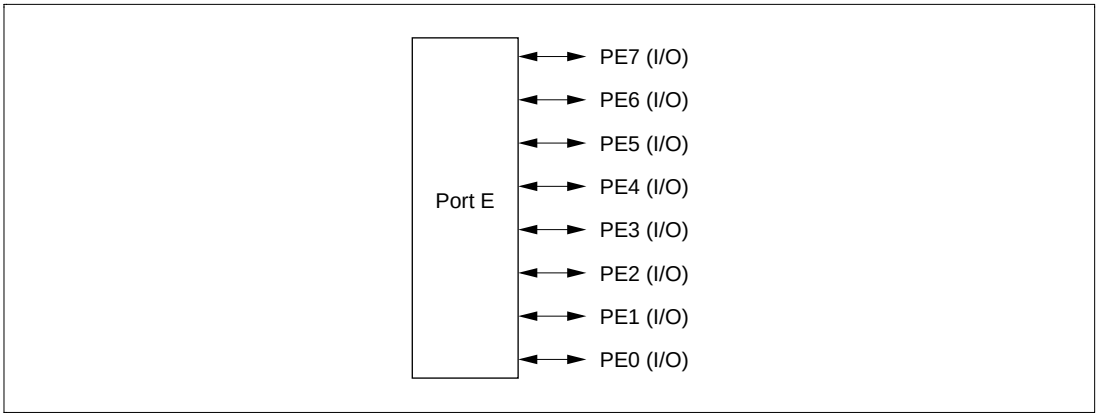


Figure 5.22 Port E Pin Functions (Mode 7)

Note: * Modes 6 and 7 are not available on the ROMless version.

5.10.4 MOS Input Pull-Up Function

Port E has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in modes 4, 5, and 6 when 8-bit bus mode is selected, or in mode 7, and can be specified as on or off on an individual bit basis.

When a PEDDR bit is cleared to 0 in mode 4, 5, or 6 when 8-bit bus mode is selected, or in mode 7, setting the corresponding PEPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset, and in hardware standby mode. The prior state is retained in software standby mode.

Table 5.18 summarizes the MOS input pull-up states.

Table 5.18 MOS Input Pull-Up States (Port E)

Modes		Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
7		OFF	OFF	ON/OFF	ON/OFF
4 to 6	8-bit bus				
	16-bit bus			OFF	OFF

Legend

OFF: MOS input pull-up is always off.

ON/OFF: On when PEDDR = 0 and PEPCR = 1; otherwise off.

5.11 Port F

5.11.1 Overview

Port F is an 8-bit I/O port. Port F pins also function as bus control signal input/output pins ($\overline{AS}$, $\overline{RD}$, $\overline{HWR}$, $\overline{LWR}$, $\overline{WAIT}$, $\overline{BREQ}$, $\overline{BACK}$, $\overline{BREQO}$, $\overline{CS4}$, and $\overline{CS5}$), the system clock (ø) output pin and interrupt input pins ($\overline{IRQ0}$ to $\overline{IRQ3}$).

The interrupt input pins ($\overline{IRQ0}$ to $\overline{IRQ3}$) are Schmitt-triggered inputs.

Figure 5.23 shows the port F pin configuration.

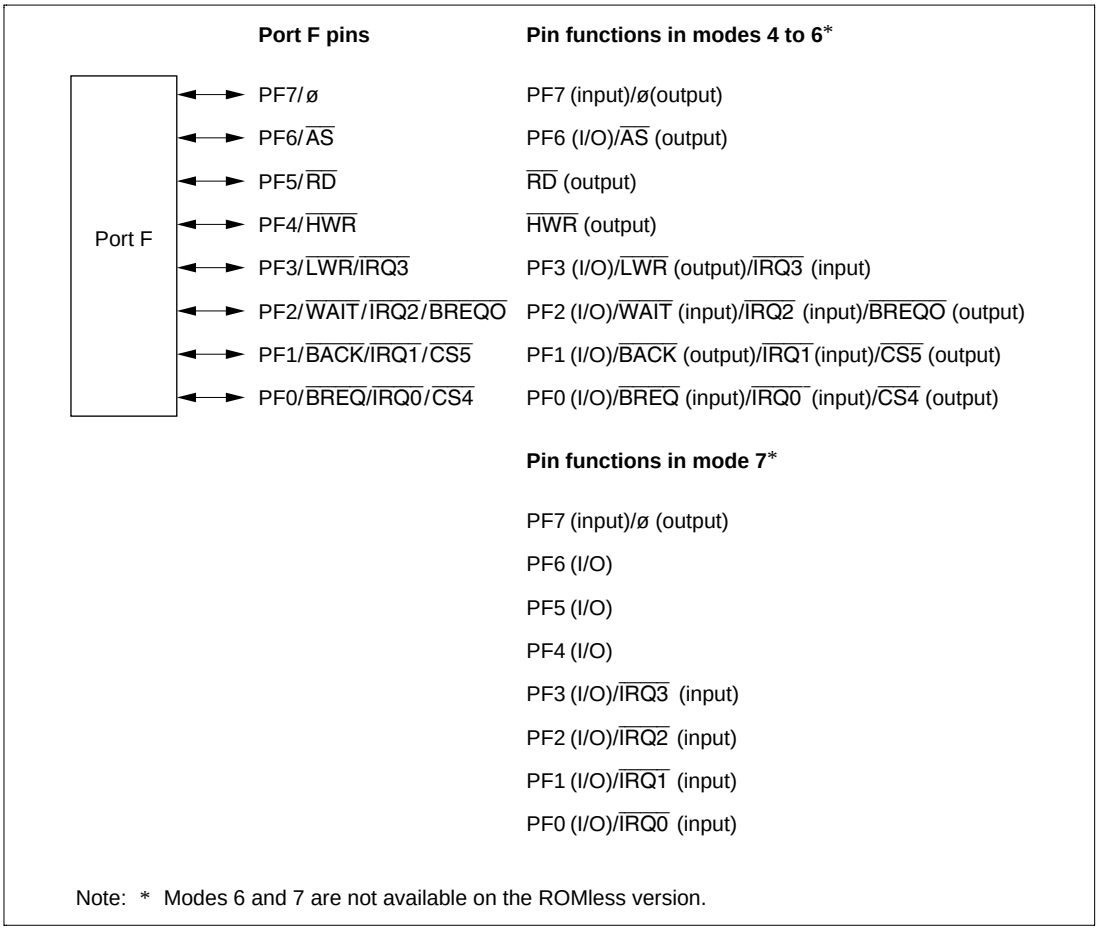


Figure 5.23 Port F Pin Functions

5.11.2 Register Configuration

Table 5.19 shows the port F register configuration.

Table 5.19 Port F Registers

Name	Abbreviation	R/W	Initial Value	Address*[1]
Port F data direction register	PFDDR	W	H'80/H'00*[2]	H'FEBE
Port F data register	PFDR	R/W	H'00	H'FF6E
Port F register	PORTF	R	Undefined	H'FF5E
Bus control register L	BCRL	R/W	H'3C	H'FED5
System control register	SYSCR	R/W	H'01	H'FF39
Port function control register 1	PFCR1	R/W	H'0F	H'FF45
Port function control register 2	PFCR2	R/W	H'30	H'FFAC

Notes: 1. Lower 16 bits of the address.
2. Initial value depends on the mode.

Port F Data Direction Register (PFDDR)

Bit	:	7	6	5	4	3	2	1	0
		PF7DDR	PF6DDR	PF5DDR	PF4DDR	PF3DDR	PF2DDR	PF1DDR	PF0DDR
Modes 4 to 6*									
Initial value	:	1	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W
Mode 7*									
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

PFDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port F. PFDDR cannot be read; if it is, an undefined value will be read.

PFDDR is initialized by a reset, and in hardware standby mode, to H'80 in modes 4 to 6*, and to H'00 in mode 7*. It retains its prior state after in software standby mode. The OPE bit in SBYCR is used to select whether the bus control output pins retain their output state or become high-impedance when a transition is made to software standby mode.

Note: * Modes 6 and 7 are not available on the ROMless version.

Port F Data Register (PFDR)

Bit	:	7	6	5	4	3	2	1	0
		PF7DR	PF6DR	PF5DR	PF4DR	PF3DR	PF2DR	PF1DR	PF0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PFDR is an 8-bit readable/writable register that stores output data for the port F pins (PF7 to PF0).

PFDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state after in software standby mode.

Port F Register (PORTF)

Bit	:	7	6	5	4	3	2	1	0
		PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins PF7 to PF0.

PORTF is an 8-bit read-only register that shows the pin states, and cannot be modified. Writing of output data for the port F pins (PF7 to PF0) must always be performed on PFDR.

If a port F read is performed while PFDDR bits are set to 1, the PFDR values are read. If a port F read is performed while PFDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTF contents are determined by the pin states, as PFDDR and PFDR are initialized. PORTF retains its prior state after in software standby mode.

Port Function Control Register 1 (PFCR1)

Bit	:	7	6	5	4	3	2	1	0
		CSS17	CSS36	PF1CS5S	PF0CS4S	A23E	A22E	A21E	A20E
Initial value	:	0	0	0	0	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PFCR1 is an 8-bit readable/writable register that performs I/O port control. PFCR1 is initialized to H'0F by a reset, and in hardware standby mode.

Bit 7—CS17 Select (CSS17): Selects whether $\overline{CS1}$ or $\overline{CS7}$ is output from the PG3 pin. For details see section 5.12 port G.

Bit 6—CS36 Select (CSS36): Selects whether $\overline{CS3}$ or $\overline{CS6}$ is output from the PG1 pin. For details, see section 5.12 port G.

Bit 5—Port F1 Chip Select 5 Select (PF1CS5S): Selects enabling or disabling of $\overline{CS5}$ output. This bit is valid in modes 4 to 6.

Bit 5 PF1CS5S	Description	
0	PF1 is the PF1/$\overline{BACK}$/$\overline{IRQ1}$ pin	(Initial value)
1	PF1 is the PF1/$\overline{BACK}$/$\overline{IRQ1}$/$\overline{CS5}$ pin. $\overline{CS5}$ output is enabled when BRLE = 0, CS25E = 1, and PF1DDR = 1	

Bit 4—Port F0 Chip Select 4 Select (PF0CS4S): Selects enabling or disabling of $\overline{CS4}$ output. This bit is valid in modes 4 to 6.

Bit 4 PF0CS4S	Description	
0	PF0 is the PF0/$\overline{BREQ}$/$\overline{IRQ0}$ pin	(Initial value)
1	PF0 is the PF0/$\overline{BREQ}$/$\overline{IRQ0}$/$\overline{CS4}$ pin. $\overline{CS4}$ output is enabled when BRLE = 0, CS25E = 1, and PF0DDR = 1	

Bit 3—Address 23 Enable (A23E): Enables or disables address output 23 (A23). For details, see section 5.2 port 1.

Bit 2—Address 22 Enable (A22E): Enables or disables address output 22 (A22). For details, see section 5.2 port 1.

Bit 1—Address 21 Enable (A21E): Enables or disables address output 21 (A21). For details, see section 5.2 port 1.

Bit 0—Address 20 Enable (A20E): Enables or disables address output 20 (A20). For details, see section 5.2 port 1.

Port Function Control Register 2 (PFCR2)

Bit	:	7	6	5	4	3	2	1	0
		—	—	CS167E	CS25E	ASOD	—	—	—
Initial value	:	0	0	1	1	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R	R	R

PFCR2 is an 8-bit readable/writable register that performs I/O port control. PFCR2 is initialized to H'30 by a reset, and in hardware standby mode.

Bits 7 and 6—Reserved.

Bit 5—CS167 Enable (CS167E): Enables or disables $\overline{CS1}$, $\overline{CS6}$, and $\overline{CS7}$ output. For details, see section 5.12 port G.

Bit 4—CS25 Enable (CS25E): Enables or disables $\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$, and $\overline{CS5}$ output. Change the CS25E setting only when the DDR bits are cleared to 0. This bit is valid in modes 4 to 6.

Bit 4 CS25E	Description
0	$\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$, and $\overline{CS5}$ output disabled (can be used as I/O ports)
1	$\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$, and $\overline{CS5}$ output enabled (Initial value)

Bit 3—AS Output Disable (ASOD): Enables or disables $\overline{AS}$ output. This bit is valid in modes 4 to 6.

Bit 3 ASOD	Description
0	PF6 is used as $\overline{AS}$ output pin (Initial value)
1	PF6 is designated as I/O port, and does not function as $\overline{AS}$ output pin

Bits 2 to 0—Reserved.

System Control Register (SYSCR)

Bit :	7	6	5	4	3	2	1	0
	—	—	INTM1	INTM0	NMIEG	LWROD	—	RAME
Initial value :	0	0	0	0	0	0	0	1
R/W :	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W

Bit 2—LWR Output Disable (LWROD): Enables or disables $\overline{LWR}$ output. This bit is valid in modes 4 to 6.

Bit 2 LWROD	Description
0	PF3 is designated as $\overline{LWR}$ output pin (Initial value)
1	PF3 is designated as I/O port, and does not function as $\overline{LWR}$ output pin

Bus Control Register L (BCRL)

Bit	:	7	6	5	4	3	2	1	0
		BRLE	BREQOE	EAE	—	—	—	—	WAITE
Initial value	:	0	0	1	1	1	1	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BCRL is an 8-bit readable/writable register that performs selection of the external bus-released state protocol, selection of the area partition unit, and enabling or disabling of $\overline{\text{WAIT}}$ pin input.

BCRL is initialized to H'3C by a reset, and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—Bus Release Enable (BRLE): Enables or disables external bus release.

Bit 7 BRLE	Description	
0	External bus release disabled. $\overline{\text{BREQ}}$, $\overline{\text{BACK}}$, and $\overline{\text{BREQO}}$ pins can be used as I/O ports	(Initial value)
1	External bus release enabled	

Bit 6—BREQO Pin Enable (BREQOE): Outputs a signal that requests the external bus master to drop the bus request signal ($\overline{\text{BREQ}}$) in the external bus-released state, or when an internal bus master performs an external space access.

Bit 6 BREQOE	Description	
0	$\overline{\text{BREQO}}$ output disabled. $\overline{\text{BREQO}}$ pin can be used as I/O port	(Initial value)
1	$\overline{\text{BREQO}}$ output enabled	

Bit 0—WAIT Pin Enable (WAITE): Selects enabling or disabling of wait input by the $\overline{\text{WAIT}}$ pin.

Bit 0 WAITE	Description	
0	Wait input by $\overline{\text{WAIT}}$ pin disabled. $\overline{\text{WAIT}}$ pin can be used as I/O port	(Initial value)
1	Wait input by $\overline{\text{WAIT}}$ pin enabled	

5.11.3 Pin Functions

Port F pins also function as bus control signal input/output pins ($\overline{AS}$, $\overline{RD}$, $\overline{HWR}$, $\overline{LWR}$, $\overline{WAIT}$, $\overline{BREQ}$, $\overline{BACK}$, $\overline{BREQO}$, $\overline{CS4}$, and $\overline{CS5}$) the system clock (ø) output pin and interrupt input pins ($\overline{IRQ0}$ to $\overline{IRQ3}$). The pin functions differ between modes 4, 5, and 6*[1], and mode 7*[1]. Port F pin functions are shown in table 5.20.

Table 5.20 Port F Pin Functions

PF7/ø

The pin function is switched as shown below according to bit PF7DDR.

PF7DDR	0	1
Pin function	PF7 input pin	ø output pin

PF6/$\overline{AS}$

The pin function is switched as shown below according to the operating mode, and bit PF6DDR, and bit ASOD in PFCR2.

Operating Mode	Modes 4, 5, 6*[1]			Mode 7*[1]	
ASOD	0	1		—	
PF6DDR	—	0	1	0	1
Pin function	$\overline{AS}$ output pin	PF6 input pin	PF6 output pin	PF6 input pin	PF6 output pin

PF5/$\overline{RD}$

The pin function is switched as shown below according to the operating mode and bit PF5DDR.

Operating Mode	Modes 4, 5, 6*[1]	Mode 7*[1]	
PF5DDR	—	0	1
Pin function	$\overline{RD}$ output pin	PF5 input pin	PF5 output pin

PF4/$\overline{HWR}$

The pin function is switched as shown below according to the operating mode and bit PF4DDR.

Operating Mode	Modes 4, 5, 6*[1]	Mode 7*[1]	
PF4DDR	—	0	1
Pin function	$\overline{HWR}$ output pin	PF4 input pin	PF4 output pin

Pin	Selection Method and Pin Functions

PF3/$\overline{\text{LWR}}$/$\overline{\text{IRQ3}}$

The pin function is switched as shown below according to the operating mode, and bit PF3DDR, and bit LWROD in SYSCR.

Operating Mode	Modes 4, 5, 6*[1]			Mode 7*[1]	
LWROD	0	1*[3]		—	
PF3DDR	—	0	1	0	1
Pin function	$\overline{\text{LWR}}$ output pin	PF3 input pin	PF3 output pin	PF3 input pin	PF3 output pin
	$\overline{\text{IRQ3}}$ interrupt input pin*[2]				

PF2/$\overline{\text{WAIT}}$/$\overline{\text{IRQ2}}$/$\overline{\text{BREQO}}$

The pin function is switched as shown below according to the operating mode, and WAITE bit, BREQOE bit in BCRL and PF2DDR bit.

Operating Mode	Modes 4, 5, 6*[1]						Mode 7*[1]	
BREQOE	0				1		—	
WAITE	0		1		0	1	—	
PF2DDR	0	1	0	1	—	—	0	1
Pin function	PF2 input pin	PF2 output pin	$\overline{\text{WAIT}}$ input pin	Setting prohibited	$\overline{\text{BREQO}}$ output pin	Setting prohibited	PF2 input pin	PF2 output pin
	$\overline{\text{IRQ2}}$ interrupt input pin*[2]							

Pin	Selection Method and Pin Functions

PF1/$\overline{\text{BACK}}$/$\overline{\text{IRQ1}}$/$\overline{\text{CS5}}$

The pin function is switched as shown below according to the operating mode, and the BRLE bit in BCRL, PF1CS5S bit in PFCR1, and CS25E bit in PFCR2 and PF1DDR bit.

Operating Mode	Modes 4, 5, 6*[1]					Mode 7*[1]	
BRLE	0				1	—	
PF1DDR	0	1			—	0	1
CS25E	—	0	1		—	—	—
PF1CS5S	—	—	0	1	—	—	—
Pin function	PF1 input pin	PF1 output pin		$\overline{\text{CS5}}$ output pin	$\overline{\text{BACK}}$ output pin	PF1 input pin	PF1 output pin
	$\overline{\text{IRQ1}}$ interrupt input pin*[2]						

PF0/$\overline{\text{BREQ}}$/$\overline{\text{IRQ0}}$/$\overline{\text{CS4}}$

The pin function is switched as shown below according to the operating mode, and the BRLE bit in BCRL and PF0CS4S bit in PFCR1 and CS25E bit in PFCR2 and PF0DDR bit.

Operating Mode	Modes 4, 5, 6*[1]					Mode 7*[1]	
BRLE	0				1	—	
PF0DDR	0	1			—	0	1
CS25E	—	0	1		—	—	—
PF0CS4S	—	—	0	1	—	—	—
Pin function	PF0 input pin	PF0 output pin		$\overline{\text{CS4}}$ output pin	$\overline{\text{BREQ}}$ output pin	PF0 input pin	PF0 output pin
	$\overline{\text{IRQ0}}$ interrupt input pin*[2]						

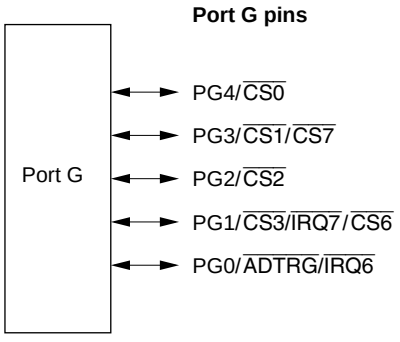
Notes: 1. Modes 6 and 7 are not available on the ROMless version.
2. When this pin is used as an external interrupt input, the pin function should be set as a port (PFn) input pin.
3. Valid only in 8-bit-bus mode.

5.12 Port G

5.12.1 Overview

Port G is a 5-bit I/O port. Port G pins also function as bus control signal output pins ($\overline{CS0}$ to $\overline{CS3}$, $\overline{CS6}$, $\overline{CS7}$). The A/D converter input pin ($\overline{ADTRG}$), and interrupt input pins ($\overline{IRQ6}$, $\overline{IRQ7}$). The interrupt input pins ($\overline{IRQ6}$, $\overline{IRQ7}$) are Schmitt-triggered inputs.

Figure 5.24 shows the port G pin configuration.



Pin functions in modes 4 to 6*	Pin functions in mode 7*
PG4 (I/O)/$\overline{CS0}$ (output)	PG4 (I/O)
PG3 (I/O)/$\overline{CS1}$ (output)/ $\overline{CS7}$ (output)	PG3 (I/O)
PG2 (I/O)/$\overline{CS2}$ (output)	PG2 (I/O)
PG1 (I/O)/$\overline{CS3}$ (output)/$\overline{IRQ7}$ (input)/ $\overline{CS6}$ (output)	PG1 (I/O)/$\overline{IRQ7}$ (input)
PG0 (I/O)/$\overline{ADTRG}$ (input)/$\overline{IRQ6}$ (input)	PG0 (I/O)/ $\overline{ADTRG}$ (input)/$\overline{IRQ6}$ (input)

Note: * Modes 6 and 7 are not available on the ROMless version.

Figure 5.24 Port G Pin Functions

5.12.2 Register Configuration

Table 5.21 shows the port G register configuration.

Table 5.21 Port G Registers

Name	Abbreviation	R/W	Initial Value*[1]	Address*[2]
Port G data direction register	PGDDR	W	H'10/H'00*[3]	H'FEBF
Port G data register	PGDR	R/W	H'00	H'FF6F
Port G register	PORTG	R	Undefined	H'FF5F
Port function control register 1	PFCR1	R/W	H'0F	H'FF45
Port function control register 2	PFCR2	R/W	H'30	H'FFAC

Notes: 1. Value of bits 4 to 0.
2. Lower 16 bits of the address.
3. Initial value depends on the mode.

Port G Data Direction Register (PGDDR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	PG4DDR	PG3DDR	PG2DDR	PG1DDR	PG0DDR
Modes 4 and 5									
Initial value	:	Undefined	Undefined	Undefined	1	0	0	0	0
R/W	:	—	—	—	W	W	W	W	W
Modes 6 and 7*									
Initial value	:	Undefined	Undefined	Undefined	0	0	0	0	0
R/W	:	—	—	—	W	W	W	W	W

PGDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port G. PGDDR cannot be read, and bits 7 to 5 are reserved. If PGDDR is read, an undefined value will be read.

The PGDDR is initialized by a reset and in hardware standby mode, to H'10 (bits 4 to 0) in modes 4 and 5, and to H'00 (bits 4 to 0) in modes 6 and 7*. It retains its prior state after in software standby mode. The OPE bit in SBYCR is used to select whether the bus control output pins retain their output state or become high-impedance when a transition is made to software standby mode.

Note: * Modes 6 and 7 are not available on the ROMless version.

Port G Data Register (PGDR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	PG4DR	PG3DR	PG2DR	PG1DR	PG0DR
Initial value	:	Undefined	Undefined	Undefined	0	0	0	0	0
R/W	:	—	—	—	R/W	R/W	R/W	R/W	R/W

PGDR is an 8-bit readable/writable register that stores output data for the port G pins (PG4 to PG0).

Bits 7 to 5 are reserved; they return an undetermined value if read, and cannot be modified.

PGDR is initialized to H'00 (bits 4 to 0) by a reset, and in hardware standby mode. It retains its prior state after in software standby mode.

Port G Register (PORTG)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	PG4	PG3	PG2	PG1	PG0
Initial value	:	Undefined	Undefined	Undefined	—*	—*	—*	—*	—*
R/W	:	—	—	—	R	R	R	R	R

Note: * Determined by state of pins PG4 to PG0.

PORTG is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port G pins (PG4 to PG0) must always be performed on PGDR.

Bits 7 to 5 are reserved; they return an undetermined value if read, and cannot be modified.

If a port G read is performed while PGDDR bits are set to 1, the PGDR values are read. If a port G read is performed while PGDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTG contents are determined by the pin states, as PGDDR and PGDR are initialized. PORTG retains its prior state after in software standby mode.

Port Function Control Register 1 (PFCR1)

Bit	:	7	6	5	4	3	2	1	0
		CSS17	CSS36	PF1CS5S	PF0CS4S	A23E	A22E	A21E	A20E
Initial value	:	0	0	0	0	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PFCR1 is an 8-bit readable/writable register that performs I/O port control. PFCR1 is initialized to H'0F by a reset, and in hardware standby mode.

Bit 7—CS17 Select (CSS17): Selects whether $\overline{CS1}$ or $\overline{CS7}$ is output from the PG3 pin. Change the CSS17 bit setting only when the corresponding DDR bit is 0. This bit is valid in modes 4 to 6.

Bit 7 CSS17	Description
0	PG3 is the PG3/$\overline{CS1}$ pin. $\overline{CS1}$ output is enabled when CS167E = 1 and PG3DDR = 1 (Initial value)
1	PG3 is the PG3/$\overline{CS7}$ pin. $\overline{CS7}$ output is enabled when CS167E = 1 and PG3DDR = 1

Bit 6—CS36 Select (CSS36): Selects whether $\overline{CS3}$ or $\overline{CS6}$ is output from the PG1 pin. Change the CSS36 bit setting only when the corresponding DDR bit is 0. This bit is valid in modes 4 to 6.

Bit 6 CSS36	Description
0	PG1 is the PG1/$\overline{IRQ7}$/$\overline{CS3}$ pin. $\overline{CS3}$ output is enabled when CS25E = 1 and PG1DDR = 1 (Initial value)
1	PG1 is the PG1/ $\overline{IRQ7}$/$\overline{CS6}$ pin. $\overline{CS6}$ output is enabled when CS167E = 1 and PG1DDR = 1

Bit 5—Port F1 Chip Select 5 Select (PF1CS5S): Enables or disables $\overline{CS5}$ output. For details, see section 5.11, Port F.

Bit 4—Port F0 Chip Select 4 Select (PF0CS4S): Enables or disables $\overline{CS4}$ output. For details, see section 5.11, Port F.

Bit 3—Address 23 Enable (A23E): Enables or disables address output 23 (A23). For details, see section 5.2, Port 1.

Bit 2—Address 22 Enable (A22E): Enables or disables address output 22 (A22). For details, see section 5.2,, Port 1.

Bit 1—Address 21 Enable (A21E): Enables or disables address output 21 (A21). For details, see section 5.2, Port 1.

Bit 0—Address 20 Enable (A20E): Enables or disables address output 20 (A20). For details, see section 5.2, Port 1.

Port Function Control Register 2 (PFCR2)

Bit	:	7	6	5	4	3	2	1	0
		—	—	CS167E	CS25E	ASOD	—	—	—
Initial value	:	0	0	1	1	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R	R	R

PFCR2 is an 8-bit readable/writable register that performs I/O port control. PFCR2 is initialized to H'30 by a reset, and in hardware standby mode. This bit is valid in modes 4 to 6.

Bits 7 and 6—Reserved.

Bit 5—CS167 Enable (CS167E): Enables or disables $\overline{CS1}$, $\overline{CS6}$, and $\overline{CS7}$ output. Change the CS167E setting only when the DDR bits are cleared to 0.

Bit 5 CS167E	Description	
0	$\overline{CS1}$, $\overline{CS6}$, and $\overline{CS7}$ output disabled (can be used as I/O ports)	
1	$\overline{CS1}$, $\overline{CS6}$, and $\overline{CS7}$ output enabled	(Initial value)

Bit 4—CS25 Enable (CS25E): Enables or disables $\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$, and $\overline{CS5}$ output. Change the CS25E setting only when the DDR bits are cleared to 0. This bit is valid in modes 4 to 6.

Bit 4 CS25E	Description	
0	$\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$, and $\overline{CS5}$ output disabled (can be used as I/O ports)	
1	$\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$, and $\overline{CS5}$ output enabled	(Initial value)

Bit 3—AS Output Disable (ASOD): Enables or disables $\overline{AS}$ output. This bit is valid in modes 4 to 6. For details, see section 5.11, Port F.

Bits 2 to 0—Reserved.

5.12.3 Pin Functions

Port G pins also function as bus control signal output pins ($\overline{CS0}$ to $\overline{CS3}$, $\overline{CS6}$, $\overline{CS7}$) the A/D converter input pin ($\overline{ADTRG}$), and interrupt input pins ($\overline{IRQ6}$, $\overline{IRQ7}$). The pin functions are different in mode 7*, and modes 4 to 6*. Port G pin functions are shown in table 5.22.

Table 5.22 Port G Pin Functions

Pin — **Selection Method and Pin Functions**

PG4/$\overline{CS0}$

The pin function is switched as shown below according to the operating mode and bit PG4DDR.

Operating Mode	Modes 4, 5, 6*[1]		Mode 7*[1]	
PG4DDR	0	1	0	1
Pin function	PG4 input pin	$\overline{CS0}$ output pin	PG4 input pin	PG4 output pin

PG3/$\overline{CS1}$/$\overline{CS7}$

The pin function is switched as shown below according to the operating mode and CSS17 bit in PFCR1, CS167E bit in PFCR2, and bit PG3DDR.

Operating Mode	Modes 4, 5, 6*[1]				Mode 7*[1]	
PG3DDR	0	1			0	1
CS167E	—	0	1		—	—
CSS17	—	—	0	1	—	—
Pin function	PG3 input pin	PG3 output pin	$\overline{CS1}$ output pin	$\overline{CS7}$ output pin	PG3 input pin	PG3 output pin

PG2/$\overline{CS2}$

The pin function is switched as shown below according to the operating mode and CS25E bit in PFCR2, and bit PG2DDR.

Operating Mode	Modes 4, 5, 6*[1]			Mode 7*[1]	
PG2DDR	0	1		0	1
CS25E	—	0	1	—	—
Pin function	PG2 input pin	PG2 output pin	$\overline{CS2}$ output pin	PG2 input pin	PG2 output pin

Pin	Selection Method and Pin Functions

PG1/$\overline{\text{CS3}}$/$\overline{\text{CS6}}$/$\overline{\text{IRQ7}}$

The pin function is switched as shown below according to the combination of operating mode and CSS36 bit in PFCR1, CS167E bit in PFCR2, CS25E bit and bit PG1DDR.

Operating Mode	Modes 4, 5, 6*[1]								Mode 7*[1]	
PG1DDR	0	1							0	1
CS167E	—	0			1				—	—
CS25E	—	0		1		0		1	—	—
CSS36	—	—	0	1	0	1	0	1	—	—
Pin function	PG1 input pin	PG1 output pin	$\overline{\text{CS3}}$ output pin	PG1 output pin		$\overline{\text{CS6}}$ output pin	$\overline{\text{CS3}}$ output pin	$\overline{\text{CS6}}$ output pin	PG1 input pin	PG1 output pin
	$\overline{\text{IRQ7}}$ interrupt input pin*[2]									

PG0/$\overline{\text{ADTRG}}$/$\overline{\text{IRQ6}}$

The pin function is switched as shown below according to the combination of bits TRGS1 and TRGS0 (trigger select 1 and 0) in the A/D control register (ADCR).

PG0DDR	0	1
Pin function	PG0 input	PG0 output
	$\overline{\text{ADTRG}}$ input pin*[3]	
	$\overline{\text{IRQ6}}$ interrupt input pin*[2]	

Notes: 1. Modes 6 and 7 are not available on the ROMless version.
2. When this pin is used as an external interrupt input, it should not be used as an input/output pin with other functions.
3. $\overline{\text{ADTRG}}$ input when TRGS1 = TRGS0 = 1.

5.13 Pin States

5.13.1 Port States in Each Mode

Table 5.23 I/O Port States in Each Processing State

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
P17/TIOCB2/ TCLKD P16/TIOCA2 P15/TIOCB1/ TCLKC P14/TIOCA1	4 to 7	T	T	kept	kept	I/O port
P13/TIOGD0/ TCLKB/A23 P12/TIOCC0/T CLKA/A22 P11/TIOCB0/ A21 P10/TIOCA0/ A20	4 to 6	T	T	[AnE = 0] kept [AnE · $\overline{\text{DDR}}$ = 1] kept [AnE · DDR · $\overline{\text{OPE}}$ = 1] T [AnE · DDR · OPE = 1] kept	[AnE = 0] kept [AnE · $\overline{\text{DDR}}$ = 1] kept [AnE · DDR = 1] T	[AnE = 0] I/O port [AnE · $\overline{\text{DDR}}$ = 1] I/O port [AnE · DDR = 1] Address output
	7	T	T	kept	kept	I/O port
Port 2	4 to 7	T	T	kept	kept	I/O port
Port 3	4 to 7	T	T	kept	kept	I/O port
P47/DA1	4 to 7	T	T	[DAOE1 = 1] kept [DAOE1 = 0] T	kept	I/O port
P46/DA0	4 to 7	T	T	[DAOE0 = 1] kept [DAOE0 = 0] T	kept	I/O port
P45 to P40	4 to 7	T	T	T	T	Input port

Port Name Pin Name	MCU Operating Mode		Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
PA3/A19 PA2/A18 PA1/A17 PA0/A16	4, 5		L	T	[OPE = 0] T [OPE = 1] kept	T	Address output
	6		T	T	[DDR · OPE = 0] T [DDR · OPE = 1] kept	T	[DDR = 0] Input port [DDR = 1] Address output
	7		T	T	kept	kept	I/O port
Port B	4, 5		L	T	[OPE = 0] T [OPE = 1] kept	T	Address output
	6		T	T	[DDR · OPE = 0] T [DDR · OPE = 1] kept	T	[DDR = 0] Input port [DDR = 1] Address output
	7		T	T	kept	kept	I/O port
Port C	4, 5		L	T	[OPE = 0] T [OPE = 1] kept	T	Address output
	6		T	T	[DDR · OPE = 0] T [DDR · OPE = 1] kept	T	[DDR = 0] Input port [DDR = 1] Address output
	7		T	T	kept	kept	I/O port
Port D	4 to 6		T	T	T	T	Data bus
	7		T	T	kept	kept	I/O port
Port E	4 to 6	8-bit bus	T	T	kept	kept	I/O port
		16-bit bus	T	T	T	T	Data bus
	7		T	T	kept	kept	I/O port

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
PF7 /ø	4 to 6	Clock output	T	[DDR = 0] Input port [DDR = 1] H	[DDR = 0] Input port [DDR = 1] Clock output	[DDR = 0] Input port [DDR = 1] Clock output
	7	T	T	[DDR = 0] Input port [DDR = 1] H	[DDR = 0] Input port [DDR = 1] Clock output	[DDR = 0] Input port [DDR = 1] Clock output
PF6/$\overline{AS}$	4 to 6	H	T	[ASOD = 1] kept [$\overline{ASOD}$ · $\overline{OPE}$ = 1] T [$\overline{ASOD}$ · OPE = 1] H	[ASOD = 1] kept [ASOD = 0] T	[ASOD = 1] I/O port [ASOD = 0] $\overline{AS}$
	7	T	T	kept	kept	I/O port
PF5/$\overline{RD}$ PF4/$\overline{HWR}$	4 to 6	H	T	[OPE = 0] T [OPE = 1] H	T	$\overline{RD}$, $\overline{HWR}$
	7	T	T	kept	kept	I/O port
PF3/$\overline{LWR}$/ $\overline{IRQ3}$	4 to 6	H	T	[LWROD = 1] kept [$\overline{LWROD}$ · $\overline{OPE}$ = 1] T [$\overline{LWROD}$ · OPE = 1] H	[LWROD = 1] kept [LWROD = 0] T	[LWROD = 1] I/O port [LWROD = 0] $\overline{LWR}$
	7	T	T	kept	kept	I/O port
PF2/$\overline{WAIT}$/ $\overline{IRQ2}$/ $\overline{BREQO}$	4 to 6	T	T	[BREQOE + WAITE = 0] kept [BREQOE = 1] kept [BREQOE = 0] And [WAITE · $\overline{DDR}$ = 1] T	[BREQOE + WAITE = 0] kept [BREQOE = 1] $\overline{BREQO}$ [BREQOE = 0] And [WAITE · $\overline{DDR}$ = 1] T	[BREQOE + WAITE = 0] I/O port [BREQOE = 1] $\overline{BREQO}$ [BREQOE = 0] And [WAITE · $\overline{DDR}$ = 1] $\overline{WAIT}$
	7	T	T	kept	kept	I/O port

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
PF1/$\overline{\text{BACK}}$ / IRQ1/$\overline{\text{CS5}}$	4 to 6	T	T	[BRLE + CS25E · PF1CS5S = 0] kept [$\overline{\text{BRLE}}$ · DDR · CS25E · PF1CS5S =1] And [OPE = 0] T [$\overline{\text{BRLE}}$ · DDR · CS25E · PF1CS5S = 1] And [OPE = 1] H [BRLE = 1] $\overline{\text{BACK}}$	L	[BRLE + CS25E · PF1CS5S = 0] I/O port [$\overline{\text{BRLE}}$ · DDR · CS25E · PF1CS5S =1] $\overline{\text{CS5}}$ [BRLE = 1] $\overline{\text{BACK}}$
	7	T	T	kept	kept	I/O port
PF0/$\overline{\text{BREQ}}$/ IRQ0/$\overline{\text{CS4}}$	4 to 6	T	T	[BRLE + CS25E · PF0CS4S = 0] kept [$\overline{\text{BRLE}}$ · DDR · CS25E · PF0CS4S = 1] And [OPE = 0] T [$\overline{\text{BRLE}}$ · DDR · CS25E · PF0CS4S = 1] And [OPE = 1] H [BRLE = 1] T	T	[BRLE + CS25E · PF0CS4S = 0] I/O port [$\overline{\text{BRLE}}$ · DDR · CS25E · PF0CS4S = 1] $\overline{\text{CS4}}$ [BRLE = 1] $\overline{\text{BREQ}}$
	7	T	T	kept	kept	I/O port

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
PG4/$\overline{CS0}$	4, 5	H	T	[DDR · OPE = 0] T	T	[DDR = 0] Input port
	6	T		[DDR · OPE = 1] H		[DDR = 1] $\overline{CS0}$
	7	T	T	kept	kept	I/O port
PG3/$\overline{CS1}$/ $\overline{CS7}$	4 to 6	T	T	[CS167E = 0] kept	[CS167E = 0] kept	[CS167E = 0] I/O port
				[CS167E · $\overline{DDR}$ = 1] T	[CS167E = 1] T	[CS167E · $\overline{DDR}$ = 1] Input port
				[CS167E · DDR · $\overline{OPE}$ = 1] T		[CS167E · $\overline{CSS17}$ · DDR = 1] $\overline{CS1}$
				[CS167E · DDR · OPE = 1] H		[CS167E · CSS17 · DDR = 1] $\overline{CS7}$
	7	T	T	kept	kept	I/O port
PG2/$\overline{CS2}$	4 to 6	T	T	[CS25E = 0] kept	[CS25E = 0] kept	[CS25E = 0] I/O port
				[CS25E · $\overline{DDR}$ = 1] T	[CS25E = 1] T	[CS25E · $\overline{DDR}$ = 1] Input port
				[CS25E · DDR · $\overline{OPE}$ = 1] T		[CS25E · DDR = 1] $\overline{CS2}$
				[CS25E · DDR · OPE = 1] H		
	7	T	T	kept	kept	I/O port

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
PG1/$\overline{CS3}$/ $\overline{CS6}$/IRQ7	4 to 6	T	T	[$\overline{CSS36}$ · CS25E + CSS36 · CS167E = 0] kept [$\overline{CSS36}$ · CS25E · $\overline{DDR}$ = 1] T [CSS36 · CS167E · $\overline{DDR}$ = 1] T [$\overline{CSS36}$ · CS25E · DDR · $\overline{OPE}$ = 1] T [CSS36 · CS167E · DDR · $\overline{OPE}$ = 1] T [$\overline{CSS36}$ · CS25E · DDR · OPE = 1] H [CSS36 · CS167E · DDR · OPE = 1] H	[$\overline{CSS36}$ · CS25E + CSS36 · CS167E = 0] kept [$\overline{CSS36}$ · CS25E + CSS36 · CS167E = 1] T	[$\overline{CSS36}$ · CS25E + CSS36 · CS167E = 0] I/O port [$\overline{CSS36}$ · CS25E · $\overline{DDR}$ = 1] Input port [CSS36 · CS167E · $\overline{DDR}$ = 1] Input port [$\overline{CSS36}$ · CS25E · DDR = 1] $\overline{CS3}$ [CSS36 · CS167E · DDR = 1] $\overline{CS6}$
	7	T	T	kept	kept	I/O port
PG0/$\overline{ADTRG}$/ $\overline{IRQ6}$	4 to 7	T	T	kept	kept	I/O port

Legend

H:	High level
L:	Low level
T:	High impedance
kept:	Input port becomes high-impedance, output port retains state
DDR:	Data direction register
OPE:	Output port enable
WAITE:	Wait input enable
BRLE:	Bus release enable
BREQOE:	BREQO pin enable
AnE:	Address n enable (n = 23 to 20)
ASOD:	AS output disable
CS167E:	CS167 enable
CS25E:	CS25 enable
CSS36:	CS36 select
CSS17:	CS17 select
PF1CS5S:	Port F1 chip select 5 select
PF0CS4S:	Port F0 chip select 4 select
LWROD:	LWR output disable
DAOEn:	D/A output enable n (n = 0, 1)

5.14 I/O Port Block Diagrams

5.14.1 Port 1

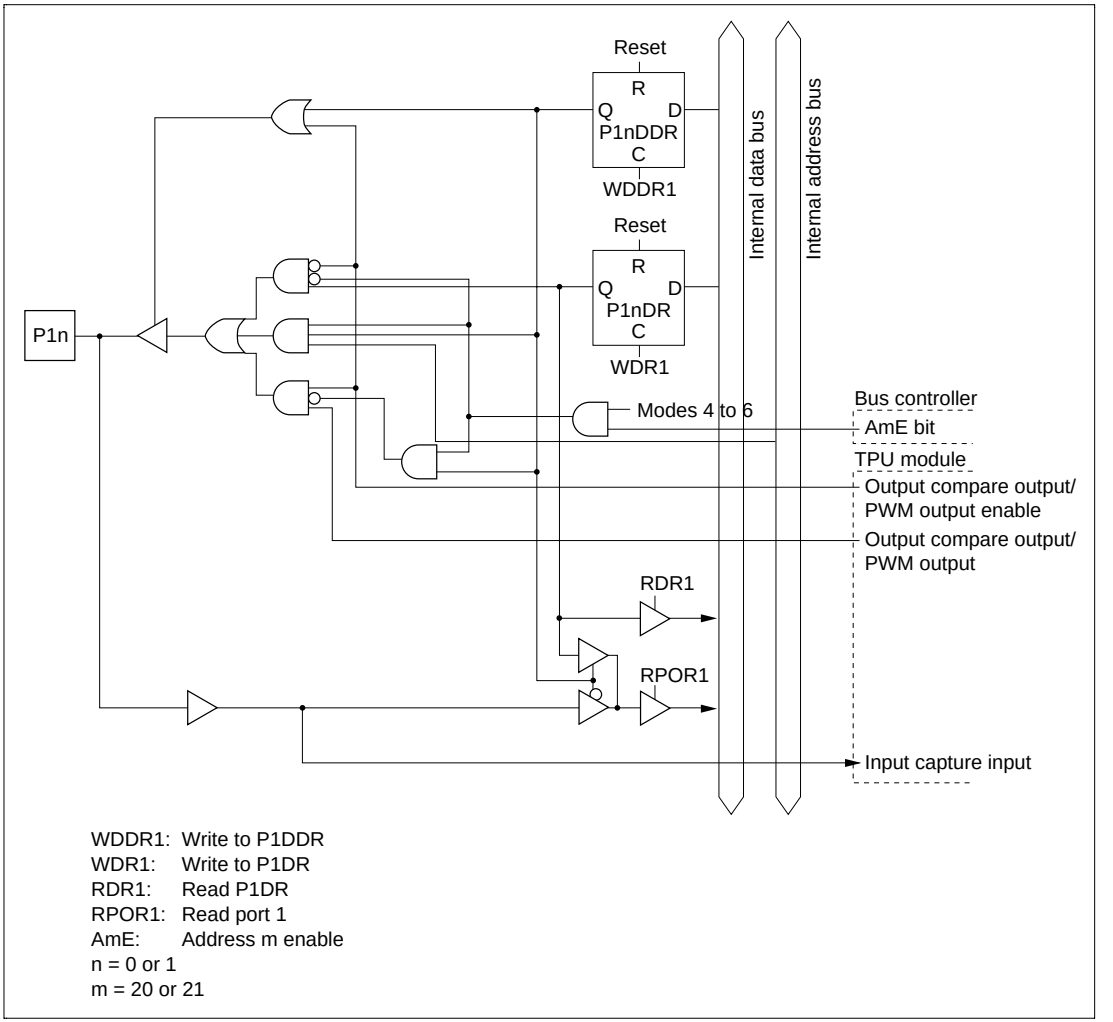


Figure 5.25 (a) Port 1 Block Diagram (Pins P10 and P11)

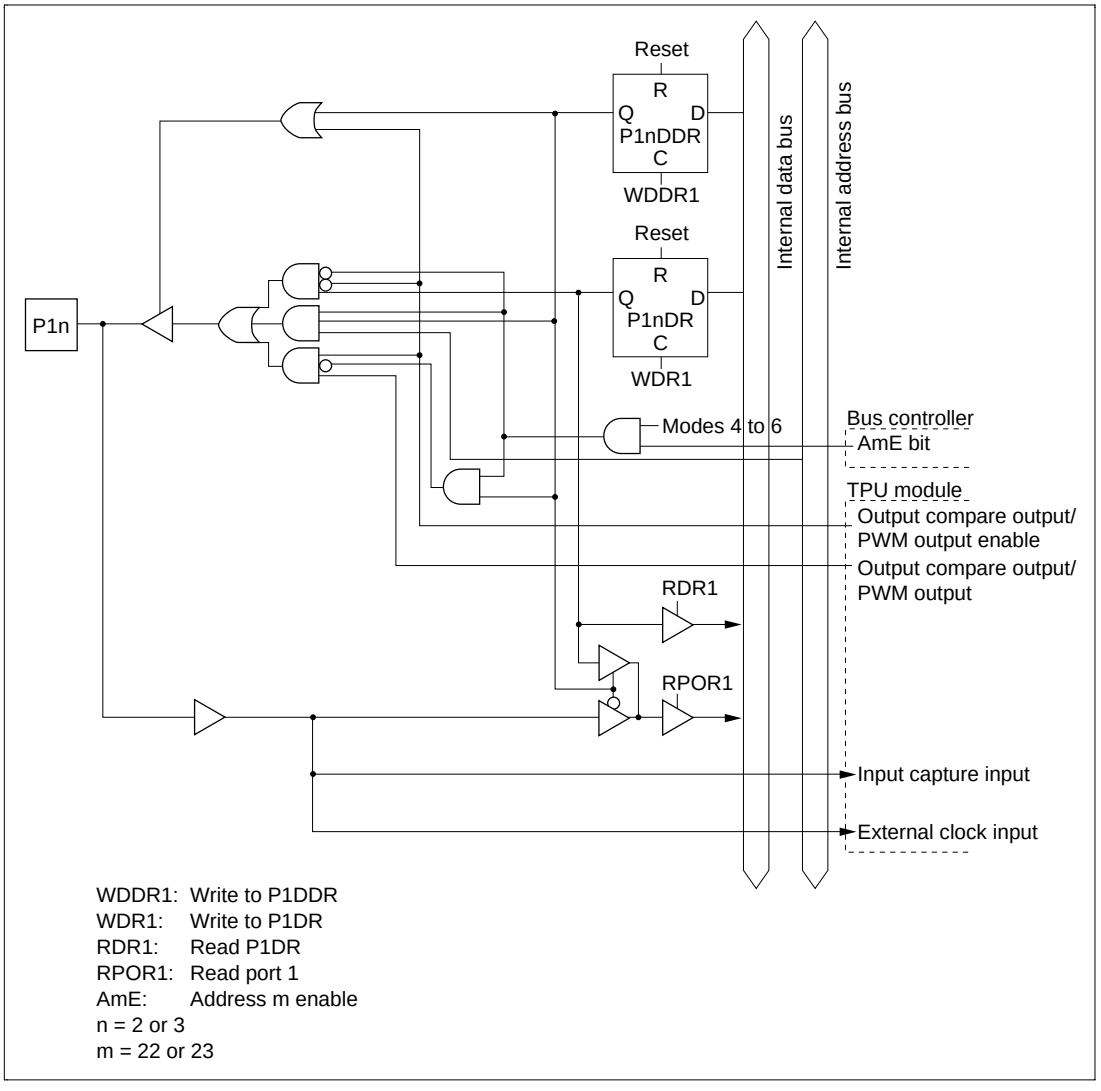


Figure 5.25 (b) Port 1 Block Diagram (Pins P12 and P13)

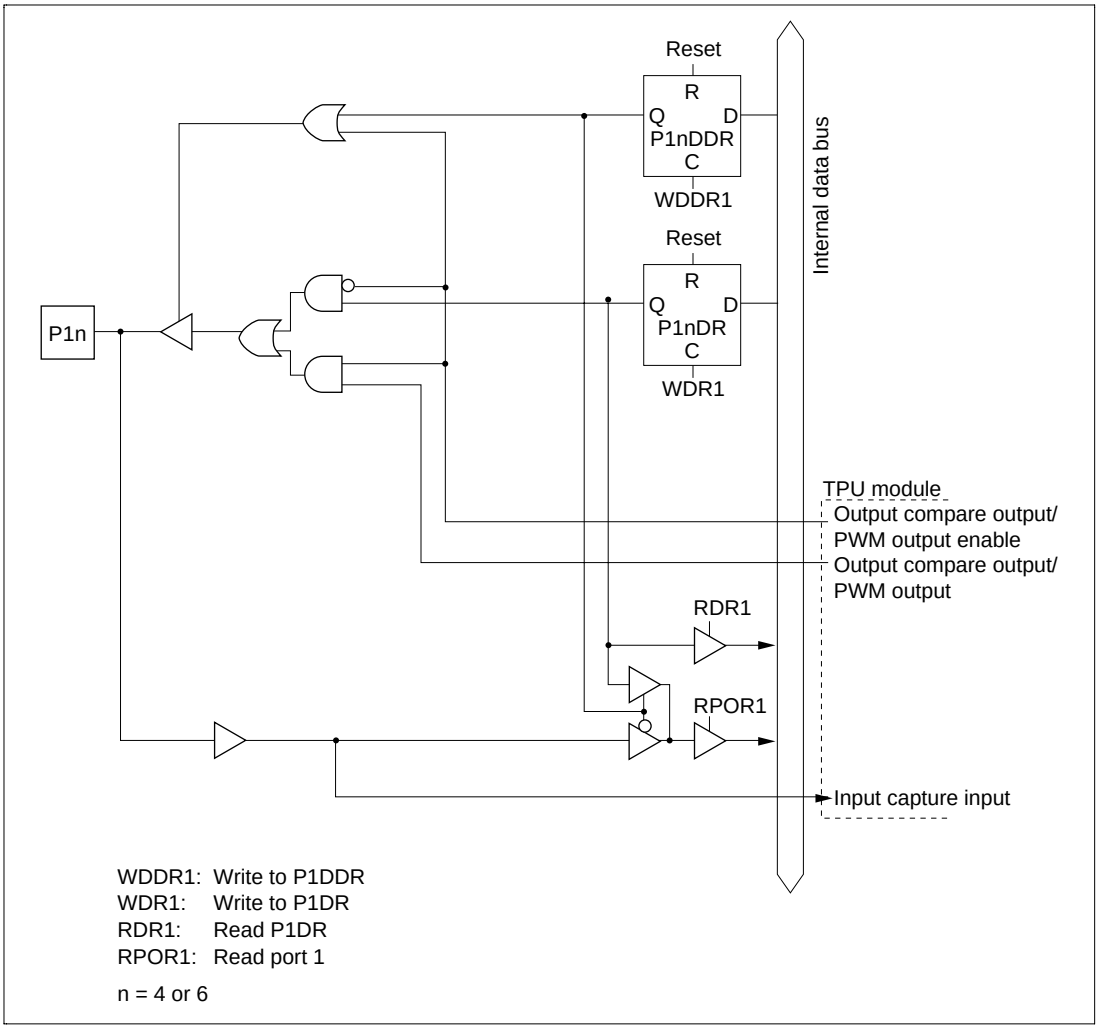


Figure 5.25 (c) Port 1 Block Diagram (Pins P14 and P16)

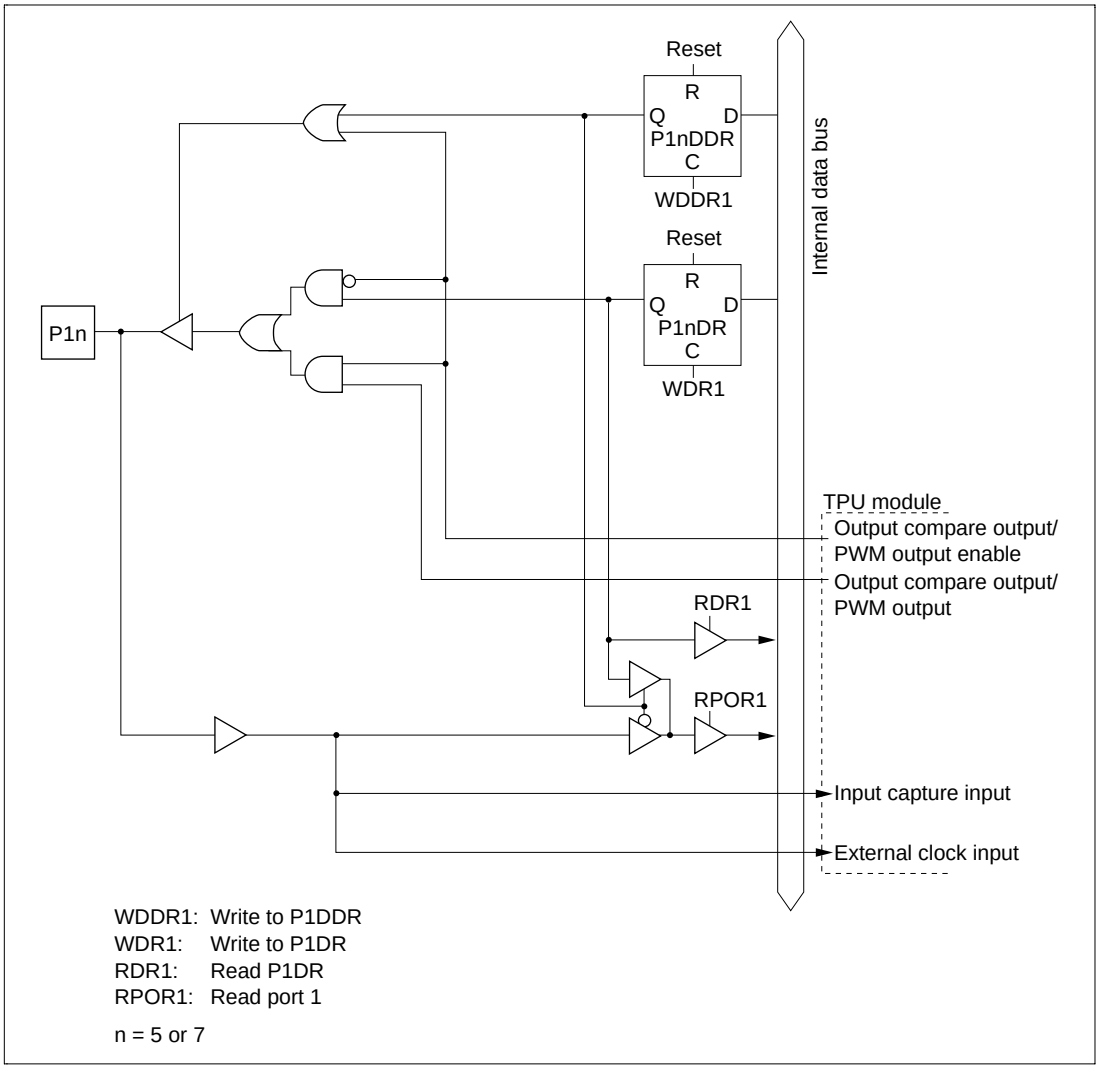


Figure 5.25 (d) Port 1 Block Diagram (Pins P15 and P17)

5.14.2 Port 2

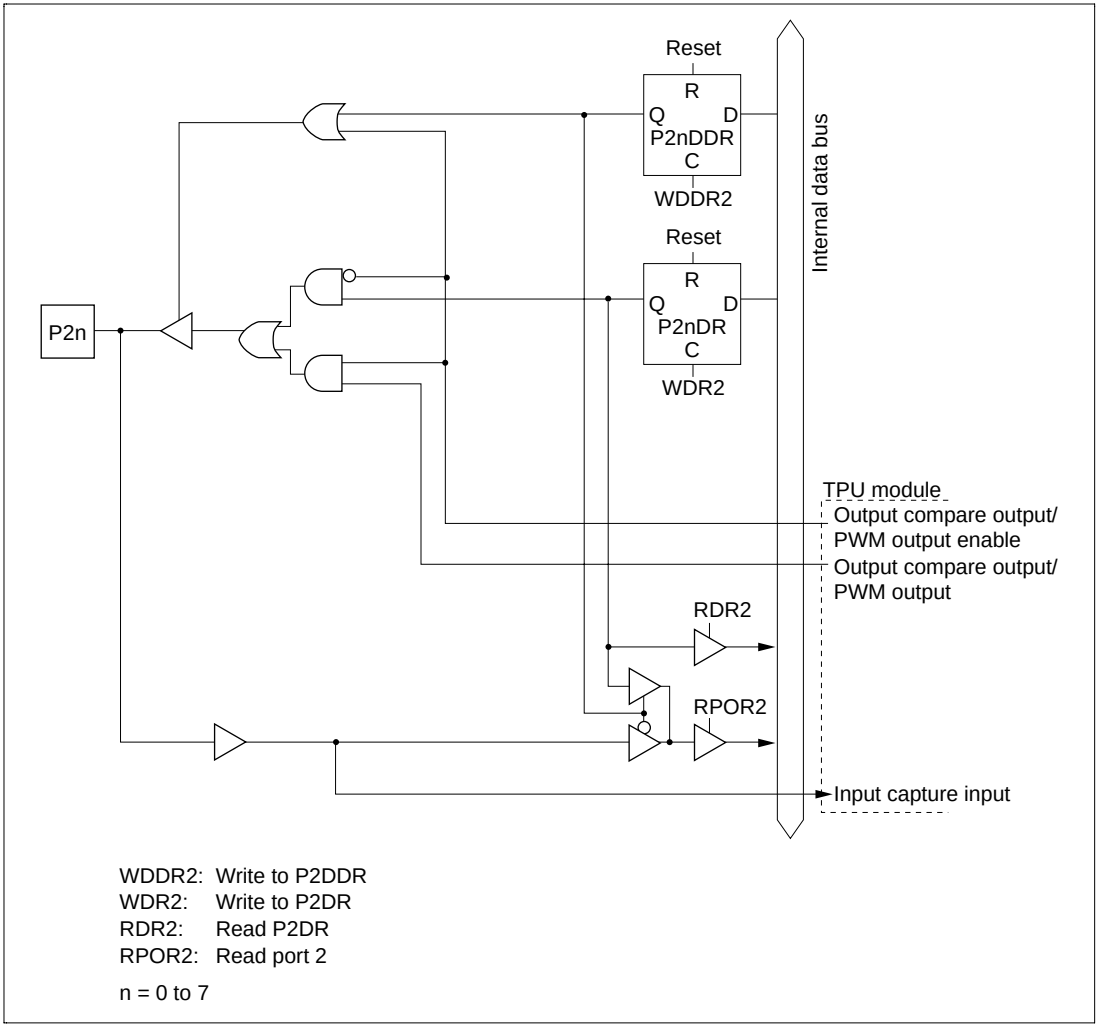


Figure 5.26 Port 2 Block Diagram (Pins P2n)

5.14.3 Port 3

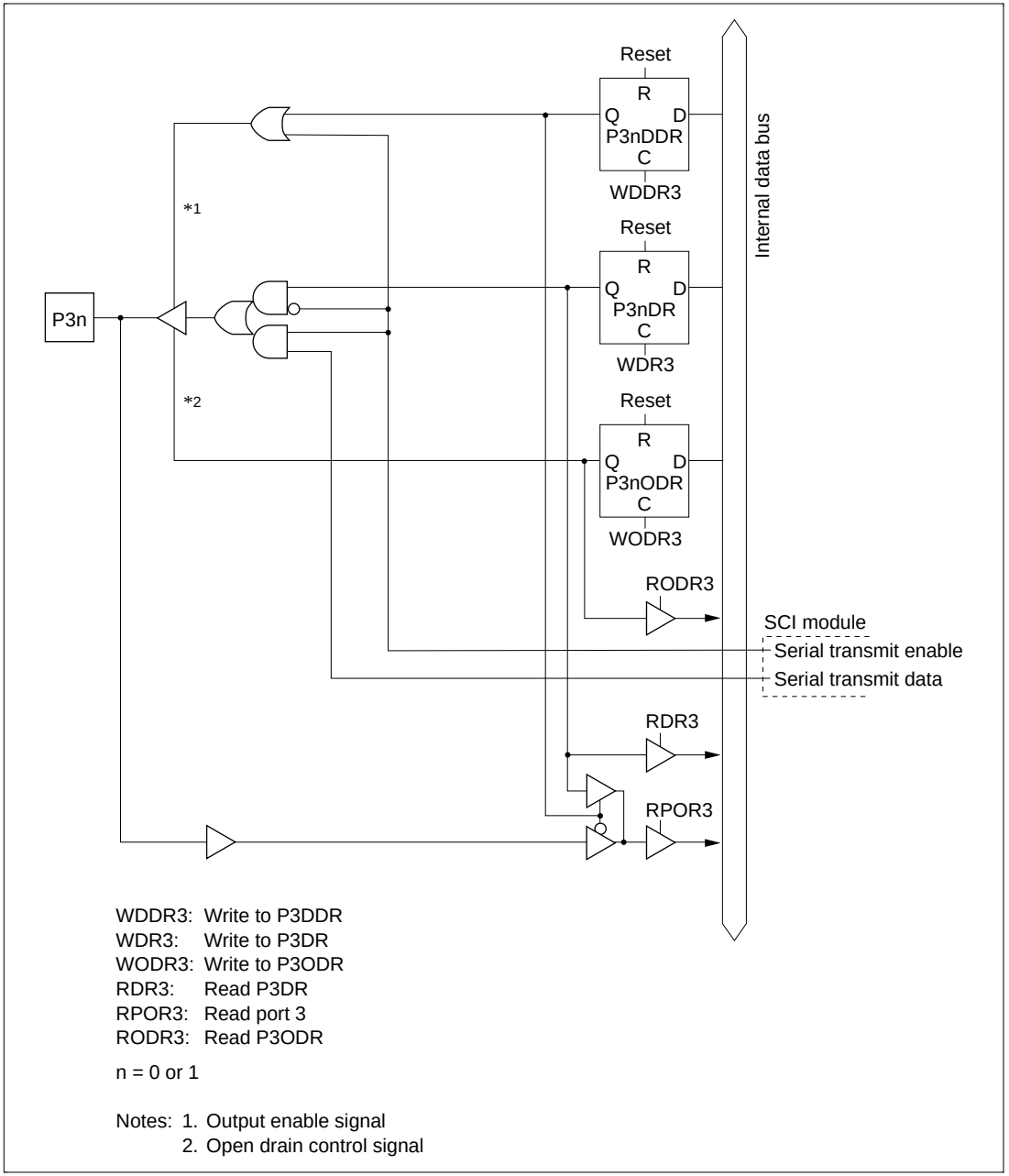
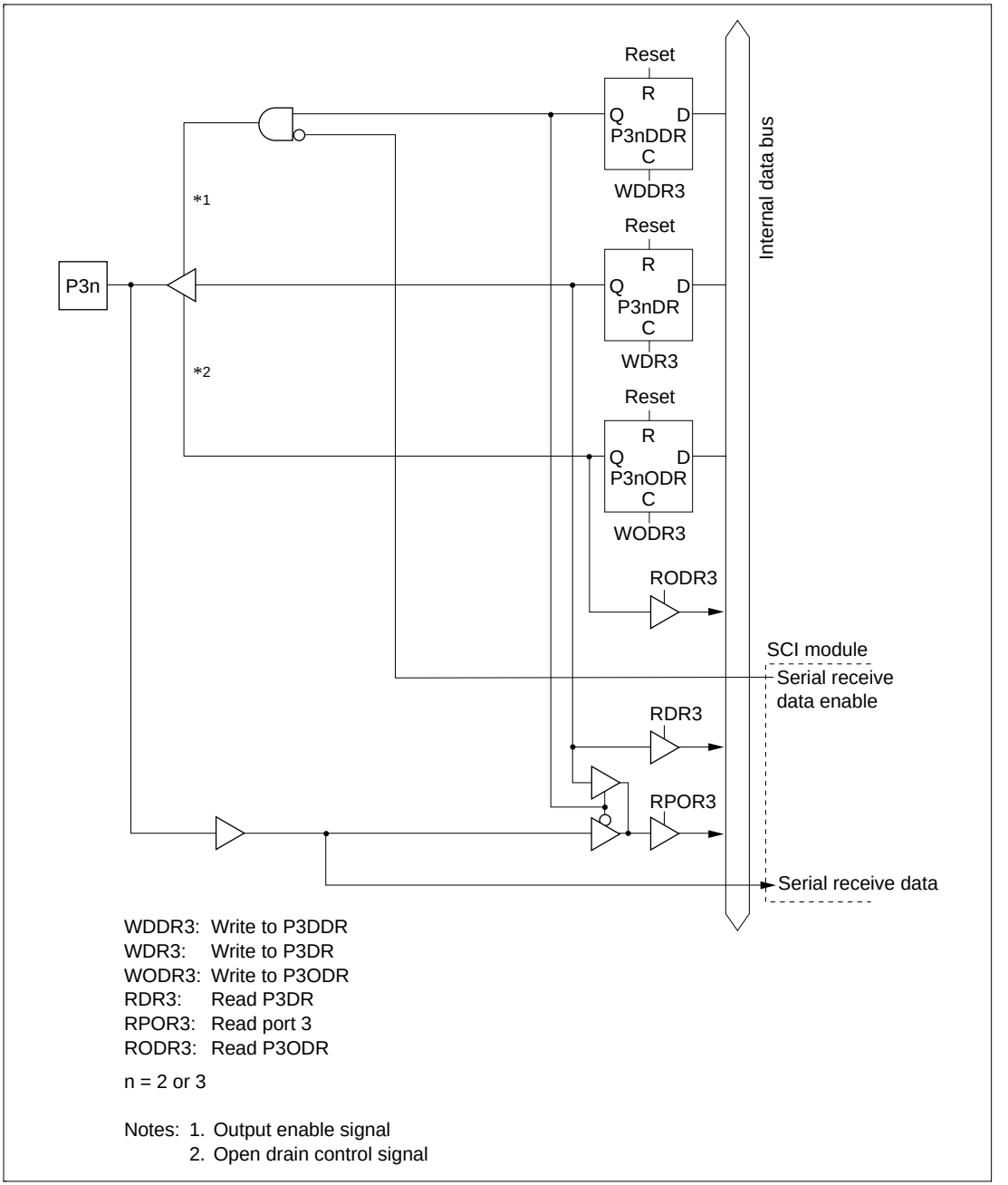


Figure 5.27 (a) Port 3 Block Diagram (Pins P30 and P31)



WDDR3: Write to P3DDR
WDR3: Write to P3DR
WODR3: Write to P3ODR
RDR3: Read P3DR
RPOR3: Read port 3
RODR3: Read P3ODR

n = 2 or 3

Notes: 1. Output enable signal
2. Open drain control signal

Figure 5.27 (b) Port 3 Block Diagram (Pins P32 and P33)

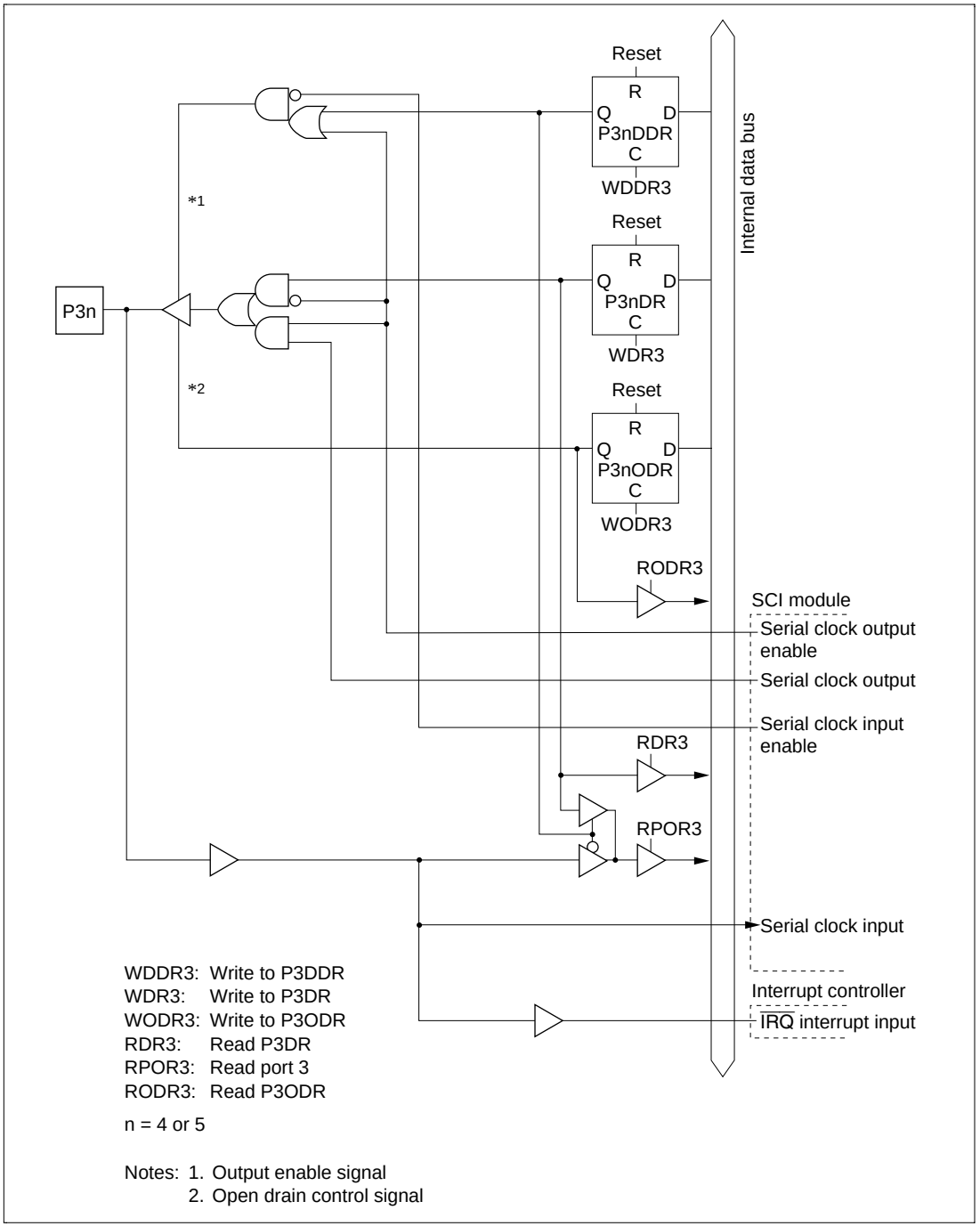


Figure 5.27 (c) Port 3 Block Diagram (Pins P34 and P35)

5.14.4 Port 4

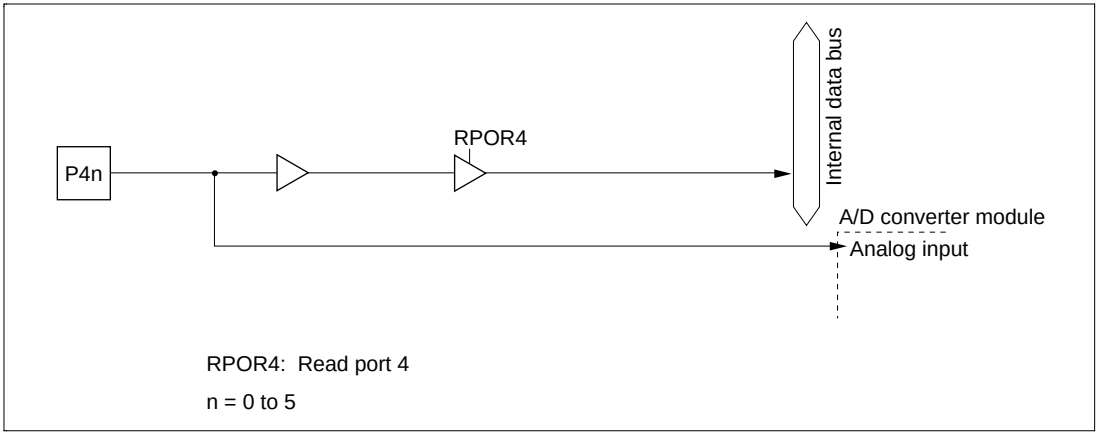


Figure 5.28 (a) Port 4 Block Diagram (Pins P40 to P45)

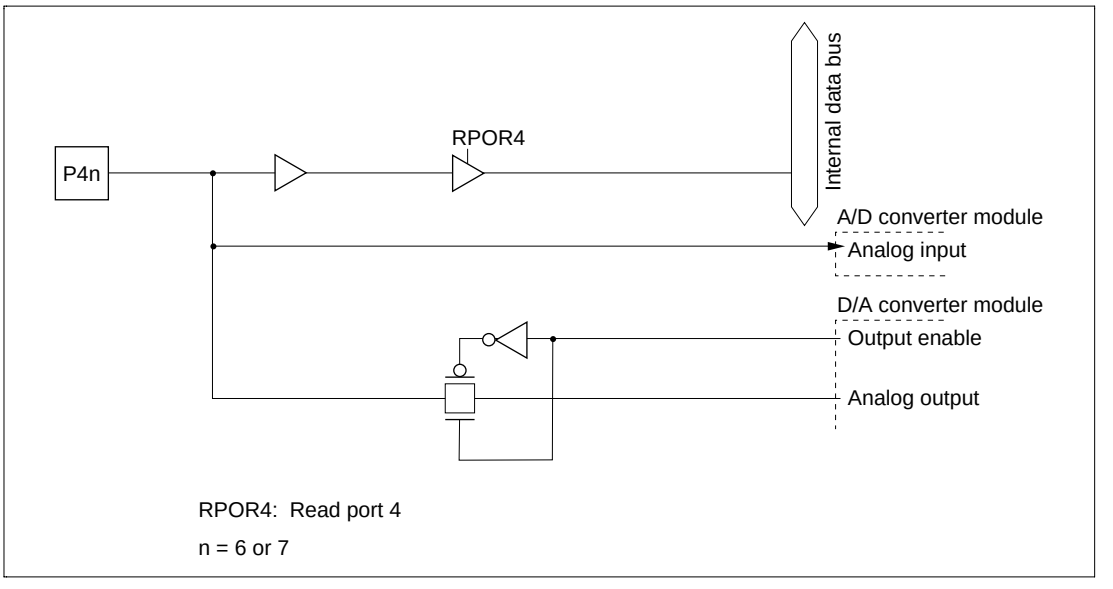


Figure 5.28 (b) Port 4 Block Diagram (Pins P46 and P47)

5.14.5 Port A

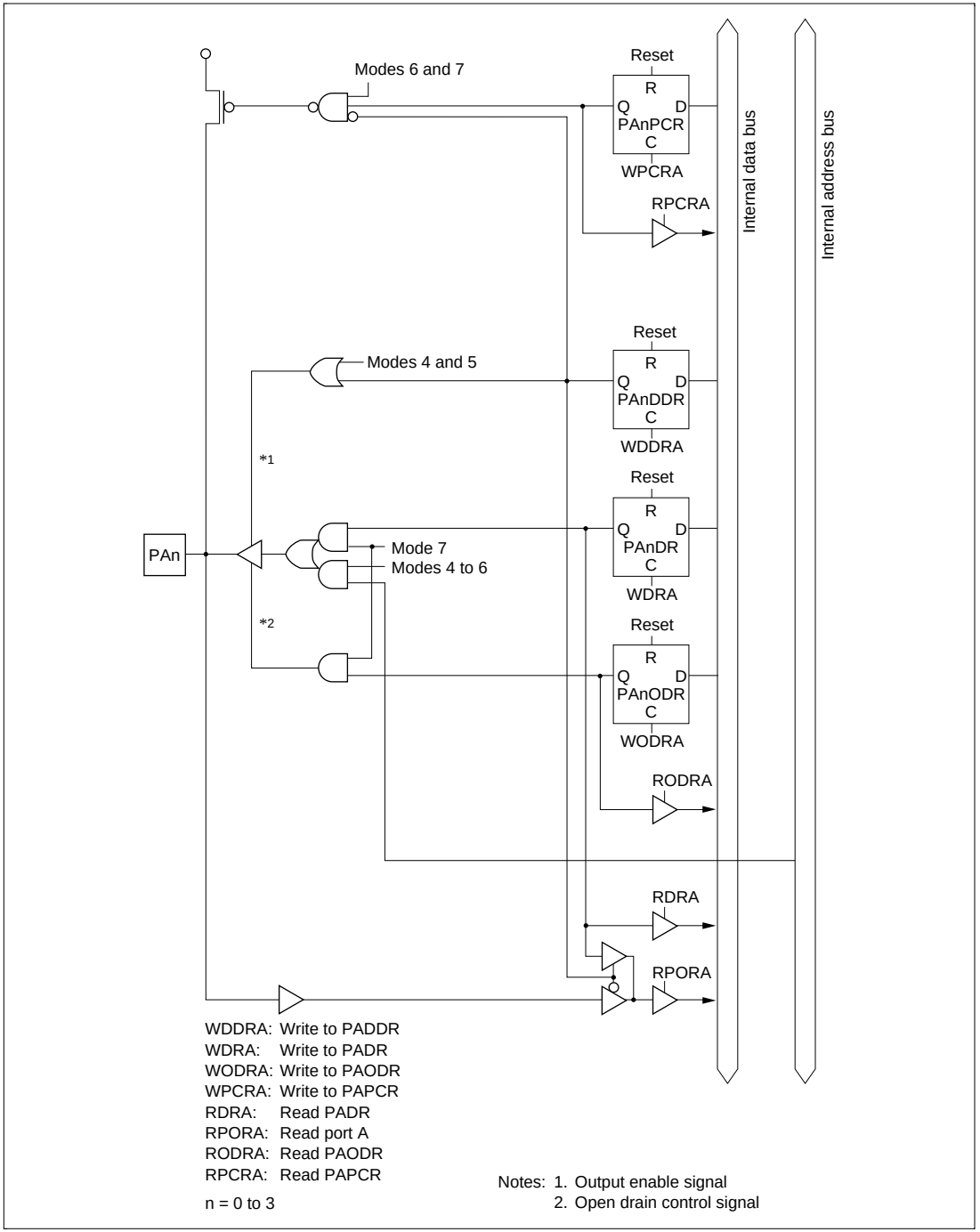


Figure 5.29 Port A Block Diagram (Pins PA0, PA1, PA2, and PA3)

5.14.6 Port B

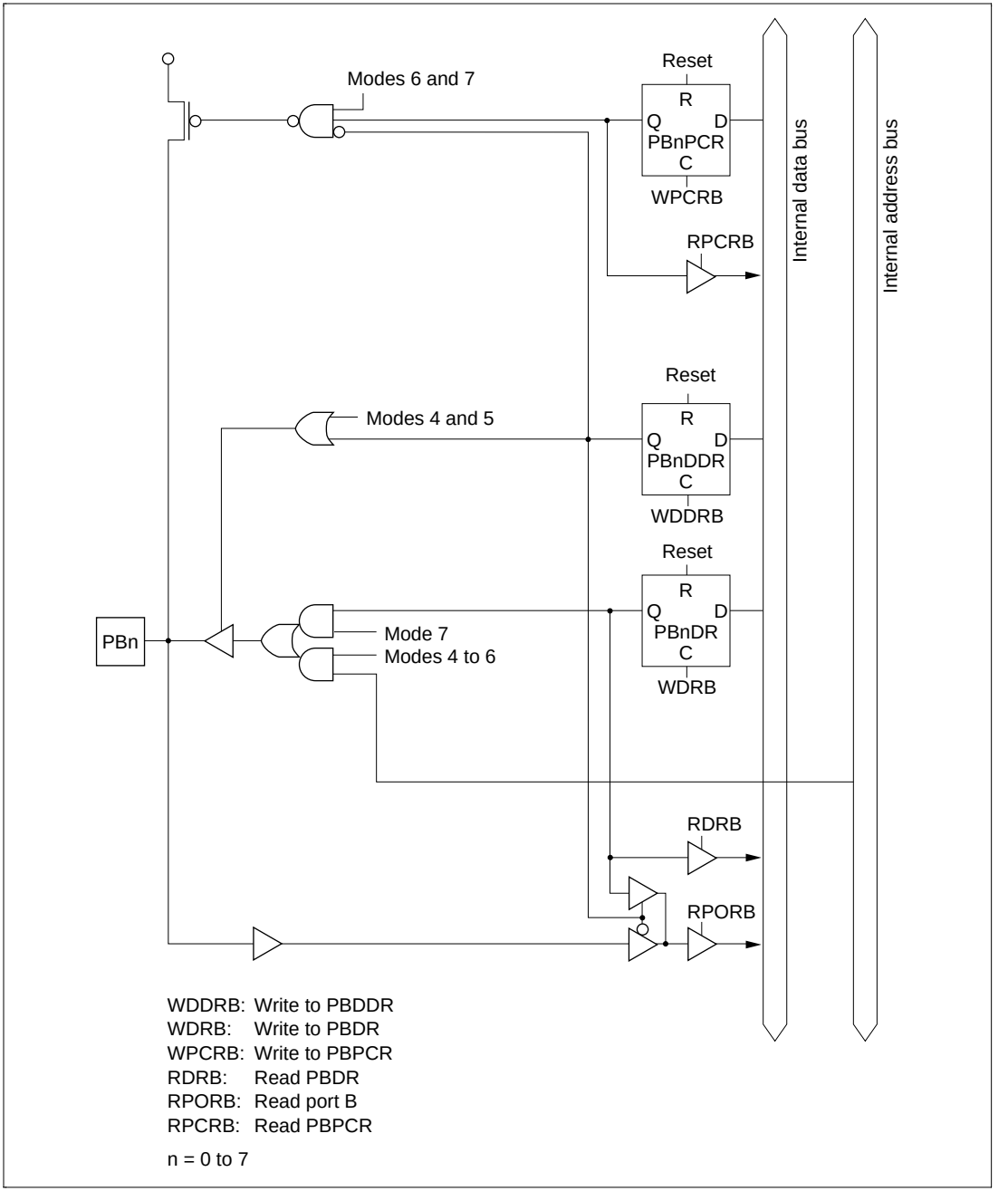


Figure 5.30 Port B Block Diagram (Pins PBn)

5.14.7 Port C

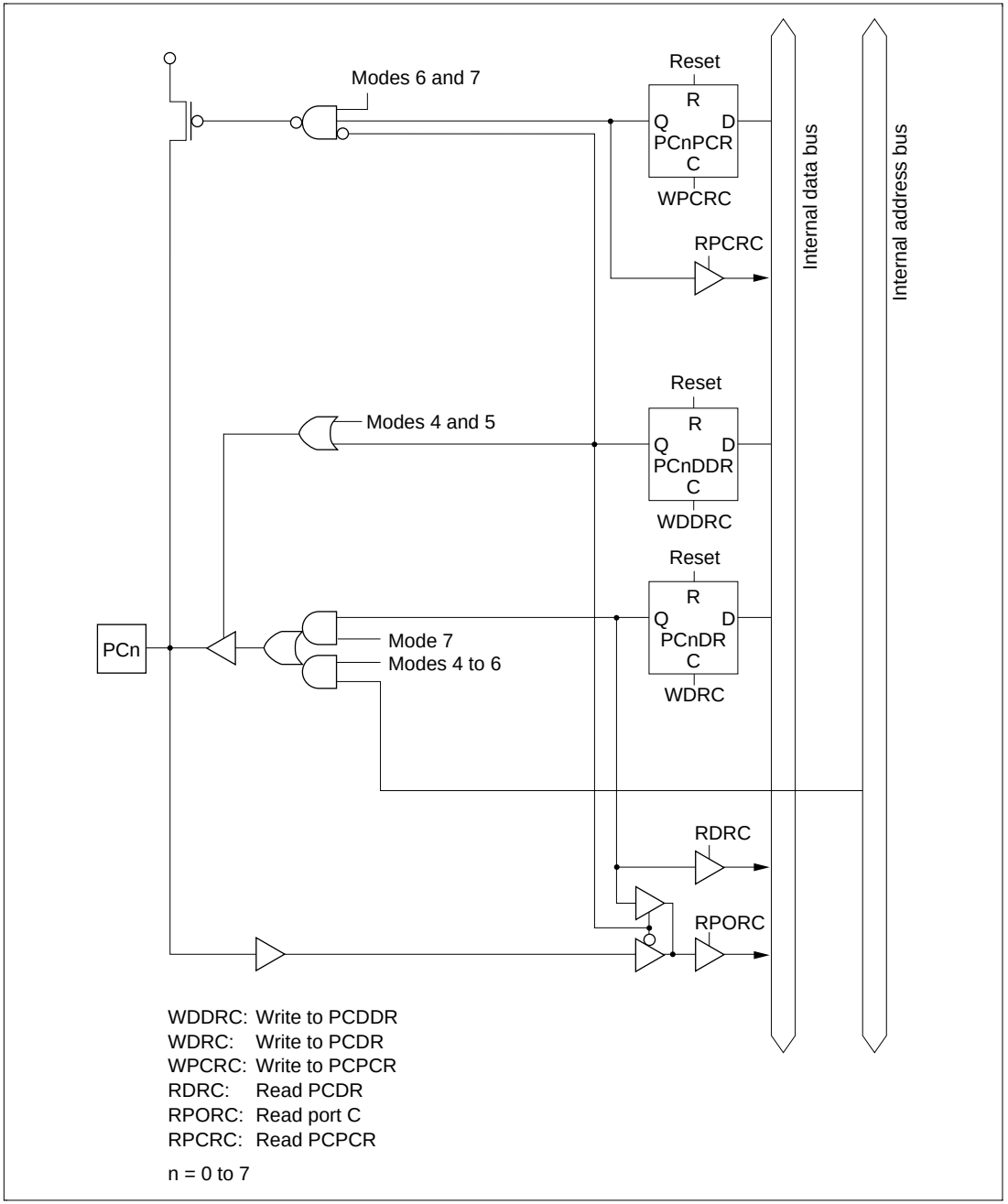


Figure 5.31 Port C Block Diagram (Pins PCn)

5.14.8 Port D

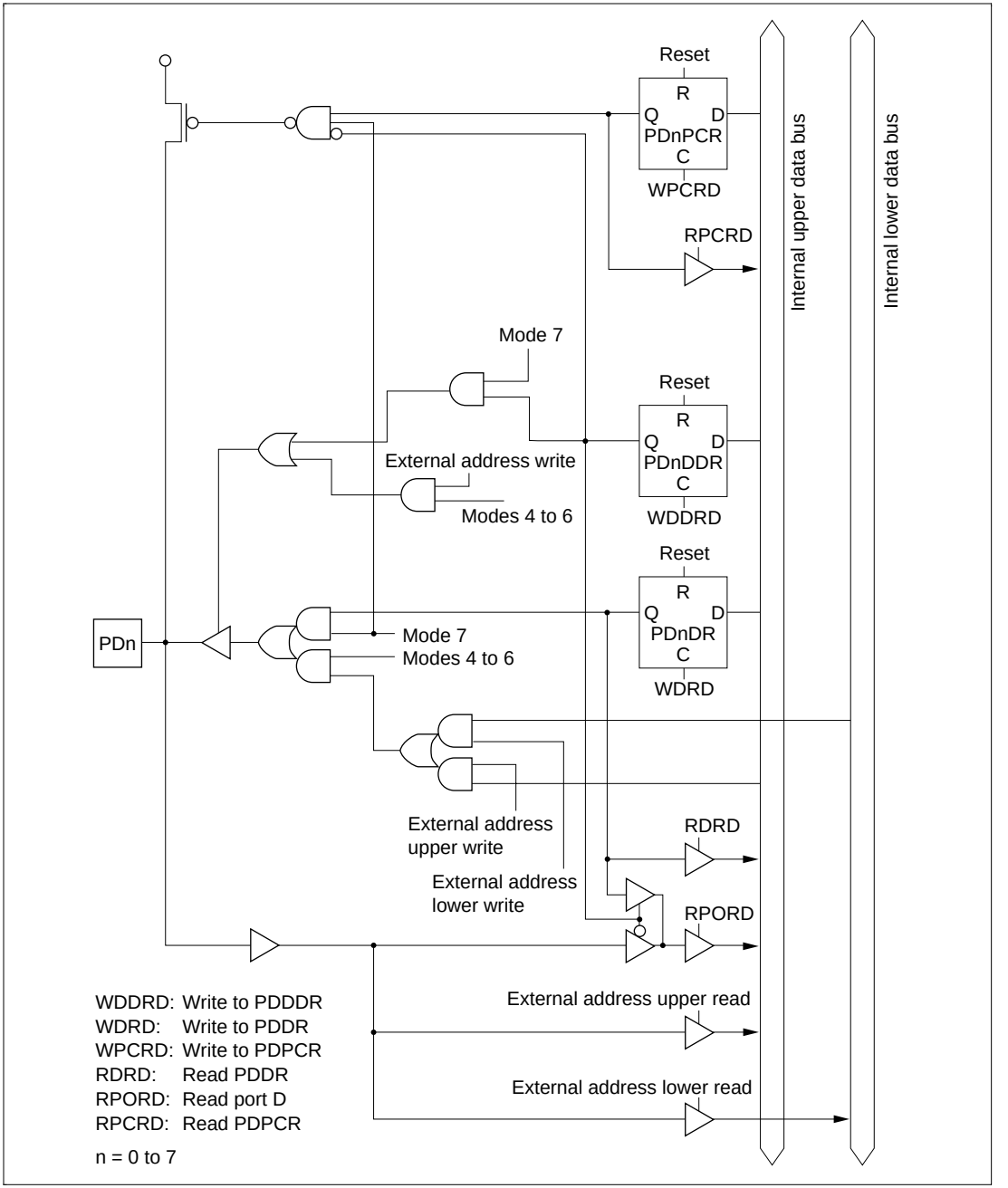


Figure 5.32 Port D Block Diagram (Pins PDn)

5.14.9 Port E

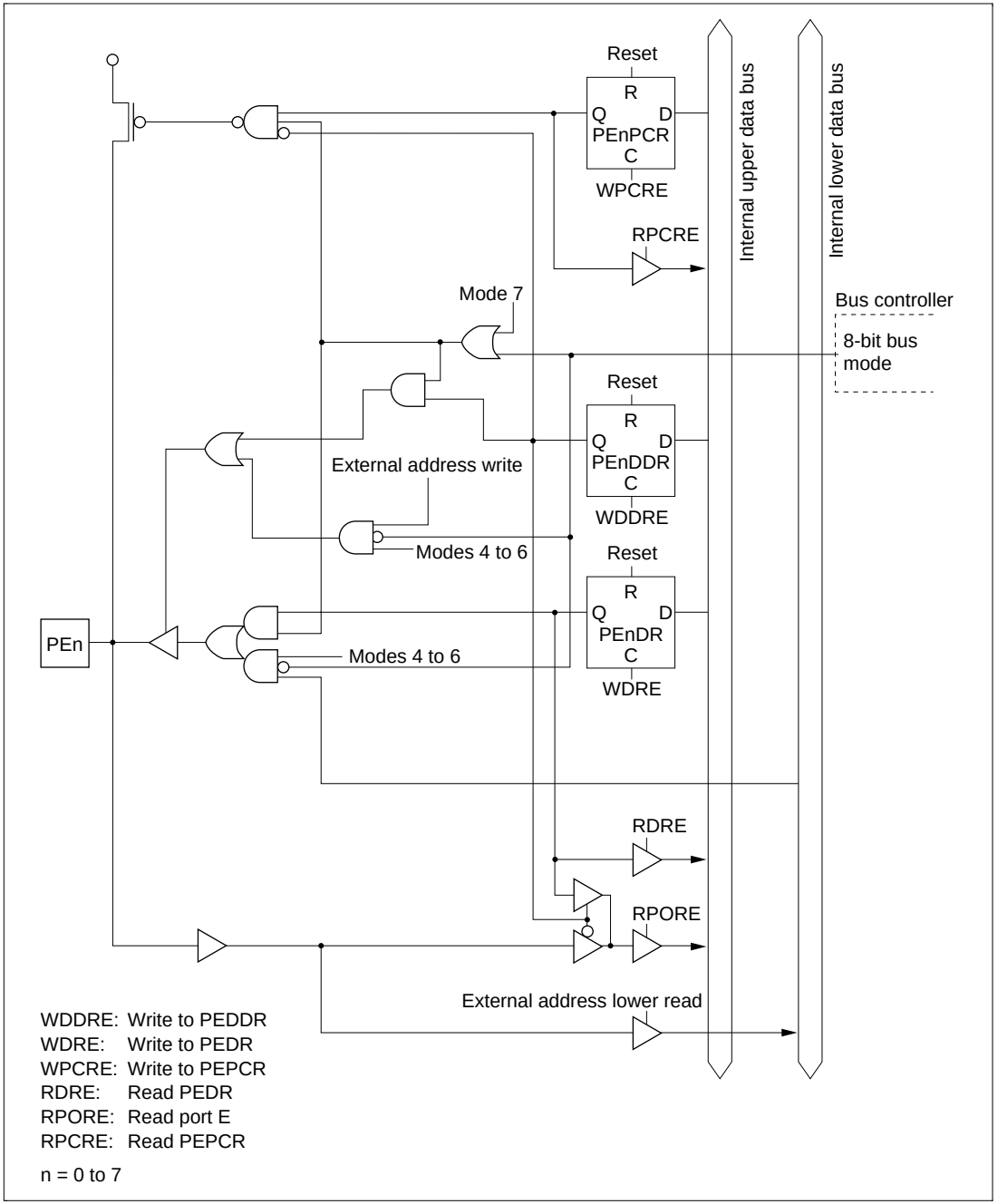


Figure 5.33 Port E Block Diagram (Pins PEn)

5.14.10 Port F

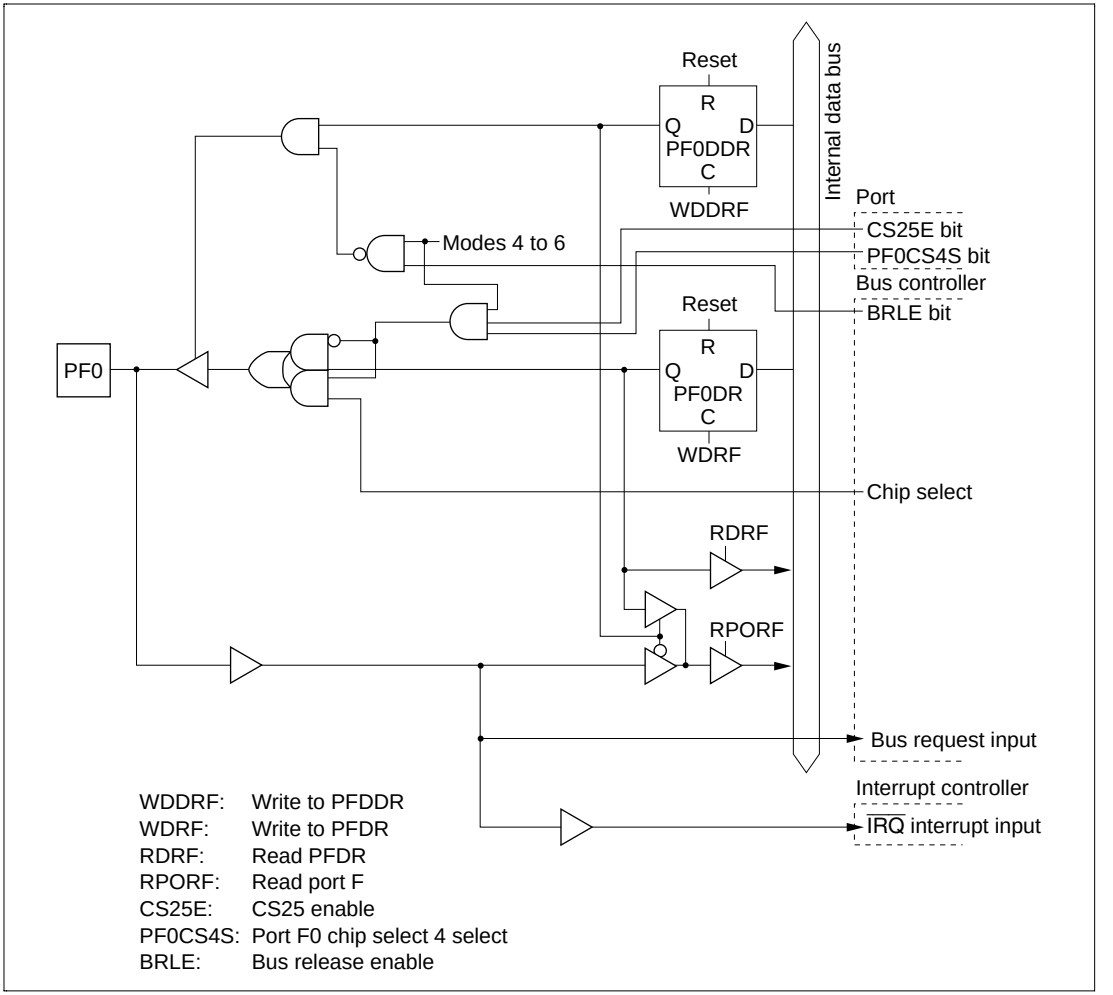


Figure 5.34 (a) Port F Block Diagram (Pin PF0)

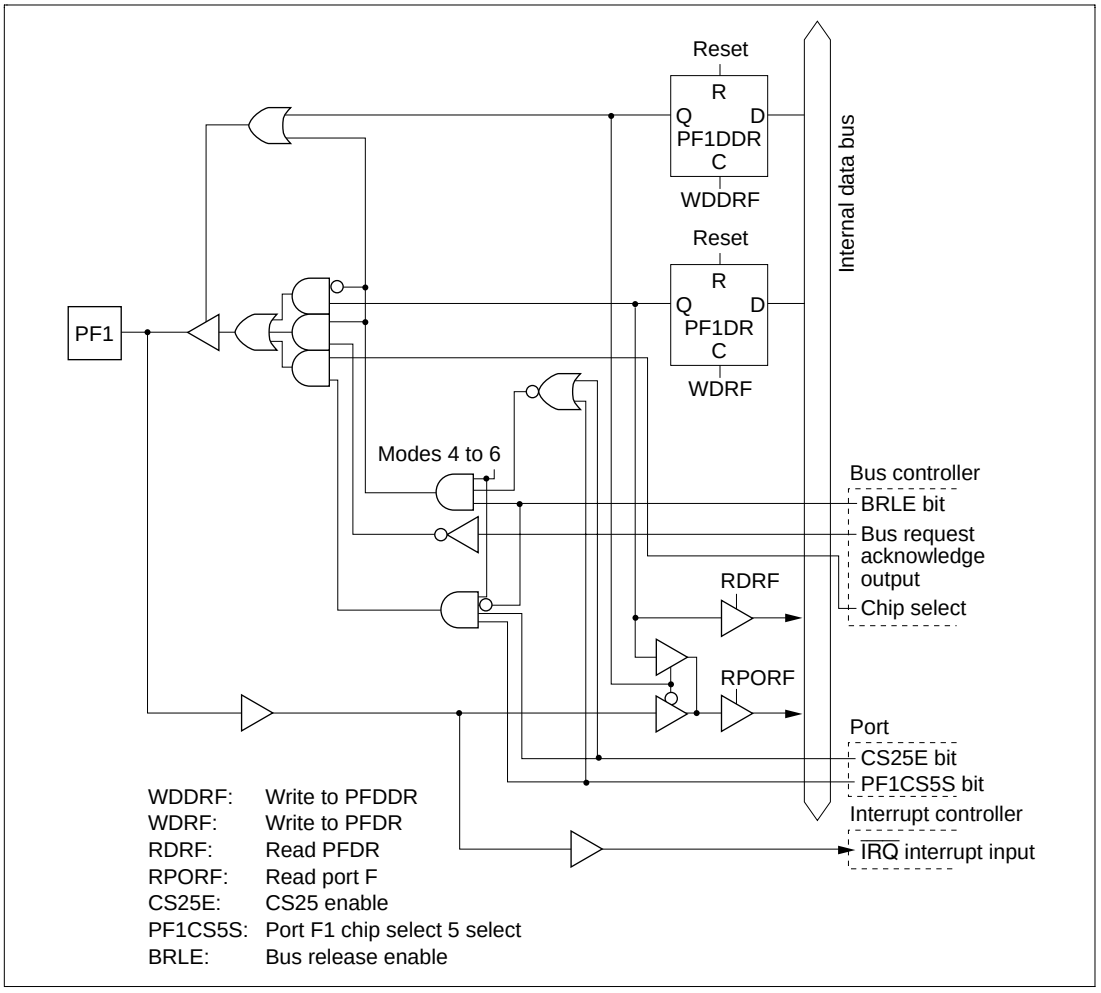


Figure 5.34 (b) Port F Block Diagram (Pin PF1)

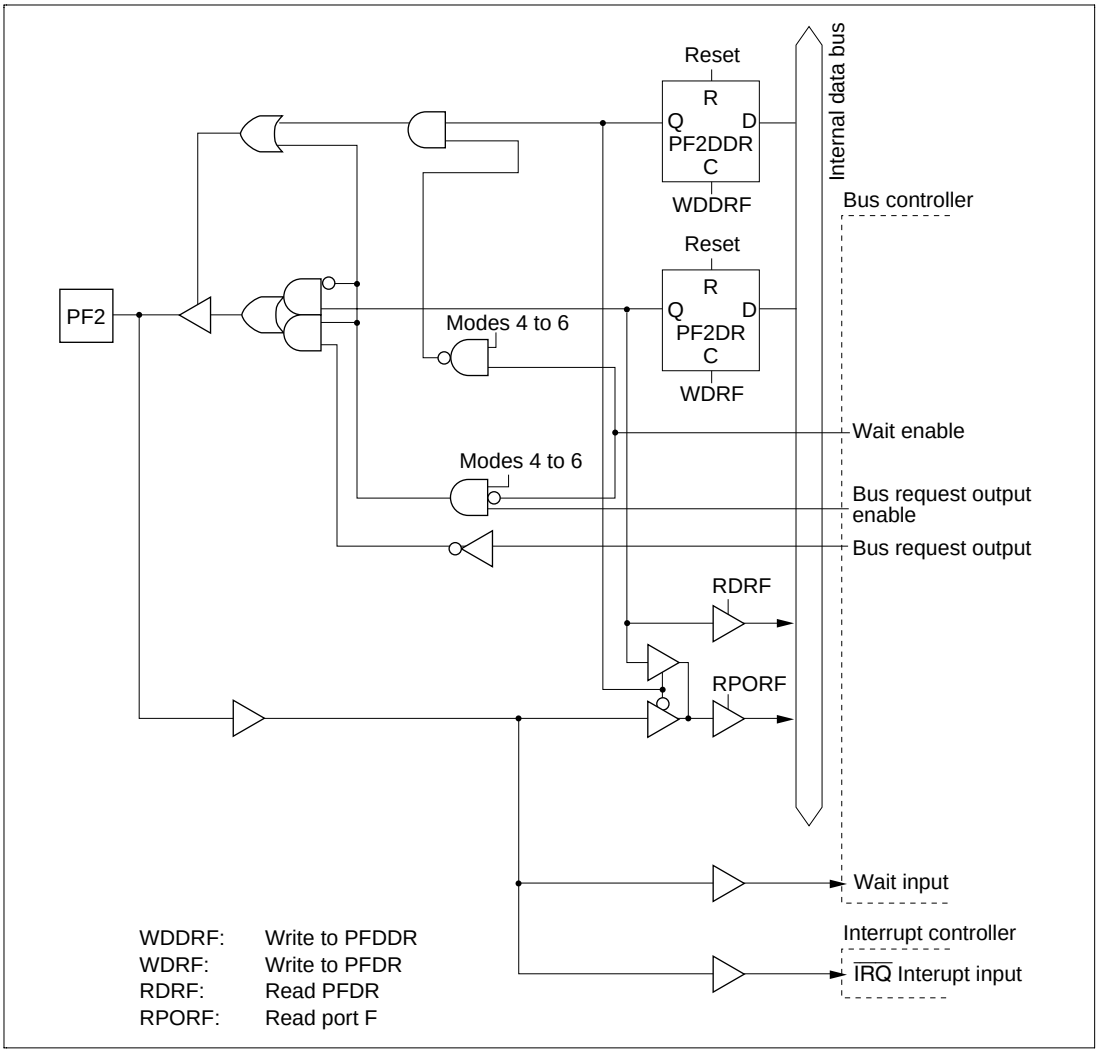


Figure 5.34 (c) Port F Block Diagram (Pin PF2)

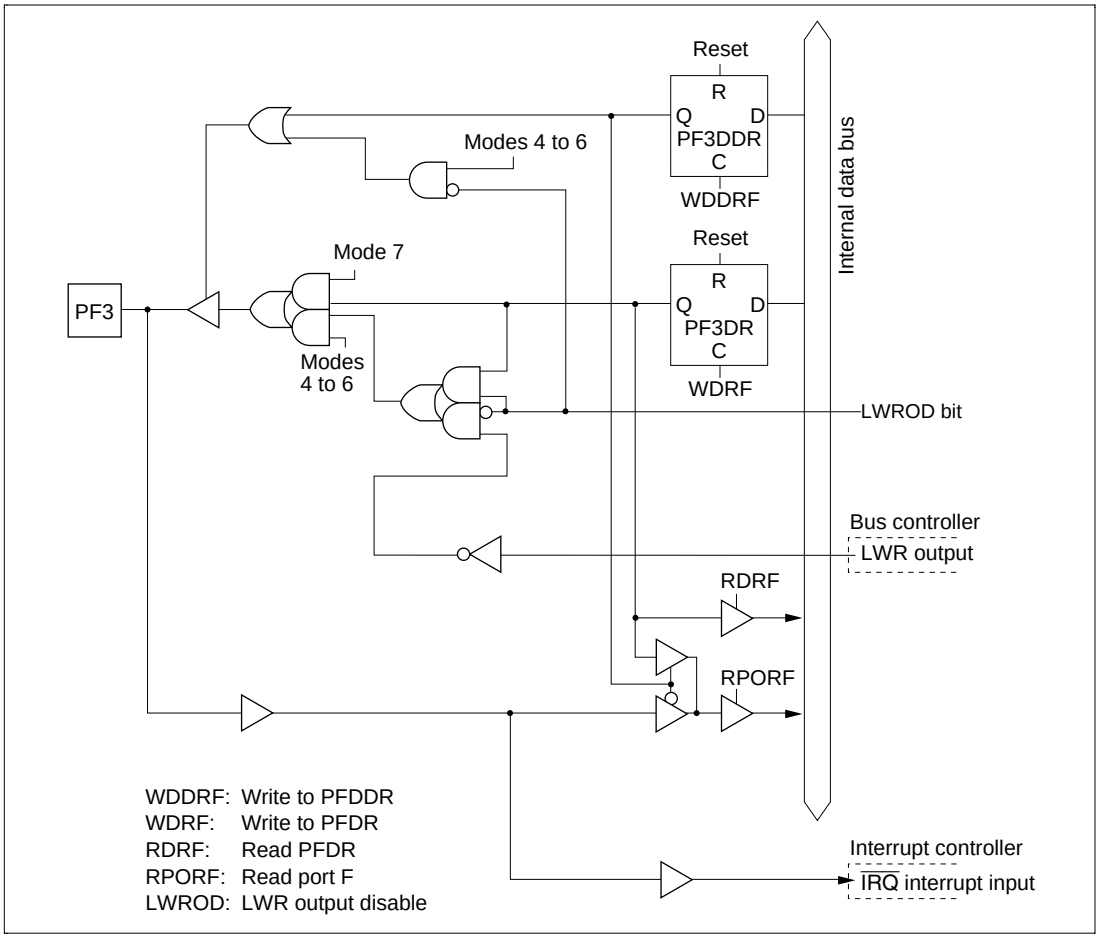


Figure 5.34 (d) Port F Block Diagram (Pin PF3)

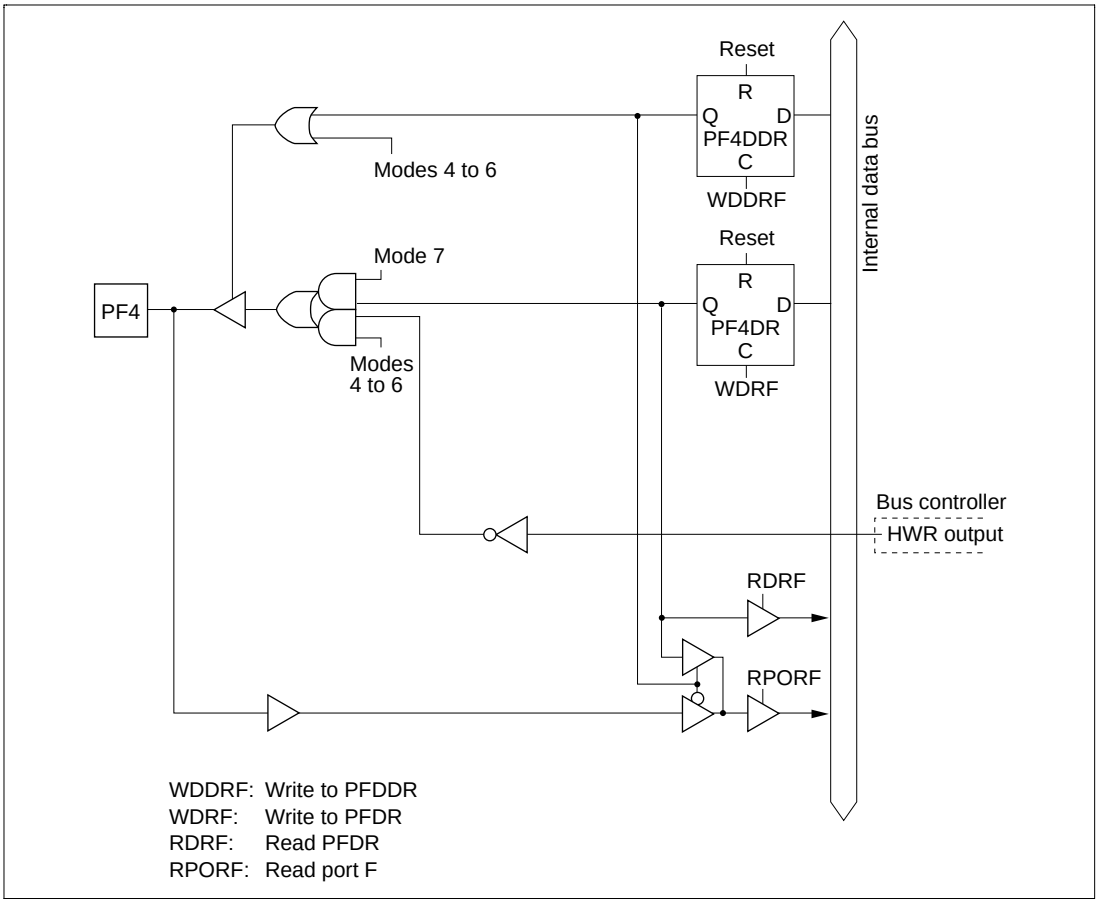


Figure 5.34 (e) Port F Block Diagram (Pin PF4)

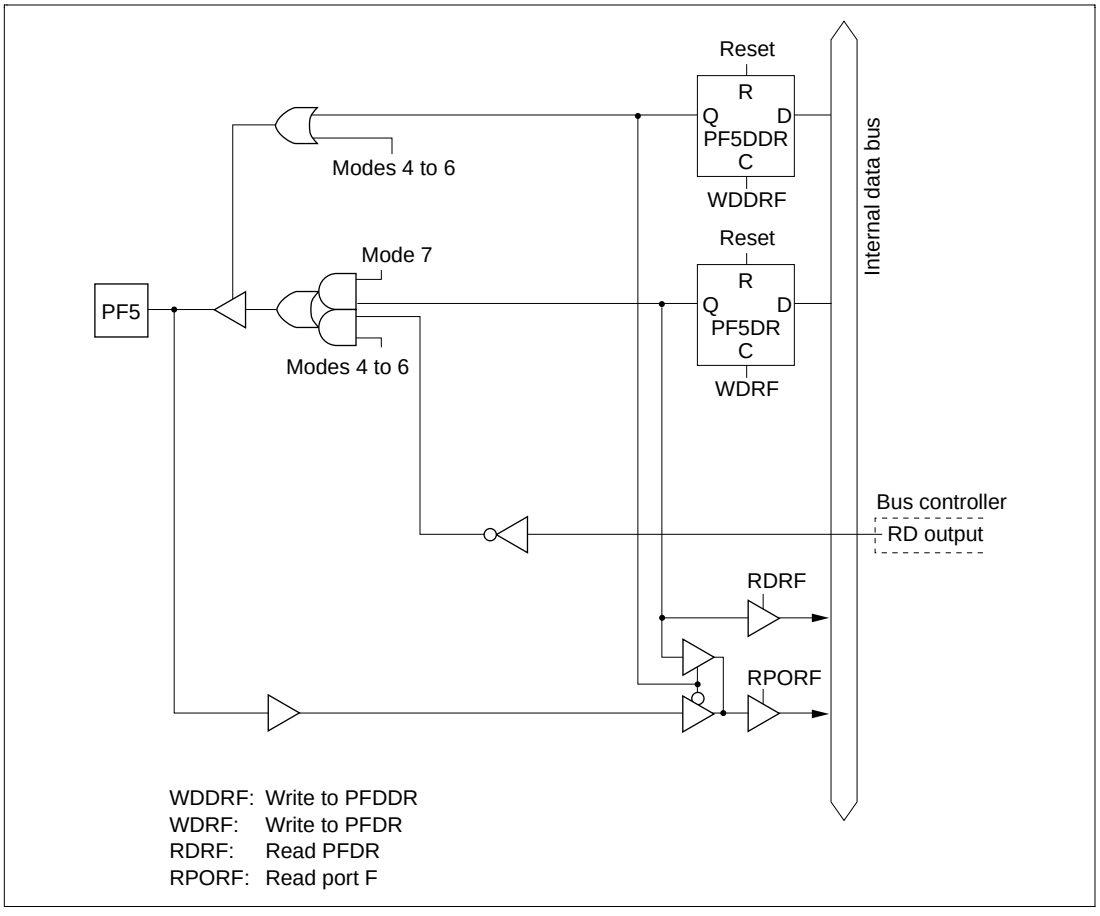


Figure 5.34 (f) Port F Block Diagram (Pin PF5)

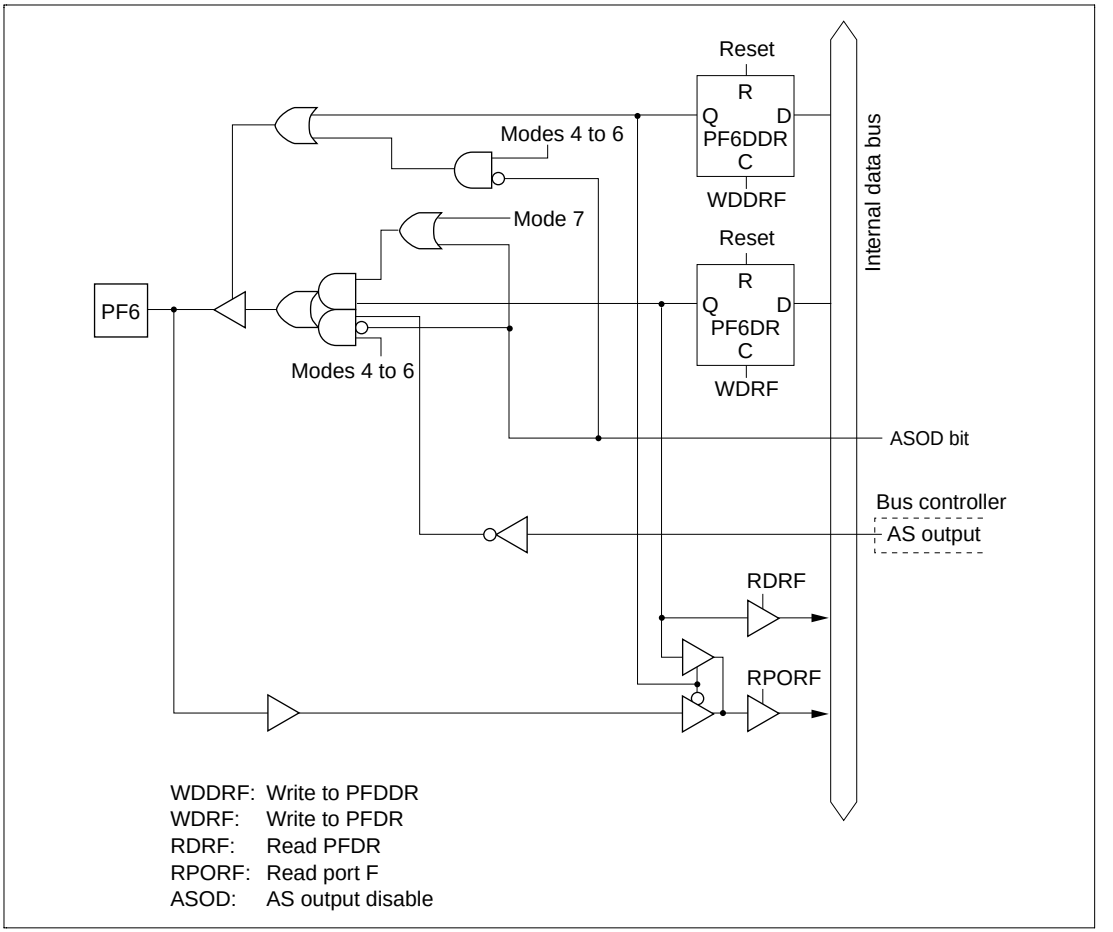


Figure 5.34 (g) Port F Block Diagram (Pin PF6)

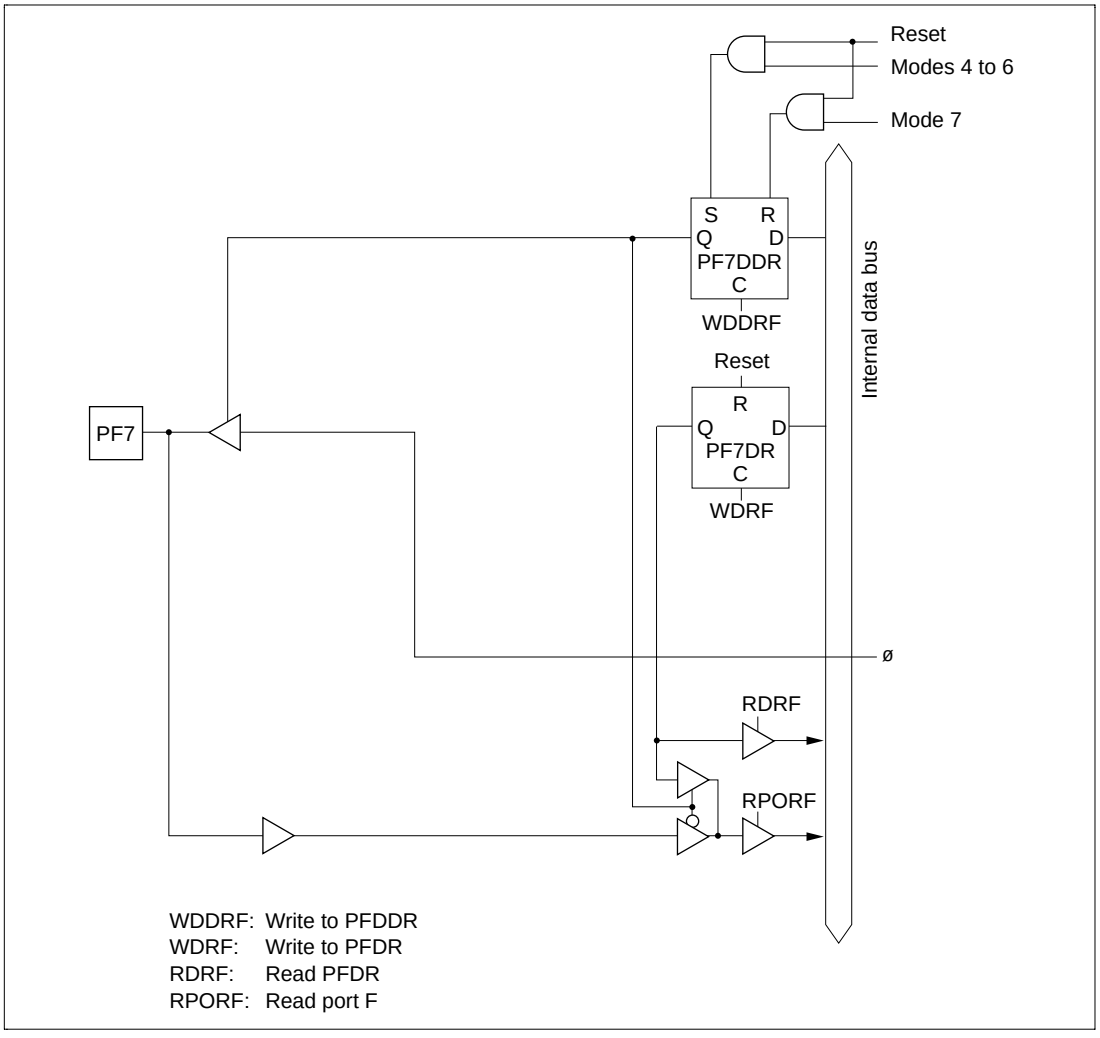


Figure 5.34 (h) Port F Block Diagram (Pin PF7)

5.14.11 Port G

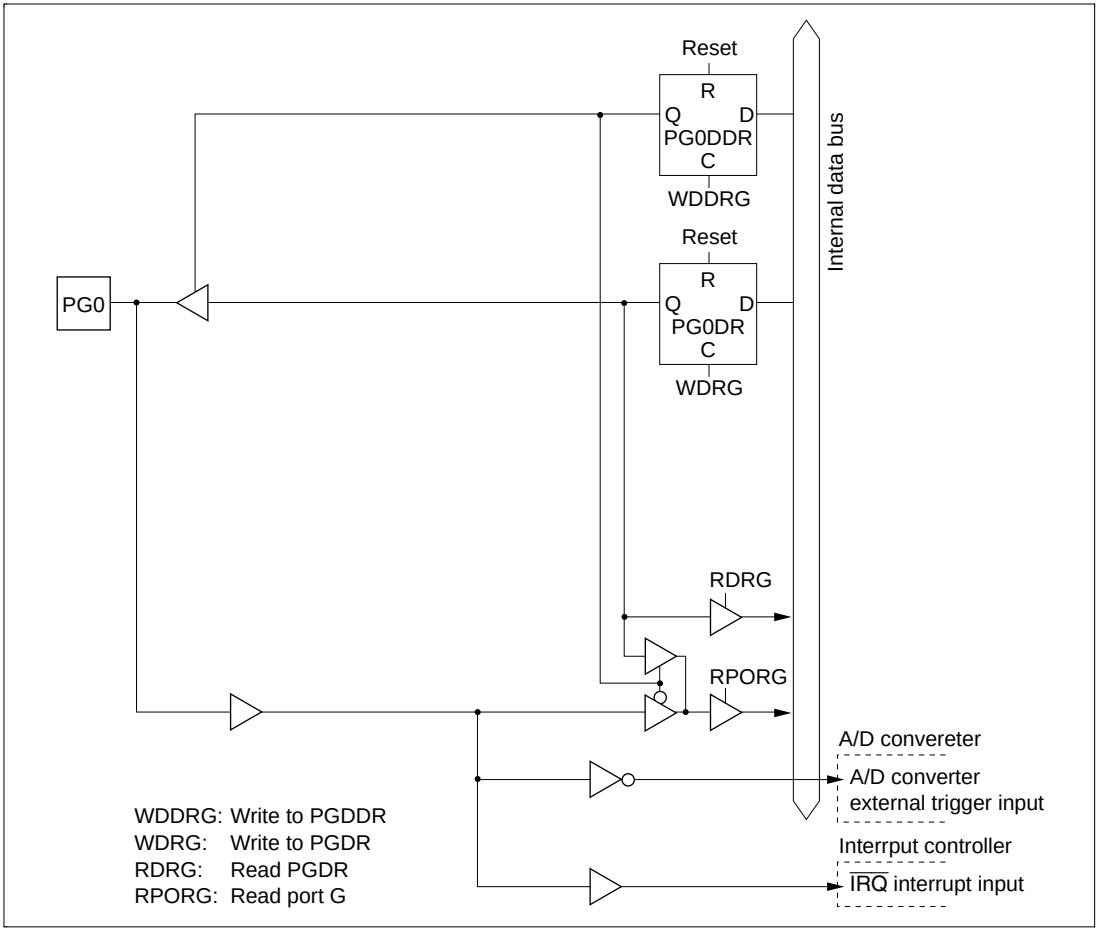


Figure 5.35 (a) Port G Block Diagram (Pin PG0)

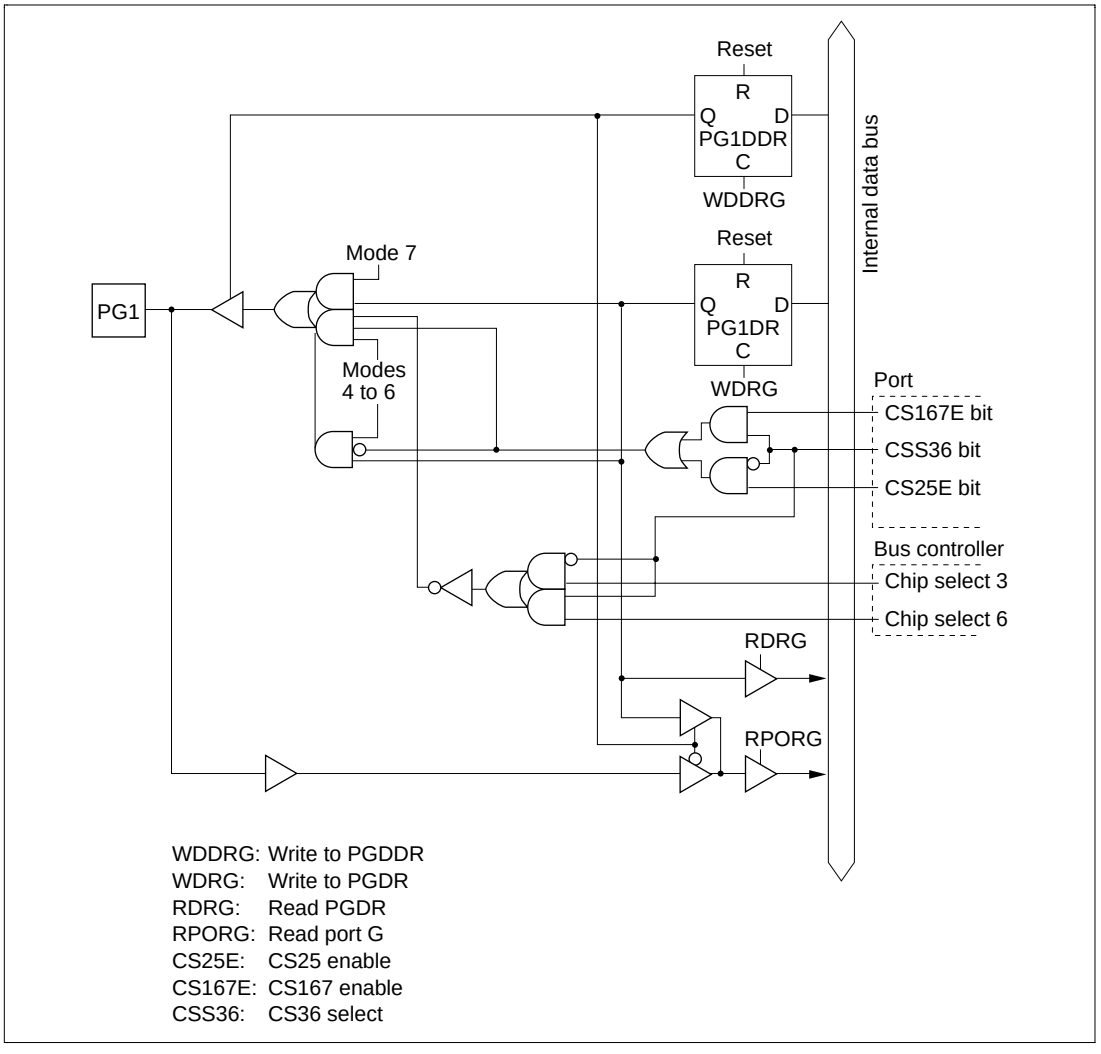


Figure 5.35 (b) Port G Block Diagram (Pin PG1)

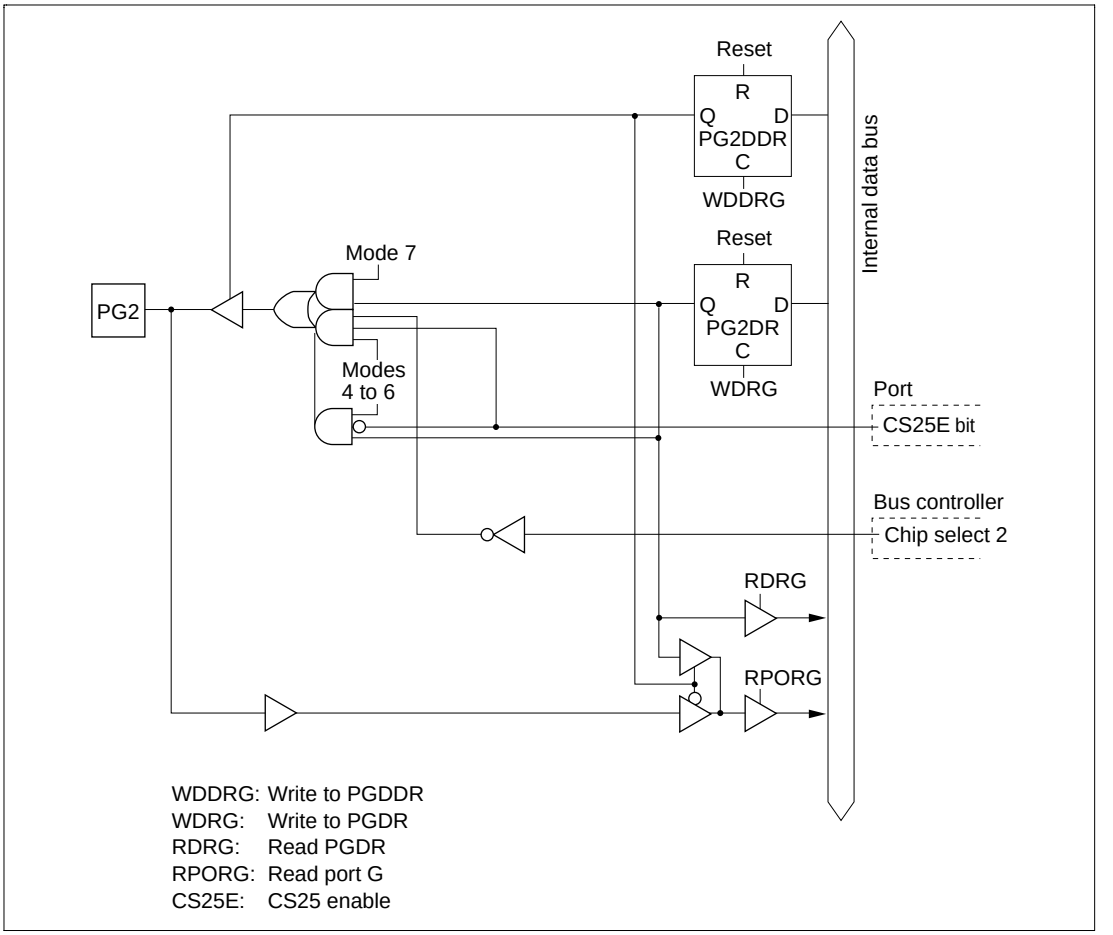


Figure 5.35 (c) Port G Block Diagram (Pin PG2)

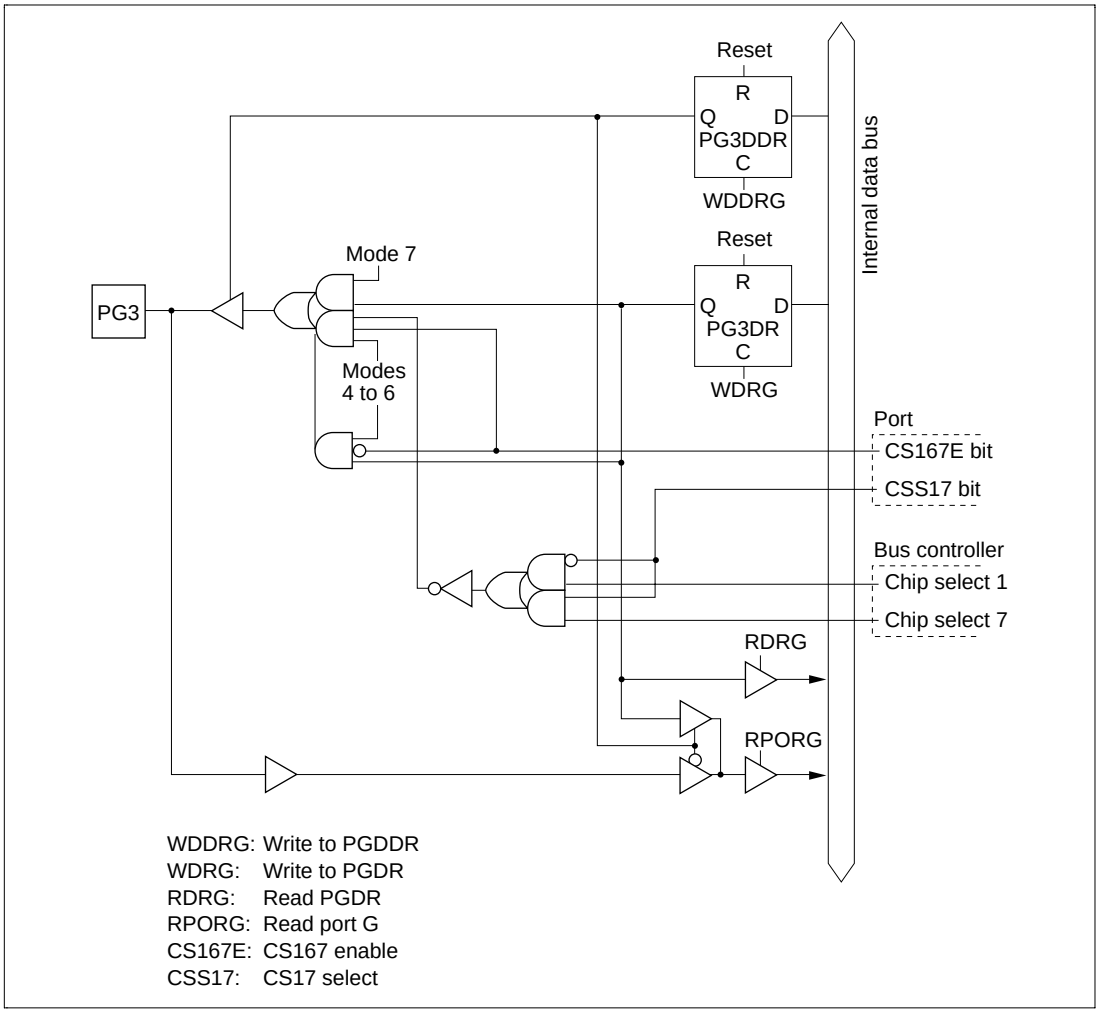


Figure 5.35 (d) Port G Block Diagram (Pin PG3)

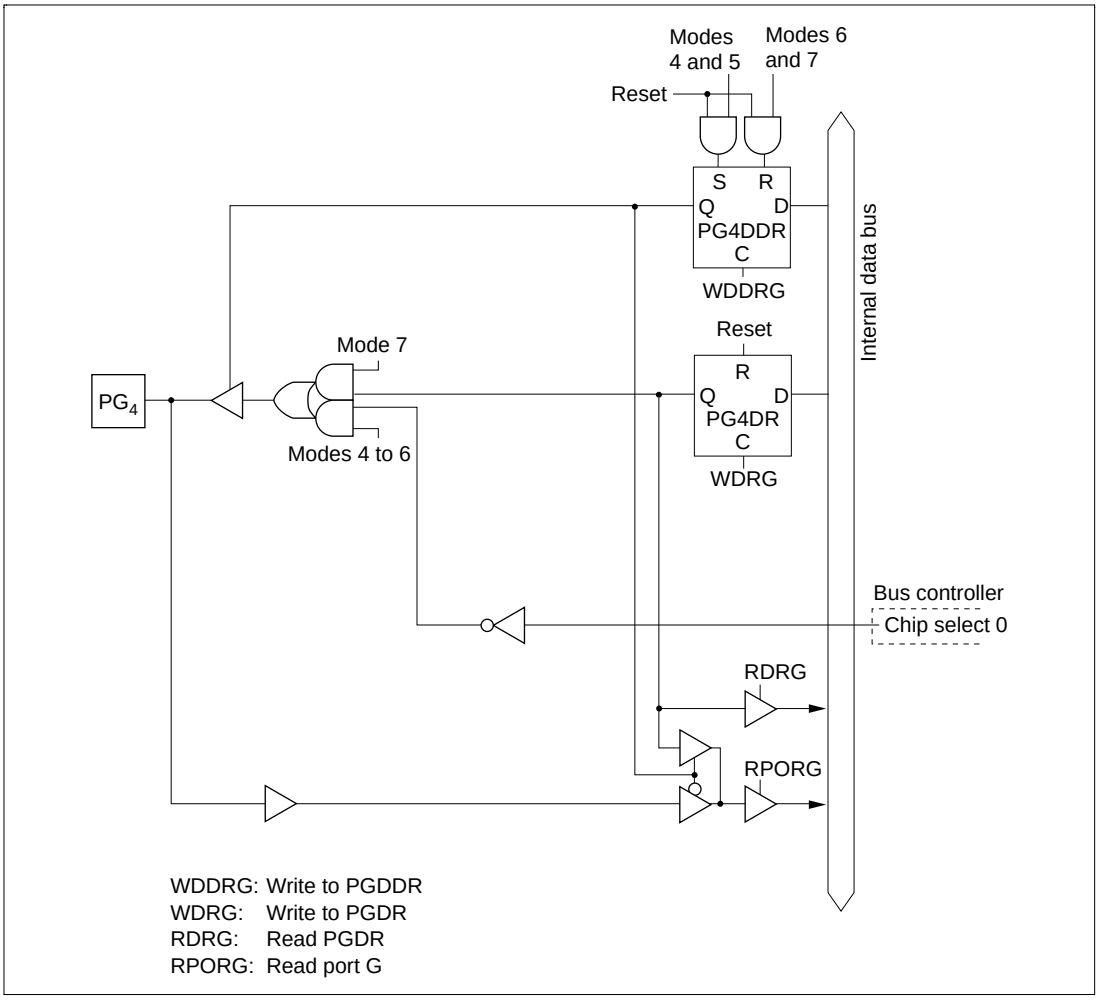


Figure 5.35 (e) Port G Block Diagram (Pin PG4)

Section 6 Supporting Module Block Diagrams

6.1 Interrupt Controller

6.1.1 Features

- Selection of two interrupt control modes
- Eight priority levels can be set for each module with IPR
- Independent vector addresses (NMI, $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$)
- Nine external interrupt pins
- DTC activation control

6.1.2 Block Diagram

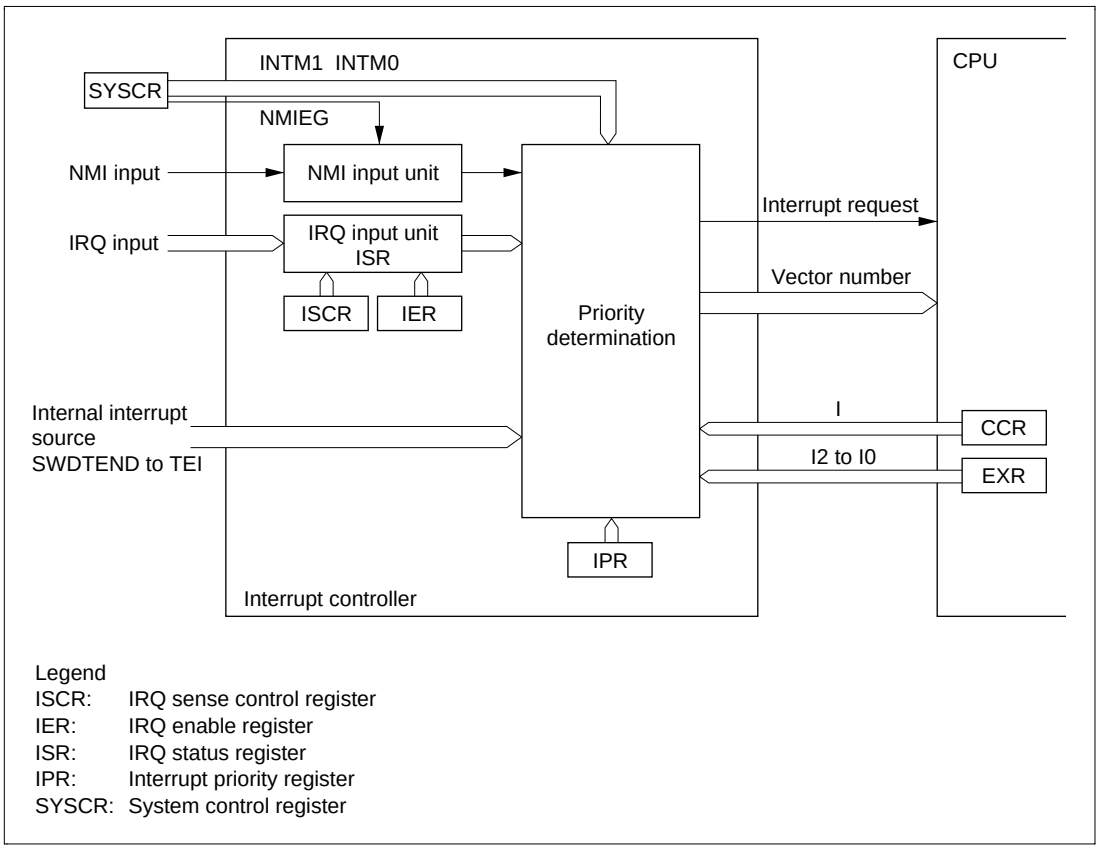


Figure 6.1 Block Diagram of Interrupt Controller

6.1.3 Pins

Table 6.1 Interrupt Controller Pins

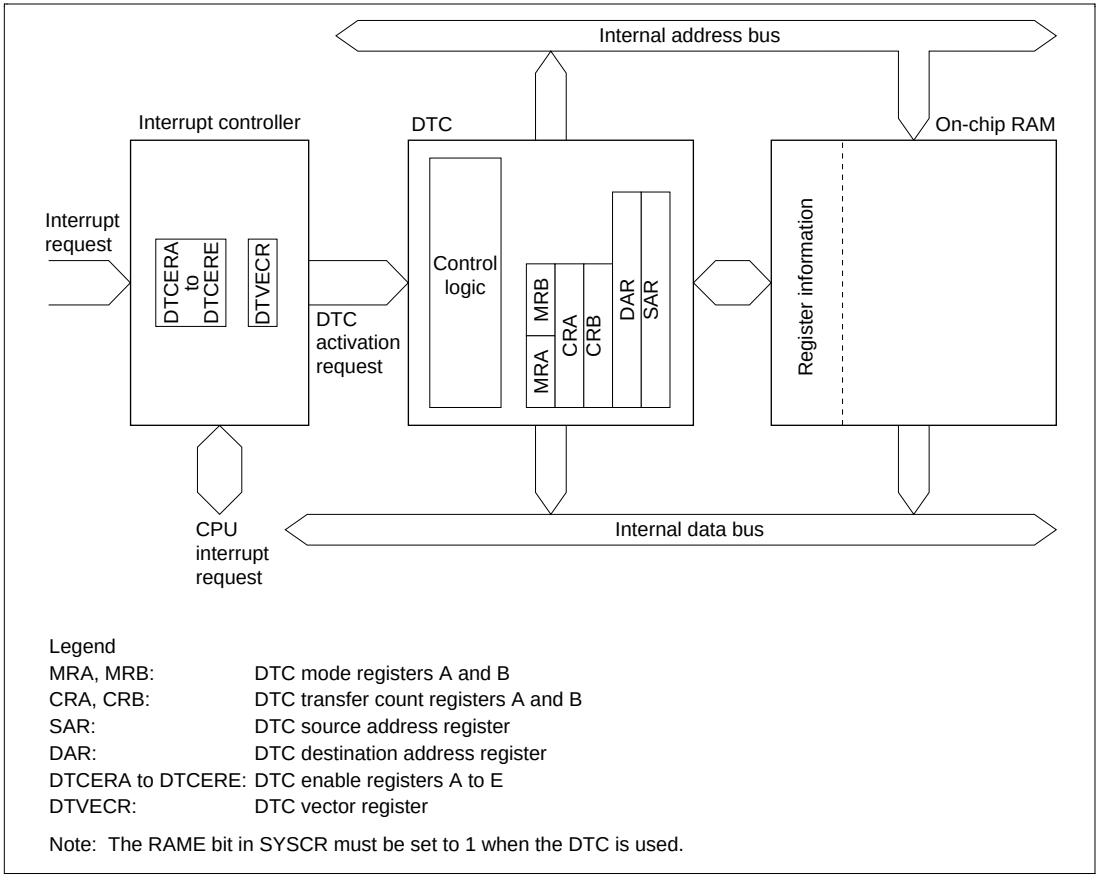
Name	Symbol	I/O	Function
Nonmaskable interrupt	NMI	Input	Nonmaskable external interrupt; rising or falling edge can be selected
External interrupt requests 7 to 0	$\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$	Input	Maskable external interrupts; rising, falling, or both edges, or level sensing, can be selected

6.2 Data Transfer Controller

6.2.1 Features

- Transfer possible over any number of channels
- Variety of transfer modes, including normal, repeat, and block transfer
- Direct specification of 16-Mbyte address space possible
- Byte or word can be selected as the transfer unit
- A CPU interrupt can be requested for an interrupt that activates the DTC
- Can be activated by software
- Module stop mode can be set
- DTC register information is located in on-chip RAM

6.2.2 Block Diagram



Legend

MRA, MRB:	DTC mode registers A and B
CRA, CRB:	DTC transfer count registers A and B
SAR:	DTC source address register
DAR:	DTC destination address register
DTCERA to DTCERE:	DTC enable registers A to E
DTVECR:	DTC vector register

Note: The RAME bit in SYSCR must be set to 1 when the DTC is used.

Figure 6.2 Block Diagram of DTC

6.3 16-Bit Timer Pulse Unit

6.3.1 Features

- Comprises six 16-bit timer channels
- Maximum 16 pulse inputs/outputs
- Selection of 8 counter input clocks for each channel
- Compare match, input capture, counter clear operation, synchronous operation, and PWM mode can be set for each channel
- Buffer operation can be set for channels 0 and 3
- Phase counting mode can be set independently for each of channels 1, 2, 4, and 5
- Cascaded operation possible by connecting two 16-bit counter channels to form a 32-bit counter
- Fast access via internal 16-bit bus
- A/D converter conversion start trigger can be generated
- Module stop mode can be set

6.3.2 Block Diagram

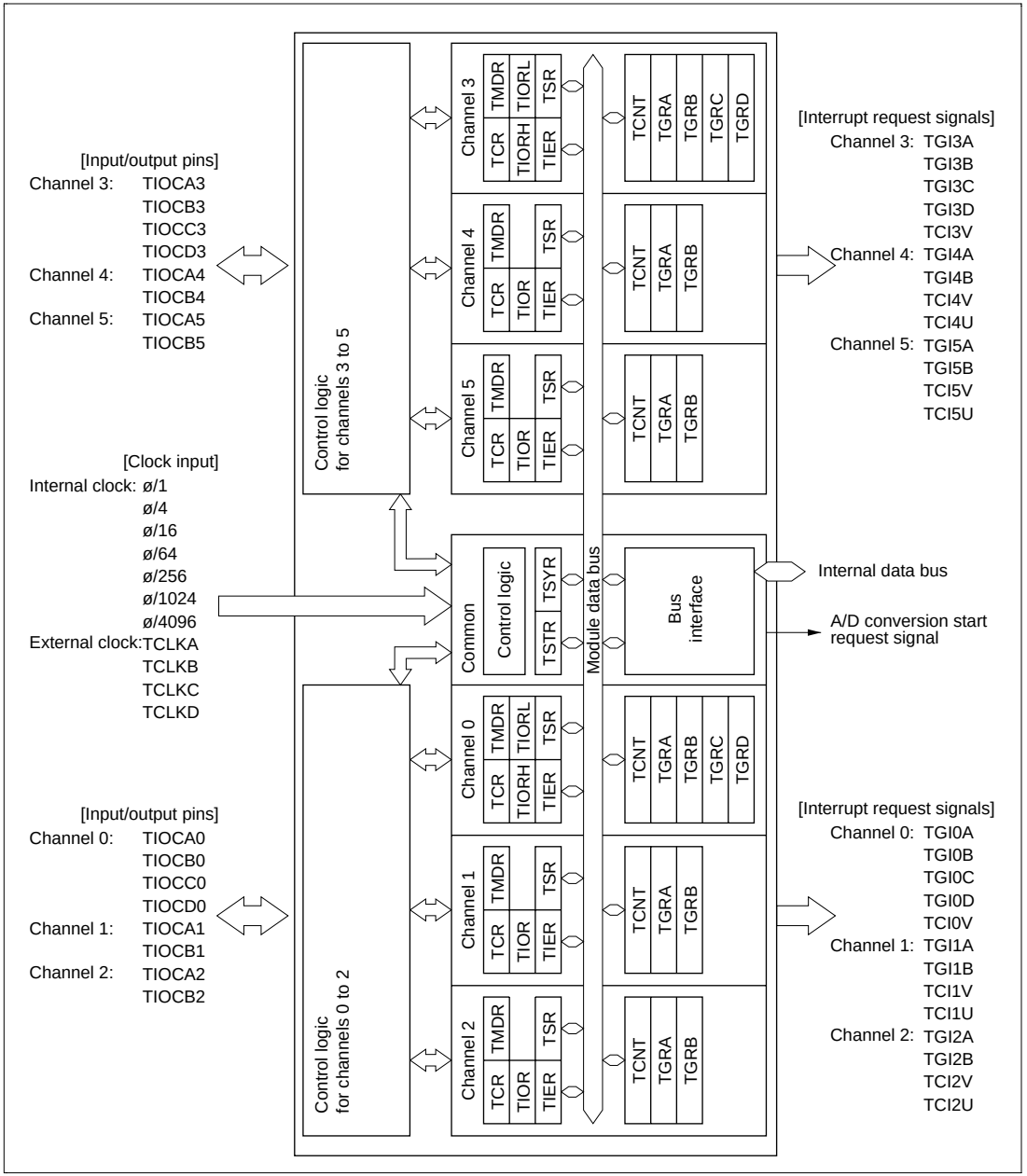


Figure 6.3 Block Diagram of TPU

6.3.3 Pins

Table 6.2 TPU Pins

Channel	Name	Symbol	I/O	Function
All	Clock input A	TCLKA	Input	External clock A input pin (Channel 1 and 5 phase counting mode A-phase input)
	Clock input B	TCLKB	Input	External clock B input pin (Channel 1 and 5 phase counting mode B-phase input)
	Clock input C	TCLKC	Input	External clock C input pin (Channel 2 and 4 phase counting mode A-phase input)
	Clock input D	TCLKD	Input	External clock D input pin (Channel 2 and 4 phase counting mode B-phase input)
0	Input capture/out compare match A0	TIOCA0	I/O	TGR0A input capture input/output compare output/PWM output pin
	Input capture/out compare match B0	TIOCB0	I/O	TGR0B input capture input/output compare output/PWM output pin
	Input capture/out compare match C0	TIOCC0	I/O	TGR0C input capture input/output compare output/PWM output pin
	Input capture/out compare match D0	TIOCD0	I/O	TGR0D input capture input/output compare output/PWM output pin
1	Input capture/out compare match A1	TIOCA1	I/O	TGR1A input capture input/output compare output/PWM output pin
	Input capture/out compare match B1	TIOCB1	I/O	TGR1B input capture input/output compare output/PWM output pin
2	Input capture/out compare match A2	TIOCA2	I/O	TGR2A input capture input/output compare output/PWM output pin
	Input capture/out compare match B2	TIOCB2	I/O	TGR2B input capture input/output compare output/PWM output pin
3	Input capture/out compare match A3	TIOCA3	I/O	TGR3A input capture input/output compare output/PWM output pin
	Input capture/out compare match B3	TIOCB3	I/O	TGR3B input capture input/output compare output/PWM output pin
	Input capture/out compare match C3	TIOCC3	I/O	TGR3C input capture input/output compare output/PWM output pin
	Input capture/out compare match D3	TIOCD3	I/O	TGR3D input capture input/output compare output/PWM output pin

Channel	Name	Symbol	I/O	Function
4	Input capture/out compare match A4	TIOCA4	I/O	TGR4A input capture input/output compare output/PWM output pin
	Input capture/out compare match B4	TIOCB4	I/O	TGR4B input capture input/output compare output/PWM output pin
5	Input capture/out compare match A5	TIOCA5	I/O	TGR5A input capture input/output compare output/PWM output pin
	Input capture/out compare match B5	TIOCB5	I/O	TGR5B input capture input/output compare output/PWM output pin

6.4 8-Bit Timer

6.4.1 Features

- Two-channel timer using 8-bit counters as base
- Selection of four counter input clocks
- Counter clearing can be specified
- Timer output by combination of two compare match signals
- Cascaded operation possible by connecting both counter channels to form a 16-bit counter
- Three interrupt sources for each channel
- A/D converter conversion start trigger can be generated
- Module stop mode can be set

6.4.2 Block Diagram

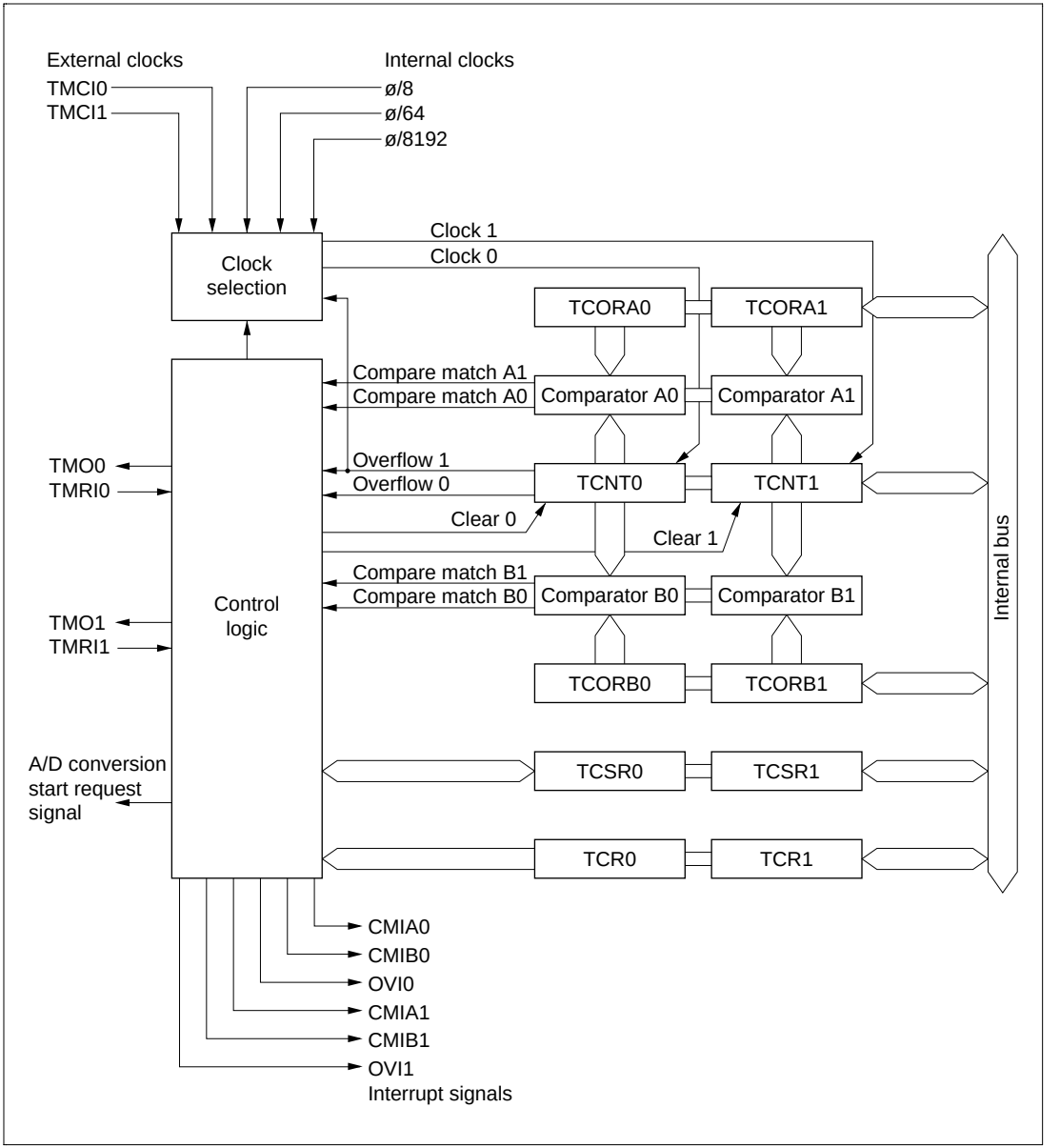


Figure 6.4 Block Diagram of 8-Bit Timer

6.4.3 Pins

Table 6.3 8-Bit Timer Pins

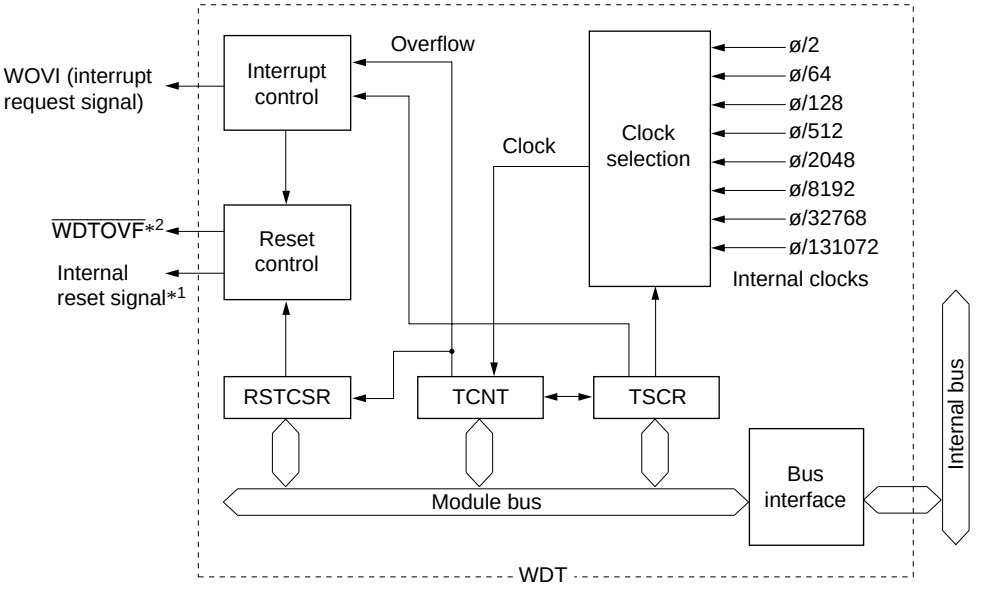
Channel	Name	Symbol	I/O	Function
0	Timer output pin 0	TMO0	Output	Compare match output
	Timer clock input pin 0	TMCI0	Input	Counter external clock input
	Timer reset input pin 0	TMRI0	Input	Counter external reset input
1	Timer output pin 1	TMO1	Output	Compare match output
	Timer clock input pin 1	TMCI1	Input	Counter external clock input
	Timer reset input pin 1	TMRI1	Input	Counter external reset input

6.5 Watchdog Timer

6.5.1 Features

- Switchable between watchdog timer mode and interval timer mode
- $\overline{\text{WDTOVF}}$ output in watchdog timer mode
- Interrupt generation when counter overflows in interval timer mode
- Selection of eight counter input clocks

6.5.2 Block Diagram



Legend
TCSR: Timer control/status register
TCNT: Timer counter
RSTCSR: Reset control/status register

Notes: 1. The internal reset signal can be generated by means of a register setting.
2. The $\overline{\text{WDTOVF}}$ pin function cannot be used in the F-ZTAT version.

Figure 6.5 Block Diagram of WDT

6.5.3 Pins

Table 6.4 WDT Pin

Name	Symbol	I/O	Function
Watchdog timer overflow	$\overline{\text{WDTOVF}}$*	Output	Outputs counter overflow signal in watchdog timer mode

Note: * The $\overline{\text{WDTOVF}}$ pin function cannot be used in the F-ZTAT version.

6.6 Serial Communication Interface

6.6.1 Features

- Two on-chip channels in the H8S/2319 and H8S/2318 Series
- Selection of synchronous or asynchronous serial communication mode
- Full-duplex communication capability
- Selection of LSB-first or MSB-first transfer
- Built-in baud rate generator allows any bit rate to be selected
- Selection of transmit/receive clock source
- Four interrupts (ERI, RXI, TXI, and TEI), of which RXI and TXI can activate the DTC
- Module stop mode can be set

6.6.2 Block Diagram

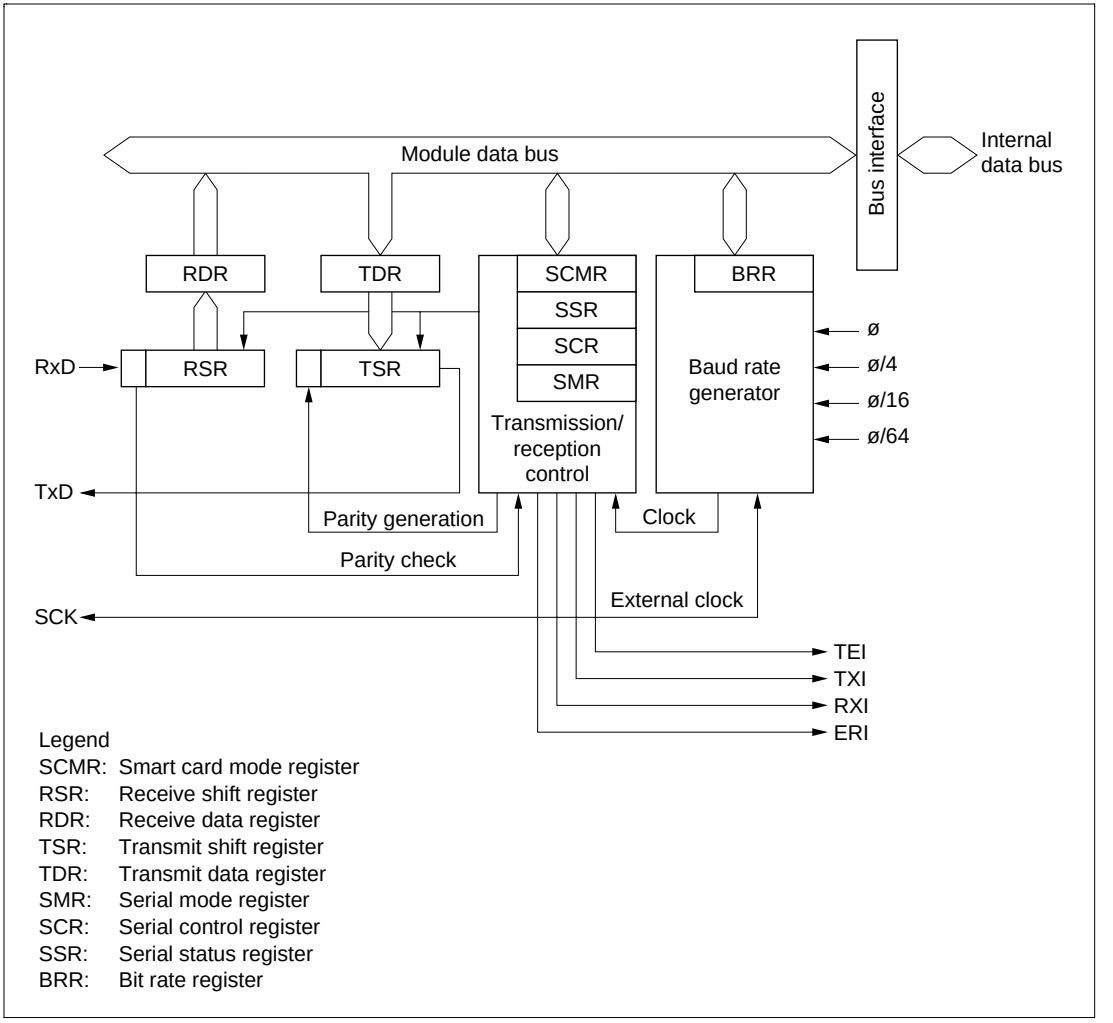


Figure 6.6 Block Diagram of SCI

6.6.3 Pins

Table 6.5 SCI Pins

Channel	Name	Symbol	I/O	Function
0	Serial clock pin 0	SCK0	I/O	SCI0 clock input/output
	Receive data pin 0	RxD0	Input	SCI0 receive data input
	Transmit data pin 0	TxD0	Output	SCI0 transmit data output
1	Serial clock pin 1	SCK1	I/O	SCI1 clock input/output
	Receive data pin 1	RxD1	Input	SCI1 receive data input
	Transmit data pin 1	TxD1	Output	SCI1 transmit data output

6.7 Smart Card Interface

6.7.1 Features

- IC card interface conforming to ISO/IEC7816-3 supported as SCI extension function
- Switching between normal SCI and smart card interface by means of register setting
- Built-in baud rate generator allows any bit rate to be selected
- Three interrupts (TXI, RXI, and ERI), of which RXI and TXI can activate the DTC

6.7.2 Block Diagram

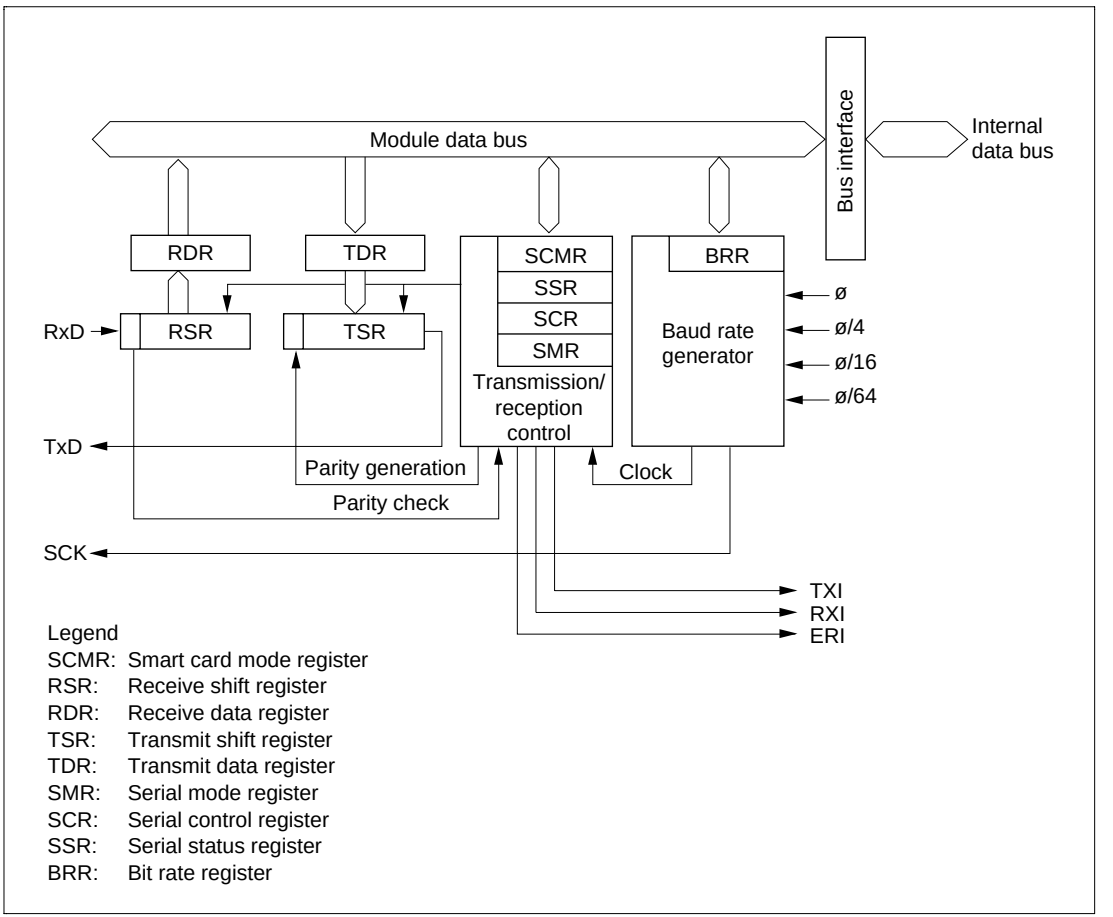


Figure 6.7 Block Diagram of Smart Card Interface

6.7.3 Pins

Table 6.6 Smart Card Interface Pins

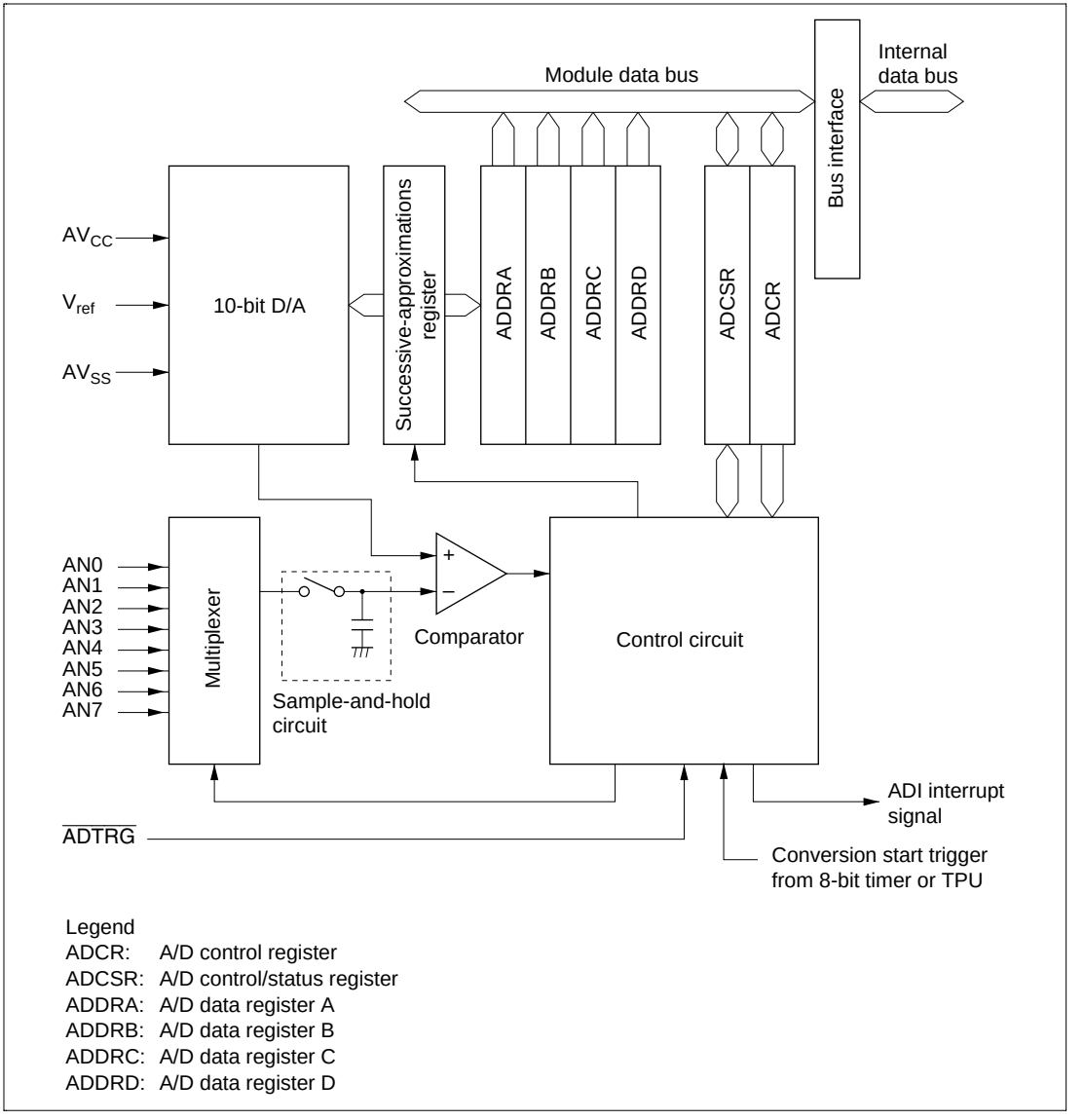
Channel	Name	Symbol	I/O	Function
0	Serial clock pin 0	SCK0	I/O	SCI0 clock input/output
	Receive data pin 0	RxD0	Input	SCI0 receive data input
	Transmit data pin 0	TxD0	Output	SCI0 transmit data output
1	Serial clock pin 1	SCK1	I/O	SCI1 clock input/output
	Receive data pin 1	RxD1	Input	SCI1 receive data input
	Transmit data pin 1	TxD1	Output	SCI1 transmit data output

6.8 A/D Converter (8 Analog Input Channel Version)

6.8.1 Features

- 10-bit resolution
- 8 input channels
- Settable analog conversion voltage range
- Conversion time: 6.7 µs per channel (at 20 MHz operation)
- Selection of single mode or scan mode as operating mode
- Four data registers
- Sample-and-hold function
- Three kinds of conversion start (software, timer conversion start trigger, or $\overline{\text{ADTRG}}$ pin)
- A/D conversion end interrupt request generation
- Module stop mode can be set

6.8.2 Block Diagram



Legend
ADCR: A/D control register
ADCSR: A/D control/status register
ADDRA: A/D data register A
ADDRB: A/D data register B
ADDRC: A/D data register C
ADDRD: A/D data register D

Figure 6.8 Block Diagram of A/D Converter

6.8.3 Pins

Table 6.7 A/D Converter Pins

Name	Symbol	I/O	Function
Analog power supply pin	AV_{CC}	Input	Analog circuit power supply
Analog ground pin	AV_{SS}	Input	Analog circuit ground and reference voltage
Reference voltage pin	V_{ref}	Input	A/D conversion reference voltage
Analog input pin 0	AN0	Input	Group 0 analog input
Analog input pin 1	AN1	Input	
Analog input pin 2	AN2	Input	
Analog input pin 3	AN3	Input	
Analog input pin 4	AN4	Input	Group 1 analog input
Analog input pin 5	AN5	Input	
Analog input pin 6	AN6	Input	
Analog input pin 7	AN7	Input	
A/D external trigger input pin	$\overline{\text{ADTRG}}$	Input	External trigger for starting A/D conversion

6.9 D/A Converter

6.9.1 Features

- 8-bit resolution
- Two output channels
- Maximum conversion time of 10 µs (with 20 pF capacitive load)
- Output voltage of 0 V to V_{ref}
- D/A output hold function in software standby mode
- Module stop mode can be set

6.9.2 Block Diagram

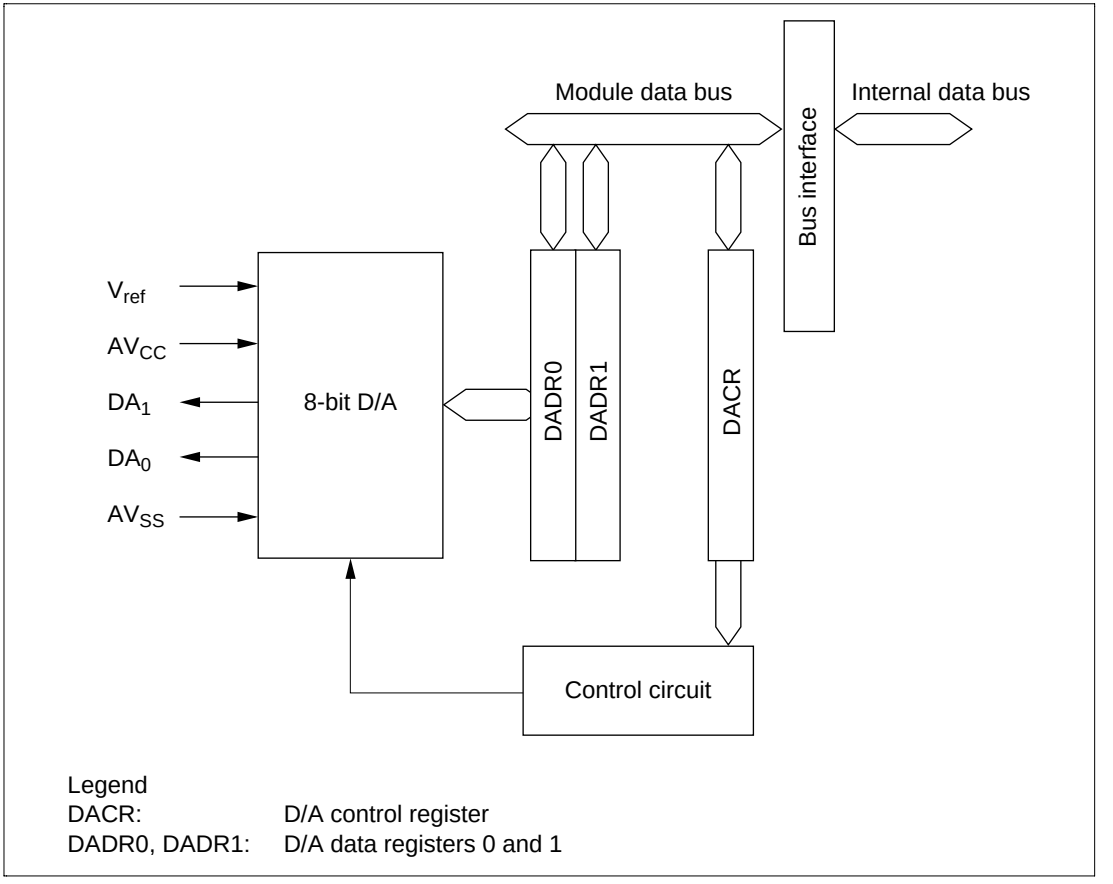


Figure 6.9 Block Diagram of D/A Converter

6.9.3 Pins

Table 6.8 D/A Converter Pins

Name	Symbol	I/O	Function
Analog power supply pin	AV_{CC}	Input	Analog circuit power supply
Analog ground pin	AV_{SS}	Input	Analog circuit ground and reference voltage
Analog output pin 0	DA0	Output	Channel 0 analog output
Analog output pin 1	DA1	Output	Channel 1 analog output
Reference voltage pin	V_{ref}	Input	Analog circuit reference voltage

6.10 RAM

6.10.1 Features

- Eight kbytes of on-chip high-speed static RAM in the H8S/2319, H8S/2318, H8S/2317, H8S/2316, H8S/2315, and H8S/2312, and two kbytes in the H8S/2313, H8S/2311, and H8S/2310
- Connected to the CPU by a 16-bit data bus, enabling one-state access to both byte data and word data
- Can be enabled or disabled by means of the RAM enable bit (RAME) in the system control register (SYSCR)

6.10.2 Block Diagram

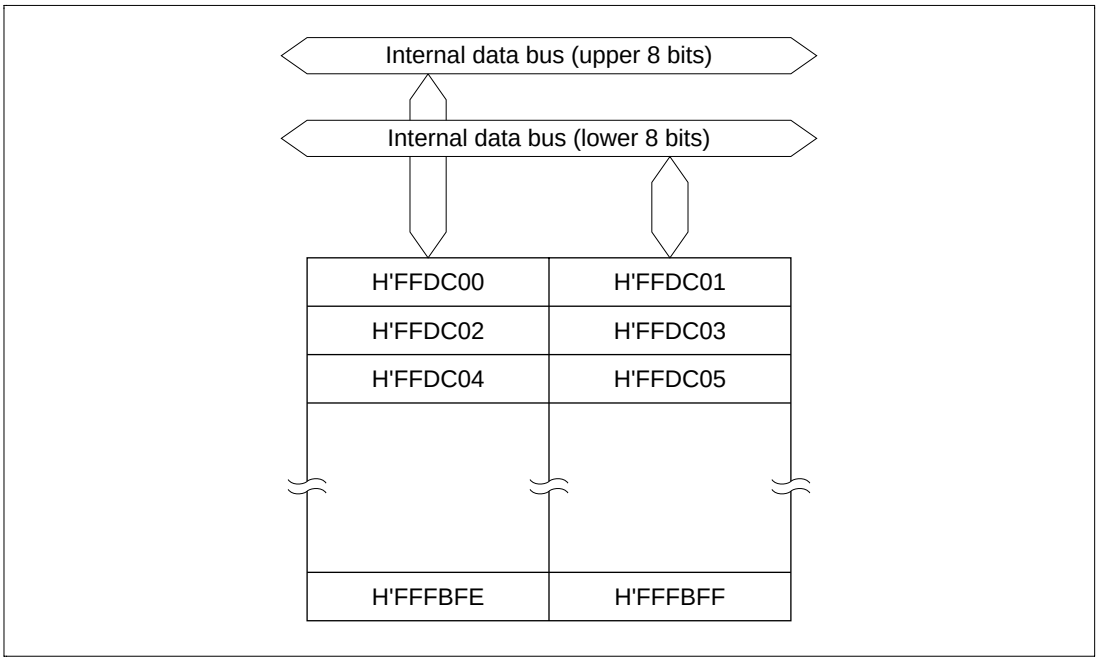


Figure 6.10 Block Diagram of RAM (8 kbytes)

6.11 ROM (H8S/2319)

6.11.1 Features

- Connected to the bus master by a 16-bit data bus, enabling one-state access to both byte data and word data
- The flash memory version (H8S/2319 F-ZTAT) can be erased and programmed with a PROM programmer, as well as on-board

6.11.2 Block Diagrams

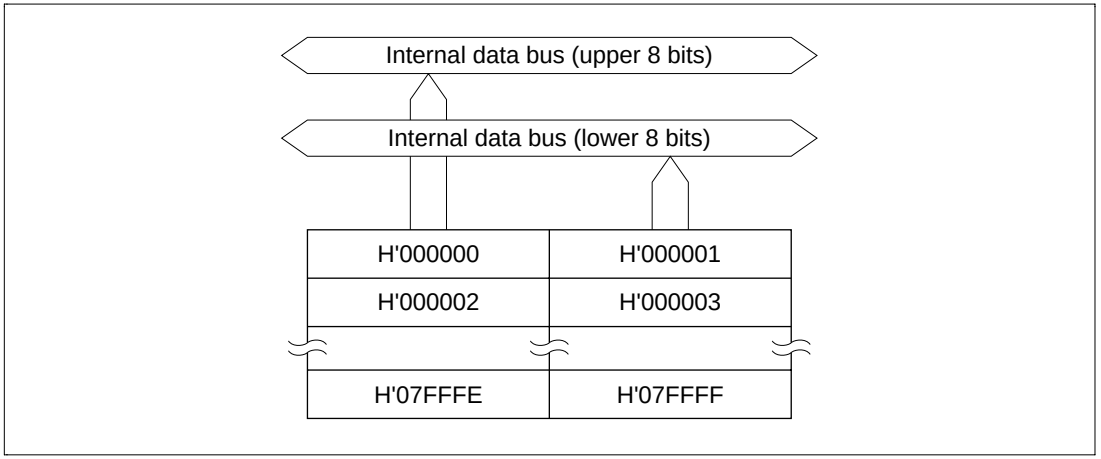
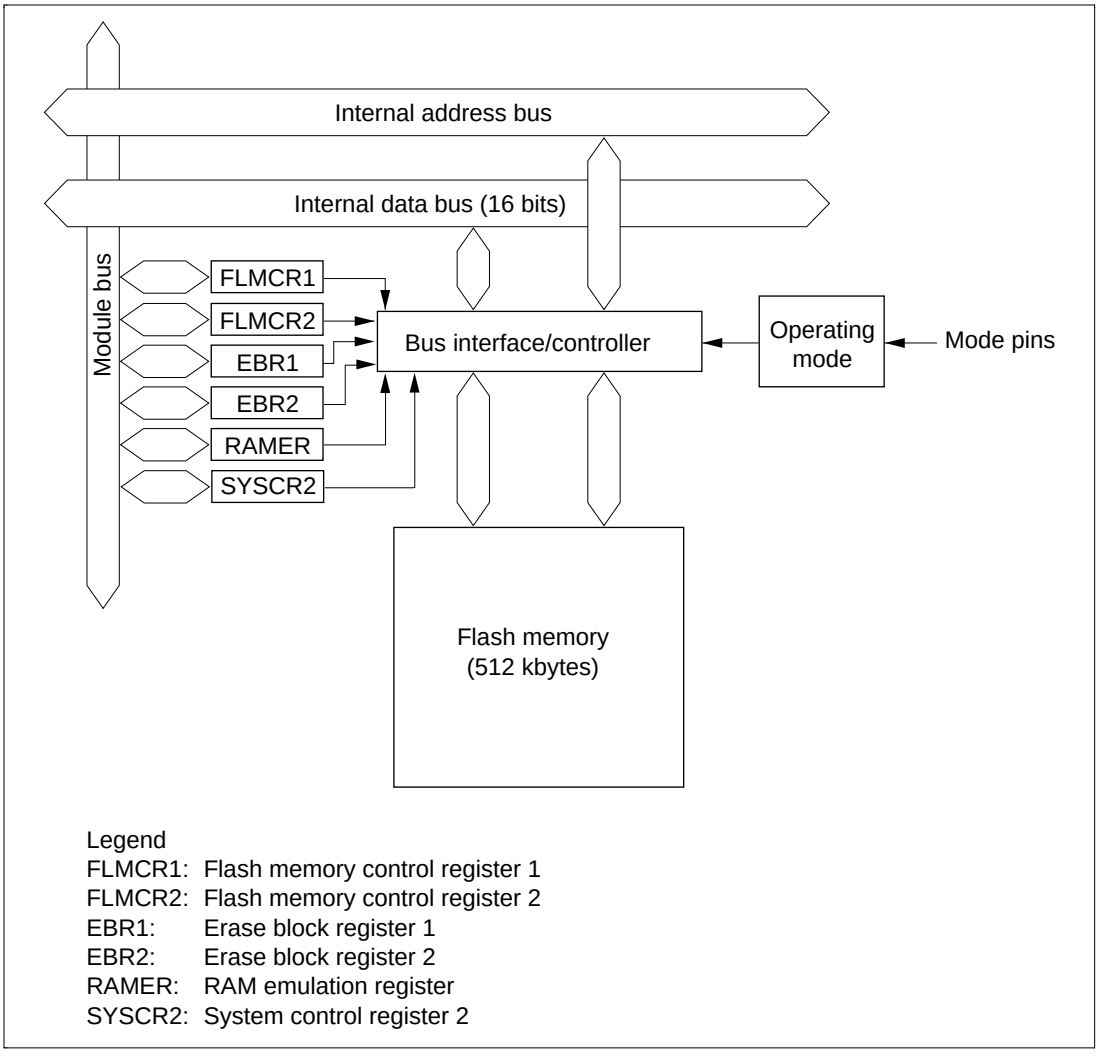


Figure 6.11 Block Diagram of Flash Memory (512 kbytes)



Legend
FLMCR1: Flash memory control register 1
FLMCR2: Flash memory control register 2
EBR1: Erase block register 1
EBR2: Erase block register 2
RAMER: RAM emulation register
SYSCR2: System control register 2

Figure 6.12 Block Diagram of Flash Memory

6.12 ROM

6.12.1 Features

- Connected to the bus master by a 16-bit data bus, enabling one-state access to both byte data and word data
- The flash memory version (256 kbytes in the H8S/2318 F-ZTAT and 384 kbytes in the H8S/2315 F-ZTAT) can be erased and programmed with a PROM programmer, as well as on-board
- The H8S/2318 has 256 kbytes, the H8S/2317 128 kbytes, the H8S/2316 and H8S/2313 64 kbytes, and the H8S/2311 32 kbytes, of on-chip mask ROM

6.12.2 Block Diagrams

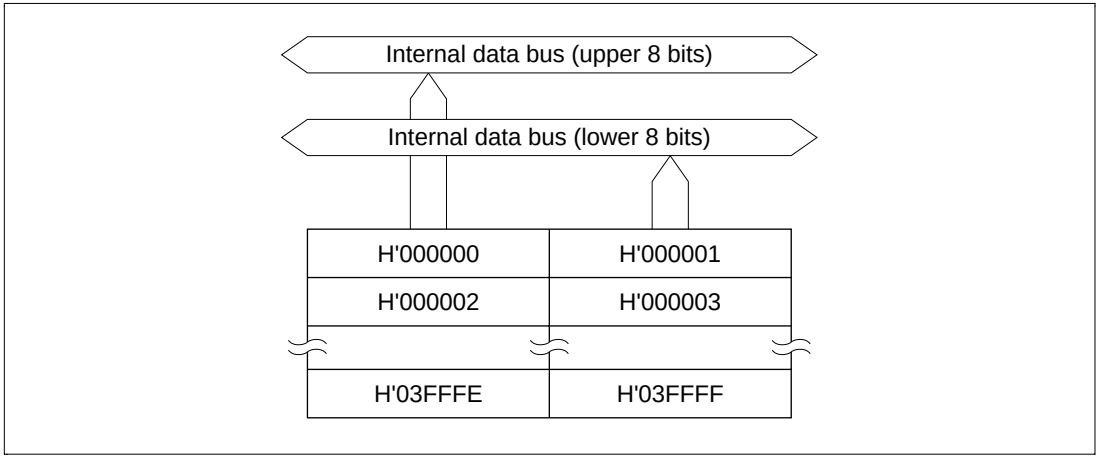


Figure 6.13 Block Diagram of Mask ROM (256 kbytes)

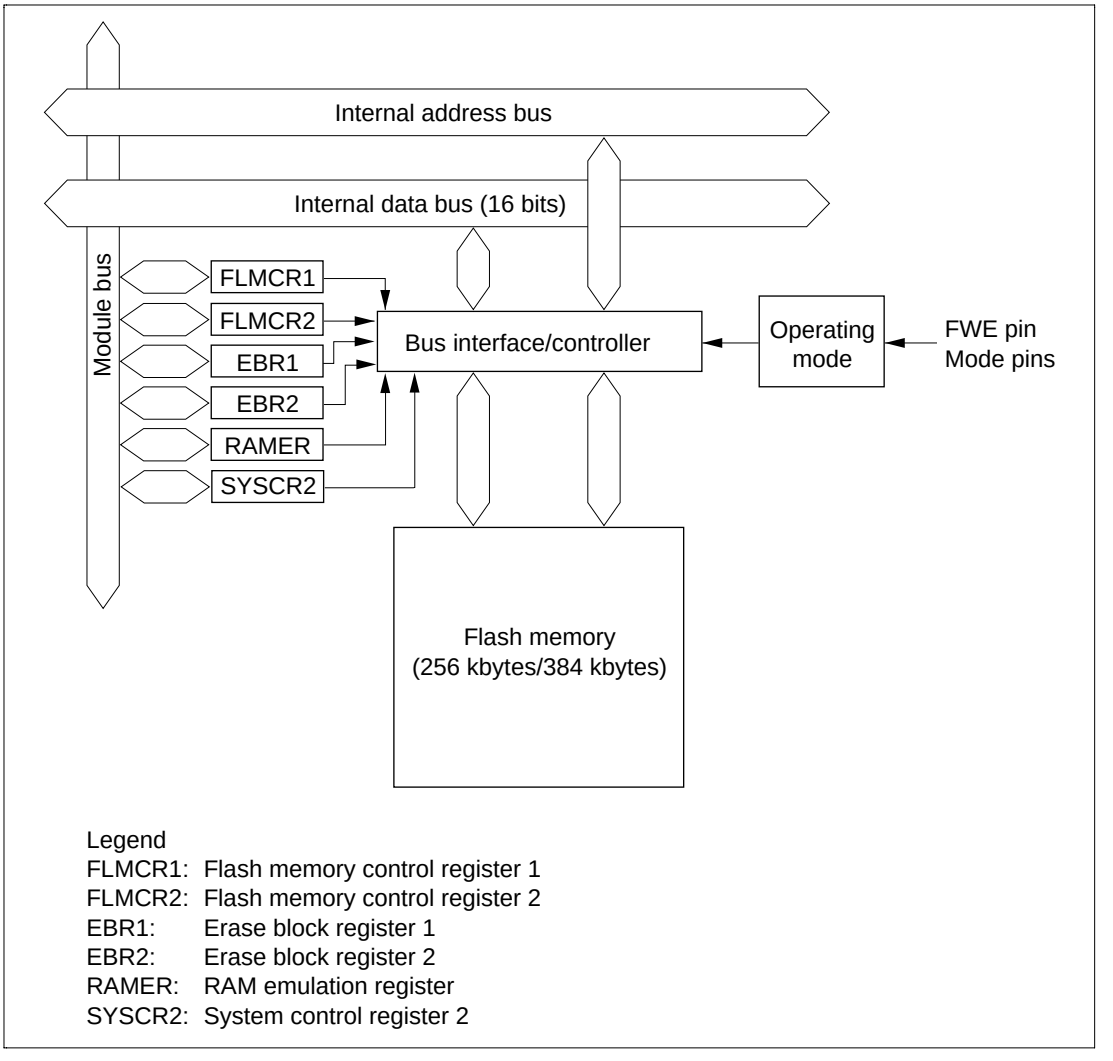


Figure 6.14 Block Diagram of Flash Memory

6.13 Clock Pulse Generator

6.13.1 Features

- Comprises an oscillator, duty correction circuit, medium-speed clock divider, and bus master clock selection circuit
- Generates system clock (ø), bus master clock, and internal clock
- Allows switching between medium-speed mode and variable clock division function

6.13.2 Block Diagram

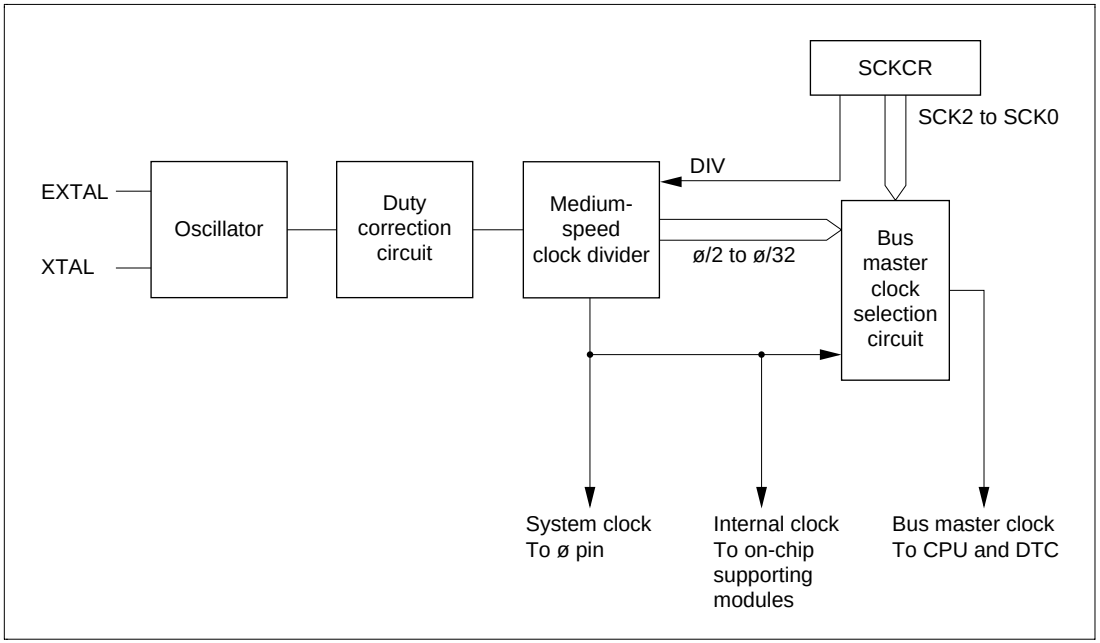


Figure 6.15 Block Diagram of Clock Pulse Generator

Section 7 Electrical Characteristics

Note: Please contact a Hitachi sales agency for the electrical characteristics of the H8S/2319 F-ZTAT version.

7.1 Electrical Characteristics of Mask ROM Version (H8S/2318, H8S/2317, H8S/2316, H8S/2313, H8S/2311) and ROMless Version (H8S/2312, H8S/2310)

7.1.1 Absolute Maximum Ratings

Table 7.1 lists the absolute maximum ratings.

Table 7.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.3 to +4.3	V
Input voltage (except port 4)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (port 4)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference power supply voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +4.3	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

7.1.2 DC Characteristics

Table 7.2 DC Characteristics

Conditions: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*[1], T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Ports 1, 2, $\overline{IRQ0}$ to $\overline{IRQ7}$	VT^-	$V_{CC} \times 0.2$	—	—	V	
		VT^+	—	—	$V_{CC} \times 0.7$	V	
		$VT^+ - VT^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD2 to MD0	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Ports 3, A to G		2.2	—	V_{CC} + 0.3	V	
	Port 4		2.2	—	AV_{CC} + 0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD2 to MD0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 3, 4, A to G		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD2 to MD0		—	—	1.0	µA	
	Port 4		—	—	1.0	µA	V_{in} = 0.5 to AV_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 1, 2, 3, A to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input pull-up MOS current	Ports A to E	$-I_p$	10	—	300	µA	V_{in} = 0V
Input capacitance	$\overline{RES}$	C_{in}	—	—	30	pF	V_{in} = 0 V
	NMI		—	—	30	pF	f = 1 MHz
	All input pins except $\overline{RES}$ and NMI		—	—	15	pF	T_a = 25°C
Current dissipation*2	Normal operation	I_{CC}*4	—	35 (3.0 V)	80	mA	f = 20 MHz
				50 (3.3 V)	100	mA	f = 25 MHz
	Sleep mode		—	25 (3.0 V)	64	mA	f = 20 MHz
				35 (3.3 V)	80	mA	f = 25 MHz
	Standby mode*3		—	0.01	10	µA	$T_a \leq 50°C$
			—	—	80		50°C < T_a
Analog power supply voltage	During A/D and D/A conversion	AI_{CC}	—	0.2 (3.0 V)	2.0	mA	
	Idle		—	0.01	5.0	µA	
Reference power supply voltage	During A/D and D/A conversion	AI_{CC}	—	1.4 (3.0 V)	3.0	mA	
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. **If the A/D and D/A converters are not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins open**. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.

2. Current dissipation values are for $V_{IH\ min} = V_{CC} - 0.2$ V and $V_{IL\ max} = 0.2$ V with all output pins unloaded and all MOS input pull-ups in the off state.

3. The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.

4. I_{CC} depends on V_{CC} and f as follows:

   I_{CC} max = 1.0 (mA) + 1.10 (mA/(MHz × V)) × V_{CC} × f (normal operation)

   I_{CC} max = 1.0 (mA) + 0.88 (mA/(MHz × V)) × V_{CC} × f (sleep mode)

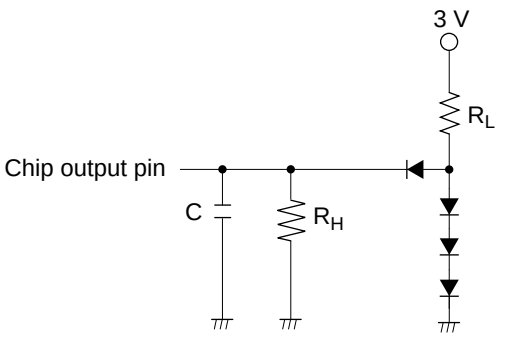
Table 7.3 Permissible Output Currents

Conditions: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	All output pins	I_{OL}	—	—	2.0	mA
Permissible output low current (total)	Total of all output pins	ΣI_{OL}	—	—	80	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	40	mA

Note: To protect chip reliability, do not exceed the output current values in table 7.3.

7.1.3 AC Characteristics



C = 50 pF: ports 1, A to F
C = 30 pF: ports 2, 3, G
R_L = 2.4 kΩ
R_H = 12 kΩ

Input/output timing measurement level:
1.5 V (V_{CC} = 2.7 V to 3.6 V)

Figure 7.1 Output Load Circuit

(1) Clock Timing

Table 7.4 Clock Timing

Condition A: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
Clock cycle time	t_{cyc}	50	500	40	500	ns	Figure 7.2
Clock pulse high width	t_{CH}	20	—	15	—	ns	
Clock pulse low width	t_{CL}	20	—	15	—	ns	
Clock rise time	t_{Cr}	—	5	—	5	ns	
Clock fall time	t_{Cf}	—	5	—	5	ns	
Reset oscillation stabilization time (crystal)	t_{OSC1}	10	—	10	—	ms	Figure 7.3
Software standby oscillation stabilization time (crystal)	t_{OSC2}	10	—	10	—	ms	
External clock output stabilization delay time	t_{DEXT}	500	—	500	—	µs	Figure 7.3

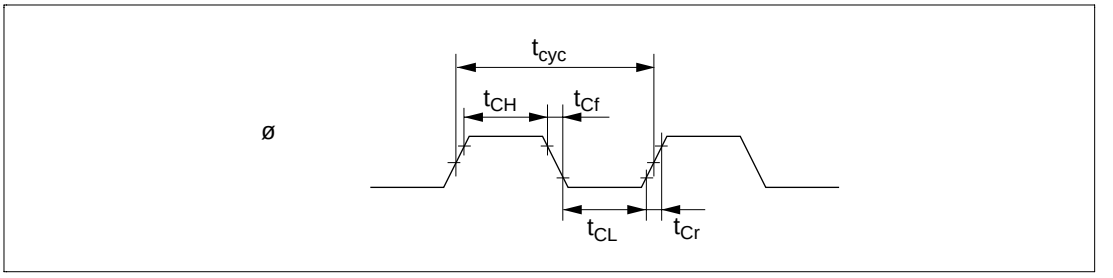


Figure 7.2 System Clock Timing

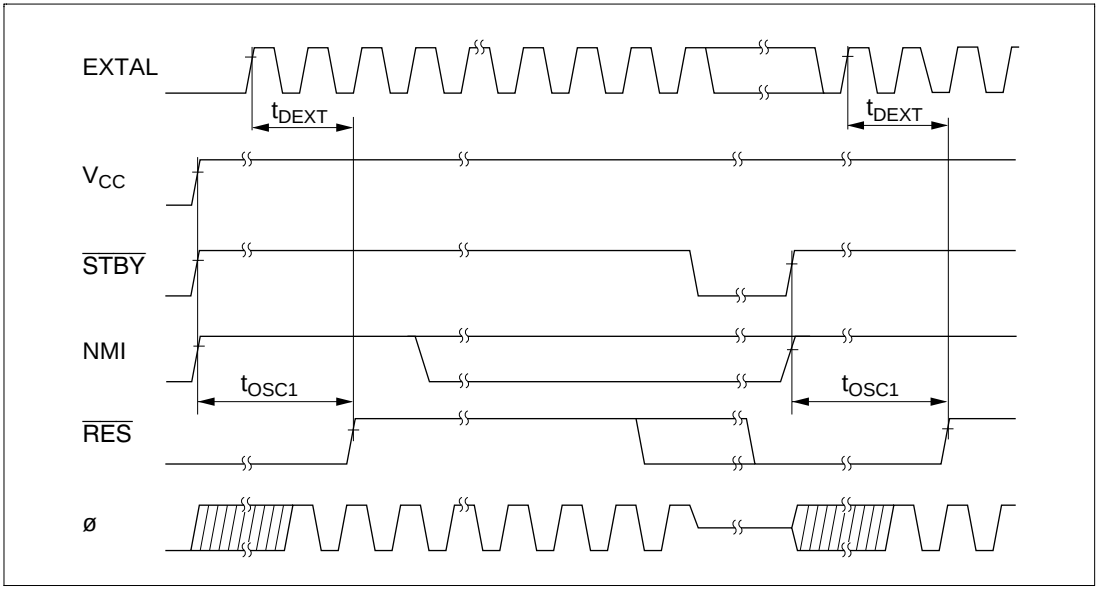


Figure 7.3 Oscillation Stabilization Timing

(2) Control Signal Timing

Table 7.5 Control Signal Timing

Condition A: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	ns	Figure 7.4
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	t_{cyc}	
NMI setup time	t_{NMIS}	150	—	150	—	ns	Figure 7.5
NMI hold time	t_{NMIH}	10	—	10	—		
NMI pulse width (in recovery from software standby mode)	t_{NMIW}	200	—	200	—		
$\overline{IRQ}$ setup time	t_{IRQS}	150	—	150	—	ns	
$\overline{IRQ}$ hold time	t_{IRQH}	10	—	10	—		
$\overline{IRQ}$ pulse width (in recovery from software standby mode)	t_{IRQW}	200	—	200	—		

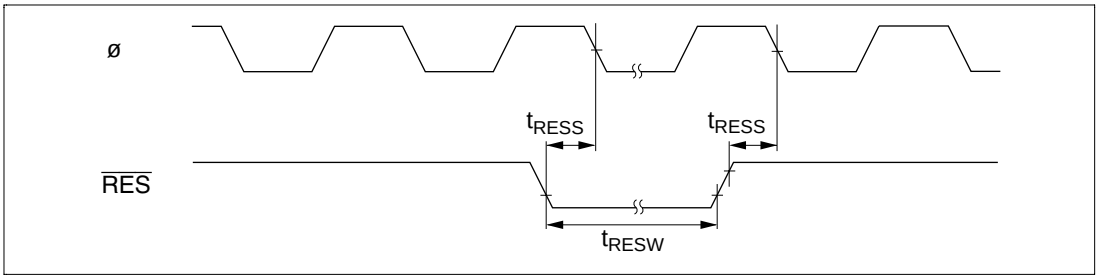


Figure 7.4 Reset Input Timing

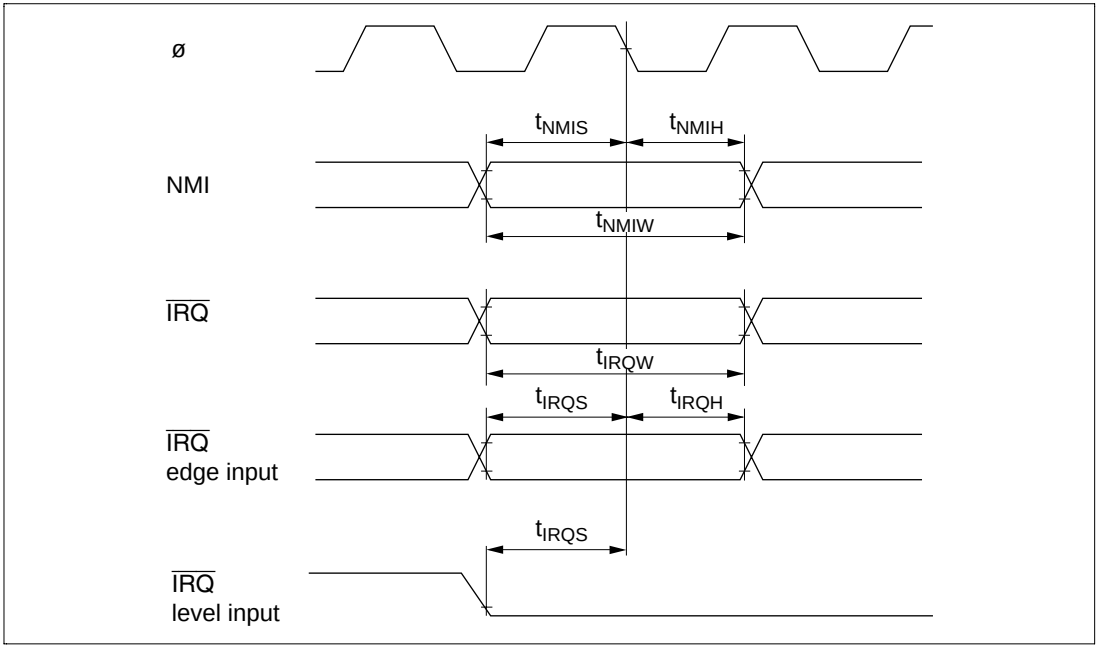


Figure 7.5 Interrupt Input Timing

(3) Bus Timing

Table 7.6 Bus Timing

Condition A: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

		Condition A		Condition B			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Address delay time	t_{AD}	—	20	—	20	ns	Figures 7.6 to 7.10
Address setup time	t_{AS}	0.5 × t_{cyc} – 15	—	0.5 × t_{cyc} – 15	—	ns	
Address hold time	t_{AH}	0.5 × t_{cyc} – 10	—	0.5 × t_{cyc} – 8	—	ns	
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	—	15	ns	
$\overline{AS}$ delay time	t_{ASD}	—	20	—	15	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	20	—	15	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	20	—	15	ns	
Read data setup time	t_{RDS}	15	—	15	—	ns	
Read data hold time	t_{RDH}	0	—	0	—	ns	
Read data access time 1	t_{ACC1}	—	1.0 × t_{cyc} – 25	—	1.0 × t_{cyc} – 20	ns	
Read data access time 2	t_{ACC2}	—	1.5 × t_{cyc} – 25	—	1.5 × t_{cyc} – 20	ns	
Read data access time 3	t_{ACC3}	—	2.0 × t_{cyc} – 25	—	2.0 × t_{cyc} – 20	ns	
Read data access time 4	t_{ACC4}	—	2.5 × t_{cyc} – 25	—	2.5 × t_{cyc} – 20	ns	
Read data access time 5	t_{ACC5}	—	3.0 × t_{cyc} – 25	—	3.0 × t_{cyc} – 20	ns	

Item	Symbol	Condition A		Condition B		Unit	Test Conditions
		Min	Max	Min	Max		
$\overline{WR}$ delay time 1	t_{WRD1}	—	20	—	15	ns	Figures 7.6 to 7.10
$\overline{WR}$ delay time 2	t_{WRD2}	—	20	—	15	ns	
$\overline{WR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc} - 20$	—	$1.0 \times t_{cyc} - 15$	—	ns	
$\overline{WR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc} - 20$	—	$1.5 \times t_{cyc} - 15$	—	ns	
Write data delay time	t_{WDD}	—	30	—	20	ns	
Write data setup time	t_{WDS}	$0.5 \times t_{cyc} - 20$	—	$0.5 \times t_{cyc} - 15$	—	ns	
Write data hold time	t_{WDH}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 8$	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	30	—	25	—	ns	Figure 7.8
$\overline{WAIT}$ hold time	t_{WTH}	5	—	5	—	ns	
$\overline{BREQ}$ setup time	t_{BRQS}	30	—	30	—	ns	Figure 7.11
$\overline{BACK}$ delay time	t_{BACD}	—	15	—	15	ns	
Bus floating time	t_{BZD}	—	50	—	40	ns	
$\overline{BREQO}$ delay time	t_{BRQOD}	—	30	—	25	ns	Figure 7.12

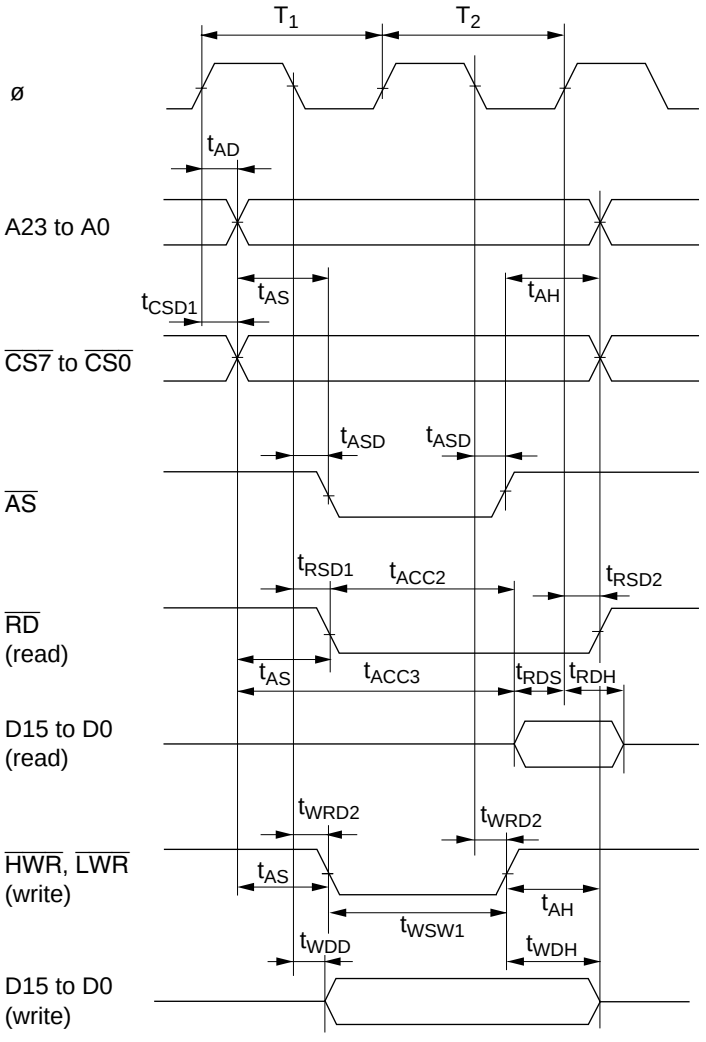


Figure 7.6 Basic Bus Timing (2-State Access)

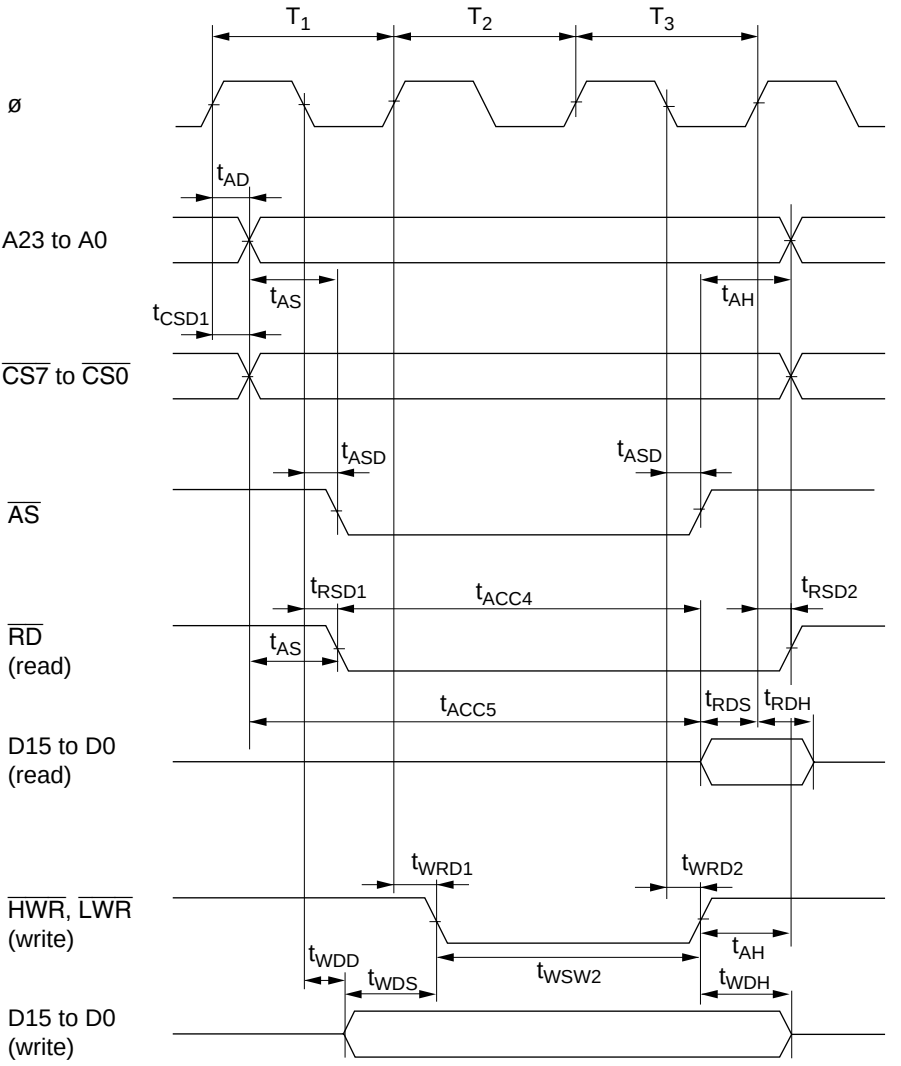


Figure 7.7 Basic Bus Timing (3-State Access)

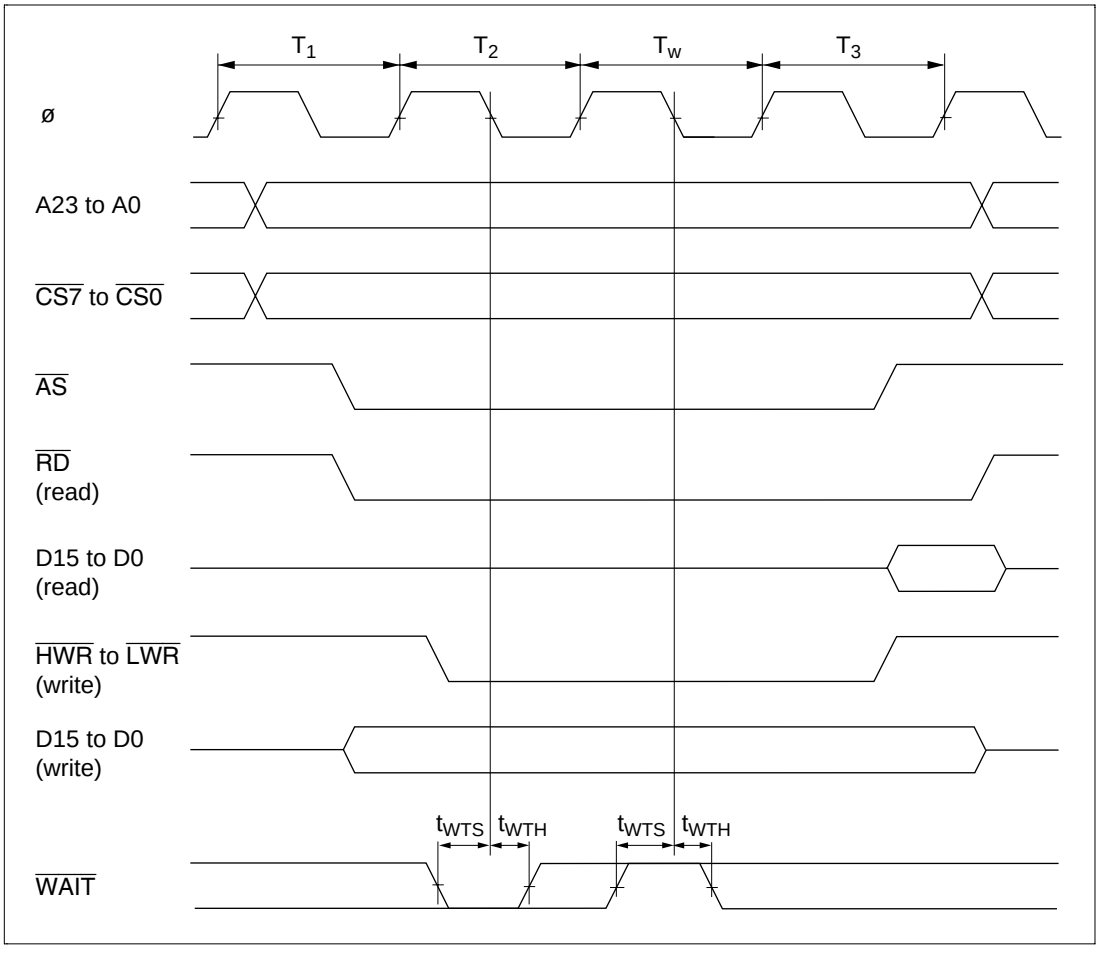


Figure 7.8 Basic Bus Timing (3-State Access, 1 Wait)

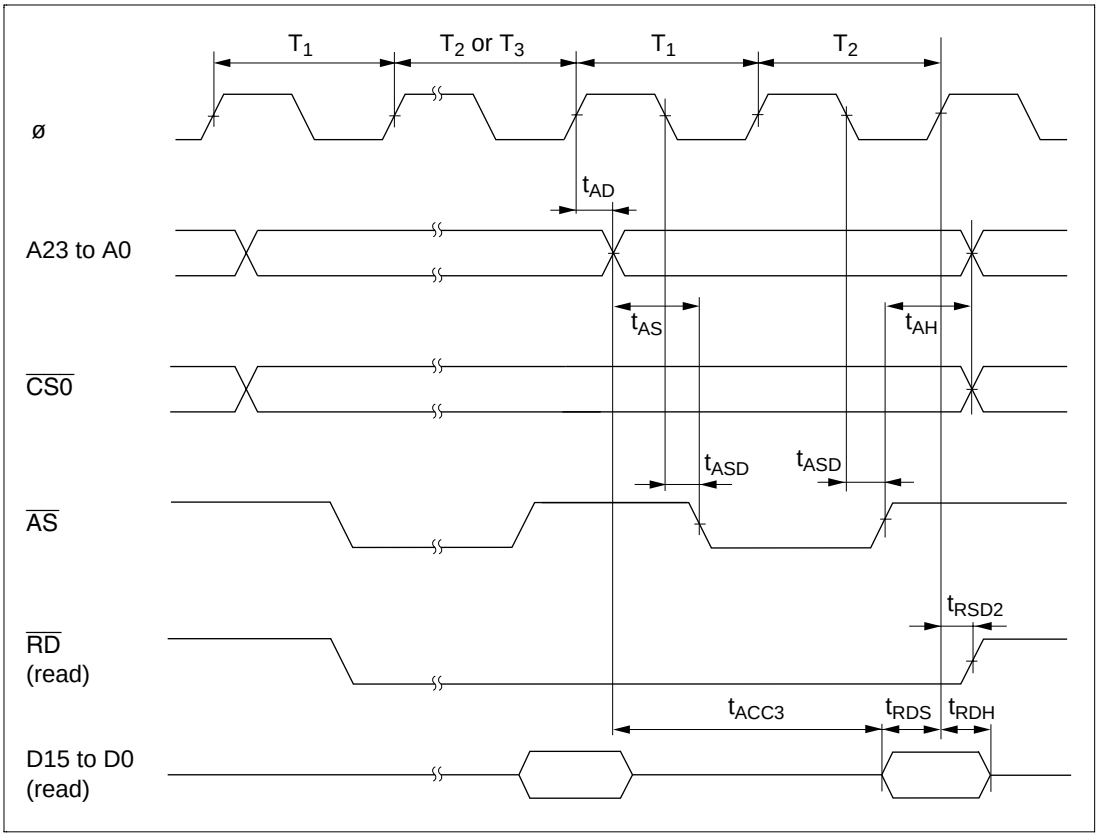


Figure 7.9 Burst ROM Access Timing (2-State Access)

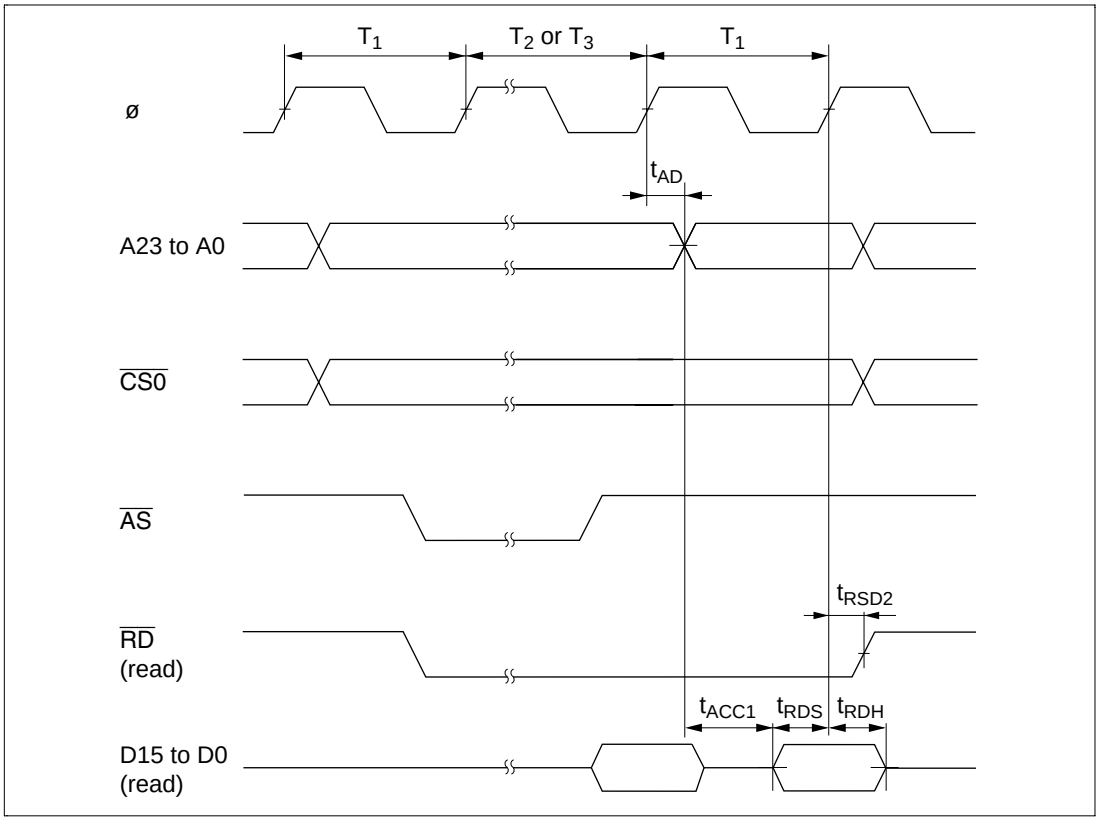


Figure 7.10 Burst ROM Access Timing (1-State Access)

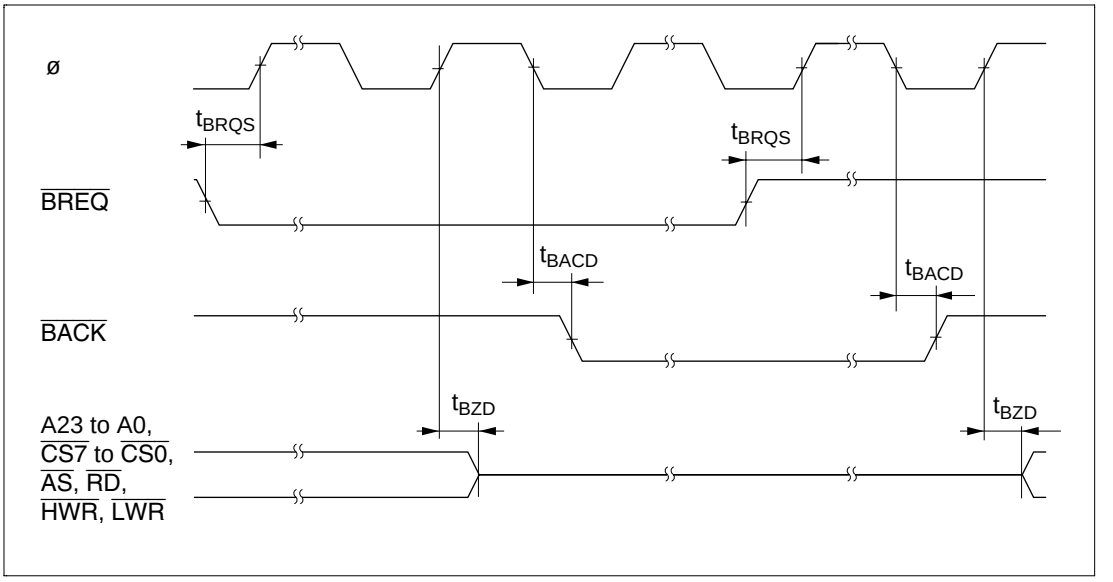


Figure 7.11 External Bus Release Timing

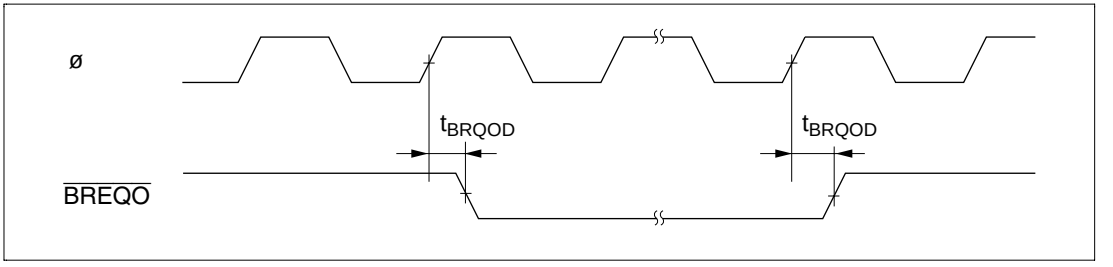


Figure 7.12 External Bus Request Output Timing

(4) Timing of On-Chip Supporting Modules

Table 7.7 Timing of On-Chip Supporting Modules

Condition A: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

				Condition A		Condition B			Test
Item			**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
I/O ports	Output data delay time		t_{PWD}	—	50	—	40	ns	Figure 7.13
	Input data setup time		t_{PRS}	30	—	25	—		
	Input data hold time		t_{PRH}	30	—	25	—		
TPU	Timer output delay time		t_{TOCD}	—	50	—	40	ns	Figure 7.14
	Timer input setup time		t_{TICS}	30	—	25	—		
	Timer clock input setup time		t_{TCKS}	30	—	25	—	ns	Figure 7.15
	Timer clock pulse width	Single-edge specification	t_{TCKWH}	1.5	—	1.5	—	t_{cyc}	
		Both-edge specification	t_{TCKWL}	2.5	—	2.5	—		
8-bit timer	Timer output delay time		t_{TMOD}	—	50	—	40	ns	Figure 7.16
	Timer reset input setup time		t_{TMRS}	30	—	25	—	ns	Figure 7.18
	Timer clock input setup time		t_{TMCS}	30	—	25	—	ns	Figure 7.17
	Timer clock pulse width	Single-edge specification	t_{TMCWH}	1.5	—	1.5	—	t_{cyc}	
		Both-edge specification	t_{TMCWL}	2.5	—	2.5	—		
WDT	Overflow output delay time		t_{WOVD}	—	50	—	40	ns	Figure 7.19

Item			Symbol	Condition A Min	Condition A Max	Condition B Min	Condition B Max	Unit	Test Conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	4	—	t_{cyc}	Figure 7.20
		Synchronous		6	—	6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	1.5	—	1.5	t_{cyc}	
	Input clock fall time		t_{SCKf}	—	1.5	—	1.5		
	Transmit data delay time		t_{TXD}	—	50	—	40	ns	Figure 7.21
	Receive data setup time (synchronous)		t_{RXS}	50	—	40	—	ns	
	Receive data hold time (synchronous)		t_{RXH}	50	—	40	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	30	—	30	—	ns	Figure 7.22

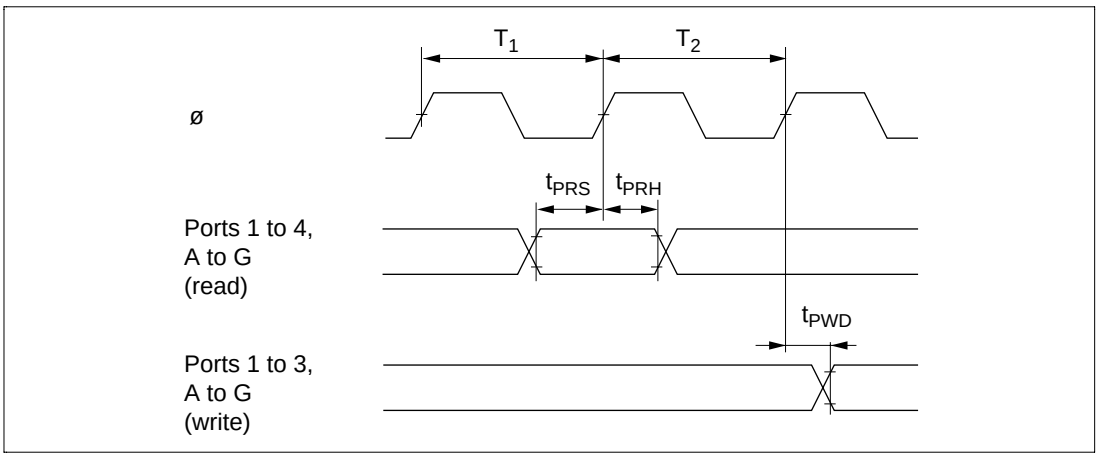


Figure 7.13 I/O Port Input/Output Timing

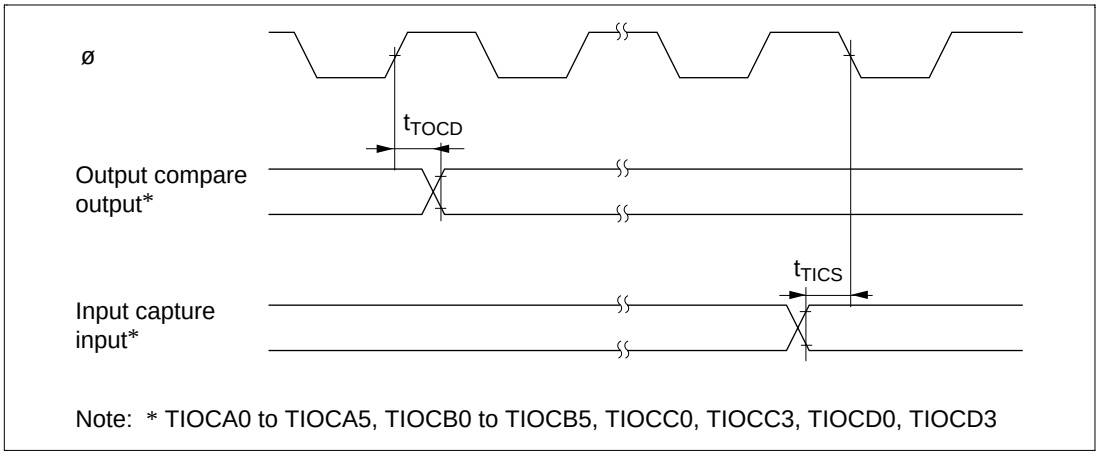


Figure 7.14 TPU Input/Output Timing

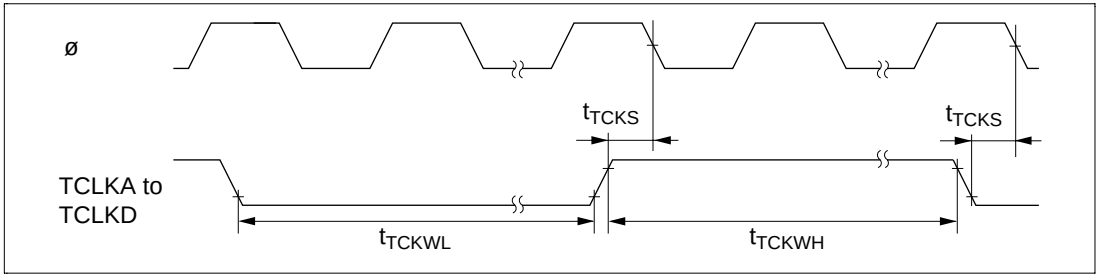


Figure 7.15 TPU Clock Input Timing

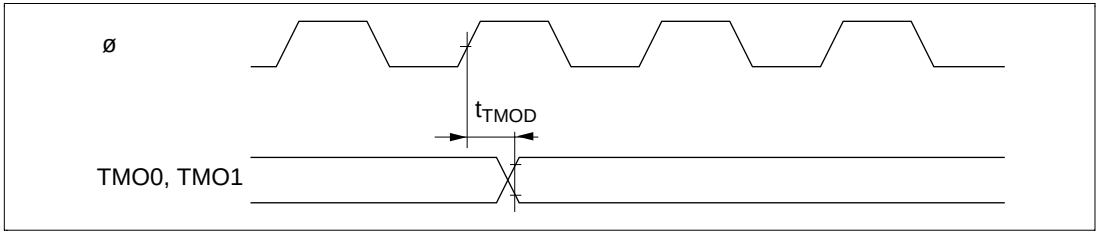


Figure 7.16 8-Bit Timer Output Timing

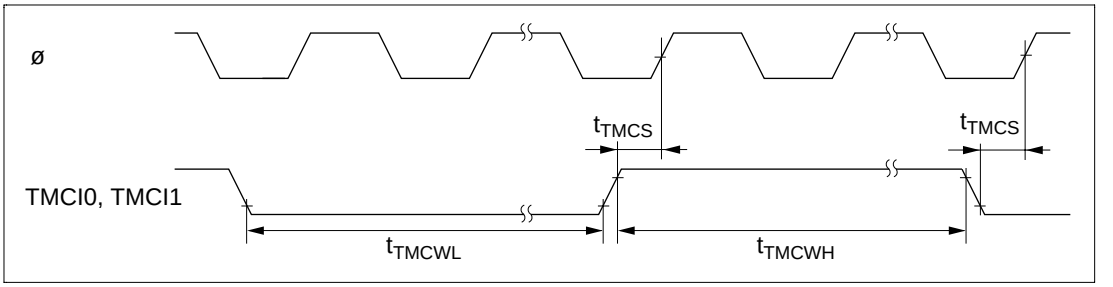


Figure 7.17 8-Bit Timer Clock Input Timing

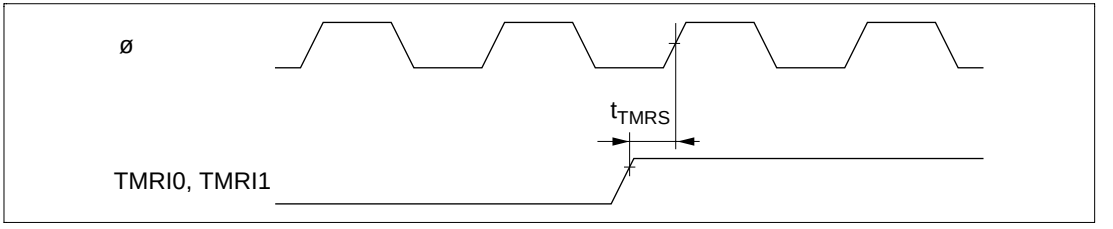


Figure 7.18 8-Bit Timer Reset Input Timing

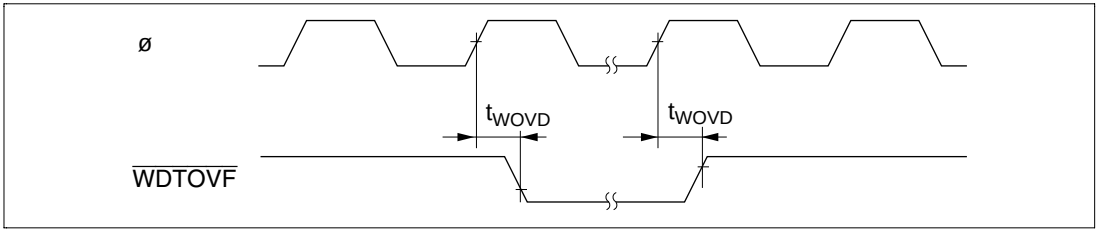


Figure 7.19 WDT Output Timing

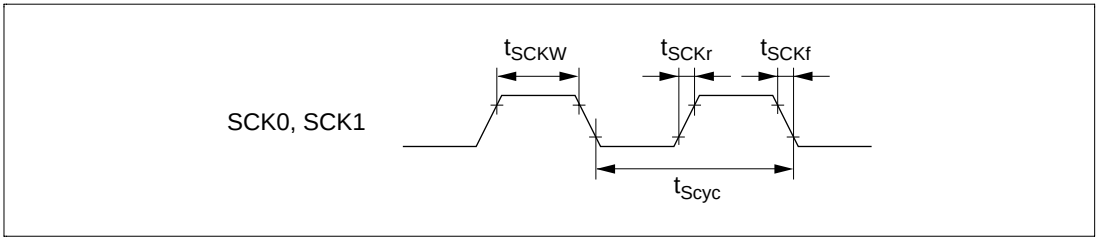


Figure 7.20 SCK Clock Input Timing

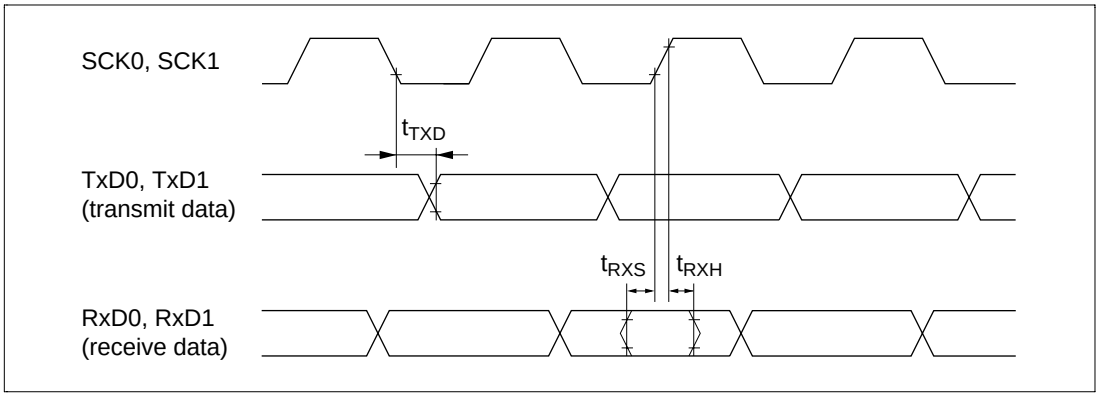


Figure 7.21 SCI Input/Output Timing (Synchronous Mode)

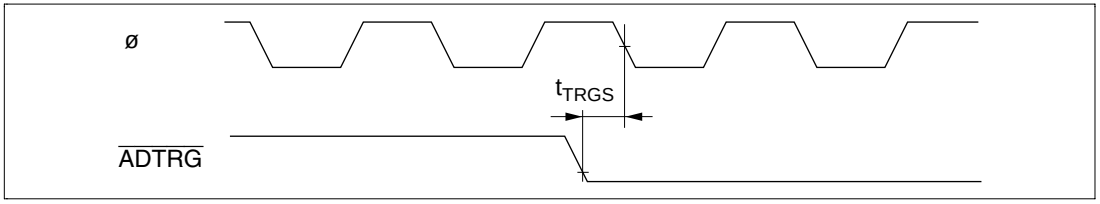


Figure 7.22 A/D Converter External Trigger Input Timing

7.1.4 A/D Conversion Characteristics

Table 7.8 A/D Conversion Characteristics

Condition A: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

	Condition A			Condition B			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	Bits
Conversion time	6.7	—	—	10.6	—	—	µs
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal source impedance	—	—	5	—	—	5	kΩ
Nonlinearity error	—	—	±5.5	—	—	±5.5	LSB
Offset error	—	—	±5.5	—	—	±5.5	LSB
Full-scale error	—	—	±5.5	—	—	±5.5	LSB
Quantization error	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±6.0	—	—	±6.0	LSB

7.1.5 D/A Conversion Characteristics

Table 7.9 D/A Conversion Characteristics

Condition A: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

	Condition A			Condition B				
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Resolution	8	8	8	8	8	8	Bits	
Conversion time	—	—	10	—	—	10	µs	20 pF capacitive load
Absolute accuracy	—	±2.0	±3.0	—	±2.0	±3.0	LSB	2 MΩ resistive load
	—	—	±2.0	—	—	±2.0	LSB	4 MΩ resistive load

7.2 Electrical Characteristics of Mask ROM Version (H8S/2318, H8S/2317) in Low-Voltage Operation

7.2.1 Absolute Maximum Ratings

Table 7.10 lists the absolute maximum ratings.

Table 7.10 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.3 to +4.3	V
Input voltage (except port 4)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (port 4)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference power supply voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +4.3	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

7.2.2 DC Characteristics

Table 7.11 DC Characteristics

Condition C: V_{CC} = 2.4 V to 3.6 V, AV_{CC} = 2.4 V to 3.6 V, V_{ref} = 2.4 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*[1], T_a = –20°C to +75°C (regular specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Ports 1, 2, $\overline{IRQ0}$ to $\overline{IRQ7}$	VT^-	$V_{CC} \times 0.2$	—	—	V	
		VT^+	—	—	$V_{CC} \times 0.7$	V	
		$VT^+ - VT^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD2 to MD0	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Ports 3, A to G		2.2	—	V_{CC} + 0.3	V	
	Port 4		2.2	—	AV_{CC} + 0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD2 to MD0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 3, 4, A to G		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD2 to MD0		—	—	1.0	µA	
	Port 4		—	—	1.0	µA	V_{in} = 0.5 to AV_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 1, 2, 3, A to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input pull-up MOS current	Ports A to E	$-I_p$	10	—	300	µA	V_{in} = 0V
Input capacitance	$\overline{RES}$	C_{in}	—	—	30	pF	V_{in} = 0 V
	NMI		—	—	30	pF	f = 1 MHz
	All input pins except $\overline{RES}$ and NMI		—	—	15	pF	T_a = 25°C
Current dissipation*[2]	Normal operation	I_{CC}*[4]	—	18 (2.7 V)	39	mA	f = 14 MHz
	Sleep mode		—	12 (2.7 V)	26	mA	f = 14 MHz
	Standby mode*[3]		—	0.01	10	µA	$T_a \leq 50°C$
			—	—	80		50°C < T_a
Analog power supply voltage	During A/D and D/A conversion	AI_{CC}	—	0.2 (3.0 V)	2.0	mA	
	Idle		—	0.01	5.0	µA	
Reference power supply voltage	During A/D and D/A conversion	AI_{CC}	—	1.4 (3.0 V)	3.0	mA	
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. **If the A/D and D/A converters are not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins open**. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.

2. Current dissipation values are for $V_{IH\ min} = V_{CC} - 0.2$ V and $V_{IL\ max} = 0.2$ V with all output pins unloaded and all MOS input pull-ups in the off state.

3. The values are for $V_{RAM} \leq V_{CC} < 2.4$ V, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.

4. I_{CC} depends on V_{CC} and f as follows:

   I_{CC} max = 1.0 (mA) + 0.74 (mA/(MHz × V)) × V_{CC} × f (normal operation)

   I_{CC} max = 1.0 (mA) + 0.50 (mA/(MHz × V)) × V_{CC} × f (sleep mode)

Table 7.12 Permissible Output Currents

Condition C: V_{CC} = 2.4 V to 3.6 V, AV_{CC} = 2.4 V to 3.6 V, V_{ref} = 2.4 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	All output pins	I_{OL}	—	—	2.0	mA
Permissible output low current (total)	Total of all output pins	ΣI_{OL}	—	—	80	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	40	mA

Note: To protect chip reliability, do not exceed the output current values in table 7.12.

7.2.3 AC Characteristics

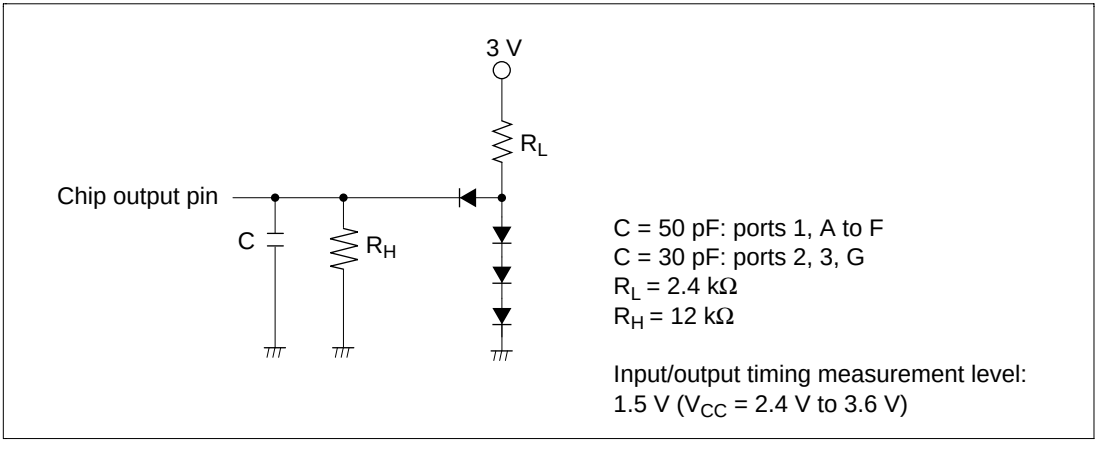


Figure 7.23 Output Load Circuit

(1) Clock Timing

Table 7.13 Clock Timing

Condition C: V_{CC} = 2.4 V to 3.6 V, AV_{CC} = 2.4 V to 3.6 V, V_{ref} = 2.4 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 14 MHz, T_a = –20°C to 75°C (regular specifications)

		Condition C			
Item	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
Clock cycle time	t_{cyc}	71	500	ns	Figure 7.2
Clock pulse high width	t_{CH}	28	—	ns	
Clock pulse low width	t_{CL}	28	—	ns	
Clock rise time	t_{Cr}	—	7.5	ns	
Clock fall time	t_{Cf}	—	7.5	ns	
Reset oscillation stabilization time (crystal)	t_{OSC1}	10	—	ms	Figure 7.3
Software standby oscillation stabilization time (crystal)	t_{OSC2}	10	—	ms	
External clock output stabilization delay time	t_{DEXT}	500	—	µs	Figure 7.3

(2) Control Signal Timing

Table 7.14 Control Signal Timing

Condition C: V_{CC} = 2.4 V to 3.6 V, AV_{CC} = 2.4 V to 3.6 V, V_{ref} = 2.4 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 14 MHz, T_a = –20°C to 75°C (regular specifications)

		Condition C			
Item	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{RES}$ setup time	t_{RESS}	200	—	ns	Figure 7.4
$\overline{RES}$ pulse width	t_{RESW}	20	—	t_{cyc}	
NMI setup time	t_{NMIS}	150	—	ns	Figure 7.5
NMI hold time	t_{NMIH}	10	—		
NMI pulse width (in recovery from software standby mode)	t_{NMIW}	200	—		
$\overline{IRQ}$ setup time	t_{IRQS}	150	—	ns	
$\overline{IRQ}$ hold time	t_{IRQH}	10	—		
$\overline{IRQ}$ pulse width (in recovery from software standby mode)	t_{IRQW}	200	—		

(3) Bus Timing

Table 7.15 Bus Timing

Condition C: V_{CC} = 2.4 V to 3.6 V, AV_{CC} = 2.4 V to 3.6 V, V_{ref} = 2.4 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 14 MHz, T_a = –20°C to 75°C (regular specifications)

		Condition C			
Item	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
Address delay time	t_{AD}	—	20	ns	Figures 7.6 to 7.10
Address setup time	t_{AS}	$0.5 \times t_{cyc} - 15$	—	ns	
Address hold time	t_{AH}	$0.5 \times t_{cyc} - 15$	—	ns	
$\overline{CS}$ delay time 1	t_{CSD1}	—	25	ns	
$\overline{AS}$ delay time	t_{ASD}	—	25	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	25	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	25	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
Read data access time 1	t_{ACC1}	—	$1.0 \times t_{cyc} - 35$	ns	
Read data access time 2	t_{ACC2}	—	$1.5 \times t_{cyc} - 35$	ns	
Read data access time 3	t_{ACC3}	—	$2.0 \times t_{cyc} - 35$	ns	
Read data access time 4	t_{ACC4}	—	$2.5 \times t_{cyc} - 35$	ns	
Read data access time 5	t_{ACC5}	—	$3.0 \times t_{cyc} - 35$	ns	
$\overline{WR}$ delay time 1	t_{WRD1}	—	25	ns	
$\overline{WR}$ delay time 2	t_{WRD2}	—	25	ns	
$\overline{WR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc} - 25$	—	ns	
$\overline{WR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc} - 25$	—	ns	
Write data delay time	t_{WDD}	—	30	ns	
Write data setup time	t_{WDS}	$0.5 \times t_{cyc} - 25$	—	ns	
Write data hold time	t_{WDH}	$0.5 \times t_{cyc} - 15$	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	40	—	ns	Figure 7.8
$\overline{WAIT}$ hold time	t_{WTH}	5	—	ns	
$\overline{BREQ}$ setup time	t_{BRQS}	30	—	ns	Figure 7.11
$\overline{BACK}$ delay time	t_{BACD}	—	15	ns	
Bus floating time	t_{BZD}	—	70	ns	
$\overline{BREQO}$ delay time	t_{BRQOD}	—	40	ns	Figure 7.12

(4) Timing of On-Chip Supporting Modules

Table 7.16 Timing of On-Chip Supporting Modules

Condition C: V_{CC} = 2.4 V to 3.6 V, AV_{CC} = 2.4 V to 3.6 V, V_{ref} = 2.4 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 14 MHz, T_a = –20°C to 75°C (regular specifications)

				Condition C			
Item			**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
I/O ports	Output data delay time		t_{PWD}	—	70	ns	Figure 7.13
	Input data setup time		t_{PRS}	40	—		
	Input data hold time		t_{PRH}	40	—		
TPU	Timer output delay time		t_{TOCD}	—	70	ns	Figure 7.14
	Timer input setup time		t_{TICS}	40	—		
	Timer clock input setup time		t_{TCKS}	40	—	ns	Figure 7.15
	Timer clock pulse width	Single-edge specification	t_{TCKWH}	1.5	—	t_{cyc}	
		Both-edge specification	t_{TCKWL}	2.5	—		
8-bit timer	Timer output delay time		t_{TMOD}	—	70	ns	Figure 7.16
	Timer reset input setup time		t_{TMRS}	40	—	ns	Figure 7.18
	Timer clock input setup time		t_{TMCS}	40	—	ns	Figure 7.17
	Timer clock pulse width	Single-edge specification	t_{TMCWH}	1.5	—	t_{cyc}	
		Both-edge specification	t_{TMCWL}	2.5	—		
WDT	Overflow output delay time		t_{WOVD}	—	70	ns	Figure 7.19
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{cyc}	Figure 7.20
		Synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	1.5	t_{cyc}	
	Input clock fall time		t_{SCKf}	—	1.5		
	Transmit data delay time		t_{TXD}	—	70	ns	Figure 7.21
	Receive data setup time (synchronous)		t_{RXS}	70	—	ns	
	Receive data hold time (synchronous)		t_{RXH}	70	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	30	—	ns	Figure 7.22

7.2.4 A/D Conversion Characteristics

Table 7.17 A/D Conversion Characteristics

Condition C: V_{CC} = 2.4 V to 3.6 V, AV_{CC} = 2.4 V to 3.6 V, V_{ref} = 2.4 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 14 MHz, T_a = –20°C to 75°C (regular specifications)

	Condition C			
Item	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	Bits
Conversion time	19.0	—	—	µs
Analog input capacitance	—	—	20	pF
Permissible signal source impedance	—	—	5	kΩ
Nonlinearity error	—	—	±7.5	LSB
Offset error	—	—	±7.5	LSB
Full-scale error	—	—	±7.5	LSB
Quantization error	—	—	±0.5	LSB
Absolute accuracy	—	—	±8.0	LSB

7.2.5 D/A Conversion Characteristics

Table 7.18 D/A Conversion Characteristics

Condition C: V_{CC} = 2.4 V to 3.6 V, AV_{CC} = 2.4 V to 3.6 V, V_{ref} = 2.4 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 14 MHz, T_a = –20°C to 75°C (regular specifications)

	Condition C				
Item	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
Resolution	8	8	8	Bits	
Conversion time	—	—	10	µs	20 pF capacitive load
Absolute accuracy	—	±2.0	±3.0	LSB	2 MΩ resistive load
	—	—	±2.0	LSB	4 MΩ resistive load

7.3 Electrical Characteristics of F-ZTAT Version (H8S/2318)

7.3.1 Absolute Maximum Ratings

Table 7.19 Absolute Maximum Ratings — Preliminary —

Condition A (In planning):
V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.3 to +4.3	V
Input voltage (FWE)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (except port 4)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (port 4)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference power supply voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +4.3	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75*	°C
		Wide-range specifications: –40 to +85*	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

Note: * Condition A (In planning):
The operating temperature ranges for flash memory programming/erasing are T_a = 0°C to +TBD°C (regular specifications) and T_a = 0°C to +TBD°C (wide-range specifications).
The power-supply voltage range for flash memory programming/erasing is V_{CC} = 3.0 V to 3.6 V.

Condition B: The operating temperature ranges for flash memory programming/erasing are T_a = 0°C to +75°C (regular specifications) and T_a = 0°C to +85°C (wide-range specifications).

7.3.2 DC Characteristics

Table 7.20 (a) DC Characteristics — Preliminary —

Condition A (In planning): V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*[1], T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Ports 1, 2, $\overline{IRQ0}$ to $\overline{IRQ7}$	VT^-	$V_{CC} \times 0.2$	—	—	V	
		VT^+	—	—	$V_{CC} \times 0.7$	V	
		$VT^+ - VT^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD2 to MD0, FWE	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Ports 3, A to G		2.2	—	V_{CC} + 0.3	V	
	Port 4		2.2	—	AV_{CC} + 0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD2 to MD0, FWE	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 3, 4, A to G		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD2 to MD0, FWE		—	—	1.0	µA	
	Port 4		—	—	1.0	µA	V_{in} = 0.5 to AV_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 1, 2, 3, A to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input pull-up MOS current	Ports A to E	$-I_p$	10	—	300	µA	V_{CC} = 2.7 V to 3.6 V, V_{in} = 0 V
Input capacitance	$\overline{RES}$	C_{in}	—	—	30	pF	V_{in} = 0 V
	NMI		—	—	30	pF	f = 1 MHz
	All input pins except $\overline{RES}$ and NMI		—	—	15	pF	T_a = 25°C
Current dissipation*2	Normal operation	I_{CC}*4	—	35 (3.0 V)	80	mA	f = 20 MHz
	Sleep mode			25 (3.0 V)	64	mA	f = 20 MHz
	Standby mode*3		—	0.01	10	µA	$T_a \leq$ 50°C
			—	—	80		50°C < T_a
Analog power supply voltage	During A/D and D/A conversion	AI_{CC}	—	0.2 (3.0 V)	2.0	mA	
	Idle		—	0.01	5.0	µA	
Reference power supply voltage	During A/D and D/A conversion	AI_{CC}	—	1.4 (3.0 V)	3.0	mA	
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. **If the A/D and D/A converters are not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins open**. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.

2. Current dissipation values are for $V_{IH\ min} = V_{CC} - 0.2$ V and $V_{IL\ max} = 0.2$ V with all output pins unloaded and all MOS input pull-ups in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.
4. I_{CC} depends on V_{CC} and f as follows:

   I_{CC} max = 1.0 (mA) + 1.10 (mA/(MHz × V)) × V_{CC} × f (normal operation)

   I_{CC} max = 1.0 (mA) + 0.88 (mA/(MHz × V)) × V_{CC} × f (sleep mode)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*[1], T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Ports 1, 2, $\overline{IRQ0}$ to $\overline{IRQ7}$	VT^-	$V_{CC} \times 0.2$	—	—	V	
		VT^+	—	—	$V_{CC} \times 0.7$	V	
		$VT^+ - VT^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD2 to MD0, FWE	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Ports 3, A to G		2.2	—	V_{CC} + 0.3	V	
	Port 4		2.2	—	AV_{CC} + 0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD2 to MD0, FWE	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 3, 4, A to G		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD2 to MD0, FWE		—	—	1.0	µA	
	Port 4		—	—	1.0	µA	V_{in} = 0.5 to AV_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 1, 2, 3, A to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input pull-up MOS current	Ports A to E	$-I_p$	10	—	300	µA	V_{CC} = 3.0 V to 3.6 V, V_{in} = 0 V
Input capacitance	$\overline{RES}$	C_{in}	—	—	30	pF	V_{in} = 0 V
	NMI		—	—	30	pF	f = 1 MHz
	All input pins except $\overline{RES}$ and NMI		—	—	15	pF	T_a = 25°C
Current dissipation*2	Normal operation	I_{CC}*4	—	50 (3.3 V)	100	mA	f = 25 MHz
	Sleep mode			35 (3.3 V)	80	mA	f = 25 MHz
	Standby mode*3		—	0.01	10	µA	$T_a \leq$ 50°C
			—	—	80		50°C < T_a
Analog power supply voltage	During A/D and D/A conversion	AI_{CC}	—	0.2 (3.0 V)	2.0	mA	
	Idle		—	0.01	5.0	µA	
Reference power supply voltage	During A/D and D/A conversion	AI_{CC}	—	1.4 (3.0 V)	3.0	mA	
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. **If the A/D and D/A converters are not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins open**. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.

2. Current dissipation values are for $V_{IH\ min} = V_{CC} - 0.2$ V and $V_{IL\ max} = 0.2$ V with all output pins unloaded and all MOS input pull-ups in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 3.0$ V, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.
4. I_{CC} depends on V_{CC} and f as follows:

   I_{CC} max = 1.0 (mA) + 1.10 (mA/(MHz × V)) × V_{CC} × f (normal operation)

   I_{CC} max = 1.0 (mA) + 0.88 (mA/(MHz × V)) × V_{CC} × f (sleep mode)

Table 7.21 (a) Permissible Output Currents **— Preliminary —**

Condition A (In planning): V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	All output pins	I_{OL}	—	—	2.0	mA
Permissible output low current (total)	Total of all output pins	$\sum I_{OL}$	—	—	80	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\sum -I_{OH}$	—	—	40	mA

Note: To protect chip reliability, do not exceed the output current values in table 7.12 (a).

Table 7.21 (b) Permissible Output Currents **— Preliminary —**

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	All output pins	I_{OL}	—	—	2.0	mA
Permissible output low current (total)	Total of all output pins	$\sum I_{OL}$	—	—	80	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\sum -I_{OH}$	—	—	40	mA

Note: To protect chip reliability, do not exceed the output current values in table 7.12 (b).

7.3.3 AC Characteristics

(1) Clock Timing

Table 7.22 Clock Timing **— Preliminary —**

Condition A (In planning):
V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
Clock cycle time	t_{cyc}	50	500	40	500	ns	Figure 7.2
Clock pulse high width	t_{CH}	20	—	15	—	ns	
Clock pulse low width	t_{CL}	20	—	15	—	ns	
Clock rise time	t_{Cr}	—	5	—	5	ns	
Clock fall time	t_{Cf}	—	5	—	5	ns	
Reset oscillation stabilization time (crystal)	t_{OSC1}	10	—	10	—	ms	Figure 7.3
Software standby oscillation stabilization time (crystal)	t_{OSC2}	10	—	10	—	ms	
External clock output stabilization delay time	t_{DEXT}	500	—	500	—	µs	Figure 7.3

(2) Control Signal Timing

Table 7.23 Control Signal Timing **— Preliminary —**

Condition A (In planning):
V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	ns	Figure 7.4
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	t_{cyc}	
NMI setup time	t_{NMIS}	150	—	150	—	ns	Figure 7.5
NMI hold time	t_{NMIH}	10	—	10	—		
NMI pulse width (in recovery from software standby mode)	t_{NMIW}	200	—	200	—		
$\overline{IRQ}$ setup time	t_{IRQS}	150	—	150	—	ns	
$\overline{IRQ}$ hold time	t_{IRQH}	10	—	10	—		
$\overline{IRQ}$ pulse width (in recovery from software standby mode)	t_{IRQW}	200	—	200	—		

(3) Bus Timing

Table 7.24 Bus Timing **— Preliminary —**

Condition A (In planning):
V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

		Condition A		Condition B			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Address delay time	t_{AD}	—	20	—	20	ns	Figures 7.6 to 7.10
Address setup time	t_{AS}	0.5 × t_{cyc} – 15	—	0.5 × t_{cyc} – 15	—	ns	
Address hold time	t_{AH}	0.5 × t_{cyc} – 10	—	0.5 × t_{cyc} – 8	—	ns	
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	—	15	ns	
$\overline{AS}$ delay time	t_{ASD}	—	20	—	15	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	20	—	15	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	20	—	15	ns	
Read data setup time	t_{RDS}	15	—	15	—	ns	
Read data hold time	t_{RDH}	0	—	0	—	ns	
Read data access time 1	t_{ACC1}	—	1.0 × t_{cyc} – 25	—	1.0 × t_{cyc} – 20	ns	
Read data access time 2	t_{ACC2}	—	1.5 × t_{cyc} – 25	—	1.5 × t_{cyc} – 20	ns	
Read data access time 3	t_{ACC3}	—	2.0 × t_{cyc} – 25	—	2.0 × t_{cyc} – 20	ns	
Read data access time 4	t_{ACC4}	—	2.5 × t_{cyc} – 25	—	2.5 × t_{cyc} – 20	ns	
Read data access time 5	t_{ACC5}	—	3.0 × t_{cyc} – 25	—	3.0 × t_{cyc} – 20	ns	

Item	Symbol	Condition A		Condition B		Unit	Test Conditions
		Min	Max	Min	Max		
$\overline{WR}$ delay time 1	t_{WRD1}	—	20	—	15	ns	Figures 7.6 to 7.10
$\overline{WR}$ delay time 2	t_{WRD2}	—	20	—	15	ns	
$\overline{WR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc} - 20$	—	$1.0 \times t_{cyc} - 15$	—	ns	
$\overline{WR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc} - 20$	—	$1.5 \times t_{cyc} - 15$	—	ns	
Write data delay time	t_{WDD}	—	30	—	20	ns	
Write data setup time	t_{WDS}	$0.5 \times t_{cyc} - 20$	—	$0.5 \times t_{cyc} - 15$	—	ns	
Write data hold time	t_{WDH}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 8$	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	30	—	25	—	ns	Figure 7.8
$\overline{WAIT}$ hold time	t_{WTH}	5	—	5	—	ns	
$\overline{BREQ}$ setup time	t_{BRQS}	30	—	30	—	ns	Figure 7.11
$\overline{BACK}$ delay time	t_{BACD}	—	15	—	15	ns	
Bus floating time	t_{BZD}	—	50	—	40	ns	
$\overline{BREQO}$ delay time	t_{BRQOD}	—	30	—	25	ns	Figure 7.12

(4) Timing of On-Chip Supporting Modules

Table 7.25 Timing of On-Chip Supporting Modules —Preliminary—

Condition A (In planning):
V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

				Condition A		Condition B			Test
Item			**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
I/O ports	Output data delay time		t_{PWD}	—	50	—	40	ns	Figure 7.13
	Input data setup time		t_{PRS}	30	—	25	—		
	Input data hold time		t_{PRH}	30	—	25	—		
TPU	Timer output delay time		t_{TOCD}	—	50	—	40	ns	Figure 7.14
	Timer input setup time		t_{TICS}	30	—	25	—		
	Timer clock input setup time		t_{TCKS}	30	—	25	—	ns	Figure 7.15
	Timer clock pulse width	Single-edge specification	t_{TCKWH}	1.5	—	1.5	—	t_{cyc}	
		Both-edge specification	t_{TCKWL}	2.5	—	2.5	—		
8-bit timer	Timer output delay time		t_{TMOD}	—	50	—	40	ns	Figure 7.16
	Timer reset input setup time		t_{TMRS}	30	—	25	—	ns	Figure 7.18
	Timer clock input setup time		t_{TMCS}	30	—	25	—	ns	Figure 7.17
	Timer clock pulse width	Single-edge specification	t_{TMCWH}	1.5	—	1.5	—	t_{cyc}	
		Both-edge specification	t_{TMCWL}	2.5	—	2.5	—		

Item			Symbol	Condition A Min	Condition A Max	Condition B Min	Condition B Max	Unit	Test Conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	4	—	t_{cyc}	Figure 7.20
		Synchronous		6	—	6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	1.5	—	1.5	t_{cyc}	
	Input clock fall time		t_{SCKf}	—	1.5	—	1.5		
	Transmit data delay time		t_{TXD}	—	50	—	40	ns	Figure 7.21
	Receive data setup time (synchronous)		t_{RXS}	50	—	40	—	ns	
	Receive data hold time (synchronous)		t_{RXH}	50	—	40	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	30	—	30	—	ns	Figure 7.22

7.3.4 A/D Conversion Characteristics

Table 7.26 A/D Conversion Characteristics — Preliminary —

Condition A (In planning):
V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

	Condition A			Condition B			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	Bits
Conversion time	6.7	—	—	10.6	—	—	µs
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal source impedance	—	—	5	—	—	5	kΩ
Nonlinearity error	—	—	±5.5	—	—	±5.5	LSB
Offset error	—	—	±5.5	—	—	±5.5	LSB
Full-scale error	—	—	±5.5	—	—	±5.5	LSB
Quantization error	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±6.0	—	—	±6.0	LSB

7.3.5 D/A Conversion Characteristics

Table 7.27 D/A Conversion Characteristics — Preliminary —

Condition A (In planning):
V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

	Condition A			Condition B				
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Resolution	8	8	8	8	8	8	Bits	
Conversion time	—	—	10	—	—	10	µs	20 pF capacitive load
Absolute accuracy	—	±2.0	±3.0	—	±2.0	±3.0	LSB	2 MΩ resistive load
	—	—	±2.0	—	—	±2.0	LSB	4 MΩ resistive load

7.3.6 Flash Memory Characteristics

Table 7.28 (a) Flash Memory Characteristics — Preliminary —

Condition A*[7] (In planning):

V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, (program/erase power-supply voltage range: V_{CC} = 3.0 V to 3.6 V), T_a = 0°C to +75°C (program/erase operating temperature range: regular specifications), T_a = 0°C to +85°C (program/erase operating temperature range: wide-range specifications)

Item		Symbol		Min	Typ	Max	Unit	Test Conditions
Programming time*[1, 2, 4]		t_P		—	TBD	200	ms/ 128 bytes	
Erase time*[1, 3, 6]		t_E		—	TBD	1000	ms/block	
Rewrite times		NWEC		—	—	TBD	Times	
Programming	Wait time after SWE bit setting*[1]	x		1	—	—	µs	
	Wait time after PSU bit setting*[1]	y		50	—	—	µs	
	Wait time after P bit setting*[1, 4]	z	(z1)	—	—	30	µs	1 ≤ n ≤ 6
			(z2)	—	—	200	µs	7 ≤ n ≤ 1000
			(z3)	—	—	10	µs	Additional-programming time wait
	Wait time after P bit clearing*[1]	α		5	—	—	µs	
	Wait time after PSU bit clearing*[1]	β		5	—	—	µs	
	Wait time after PV bit setting*[1]	γ		4	—	—	µs	
	Wait time after H'FF dummy write*[1]	ε		2	—	—	µs	
	Wait time after PV bit clearing*[1]	η		2	—	—	µs	
	Wait time after SWE bit clearing*[1]	θ		100	—	—	µs	
	Maximum number of writes*[1, 4]	N		—	—	1000*[5]	Times	
Erasing	Wait time after SWE bit setting*[1]	x		1	—	—	µs	
	Wait time after ESU bit setting*[1]	y		100	—	—	µs	
	Wait time after E bit setting*[1, 6]	z		—	—	10	µs	
	Wait time after E bit clearing*[1]	α		10	—	—	µs	
	Wait time after ESU bit clearing*[1]	β		10	—	—	µs	
	Wait time after EV bit setting*[1]	γ		20	—	—	µs	
	Wait time after H'FF dummy write*[1]	ε		2	—	—	µs	
	Wait time after EV bit clearing*[1]	η		4	—	—	µs	
	Wait time after SWE bit clearing*[1]	θ		100	—	—	µs	
	Maximum number of erases*[1, 6]	N		—	—	100	Times	

Notes:
1. Follow the program/erase algorithms when making the time settings.
2. Programming time per 128 bytes. (Indicates the total time during which the P bit is set in flash memory control register 1 (FLMCR1). Does not include the program-verify time.)
3. Time to erase one block. (Indicates the time during which the E bit is set in FLMCR1. Does not include the erase-verify time.)
4. Maximum programming time

   $t_P(max) = \sum_{i=1}^{N}$ wait time after P bit setting (z)
5. The maximum number of writes (N) should be set as shown below according to the actual set value of z so as not to exceed the maximum programming time ($t_P(max)$).

   The wait time after P bit setting (z) should be changed as follows according to the number of writes (n).

   Number of writes (n)

   $1 \leq n \leq 6$ z = 30 µs

   $7 \leq n \leq 1000$ z = 200 µs

   [In additional programming]

   Number of writes (n)

   $1 \leq n \leq 6$ z = 10 µs
6. For the maximum erase time ($t_E(max)$), the following relationship applies between the wait time after E bit setting (z) and the maximum number of erases (N):

   $t_E(max)$ = Wait time after E bit setting (z) $\times$ maximum number of erases (N)
7. The power-supply voltage range for flash memory programming/erasing is V_{CC} = 3.0 V to 3.6 V.

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = 0°C to +75°C (program/erase operating temperature range: regular specifications), T_a = 0°C to +85°C (program/erase operating temperature range: wide-range specifications)

Item		Symbol		Min	Typ	Max	Unit	Test Conditions
Programming time*1, *2, *4		t_P		—	10	200	ms/ 128 bytes	
Erase time*1, *3, *6		t_E		—	50	1000	ms/block	
Rewrite times		NWEC		—	—	100	Times	
Programming	Wait time after SWE bit setting*1	x		1	—	—	µs	
	Wait time after PSU bit setting*1	y		50	—	—	µs	
	Wait time after P bit setting*1, *4	z	(z1)	—	—	30	µs	1 ≤ n ≤ 6
			(z2)	—	—	200	µs	7 ≤ n ≤ 1000
			(z3)	—	—	10	µs	Additional-programming time wait
	Wait time after P bit clearing*1	α		5	—	—	µs	
	Wait time after PSU bit clearing*1	β		5	—	—	µs	
	Wait time after PV bit setting*1	γ		4	—	—	µs	
	Wait time after H'FF dummy write*1	ε		2	—	—	µs	
	Wait time after PV bit clearing*1	η		2	—	—	µs	
	Wait time after SWE bit clearing*1	θ		100	—	—	µs	
	Maximum number of writes*1, *4	N		—	—	1000*5	Times	
Erasing	Wait time after SWE bit setting*1	x		1	—	—	µs	
	Wait time after ESU bit setting*1	y		100	—	—	µs	
	Wait time after E bit setting*1, *6	z		—	—	10	µs	
	Wait time after E bit clearing*1	α		10	—	—	µs	
	Wait time after ESU bit clearing*1	β		10	—	—	µs	
	Wait time after EV bit setting*1	γ		20	—	—	µs	
	Wait time after H'FF dummy write*1	ε		2	—	—	µs	
	Wait time after EV bit clearing*1	η		4	—	—	µs	
	Wait time after SWE bit clearing*1	θ		100	—	—	µs	
	Maximum number of erases*1, *6	N		—	—	100	Times	

Notes: 1. Follow the program/erase algorithms when making the time settings.
2. Programming time per 128 bytes. (Indicates the total time during which the P bit is set in flash memory control register 1 (FLMCR1). Does not include the program-verify time.)
3. Time to erase one block. (Indicates the time during which the E bit is set in FLMCR1. Does not include the erase-verify time.)

4. Maximum programming time

$$t_P(max) = \sum_{i=1}^{N} \text{wait time after P bit setting (z)}$$

5. The maximum number of writes (N) should be set as shown below according to the actual set value of z so as not to exceed the maximum programming time (t_P(max)).

   The wait time after P bit setting (z) should be changed as follows according to the number of writes (n).

   Number of writes (n)

   $1 \leq n \leq 6$ z = 30 µs

   $7 \leq n \leq 1000$ z = 200 µs

   [In additional programming]

   Number of writes (n)

   $1 \leq n \leq 6$ z = 10 µs

6. For the maximum erase time (t_E(max)), the following relationship applies between the wait time after E bit setting (z) and the maximum number of erases (N):

   t_E(max) = Wait time after E bit setting (z) $\times$ maximum number of erases (N)

7. The power-supply voltage range for flash memory programming/erasing is V_{CC} = 3.0 V to 3.6 V.

7.4 Electrical Characteristics of F-ZTAT Version (H8S/2315) (Under Development)

7.4.1 Absolute Maximum Ratings

Table 7.29 Absolute Maximum Ratings — Preliminary —

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.3 to +4.3	V
Input voltage (FWE)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (except port 4)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (port 4)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference power supply voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +4.3	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75*	°C
		Wide-range specifications: –40 to +85*	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

Note: * The operating temperature ranges for flash memory programming/erasing are as follows: T_a = 0°C to +TBD°C (regular specifications), T_a = 0°C to +TBD°C (wide-range specifications).
The power-supply voltage range for flash memory programming/erasing is V_{CC} = 3.0 V to 3.6 V.

7.4.2 DC Characteristics

Table 7.30 (a) DC Characteristics — Preliminary —

Condition A (In planning):

V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V*[1], T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Ports 1, 2, $\overline{IRQ0}$ to $\overline{IRQ7}$	VT^-	$V_{CC} \times 0.2$	—	—	V	
		VT^+	—	—	$V_{CC} \times 0.7$	V	
		$VT^+ - VT^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD2 to MD0, FWE	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Ports 3, A to G		2.2	—	V_{CC} + 0.3	V	
	Port 4		2.2	—	AV_{CC} + 0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD2 to MD0, FWE	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 3, 4, A to G		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD2 to MD0, FWE		—	—	1.0	µA	
	Port 4		—	—	1.0	µA	V_{in} = 0.5 to AV_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 1, 2, 3, A to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input pull-up MOS current	Ports A to E	$-I_p$	10	—	300	µA	V_{CC} = 2.7 V to 3.6 V, V_{in} = 0 V
Input capacitance	$\overline{RES}$	C_{in}	—	—	30	pF	V_{in} = 0 V
	NMI		—	—	30	pF	f = 1 MHz
	All input pins except $\overline{RES}$ and NMI		—	—	15	pF	T_a = 25°C
Current dissipation*2	Normal operation	I_{CC}*4	—	TBD (3.0 V)	TBD	mA	f = 20 MHz
	Sleep mode			TBD (3.0 V)	TBD	mA	f = 20 MHz
	Standby mode*3		—	0.01	10	µA	$T_a \leq$ 50°C
			—	—	80		50°C < T_a
Analog power supply voltage	During A/D and D/A conversion	AI_{CC}	—	0.2 (3.0 V)	2.0	mA	
	Idle		—	0.01	5.0	µA	
Reference power supply voltage	During A/D and D/A conversion	AI_{CC}	—	1.4 (3.0 V)	3.0	mA	
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. **If the A/D and D/A converters are not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins open**. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.

2. Current dissipation values are for $V_{IH\ min} = V_{CC} - 0.2$ V and $V_{IL\ max} = 0.2$ V with all output pins unloaded and all MOS input pull-ups in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.
4. I_{CC} depends on V_{CC} and f as follows:
   I_{CC} max = 1.0 (mA) + TBD (mA/(MHz × V)) × V_{CC} × f (normal operation)
   I_{CC} max = 1.0 (mA) + TBD (mA/(MHz × V)) × V_{CC} × f (sleep mode)

Condition B (Under development):

V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V*[1], T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Ports 1, 2, $\overline{IRQ0}$ to $\overline{IRQ7}$	VT^-	$V_{CC} \times 0.2$	—	—	V	
		VT^+	—	—	$V_{CC} \times 0.7$	V	
		$VT^+ - VT^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD2 to MD0, FWE	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Ports 3, A to G		2.2	—	V_{CC} + 0.3	V	
	Port 4		2.2	—	AV_{CC} + 0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD2 to MD0, FWE	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 3, 4, A to G		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD2 to MD0, FWE		—	—	1.0	µA	
	Port 4		—	—	1.0	µA	V_{in} = 0.5 to AV_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 1, 2, 3, A to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input pull-up MOS current	Ports A to E	$-I_p$	10	—	300	µA	V_{CC} = 3.0 V to 3.6 V, V_{in} = 0 V
Input capacitance	$\overline{RES}$	C_{in}	—	—	30	pF	V_{in} = 0 V
	NMI		—	—	30	pF	f = 1 MHz
	All input pins except $\overline{RES}$ and NMI		—	—	15	pF	T_a = 25°C
Current dissipation*2	Normal operation	I_{CC}*4	—	TBD (3.3 V)	TBD	mA	f = 25 MHz
	Sleep mode			TBD (3.3 V)	TBD	mA	f = 25 MHz
	Standby mode*3		—	0.01	10	µA	$T_a \leq$ 50°C
			—	—	80		50°C < T_a
Analog power supply voltage	During A/D and D/A conversion	AI_{CC}	—	0.2 (3.0 V)	2.0	mA	
	Idle		—	0.01	5.0	µA	
Reference power supply voltage	During A/D and D/A conversion	AI_{CC}	—	1.4 (3.0 V)	3.0	mA	
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. **If the A/D and D/A converters are not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins open**. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.

2. Current dissipation values are for $V_{IH\ min} = V_{CC} - 0.2$ V and $V_{IL\ max} = 0.2$ V with all output pins unloaded and all MOS input pull-ups in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 3.0$ V, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.
4. I_{CC} depends on V_{CC} and f as follows:
   I_{CC} max = 1.0 (mA) + TBD (mA/(MHz × V)) × V_{CC} × f (normal operation)
   I_{CC} max = 1.0 (mA) + TBD (mA/(MHz × V)) × V_{CC} × f (sleep mode)

Table 7.31 (a) Permissible Output Currents **— Preliminary —**

Condition A (In planning):

V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 to 3.6 V, V_{ref} = 2.7 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, T_a = –20 to +75°C (regular specifications),
T_a = –40 to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	All output pins	I_{OL}	—	—	2.0	mA
Permissible output low current (total)	Total of all output pins	$\sum I_{OL}$	—	—	80	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\sum -I_{OH}$	—	—	40	mA

Note: To protect chip reliability, do not exceed the output current values in table 7.31 (a).

Table 7.31 (b) Permissible Output Currents **— Preliminary —**

Condition B (Under development):

V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 to 3.6 V, V_{ref} = 3.0 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, T_a = –20 to +75°C (regular specifications),
T_a = –40 to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	All output pins	I_{OL}	—	—	2.0	mA
Permissible output low current (total)	Total of all output pins	$\sum I_{OL}$	—	—	80	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\sum -I_{OH}$	—	—	40	mA

Note: To protect chip reliability, do not exceed the output current values in table 7.31 (b).

7.4.3 AC Characteristics

(1) Clock Timing

Table 7.32 Clock Timing **— Preliminary —**

Condition A (In planning):

V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications),
T_a = –40°C to 85°C (wide-range specifications)

Condition B (Under development):

V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications),
T_a = –40°C to 85°C (wide-range specifications)

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
Clock cycle time	t_{cyc}	50	500	40	500	ns	Figure 7.2
Clock pulse high width	t_{CH}	20	—	15	—	ns	
Clock pulse low width	t_{CL}	20	—	15	—	ns	
Clock rise time	t_{Cr}	—	5	—	5	ns	
Clock fall time	t_{Cf}	—	5	—	5	ns	
Reset oscillation stabilization time (crystal)	t_{OSC1}	10	—	10	—	ms	Figure 7.3
Software standby oscillation stabilization time (crystal)	t_{OSC2}	10	—	10	—	ms	
External clock output stabilization delay time	t_{DEXT}	500	—	500	—	µs	Figure 7.3

(2) Control Signal Timing

Table 7.33 Control Signal Timing — Preliminary —

Condition A (In planning):

V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications),
T_a = –40°C to 85°C (wide-range specifications)

Condition B (Under development):

V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications),
T_a = –40°C to 85°C (wide-range specifications)

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	ns	Figure 7.4
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	t_{cyc}	
NMI setup time	t_{NMIS}	150	—	150	—	ns	Figure 7.5
NMI hold time	t_{NMIH}	10	—	10	—		
NMI pulse width (in recovery from software standby mode)	t_{NMIW}	200	—	200	—		
$\overline{IRQ}$ setup time	t_{IRQS}	150	—	150	—	ns	
$\overline{IRQ}$ hold time	t_{IRQH}	10	—	10	—		
$\overline{IRQ}$ pulse width (in recovery from software standby mode)	t_{IRQW}	200	—	200	—		

(3) Bus Timing

Table 7.34 Bus Timing **— Preliminary —**

Condition A (In planning):

V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications),
T_a = –40°C to 85°C (wide-range specifications)

Condition B (Under development):

V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications),
T_a = –40°C to 85°C (wide-range specifications)

		Condition A		Condition B			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Address delay time	t_{AD}	—	20	—	20	ns	Figures 7.6 to 7.10
Address setup time	t_{AS}	0.5 × t_{cyc} – 15	—	0.5 × t_{cyc} – 15	—	ns	
Address hold time	t_{AH}	0.5 × t_{cyc} – 10	—	0.5 × t_{cyc} – 8	—	ns	
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	—	15	ns	
$\overline{AS}$ delay time	t_{ASD}	—	20	—	15	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	20	—	15	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	20	—	15	ns	
Read data setup time	t_{RDS}	15	—	15	—	ns	
Read data hold time	t_{RDH}	0	—	0	—	ns	
Read data access time 1	t_{ACC1}	—	1.0 × t_{cyc} – 25	—	1.0 × t_{cyc} – 20	ns	
Read data access time 2	t_{ACC2}	—	1.5 × t_{cyc} – 25	—	1.5 × t_{cyc} – 20	ns	
Read data access time 3	t_{ACC3}	—	2.0 × t_{cyc} – 25	—	2.0 × t_{cyc} – 20	ns	
Read data access time 4	t_{ACC4}	—	2.5 × t_{cyc} – 25	—	2.5 × t_{cyc} – 20	ns	
Read data access time 5	t_{ACC5}	—	3.0 × t_{cyc} – 25	—	3.0 × t_{cyc} – 20	ns	

Item	Symbol	Condition A		Condition B		Unit	Test Conditions
		Min	Max	Min	Max		
$\overline{WR}$ delay time 1	t_{WRD1}	—	20	—	15	ns	Figures 7.6 to 7.10
$\overline{WR}$ delay time 2	t_{WRD2}	—	20	—	15	ns	
$\overline{WR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc} - 20$	—	$1.0 \times t_{cyc} - 15$	—	ns	
$\overline{WR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc} - 20$	—	$1.5 \times t_{cyc} - 15$	—	ns	
Write data delay time	t_{WDD}	—	30	—	20	ns	
Write data setup time	t_{WDS}	$0.5 \times t_{cyc} - 20$	—	$0.5 \times t_{cyc} - 15$	—	ns	
Write data hold time	t_{WDH}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 8$	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	30	—	25	—	ns	Figure 7.8
$\overline{WAIT}$ hold time	t_{WTH}	5	—	5	—	ns	
$\overline{BREQ}$ setup time	t_{BRQS}	30	—	30	—	ns	Figure 7.11
$\overline{BACK}$ delay time	t_{BACD}	—	15	—	15	ns	
Bus floating time	t_{BZD}	—	50	—	40	ns	
$\overline{BREQO}$ delay time	t_{BRQOD}	—	30	—	25	ns	Figure 7.12

(4) Timing of On-Chip Supporting Modules

Table 7.35 Timing of On-Chip Supporting Modules —Preliminary—

Condition A (In planning):

V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B (Under development):

V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

				Condition A		Condition B			Test
Item			**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
I/O ports	Output data delay time		t_{PWD}	—	50	—	40	ns	Figure 7.13
	Input data setup time		t_{PRS}	30	—	25	—		
	Input data hold time		t_{PRH}	30	—	25	—		
TPU	Timer output delay time		t_{TOCD}	—	50	—	40	ns	Figure 7.14
	Timer input setup time		t_{TICS}	30	—	25	—		
	Timer clock input setup time		t_{TCKS}	30	—	25	—	ns	Figure 7.15
	Timer clock pulse width	Single-edge specification	t_{TCKWH}	1.5	—	1.5	—	t_{cyc}	
		Both-edge specification	t_{TCKWL}	2.5	—	2.5	—		
8-bit timer	Timer output delay time		t_{TMOD}	—	50	—	40	ns	Figure 7.16
	Timer reset input setup time		t_{TMRS}	30	—	25	—	ns	Figure 7.18
	Timer clock input setup time		t_{TMCS}	30	—	25	—	ns	Figure 7.17
	Timer clock pulse width	Single-edge specification	t_{TMCWH}	1.5	—	1.5	—	t_{cyc}	
		Both-edge specification	t_{TMCWL}	2.5	—	2.5	—		

Item			Symbol	Condition A Min	Condition A Max	Condition B Min	Condition B Max	Unit	Test Conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	4	—	t_{cyc}	Figure 7.20
		Synchronous		6	—	6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	1.5	—	1.5	t_{cyc}	
	Input clock fall time		t_{SCKf}	—	1.5	—	1.5		
	Transmit data delay time		t_{TXD}	—	50	—	40	ns	Figure 7.21
	Receive data setup time (synchronous)		t_{RXS}	50	—	40	—	ns	
	Receive data hold time (synchronous)		t_{RXH}	50	—	40	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	30	—	30	—	ns	Figure 7.22

7.4.4 A/D Conversion Characteristics

Table 7.36 A/D Conversion Characteristics — Preliminary —

Condition A (In planning):

V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications),
T_a = –40°C to 85°C (wide-range specifications)

Condition B (Under development):

V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications),
T_a = –40°C to 85°C (wide-range specifications)

	Condition A			Condition B			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	Bits
Conversion time	6.7	—	—	10.6	—	—	µs
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal source impedance	—	—	5	—	—	5	kΩ
Nonlinearity error	—	—	±5.5	—	—	±5.5	LSB
Offset error	—	—	±5.5	—	—	±5.5	LSB
Full-scale error	—	—	±5.5	—	—	±5.5	LSB
Quantization error	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±6.0	—	—	±6.0	LSB

7.4.5 D/A Conversion Characteristics

Table 7.37 D/A Conversion Characteristics — Preliminary —

Condition A (In planning):

V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications),
T_a = –40°C to 85°C (wide-range specifications)

Condition B (Under development):

V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications),
T_a = –40°C to 85°C (wide-range specifications)

	Condition A			Condition B				Test
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
Resolution	8	8	8	8	8	8	Bits	
Conversion time	—	—	10	—	—	10	µs	20 pF capacitive load
Absolute accuracy	—	±2.0	±3.0	—	±2.0	±3.0	LSB	2 MΩ resistive load
	—	—	±2.0	—	—	±2.0	LSB	4 MΩ resistive load

7.4.6 Flash Memory Characteristics

Table 7.38 (a) Flash Memory Characteristics — Preliminary —

Condition A*[7] (In planning):

V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, (program/erase power-supply voltage range: V_{CC} = 3.0 V to 3.6 V), T_a = 0°C to +75°C (program/erase operating temperature range: regular specifications), T_a = 0°C to +85°C (program/erase operating temperature range: wide-range specifications)

Item		Symbol		Min	Typ	Max	Unit	Test Conditions
Programming time*[1, 2, 4]		t_P		—	TBD	200	ms/ 128 bytes	
Erase time*[1, 3, 6]		t_E		—	TBD	1000	ms/block	
Rewrite times		NWEC		—	—	TBD	Times	
Programming	Wait time after SWE bit setting*[1]	x		1	—	—	µs	
	Wait time after PSU bit setting*[1]	y		50	—	—	µs	
	Wait time after P bit setting*[1, 4]	z	(z1)	—	—	30	µs	1 ≤ n ≤ 6
			(z2)	—	—	200	µs	7 ≤ n ≤ 1000
			(z3)	—	—	10	µs	Additional-programming time wait
	Wait time after P bit clearing*[1]	α		5	—	—	µs	
	Wait time after PSU bit clearing*[1]	β		5	—	—	µs	
	Wait time after PV bit setting*[1]	γ		4	—	—	µs	
	Wait time after H'FF dummy write*[1]	ε		2	—	—	µs	
	Wait time after PV bit clearing*[1]	η		2	—	—	µs	
	Wait time after SWE bit clearing*[1]	θ		100	—	—	µs	
	Maximum number of writes*[1, 4]	N		—	—	1000*[5]	Times	
Erasing	Wait time after SWE bit setting*[1]	x		1	—	—	µs	
	Wait time after ESU bit setting*[1]	y		100	—	—	µs	
	Wait time after E bit setting*[1, 6]	z		—	—	10	µs	
	Wait time after E bit clearing*[1]	α		10	—	—	µs	
	Wait time after ESU bit clearing*[1]	β		10	—	—	µs	
	Wait time after EV bit setting*[1]	γ		20	—	—	µs	
	Wait time after H'FF dummy write*[1]	ε		2	—	—	µs	
	Wait time after EV bit clearing*[1]	η		4	—	—	µs	
	Wait time after SWE bit clearing*[1]	θ		100	—	—	µs	
	Maximum number of erases*[1, 6]	N		—	—	100	Times	

Notes:
1. Follow the program/erase algorithms when making the time settings.
2. Programming time per 128 bytes. (Indicates the total time during which the P bit is set in flash memory control register 1 (FLMCR1). Does not include the program-verify time.)
3. Time to erase one block. (Indicates the time during which the E bit is set in FLMCR1. Does not include the erase-verify time.)
4. Maximum programming time

   $t_P(\max) = \sum_{i=1}^{N}$ wait time after P bit setting (z)
5. The maximum number of writes (N) should be set as shown below according to the actual set value of z so as not to exceed the maximum programming time ($t_P(\max)$).

   The wait time after P bit setting (z) should be changed as follows according to the number of writes (n).

   Number of writes (n)

   $1 \leq n \leq 6$ z = 30 µs

   $7 \leq n \leq 1000$ z = 200 µs

   [In additional programming]

   Number of writes (n)

   $1 \leq n \leq 6$ z = 10 µs
6. For the maximum erase time ($t_E(\max)$), the following relationship applies between the wait time after E bit setting (z) and the maximum number of erases (N):

   $t_E(\max)$ = Wait time after E bit setting (z) $\times$ maximum number of erases (N)
7. The power-supply voltage range for flash memory programming/erasing is V_{CC} = 3.0 V to 3.6 V.

Condition B (Under development):

V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = 0°C to +75°C (program/erase operating temperature range: regular specifications), T_a = 0°C to +85°C (program/erase operating temperature range: wide-range specifications)

Item		Symbol		Min	Typ	Max	Unit	Test Conditions
Programming time*1, *2, *4		t_P		—	TBD	200	ms/ 128 bytes	
Erase time*1, *3, *6		t_E		—	TBD	1000	ms/block	
Rewrite times		NWEC		—	—	TBD	Times	
Programming	Wait time after SWE bit setting*1	x		1	—	—	µs	
	Wait time after PSU bit setting*1	y		50	—	—	µs	
	Wait time after P bit setting*1, *4	z	(z1)	—	—	30	µs	1 ≤ n ≤ 6
			(z2)	—	—	200	µs	7 ≤ n ≤ 1000
			(z3)	—	—	10	µs	Additional-programming time wait
	Wait time after P bit clearing*1	α		5	—	—	µs	
	Wait time after PSU bit clearing*1	β		5	—	—	µs	
	Wait time after PV bit setting*1	γ		4	—	—	µs	
	Wait time after H'FF dummy write*1	ε		2	—	—	µs	
	Wait time after PV bit clearing*1	η		2	—	—	µs	
	Wait time after SWE bit clearing*1	θ		100	—	—	µs	
	Maximum number of writes*1, *4	N		—	—	1000*5	Times	
Erasing	Wait time after SWE bit setting*1	x		1	—	—	µs	
	Wait time after ESU bit setting*1	y		100	—	—	µs	
	Wait time after E bit setting*1, *6	z		—	—	10	µs	
	Wait time after E bit clearing*1	α		10	—	—	µs	
	Wait time after ESU bit clearing*1	β		10	—	—	µs	
	Wait time after EV bit setting*1	γ		20	—	—	µs	
	Wait time after H'FF dummy write*1	ε		2	—	—	µs	
	Wait time after EV bit clearing*1	η		4	—	—	µs	
	Wait time after SWE bit clearing*1	θ		100	—	—	µs	
	Maximum number of erases*1, *6	N		—	—	100	Times	

Notes: 1. Follow the program/erase algorithms when making the time settings.

2. Programming time per 128 bytes. (Indicates the total time during which the P bit is set in flash memory control register 1 (FLMCR1). Does not include the program-verify time.)

3. Time to erase one block. (Indicates the time during which the E bit is set in FLMCR1. Does not include the erase-verify time.)
4. Maximum programming time

   $t_P(max) = \sum_{i=1}^{N}$ wait time after P bit setting (z)

5. The maximum number of writes (N) should be set as shown below according to the actual set value of z so as not to exceed the maximum programming time ($t_P(max)$).

   The wait time after P bit setting (z) should be changed as follows according to the number of writes (n).

   Number of writes (n)

   $1 \leq n \leq 6$ z = 30 µs

   $7 \leq n \leq 1000$ z = 200 µs

   [In additional programming]

   Number of writes (n)

   $1 \leq n \leq 6$ z = 10 µs

6. For the maximum erase time ($t_E(max)$), the following relationship applies between the wait time after E bit setting (z) and the maximum number of erases (N):

   $t_E(max)$ = Wait time after E bit setting (z) $\times$ maximum number of erases (N)

7. The power-supply voltage range for flash memory programming/erasing is V_{CC} = 3.0 V to 3.6 V.

7.5 Usage Note

Although both the F-ZTAT and mask ROM versions fully meet the electrical specifications listed in this manual, there may be differences in the actual values of the electrical characteristics, operating margins, noise margins, and so forth, due to differences in the fabrication process, the on-chip ROM, and the layout patterns.

If the F-ZTAT version is used to carry out system evaluation and testing, therefore, when switching to the mask ROM version the same evaluation and testing procedures should also be conducted on this version.

8.1 List of Registers (Address Order)

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'F800	MRA	SM1	SM0	DM1	DM0	MD1	MD0	DTS	Sz	DTC	16/32*[1] bits
to	SAR										
H'FBFF											
	MRB	CHNE	DISEL	CHNS	—	—	—	—	—		
	DAR										
	CRA										
	CRB										
H'FE80	TCR3	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU3	16 bits
H'FE81	TMDR3	—	—	BFB	BFA	MD3	MD2	MD1	MD0		
H'FE82	TIOR3H	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FE83	TIOR3L	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0		
H'FE84	TIER3	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA		
H'FE85	TSR3	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA		
H'FE86	TCNT3										
H'FE87											
H'FE88	TGR3A										
H'FE89											
H'FE8A	TGR3B										
H'FE8B											
H'FE8C	TGR3C										
H'FE8D											
H'FE8E	TGR3D										
H'FE8F											

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FE90	TCR4	—	CCLR1	CCLR0	CKEG	CKEG0	TPSC2	TPSC1	TPSC0	TPU4	16 bits
H'FE91	TMDR4	—	—	—	—	MD3	MD2	MD1	MD0		
H'FE92	TIOR4	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FE94	TIER4	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FE95	TSR4	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FE96	TCNT4										
H'FE97											
H'FE98	TGR4A										
H'FE99											
H'FE9A	TGR4B										
H'FE9B											
H'FEA0	TCR5	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU5	16 bits
H'FEA1	TMDR5	—	—	—	—	MD3	MD2	MD1	MD0		
H'FEA2	TIOR5	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FEA4	TIER5	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FEA5	TSR5	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FEA6	TCNT5										
H'FEA7											
H'FEA8	TGR5A										
H'FEA9											
H'FEAA	TGR5B										
H'FEAB											
H'FEB0	P1DDR	P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR	Ports	8 bits
H'FEB1	P2DDR	P27DDR	P26DDR	P25DDR	P24DDR	P23DDR	P22DDR	P21DDR	P20DDR		
H'FEB2	P3DDR	—	—	P35DDR	P34DDR	P33DDR	P32DDR	P31DDR	P30DDR		
H'FEB9	PADDR	—	—	—	—	PA3DDR	PA2DDR	PA1DDR	PA0DDR		
H'FEBA	PBDDR	PB7DDR	PB6DDR	PB5DDR	PB4DDR	PB3DDR	PB2DDR	PB1DDR	PB0DDR		
H'FEBB	PCDDR	PC7DDR	PC6DDR	PC5DDR	PC4DDR	PC3DDR	PC2DDR	PC1DDR	PC0DDR		
H'FEBC	PDDDR	PD7DDR	PD6DDR	PD5DDR	PD4DDR	PD3DDR	PD2DDR	PD1DDR	PD0DDR		
H'FEBD	PEDDR	PE7DDR	PE6DDR	PE5DDR	PE4DDR	PE3DDR	PE2DDR	PE1DDR	PE0DDR		
H'FEBE	PFDDR	PF7DDR	PF6DDR	PF5DDR	PF4DDR	PF3DDR	PF2DDR	PF1DDR	PF0DDR		
H'FEBF	PGDDR	—	—	—	PG4DDR	PG3DDR	PG2DDR	PG1DDR	PG0DDR		

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FEC4	IPRA	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	Interrupt controller	8 bits
H'FEC5	IPRB	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FEC6	IPRC	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FEC7	IPRD	—	IPR6	IPR5	IPR4	—	—	—	—		
H'FEC8	IPRE	—	—	—	—	—	IPR2	IPR1	IPR0		
H'FEC9	IPRF	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECA	IPRG	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECB	IPRH	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECC	IPRI	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECD	IPRJ	—	—	—	—	—	IPR2	IPR1	IPR0		
H'FECE	IPRK	—	IPR6	IPR5	IPR4	—	—	—	—		
H'FED0	ABWCR	ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0	Bus controller	8 bits
H'FED1	ASTCR	AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0		
H'FED2	WCRH	W71	W70	W61	W60	W51	W50	W41	W40		
H'FED3	WCRL	W31	W30	W21	W20	W11	W10	W01	W00		
H'FED4	BCRH	ICIS1	ICIS0	BRSTRM	BRSTS1	BRSTS0	—	—	—		
H'FED5	BCRL	BRLE	BREQOE	EAE	—	—	—	—	WAITE		
H'FEDB	RAMER*[2]	—	—	—	—	RAMS	RAM2	RAM1	RAM0	Flash memory	8 bits
H'FF2C	ISCRH	IRQ7SCB	IRQ7SCA	IRQ6SCB	IRQ6SCA	IRQ5SCB	IRQ5SCA	IRQ4SCB	IRQ4SCA	Interrupt controller	8 bits
H'FF2D	ISCRL	IRQ3SCB	IRQ3SCA	IRQ2SCB	IRQ2SCA	IRQ1SCB	IRQ1SCA	IRQ0SCB	IRQ0SCA		
H'FF2E	IER	IRQ7E	IRQ6E	IRQ5E	IRQ4E	IRQ3E	IRQ2E	IRQ1E	IRQ0E		
H'FF2F	ISR	IRQ7F	IRQ6F	IRQ5F	IRQ4F	IRQ3F	IRQ2F	IRQ1F	IRQ0F		
H'FF30 to H'FF34	DTCER	DTCE7	DTCE6	DTCE5	DTCE4	DTCE3	DTCE2	DTCE1	DTCE0	DTC	8 bits
H'FF37	DTVECR	SWDTE	DTVEC6	DTVEC5	DTVEC4	DTVEC3	DTVEC2	DTVEC1	DTVEC0		
H'FF38	SBYCR	SSBY	STS2	STS1	STS0	OPE	—	—	IRQ37S	Power-down mode	8 bits
H'FF39	SYSCR	—	—	INTM1	INTM0	NMIEG	LWROD	—	RAME	MCU	8 bits
H'FF3A	SCKCR	PSTOP	—	DIV	—	—	SCK2	SCK1	SCK0	Clock pulse generator	8 bits
H'FF3B	MDCR	—	—	—	—	—	MDS2	MDS1	MDS0	MCU	8 bits
H'FF3C	MSTPCRH	MSTP15	MSTP14	MSTP13	MSTP12	MSTP11	MSTP10	MSTP9	MSTP8	Power-down mode	8 bits
H'FF3D	MSTPCRL	MSTP7	MSTP6	MSTP5	MSTP4	MSTP3	MSTP2	MSTP1	MSTP0		

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FF42	SYSCR2*2	—	—	—	—	FLSHE	—	—	—	Flash memory	8 bits
H'FF44	Reserved	—	—	—	—	—	—	—	—	Reserved	—
H'FF45	PFCR1	CSS17	CSS36	PF1CS5S	PF0CS4S	A23E	A22E	A21E	A20E	Ports	8 bits
H'FF50	PORT1	P17	P16	P15	P14	P13	P12	P11	P10		
H'FF51	PORT2	P27	P26	P25	P24	P23	P22	P21	P20		
H'FF52	PORT3	—	—	P35	P34	P33	P32	P31	P30		
H'FF53	PORT4	P47	P46	P45	P44	P43	P42	P41	P40		
H'FF59	PORTA	—	—	—	—	PA3	PA2	PA1	PA0		
H'FF5A	PORTB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0		
H'FF5B	PORTC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0		
H'FF5C	PORTD	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0		
H'FF5D	PORTE	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0		
H'FF5E	PORTF	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0		
H'FF5F	PORTG	—	—	—	PG4	PG3	PG2	PG1	PG0		
H'FF60	P1DR	P17DR	P16DR	P15DR	P14DR	P13DR	P12DR	P11DR	P10DR		
H'FF61	P2DR	P27DR	P26DR	P25DR	P24DR	P23DR	P22DR	P21DR	P20DR		
H'FF62	P3DR	—	—	P35DR	P34DR	P33DR	P32DR	P31DR	P30DR		
H'FF69	PADR	—	—	—	—	PA3DR	PA2DR	PA1DR	PA0DR		
H'FF6A	PBDR	PB7DR	PB6DR	PB5DR	PB4DR	PB3DR	PB2DR	PB1DR	PB0DR		
H'FF6B	PCDR	PC7DR	PC6DR	PC5DR	PC4DR	PC3DR	PC2DR	PC1DR	PC0DR		
H'FF6C	PDDR	PD7DR	PD6DR	PD5DR	PD4DR	PD3DR	PD2DR	PD1DR	PD0DR		
H'FF6D	PEDR	PE7DR	PE6DR	PE5DR	PE4DR	PE3DR	PE2DR	PE1DR	PE0DR		
H'FF6E	PFDR	PF7DR	PF6DR	PF5DR	PF4DR	PF3DR	PF2DR	PF1DR	PF0DR		
H'FF6F	PGDR	—	—	—	PG4DR	PG3DR	PG2DR	PG1DR	PG0DR		
H'FF70	PAPCR	—	—	—	—	PA3PCR	PA2PCR	PA1PCR	PA0PCR		
H'FF71	PBPCR	PB7PCR	PB6PCR	PB5PCR	PB4PCR	PB3PCR	PB2PCR	PB1PCR	PB0PCR		
H'FF72	PCPCR	PC7PCR	PC6PCR	PC5PCR	PC4PCR	PC3PCR	PC2PCR	PC1PCR	PC0PCR		
H'FF73	PDPCR	PD7PCR	PD6PCR	PD5PCR	PD4PCR	PD3PCR	PD2PCR	PD1PCR	PD0PCR		
H'FF74	PEPCR	PE7PCR	PE6PCR	PE5PCR	PE4PCR	PE3PCR	PE2PCR	PE1PCR	PE0PCR		
H'FF76	P3ODR	—	—	P35ODR	P34ODR	P33ODR	P32ODR	P31ODR	P30ODR		
H'FF77	PAODR	—	—	—	—	PA3ODR	PA2ODR	PA1ODR	PA0ODR		

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FF78	SMR0	C/$\overline{A}$/ GM*[3]	CHR/ BLK*[4]	PE	O/$\overline{E}$	STOP/ BCP1*[5]	MP/ BCP0*[6]	CKS1	CKS0	SCI0, smart card interface 0	8 bits
H'FF79	BRR0										
H'FF7A	SCR0	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FF7B	TDR0										
H'FF7C	SSR0	TDRE	RDRF	ORER	FER/ ERS*[7]	PER	TEND	MPB	MPBT		
H'FF7D	RDR0										
H'FF7E	SCMR0	—	—	—	—	SDIR	SINV	—	SMIF		
H'FF80	SMR1	C/$\overline{A}$/ GM*[3]	CHR/ BLK*[4]	PE	O/$\overline{E}$	STOP/ BCP1*[5]	MP/ BCP0*[6]	CKS1	CKS0	SCI1, smart card interface 1	8 bits
H'FF81	BRR1										
H'FF82	SCR1	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FF83	TDR1										
H'FF84	SSR1	TDRE	RDRF	ORER	FER/ ERS*[7]	PER	TEND	MPB	MPBT		
H'FF85	RDR1										
H'FF86	SCMR1	—	—	—	—	SDIR	SINV	—	SMIF		

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FE90	ADDRAH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D converter	8 bits
H'FE91	ADDRAL	AD1	AD0	—	—	—	—	—	—		
H'FE92	ADDRBH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FE93	ADDRBL	AD1	AD0	—	—	—	—	—	—		
H'FE94	ADDRCH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FE95	ADDRCL	AD1	AD0	—	—	—	—	—	—		
H'FE96	ADDRDH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FE97	ADDRDL	AD1	AD0	—	—	—	—	—	—		
H'FE98	ADCSR	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0		
H'FE99	ADCR	TRGS1	TRGS0	—	—	CKS1	—	—	—		
H'FFA4	DADR0									D/A converter	8 bits
H'FFA5	DADR1										
H'FFA6	DACR01	DAOE1	DAOE0	DAE	—	—	—	—	—		
H'FFAC	PFCR2	—	—	CS167E	CS25E	ASOD	—	—	—	Ports	8 bits
H'FFB0	TCR0	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	8-bit timer channel 0, 1	16 bits
H'FFB1	TCR1	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0		
H'FFB2	TCSR0	CMFB	CMFA	OVF	ADTE	OS3	OS2	OS1	OS0		
H'FFB3	TCSR1	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0		
H'FFB4	TCORA0										
H'FFB5	TCORA1										
H'FFB6	TCORB0										
H'FFB7	TCORB1										
H'FFB8	TCNT0										
H'FFB9	TCNT1										
H'FFBC (Read)	TCSR	OVF	WT/$\overline{\text{IT}}$	TME	—	—	CKS2	CKS1	CKS0	WDT	16 bits
H'FFBD (Read)	TCNT										
H'FFBF (Read)	RSTCSR	WOVF	RSTE	—	—	—	—	—	—		

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FFC0	TSTR	—	—	CST5	CST4	CST3	CST2	CST1	CST0	TPU	16 bits
H'FFC1	TSYR	—	—	SYNC5	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0		
H'FFC8	FLMCR1 *8	FWE	SWE	ESU	PSU	EV	PV	E	P	Flash memory	8 bits
H'FFC8	FLMCR1 *9	FWE	SWE1	ESU1	PSU1	EV1	PV1	E1	P1		
H'FFC9	FLMCR2 *8	FLER	—	—	—	—	—	—	—		
H'FFC9	FLMCR2 *9	FLER	SWE2	ESU2	PSU2	EV2	PV2	E2	P2		
H'FFCA	EBR1*2	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0		
H'FFCB	EBR2*2	EB15*9	EB14*9	EB13*8	EB12*8	EB11	EB10	EB9	EB8		
H'FFD0	TCR0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU0	16 bits
H'FFD1	TMDR0	—	—	BFB	BFA	MD3	MD2	MD1	MD0		
H'FFD2	TIOR0H	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FFD3	TIOR0L	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0		
H'FFD4	TIER0	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA		
H'FFD5	TSR0	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA		
H'FFD6	TCNT0										
H'FFD7											
H'FFD8	TGR0A										
H'FFD9											
H'FFDA	TGR0B										
H'FFDB											
H'FFDC	TGR0C										
H'FFDD											
H'FFDE	TGR0D										
H'FFDF											

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FFE0	TCR1	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU1	16 bits
H'FFE1	TMDR1	—	—	—	—	MD3	MD2	MD1	MD0		
H'FFE2	TIOR1	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FFE4	TIER1	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FFE5	TSR1	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FFE6	TCNT1										
H'FFE7											
H'FFE8	TGR1A										
H'FFE9											
H'FFEA	TGR1B										
H'FFEB											
H'FFF0	TCR2	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU2	16 bits
H'FFF1	TMDR2	—	—	—	—	MD3	MD2	MD1	MD0		
H'FFF2	TIOR2	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FFF4	TIER2	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FFF5	TSR2	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FFF6	TCNT2										
H'FFF7											
H'FFF8	TGR2A										
H'FFF9											
H'FFFA	TGR2B										
H'FFFB											

Notes: 1. Located in on-chip RAM. The bus width is 32 bits when the DTC accesses this area as register information, and 16 bits otherwise.
2. Valid only in F-ZTAT version.
3. Functions as C/$\overline{A}$ for SCI use, and as GM for smart card interface use.
4. Functions as CHR for SCI use, and as BLK for smart card interface use.
5. Functions as STOP for SCI use, and as BCP1 for smart card interface use.
6. Functions as MP for SCI use, and as BCP0 for smart card interface use.
7. Functions as FER for SCI use, and as ERS for smart card interface use.
8. Valid in H8S/2319 F-ZTAT and H8S/2315 F-ZTAT versions.
9. Valid in H8S/2319 F-ZTAT version only.

8.2 List of Registers (By Module)

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
Interrupt controller	System control register	SYSCR	R/W	H'01	H'FF39
	IRQ sense control register H	ISCRH	R/W	H'00	H'FF2C
	IRQ sense control register L	ISCRL	R/W	H'00	H'FF2D
	IRQ enable register	IER	R/W	H'00	H'FF2E
	IRQ status register	ISR	R/(W)*[2]	H'00	H'FF2F
	Interrupt priority register A	IPRA	R/W	H'77	H'FEC4
	Interrupt priority register B	IPRB	R/W	H'77	H'FEC5
	Interrupt priority register C	IPRC	R/W	H'77	H'FEC6
	Interrupt priority register D	IPRD	R/W	H'77	H'FEC7
	Interrupt priority register E	IPRE	R/W	H'77	H'FEC8
	Interrupt priority register F	IPRF	R/W	H'77	H'FEC9
	Interrupt priority register G	IPRG	R/W	H'77	H'FECA
	Interrupt priority register H	IPRH	R/W	H'77	H'FECB
	Interrupt priority register I	IPRI	R/W	H'77	H'FECC
	Interrupt priority register J	IPRJ	R/W	H'77	H'FECD
	Interrupt priority register K	IPRK	R/W	H'77	H'FECE
DTC	DTC mode register A	MRA	—*[3]	Undefined	—*[4]
	DTC mode register B	MRB	—*[3]	Undefined	—*[4]
	DTC source address register	SAR	—*[3]	Undefined	—*[4]
	DTC destination address register	DAR	—*[3]	Undefined	—*[4]
	DTC transfer count register A	CRA	—*[3]	Undefined	—*[4]
	DTC transfer count register B	CRB	—*[3]	Undefined	—*[4]
	DTC enable register	DTCER	R/W	H'00	H'FF30 to H'FF34
	DTC vector register	DTVECR	R/W	H'00	H'FF37
	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
Bus controller	Bus width control register	ABWCR	R/W	H'FF/H'00*[5]	H'FED0
	Access state control register	ASTCR	R/W	H'FF	H'FED1
	Wait control register H	WCRH	R/W	H'FF	H'FED2
	Wait control register L	WCRL	R/W	H'FF	H'FED3
	Bus control register H	BCRH	R/W	H'D0	H'FED4
	Bus control register L	BCRL	R/W	H'3C	H'FED5
8-bit timer 0	Timer control register 0	TCR0	R/W	H'00	H'FFB0
	Timer control/status register 0	TCSR0	R/(W)*[7]	H'00	H'FFB2
	Timer constant register A0	TCORA0	R/W	H'FF	H'FFB4
	Timer constant register B0	TCORB0	R/W	H'FF	H'FFB6
	Timer counter 0	TCNT0	R/W	H'00	H'FFB8
8-bit timer 1	Timer control register 1	TCR1	R/W	H'00	H'FFB1
	Timer control/status register 1	TCSR1	R/(W)*[7]	H'10	H'FFB3
	Timer constant register A1	TCORA1	R/W	H'FF	H'FFB5
	Timer constant register B1	TCORB1	R/W	H'FF	H'FFB7
	Timer counter 1	TCNT1	R/W	H'00	H'FFB9
All 8-bit timer channels	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C
WDT	Timer control/status register	TCSR	R/(W)*[9]	H'18	H'FFBC: Write*[8] H'FFBC: Read
	Timer counter	TCNT	R/W	H'00	H'FFBC: Write*[6] H'FFBD: Read
	Reset control/status register	RSTCSR	R/(W)*[9]	H'1F	H'FFBE: Write*[8] H'FFBF: Read

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
SCI0	Serial mode register 0	SMR0	R/W	H'00	H'FF78
	Bit rate register 0	BRR0	R/W	H'FF	H'FF79
	Serial control register 0	SCR0	R/W	H'00	H'FF7A
	Transmit data register 0	TDR0	R/W	H'FF	H'FF7B
	Serial status register 0	SSR0	R/(W)*[2]	H'84	H'FF7C
	Receive data register 0	RDR0	R	H'00	H'FF7D
	Smart card mode register 0	SCMR0	R/W	H'F2	H'FF7E
SCI1	Serial mode register 1	SMR1	R/W	H'00	H'FF80
	Bit rate register 1	BRR1	R/W	H'FF	H'FF81
	Serial control register 1	SCR1	R/W	H'00	H'FF82
	Transmit data register 1	TDR1	R/W	H'FF	H'FF83
	Serial status register 1	SSR1	R/(W)*[2]	H'84	H'FF84
	Receive data register 1	RDR1	R	H'00	H'FF85
	Smart card mode register 1	SCMR1	R/W	H'F2	H'FF86
All SCI channels	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C
SMCI0	Serial mode register 0	SMR0	R/W	H'00	H'FF78
	Bit rate register 0	BRR0	R/W	H'FF	H'FF79
	Serial control register 0	SCR0	R/W	H'00	H'FF7A
	Transmit data register 0	TDR0	R/W	H'FF	H'FF7B
	Serial status register 0	SSR0	R/(W)*[2]	H'84	H'FF7C
	Receive data register 0	RDR0	R	H'00	H'FF7D
	Smart card mode register 0	SCMR0	R/W	H'F2	H'FF7E
SMCI1	Serial mode register 1	SMR1	R/W	H'00	H'FF80
	Bit rate register 1	BRR1	R/W	H'FF	H'FF81
	Serial control register 1	SCR1	R/W	H'00	H'FF82
	Transmit data register 1	TDR1	R/W	H'FF	H'FF83
	Serial status register 1	SSR1	R/(W)*[2]	H'84	H'FF84
	Receive data register 1	RDR1	R	H'00	H'FF85
	Smart card mode register 1	SCMR1	R/W	H'F2	H'FF86

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
All SMCI channels	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C
ADC	A/D data register AH	ADDRAH	R	H'00	H'FF90
	A/D data register AL	ADDRAL	R	H'00	H'FF91
	A/D data register BH	ADDRBH	R	H'00	H'FF92
	A/D data register BL	ADDRBL	R	H'00	H'FF93
	A/D data register CH	ADDRCH	R	H'00	H'FF94
	A/D data register CL	ADDRCL	R	H'00	H'FF95
	A/D data register DH	ADDRDH	R	H'00	H'FF96
	A/D data register DL	ADDRDL	R	H'00	H'FF97
	A/D control/status register	ADCSR	R/(W)*[9]	H'00	H'FF98
	A/D control register	ADCR	R/W	H'3F	H'FF99
	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C
DAC0, 1	D/A data register 0	DADR0	R/W	H'00	H'FFA4
	D/A data register 1	DADR1	R/W	H'00	H'FFA5
	D/A control register 01	DACR01	R/W	H'1F	H'FFA6
All DAC channels	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C
On-chip RAM	System control register	SYSCR	R/W	H'01	H'FF39
TPU0	Timer control register 0	TCR0	R/W	H'00	H'FFD0
	Timer mode register 0	TMDR0	R/W	H'C0	H'FFD1
	Timer I/O control register 0H	TIOR0H	R/W	H'00	H'FFD2
	Timer I/O control register 0L	TIOR0L	R/W	H'00	H'FFD3
	Timer interrupt enable register 0	TIER0	R/W	H'40	H'FFD4
	Timer status register 0	TSR0	R/(W)*[2]	H'C0	H'FFD5
	Timer counter 0	TCNT0	R/W	H'0000	H'FFD6
	Timer general register 0A	TGR0A	R/W	H'FFFF	H'FFD8
	Timer general register 0B	TGR0B	R/W	H'FFFF	H'FFDA
	Timer general register 0C	TGR0C	R/W	H'FFFF	H'FFDC
	Timer general register 0D	TGR0D	R/W	H'FFFF	H'FFDE
TPU1	Timer control register 1	TCR1	R/W	H'00	H'FFE0
	Timer mode register 1	TMDR1	R/W	H'C0	H'FFE1

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
TPU1	Timer I/O control register 1	TIOR1	R/W	H'00	H'FFE2
	Timer interrupt enable register 1	TIER1	R/W	H'40	H'FFE4
	Timer status register 1	TSR1	R/(W) *[2]	H'C0	H'FFE5
	Timer counter 1	TCNT1	R/W	H'0000	H'FFE6
	Timer general register 1A	TGR1A	R/W	H'FFFF	H'FFE8
	Timer general register 1B	TGR1B	R/W	H'FFFF	H'FFEA
TPU2	Timer control register 2	TCR2	R/W	H'00	H'FFF0
	Timer mode register 2	TMDR2	R/W	H'C0	H'FFF1
	Timer I/O control register 2	TIOR2	R/W	H'00	H'FFF2
	Timer interrupt enable register 2	TIER2	R/W	H'40	H'FFF4
	Timer status register 2	TSR2	R/(W) *[2]	H'C0	H'FFF5
	Timer counter 2	TCNT2	R/W	H'0000	H'FFF6
	Timer general register 2A	TGR2A	R/W	H'FFFF	H'FFF8
	Timer general register 2B	TGR2B	R/W	H'FFFF	H'FFFA
TPU3	Timer control register 3	TCR3	R/W	H'00	H'FE80
	Timer mode register 3	TMDR3	R/W	H'C0	H'FE81
	Timer I/O control register 3H	TIOR3H	R/W	H'00	H'FE82
	Timer I/O control register 3L	TIOR3L	R/W	H'00	H'FE83
	Timer interrupt enable register 3	TIER3	R/W	H'40	H'FE84
	Timer status register 3	TSR3	R/(W)*[2]	H'C0	H'FE85
	Timer counter 3	TCNT3	R/W	H'0000	H'FE86
	Timer general register 3A	TGR3A	R/W	H'FFFF	H'FE88
	Timer general register 3B	TGR3B	R/W	H'FFFF	H'FE8A
	Timer general register 3C	TGR3C	R/W	H'FFFF	H'FE8C
	Timer general register 3D	TGR3D	R/W	H'FFFF	H'FE8E
TPU4	Timer control register 4	TCR4	R/W	H'00	H'FE90
	Timer mode register 4	TMDR4	R/W	H'C0	H'FE91
	Timer I/O control register 4	TIOR4	R/W	H'00	H'FE92
	Timer interrupt enable register 4	TIER4	R/W	H'40	H'FE94
	Timer status register 4	TSR4	R/(W) *[2]	H'C0	H'FE95
	Timer counter 4	TCNT4	R/W	H'0000	H'FE96
	Timer general register 4A	TGR4A	R/W	H'FFFF	H'FE98
	Timer general register 4B	TGR4B	R/W	H'FFFF	H'FE9A

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
TPU5	Timer control register 5	TCR5	R/W	H'00	H'FEA0
	Timer mode register 5	TMDR5	R/W	H'C0	H'FEA1
	Timer I/O control register 5	TIOR5	R/W	H'00	H'FEA2
	Timer interrupt enable register 5	TIER5	R/W	H'40	H'FEA4
	Timer status register 5	TSR5	R/(W) *[2]	H'C0	H'FEA5
	Timer counter 5	TCNT5	R/W	H'0000	H'FEA6
	Timer general register 5A	TGR5A	R/W	H'FFFF	H'FEA8
	Timer general register 5B	TGR5B	R/W	H'FFFF	H'FEAA
All TPU channels	Timer start register	TSTR	R/W	H'00	H'FFC0
	Timer synchro register	TSYR	R/W	H'00	H'FFC1
	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C
Flash memory	Flash memory control register 1	FLMCR1*[14]	R/W*[11]	H'00/H'80*[12]	H'FFC8*[10]
	Flash memory control register 2	FLMCR2*[14]	R/W*[11]	H'00	H'FFC9*[10]
	Erase block register 1	EBR1*[14]	R/W*[11]	H'00*[13]	H'FFCA*[10]
	Erase block register 2	EBR2*[14]	R/W*[11]	H'00*[13]	H'FFCB*[10]
	RAM emulation register	RAMER	R/W	H'00	H'FEDB
	System control register 2	SYSCR2*[15]	R/W	H'00	H'FF42
Clock pulse generator	System clock control register	SCKCR	R/W	H'00	H'FF3A
MCU	System control register	SYSCR	R/W	H'01	H'FF39
	Mode control register	MDCR	R	Undefined	H'FF3B
Power-down state	Standby control register	SBYCR	R/W	H'08	H'FF38
	Module stop control register H	MSTPCRH	R/W	H'3F	H'FF3C
	Module stop control register L	MSTPCRL	R/W	H'FF	H'FF3D
Port 1	Port 1 data direction register	P1DDR	W	H'00	H'FEB0
	Port 1 data register	P1DR	R/W	H'00	H'FF60
	Port 1 register	PORT1	R	Undefined	H'FF50
	Port function control register 1	PFCR1	R/W	H'0F	H'FF45
Port 2	Port 2 data direction register	P2DDR	W	H'00	H'FEB1
	Port 2 data register	P2DR	R/W	H'00	H'FF61
	Port 2 register	PORT2	R	Undefined	H'FF51

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
Port 3	Port 3 data direction register	P3DDR	W	H'00	H'FEB2
	Port 3 data register	P3DR	R/W	H'00	H'FF62
	Port 3 register	PORT3	R	Undefined	H'FF52
	Port 3 open drain control register	P3ODR	R/W	H'00	H'FF76
Port 4	Port 4 register	PORT4	R	Undefined	H'FF53
Port A	Port A data direction register	PADDR	W	H'0*[16]	H'FEB9
	Port A data register	PADR	R/W	H'0*[16]	H'FF69
	Port A register	PORTA	R	Undefined*[16]	H'FF59
	Port A MOS pull-up control register	PAPCR	R/W	H'0*[16]	H'FF70
	Port A open drain control register	PAODR	R/W	H'0*[16]	H'FF77
Port B	Port B data direction register	PBDDR	W	H'00	H'FEBA
	Port B data register	PBDR	R/W	H'00	H'FF6A
	Port B register	PORTB	R	Undefined	H'FF5A
	Port B MOS pull-up control register	PBPCR	R/W	H'00	H'FF71
Port C	Port C data direction register	PCDDR	W	H'00	H'FEBB
	Port C data register	PCDR	R/W	H'00	H'FF6B
	Port C register	PORTC	R	Undefined	H'FF5B
	Port C MOS pull-up control register	PCPCR	R/W	H'00	H'FF72
Port D	Port D data direction register	PDDDR	W	H'00	H'FEBC
	Port D data register	PDDR	R/W	H'00	H'FF6C
	Port D register	PORTD	R	Undefined	H'FF5C
	Port D MOS pull-up control register	PDPCR	R/W	H'00	H'FF73
Port E	Port E data direction register	PEDDR	W	H'00	H'FEBD
	Port E data register	PEDR	R/W	H'00	H'FF6D
	Port E register	PORTE	R	Undefined	H'FF5D
	Port E MOS pull-up control register	PEPCR	R/W	H'00	H'FF74
Port F	Port F data direction register	PFDDR	W	H'80/H'00*[17]	H'FEBE
	Port F data register	PFDR	R/W	H'00	H'FF6E
	Port F register	PORTF	R	Undefined	H'FF5E
	Port function control register 1	PFCR1	R/W	H'0F	H'FF45
	Port function control register 2	PFCR2	R/W	H'30	H'FFAC
	System control register	SYSCR	R/W	H'01	H'FF39

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
Port G	Port G data direction register	PGDDR	W	H'10/H'00 *[17] *[18]	H'FEBF
	Port G data register	PGDR	R/W	H'00*[18]	H'FF6F
	Port G register	PORTG	R	Undefined*[18]	H'FF5F
	Port function control register 1	PFCR1	R/W	H'0F	H'FF45
	Port function control register 2	PFCR2	R/W	H'30	H'FFAC

Notes:
1. Lower 16 bits of the address.
2. Only 0 can be written for flag clearing.
3. Registers in the DTC cannot be read or written to directly.
4. Located as register information in on-chip RAM addresses H'EBC0 to H'EFBF. Cannot be located in external memory space. Do not clear the RAME bit in SYSCR to 0 when using the DTC.
5. Determined by the MCU operating mode.
6. Bits used for pulse output cannot be written to.
7. Only 0 can be written to bits 7 to 5, to clear the flags.
8. For information on writing, see section 10.2.4, Notes on Register Access, in the Hardware Manual.
9. Only 0 can be written to bit 7, to clear the flag.
10. Flash memory registers selection is performed by means of the FLSHE bit in system control register 2 (SYSCR2).
11. In modes in which the on-chip flash memory is disabled, a read will return H'00, and writes are invalid. Writes are also disabled when the FWE bit in FLMCR1 is cleared to 0. (Except for H8S/2319 F-ZTAT)
12. In H8S/2318 F-ZTAT and H8S/2315 F-ZTAT, when a high level is input to the FWE pin, the initial value is H'80. In H8S/2319 F-ZTAT, the initial value is H'80.
13. In H8S/2318 F-ZTAT and H8S/2315 F-ZTAT, when a low level is input to the FWE pin, or if a high level is input but the SWE bit in FLMCR1 is not set, these registers are initialized to H'00.

    In the H8S/2319 F-ZTAT, the EB11 to EB0 bits are initialized to 0 when the SWE1 bit is not set to 1, and the EB15 to EB12 bits are initialized to 0 when the SWE2 bit is not set to 1.
14. FLMCR1, FLMCR2, EBR1, and EBR2 are 8-bit registers. Only byte access can be used on these registers, with the access requiring two states.
15. The SYSCR2 register can only be used in the F-ZTAT version. In the mask ROM version this register will return an undefined value if read, and cannot be written to.
16. Value of bits 3 to 0.
17. The initial value depends on the mode.
18. Value of bits 4 to 0.

8.3 Functions

MRA—DTC Mode Register A **H'F800—H'FBFF** **DTC**

Bit	7	6	5	4	3	2	1	0
	SM1	SM0	DM1	DM0	MD1	MD0	DTS	Sz
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	—	—	—	—	—	—	—	—

DTC Data Transfer Size

0	Byte-size transfer
1	Word-size transfer

DTC Transfer Mode Select

0	Destination side is repeat area or block area
1	Source side is repeat area or block area

DTC Mode

0	0	Normal mode
	1	Repeat mode
1	0	Block transfer mode
	1	—

Destination Address Mode

0	—	DAR is fixed
1	0	DAR is incremented after a transfer (by +1 when Sz = 0; by +2 when Sz = 1)
	1	DAR is decremented after a transfer (by –1 when Sz = 0; by –2 when Sz = 1)

Source Address Mode

0	—	SAR is fixed
1	0	SAR is incremented after a transfer (by +1 when Sz = 0; by +2 when Sz = 1)
	1	SAR is decremented after a transfer (by –1 when Sz = 0; by –2 when Sz = 1)

Bit	7	6	5	4	3	2	1	0
	CHNE	DISEL	CHNS	—	—	—	—	—
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	—	—	—	—	—	—	—	—

Reserved
Only 0 should be written to these bits

DTC Interrupt Select

0	After DTC data transfer ends, the CPU interrupt is disabled unless the transfer counter is 0
1	After DTC data transfer ends, the CPU interrupt is enabled

DTC Chain Transfer Enable

DTC Chain Transfer Select

CHNE	CHNS	Description
0	—	No chain transfer. (At end of DTC data transfer, DTC waits for activation)
1	0	Chain transfer every time
1	1	Chain transfer only when transfer counter = 0

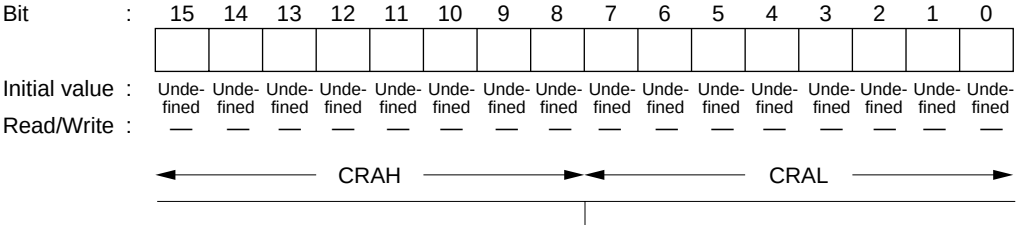
SAR—DTC Source Address Register **H'F800—H'FBFF** **DTC**

Bit	23	22	21	20	19	- - -	4	3	2	1	0
						- - -					
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	- - -	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	—	—	—	—	—	- - -	—	—	—	—	—

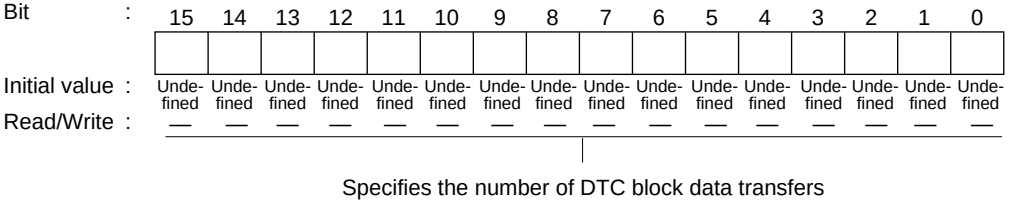
Specifies DTC transfer data source address

DAR—DTC Destination Address Register **H'F800—H'FBFF** **DTC**

CRA—DTC Transfer Count Register A **H'F800—H'FBFF** **DTC**



CRB—DTC Transfer Count Register B **H'F800—H'FBFF** **DTC**



Bit :	7	6	5	4	3	2	1	0
	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Timer Prescaler

0	0	0	Internal clock: counts on ø/1
		1	Internal clock: counts on ø/4
	1	0	Internal clock: counts on ø/16
		1	Internal clock: counts on ø/64
1	0	0	External clock: counts on TCLKA pin input
		1	Internal clock: counts on ø/1024
	1	0	Internal clock: counts on ø/256
		1	Internal clock: counts on ø/4096

Clock Edge

0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Note: The internal clock edge selection is valid when the input clock is ø/4 or slower. This setting is ignored if ø/1 or overflow/underflow on another channel is selected as the input clock.

Counter Clear

0	0	0	TCNT clearing disabled
		1	TCNT cleared by TGRA compare match/input capture
	1	0	TCNT cleared by TGRB compare match/input capture
		1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation *1
1	0	0	TCNT clearing disabled
		1	TCNT cleared by TGRC compare match/input capture *2
	1	0	TCNT cleared by TGRD compare match/input capture *2
		1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation *1

Notes: 1. Synchronous operation setting is performed by setting the SYNC bit in TSYR to 1.
2. When TGRC or TGRD is used as a buffer register, TCNT is not cleared because the buffer register setting has priority, and compare match/input capture does not occur.

Bit	:	7	6	5	4	3	2	1	0
		—	—	BFB	BFA	MD3	MD2	MD1	MD0
Initial value	:	1	1	0	0	0	0	0	0
Read/Write	:	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

* : Don't care

Notes: 1. MD3 is a reserved bit. In a write, it should always be written with 0.
2. Phase counting mode cannot be set for channels 0 and 3. In this case, 0 should always be written to MD2.

Buffer Operation A

0	TGRA operates normally
1	TGRA and TGRC used together for buffer operation

Buffer Operation B

0	TGRB operates normally
1	TGRB and TGRD used together for buffer operation

Bit :	7	6	5	4	3	2	1	0
Initial value :	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR3A I/O Control

0	0	0	0	TGR3A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR3A is input capture register	Capture input source is TIOCA3 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 4/count clock	Input capture at TCNT4 count-up/ count-down

* : Don't care

TGR3B I/O Control

0	0	0	0	TGR3B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR3B is input capture register	Capture input source is TIOCB3 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 4/count clock	Input capture at TCNT4 count-up/ count-down*1

* : Don't care

Note: 1. When bits TPSC2 to TPSC0 in TCR4 are set to B'000, and ø/1 is used as the TCNT4 count clock, this setting is invalid and input capture does not occur.

Bit	7	6	5	4	3	2	1	0
	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR3C I/O Control

0	0	0	0	TGR3C is output compare register*1	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR3C is input capture register*1	Capture input source is TIOCC3 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 4/count clock	Input capture at TCNT4 count-up/ count-down

* : Don't care

Note: 1. When the BFA bit in TMDR3 is set to 1 and TGR3C is used as a buffer register, this setting is invalid and input capture/output compare does not occur.

TGR3D I/O Control

0	0	0	0	TGR3D is output compare register *2	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR3D is input capture register *2	Capture input source is TIOCD3 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 4/count clock	Input capture at TCNT4 count-up/ count-down*1

* : Don't care

Notes: 1. When bits TPSC2 to TPSC0 in TCR4 are set to B'000 and ø/1 is used as the TCNT4 count clock, this setting is invalid and input capture does not occur.
2. When the BFB bit in TMDR3 is set to 1 and TGR3D is used as a buffer register, this setting is invalid and input capture/output compare does not occur.

Note: When TGRC or TGRD is designated for buffer operation, this setting is invalid and the register operates as a buffer register.

Bit	7	6	5	4	3	2	1	0
	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Initial value	0	1	0	0	0	0	0	0
Read/Write	R/W	—	—	R/W	R/W	R/W	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

TGR Interrupt Enable C

0	Interrupt request (TGIC) by TGFC bit disabled
1	Interrupt request (TGIC) by TGFC bit enabled

TGR Interrupt Enable D

0	Interrupt request (TGID) by TGFD bit disabled
1	Interrupt request (TGID) by TGFD bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit :	7	6	5	4	3	2	1	0
	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
Initial value :	1	1	0	0	0	0	0	0
Read/Write :	—	—	—	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT=TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Input Capture/Output Compare Flag C

0	[Clearing conditions] • When DTC is activated by TGIC interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFC after reading TGFC = 1
1	[Setting conditions] • When TCNT = TGRC while TGRC is functioning as output compare register • When TCNT value is transferred to TGRC by input capture signal while TGRC is functioning as input capture register

Input Capture/Output Compare Flag D

0	[Clearing conditions] • When DTC is activated by TGID interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFD after reading TGFD = 1
1	[Setting conditions] • When TCNT = TGRD while TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal while TGRD is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (changes from H'FFFF to H'0000)

Note: * Can only be written with 0 for flag clearing.

TCNT3—Timer Counter 3 **H'FE86** **TPU3**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up-counter

TGR3A—Timer General Register 3A **H'FE88** **TPU3**
TGR3B—Timer General Register 3B **H'FE8A** **TPU3**
TGR3C—Timer General Register 3C **H'FE8C** **TPU3**
TGR3D—Timer General Register 3D **H'FE8E** **TPU3**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Timer Prescaler

0	0	0	Internal clock: counts on ø/1
		1	Internal clock: counts on ø/4
	1	0	Internal clock: counts on ø/16
		1	Internal clock: counts on ø/64
1	0	0	External clock: counts on TCLKA pin input
		1	External clock: counts on TCLKC pin input
	1	0	Internal clock: counts on ø/1024
		1	Counts on TCNT5 overflow/underflow

Note: This setting is ignored when channel 4 is in phase counting mode.

Clock Edge

0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Note: This setting is ignored when channel 4 is in phase counting mode. The internal clock edge selection is valid when the input clock is ø/4 or slower. This setting is ignored if ø/1 or overflow/underflow on another channel is selected as the input clock.

Counter Clear

0	0	TCNT clearing disabled
	1	TCNT cleared by TGRA compare match/input capture
1	0	TCNT cleared by TGRB compare match/input capture
	1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*

Note: * Synchronous operation setting is performed by setting the SYNC bit in TSYR to 1.

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	MD3	MD2	MD1	MD0
Initial value	:	1	1	0	0	0	0	0	0
Read/Write	:	—	—	—	—	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

* : Don't care

Note: MD3 is a reserved bit. In a write, it should always be written with 0.

Bit :	7	6	5	4	3	2	1	0
	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR4A I/O Control

0	0	0	0	TGR4A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR4A is input capture register	Capture input source is TIOCA4 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is TGR3A compare match/ input capture	Input capture at generation of TGR3A compare match/input capture

* : Don't care

TGR4B I/O Control

0	0	0	0	TGR4B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR4B is input capture register	Capture input source is TIOCB4 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is TGR3C compare match/ input capture	Input capture at generation of TGR3C compare match/input capture

* : Don't care

Bit :	7	6	5	4	3	2	1	0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Initial value :	0	1	0	0	0	0	0	0
Read/Write :	R/W	—	R/W	R/W	—	—	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

Underflow Interrupt Enable

0	Interrupt request (TCIU) by TCFU disabled
1	Interrupt request (TCIU) by TCFU enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit	7	6	5	4	3	2	1	0
	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	R	—	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (changes from H'FFFF to H'0000)

Underflow Flag

0	[Clearing condition] When 0 is written to TCFU after reading TCFU = 1
1	[Setting condition] When the TCNT value underflows (changes from H'0000 to H'FFFF)

Count Direction Flag

0	TCNT counts down
1	TCNT counts up

Note: * Can only be written with 0 for flag clearing.

TCNT4—Timer Counter 4 **H'FE96** **TPU4**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up/down-counter*

Note: * This timer counter can be used as an up/down-counter only in phase counting mode or when performing overflow/underflow counting on another channel. In other cases it functions as an up-counter.

TGR4A—Timer General Register 4A **H'FE98** **TPU4**

TGR4B—Timer General Register 4B **H'FE9A** **TPU4**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit :	7	6	5	4	3	2	1	0
	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Time Prescaler

0	0	0	Internal clock: counts on ø/1
		1	Internal clock: counts on ø/4
	1	0	Internal clock: counts on ø/16
		1	Internal clock: counts on ø/64
1	0	0	External clock: counts on TCLKA pin input
		1	External clock: counts on TCLKC pin input
	1	0	Internal clock: counts on ø/256
		1	External clock: counts on TCLKD pin input

Note: This setting is ignored when channel 5 is in phase counting mode.

Clock Edge

0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Note: This setting is ignored when channel 5 is in phase counting mode. The internal clock edge selection is valid when the input clock is ø/4 or slower. This setting is ignored if ø/1 or overflow/underflow on another channel is selected as the input clock.

Counter Clear

0	0	TCNT clearing disabled
	1	TCNT cleared by TGRA compare match/input capture
1	0	TCNT cleared by TGRB compare match/input capture
	1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*

Note: * Synchronous operation setting is performed by setting the SYNC bit in TSYR to 1.

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	MD3	MD2	MD1	MD0
Initial value	:	1	1	0	0	0	0	0	0
Read/Write	:	—	—	—	—	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

* : Don't care

Note: MD3 is a reserved bit. In a write, it should always be written with 0.

Bit	:	7	6	5	4	3	2	1	0
		IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR5A I/O Control

0	0	0	0	TGR5A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	*	0	0	TGR5A is input capture register	Capture input source is TIOCA5 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges

* : Don't care

TGR5B I/O Control

0	0	0	0	TGR5B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	*	0	0	TGR5B is input capture register	Capture input source is TIOCB5 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges

* : Don't care

Bit :	7	6	5	4	3	2	1	0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Initial value :	0	1	0	0	0	0	0	0
Read/Write :	R/W	—	R/W	R/W	—	—	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

Underflow Interrupt Enable

0	Interrupt request (TCIU) by TCFU disabled
1	Interrupt request (TCIU) by TCFU enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit	7	6	5	4	3	2	1	0
	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	R	—	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (changes from H'FFFF to H'0000)

Underflow Flag

0	[Clearing condition] When 0 is written to TCFU after reading TCFU = 1
1	[Setting condition] When the TCNT value underflows (changes from H'0000 to H'FFFF)

Count Direction Flag

0	TCNT counts down
1	TCNT counts up

Note: * Can only be written with 0 for flag clearing.

TCNT5—Timer Counter 5 **H'FEA6** **TPU5**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up/down-counter*

Note: * This timer counter can be used as an up/down-counter only in phase counting mode or when performing overflow/underflow counting on another channel. In other cases it functions as an up-counter.

TGR5A—Timer General Register 5A **H'FEA8** **TPU5**
TGR5B—Timer General Register 5B **H'FEAA** **TPU5**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P1DDR—Port 1 Data Direction Register **H'FEB0** **Port 1**

Bit	:	7	6	5	4	3	2	1	0
		P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	W	W	W	W	W	W	W	W

Specify input or output for individual port 1 pins

P2DDR—Port 2 Data Direction Register **H'FEB1** **Port 2**

Bit	7	6	5	4	3	2	1	0
	P27DDR	P26DDR	P25DDR	P24DDR	P23DDR	P22DDR	P21DDR	P20DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port 2 pins

P3DDR—Port 3 Data Direction Register **H'FEB2** **Port 3**

Bit	7	6	5	4	3	2	1	0
	—	—	P35DDR	P34DDR	P33DDR	P32DDR	P31DDR	P30DDR
Initial value	Undefined	Undefined	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

Specify input or output for individual port 3 pins

PADDR—Port A Data Direction Register **H'FEB9** **Port A**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PA3DDR	PA2DDR	PA1DDR	PA0DDR
Initial value	Undefined	Undefined	Undefined	Undefined	0	0	0	0
Read/Write	—	—	—	—	W	W	W	W

Specify input or output for individual port A pins

PBDDR—Port B Data Direction Register **H'FEBA** **Port B**

Bit	7	6	5	4	3	2	1	0
	PB7DDR	PB6DDR	PB5DDR	PB4DDR	PB3DDR	PB2DDR	PB1DDR	PB0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port B pins

PCDDR—Port C Data Direction Register **H'FEBB** **Port C**

Bit	7	6	5	4	3	2	1	0
	PC7DDR	PC6DDR	PC5DDR	PC4DDR	PC3DDR	PC2DDR	PC1DDR	PC0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port C pins

PDDDR—Port D Data Direction Register **H'FEBC** **Port D**

Bit	7	6	5	4	3	2	1	0
	PD7DDR	PD6DDR	PD5DDR	PD4DDR	PD3DDR	PD2DDR	PD1DDR	PD0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port D pins

PEDDR—Port E Data Direction Register **H'FEBD** **Port E**

Bit	7	6	5	4	3	2	1	0
	PE7DDR	PE6DDR	PE5DDR	PE4DDR	PE3DDR	PE2DDR	PE1DDR	PE0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port E pins

Bit	:	7	6	5	4	3	2	1	0
		PF7DDR	PF6DDR	PF5DDR	PF4DDR	PF3DDR	PF2DDR	PF1DDR	PF0DDR
Modes 4 to 6*									
Initial value	:	1	0	0	0	0	0	0	0
Read/Write	:	W	W	W	W	W	W	W	W
Mode 7*									
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	W	W	W	W	W	W	W	W

Specify input or output for individual port F pins

Note: * Modes 6 and 7 cannot be used in the ROMless version.

PGDDR—Port G Data Direction Register H'FEBF Port G

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	PG4DDR	PG3DDR	PG2DDR	PG1DDR	PG0DDR
Modes 4 and 5									
Initial value	:	Undefined	Undefined	Undefined	1	0	0	0	0
Read/Write	:	—	—	—	W	W	W	W	W
Modes 6 and 7*									
Initial value	:	Undefined	Undefined	Undefined	0	0	0	0	0
Read/Write	:	—	—	—	W	W	W	W	W

Specify input or output for individual port G pins

Note: * Modes 6 and 7 cannot be used in the ROMless version.

IPRA — Interrupt Priority Register A	**H'FEC4**	**Interrupt Controller**
IPRB — Interrupt Priority Register B	**H'FEC5**	**Interrupt Controller**
IPRC — Interrupt Priority Register C	**H'FEC6**	**Interrupt Controller**
IPRD — Interrupt Priority Register D	**H'FEC7**	**Interrupt Controller**
IPRE — Interrupt Priority Register E	**H'FEC8**	**Interrupt Controller**
IPRF — Interrupt Priority Register F	**H'FEC9**	**Interrupt Controller**
IPRG — Interrupt Priority Register G	**H'FECA**	**Interrupt Controller**
IPRH — Interrupt Priority Register H	**H'FECB**	**Interrupt Controller**
IPRI — Interrupt Priority Register I	**H'FECC**	**Interrupt Controller**
IPRJ — Interrupt Priority Register J	**H'FECD**	**Interrupt Controller**
IPRK — Interrupt Priority Register K	**H'FECE**	**Interrupt Controller**

Bit	:	7	6	5	4	3	2	1	0
		—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0
Initial value	:	0	1	1	1	0	1	1	1
Read/Write	:	—	R/W	R/W	R/W	—	R/W	R/W	R/W

Set priority (levels 7 to 0) for interrupt sources

Correspondence between Interrupt Sources and IPR Settings

Register	Bits	
	6 to 4	2 to 0
IPRA	IRQ0	IRQ1
IPRB	IRQ2	IRQ4
	IRQ3	IRQ5
IPRC	IRQ6	DTC
	IRQ7	
IPRD	WDT	—*
IPRE	—*	A/D converter
IPRF	TPU channel 0	TPU channel 1
IPRG	TPU channel 2	TPU channel 3
IPRH	TPU channel 4	TPU channel 5
IPRI	8-bit timer channel 0	8-bit timer channel 1
IPRJ	—*	SCI channel 0
IPRK	SCI channel 1	—*

Note: * Reserved bits.

Bit	7	6	5	4	3	2	1	0
	ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0
Modes 5 to 7*								
Initial value	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Mode 4								
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Area 7 to 0 Bus Width Control

0	Area n is designated for 16-bit access
1	Area n is designated for 8-bit access

(n = 7 to 0)

Note: * Modes 6 and 7 cannot be used in the ROMless version.

ASTCR—Access State Control Register **H'FED1** **Bus Controller**

Bit	7	6	5	4	3	2	1	0
	AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Area 7 to 0 Access State Control

0	Area n is designated for 2-state access Wait state insertion in area n external space is disabled
1	Area n is designated for 3-state access Wait state insertion in area n external space is enabled

(n = 7 to 0)

Bit :	7	6	5	4	3	2	1	0
	W71	W70	W61	W60	W51	W50	W41	W40
Initial value :	1	1	1	1	1	1	1	1
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Area 4 Wait Control

0	0	Program wait not inserted
	1	1 program wait state inserted
1	0	2 program wait states inserted
	1	3 program wait states inserted

Area 5 Wait Control

0	0	Program wait not inserted
	1	1 program wait state inserted
1	0	2 program wait states inserted
	1	3 program wait states inserted

Area 6 Wait Control

0	0	Program wait not inserted
	1	1 program wait state inserted
1	0	2 program wait states inserted
	1	3 program wait states inserted

Area 7 Wait Control

0	0	Program wait not inserted
	1	1 program wait state inserted
1	0	2 program wait states inserted
	1	3 program wait states inserted

Bit :	7	6	5	4	3	2	1	0
	W31	W30	W21	W20	W11	W10	W01	W00
Initial value :	1	1	1	1	1	1	1	1
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Area 0 Wait Control

0	0	Program wait not inserted
	1	1 program wait state inserted
1	0	2 program wait states inserted
	1	3 program wait states inserted

Area 1 Wait Control

0	0	Program wait not inserted
	1	1 program wait state inserted
1	0	2 program wait states inserted
	1	3 program wait states inserted

Area 2 Wait Control

0	0	Program wait not inserted
	1	1 program wait state inserted
1	0	2 program wait states inserted
	1	3 program wait states inserted

Area 3 Wait Control

0	0	Program wait not inserted
	1	1 program wait state inserted
1	0	2 program wait states inserted
	1	3 program wait states inserted

Bit	7	6	5	4	3	2	1	0
	ICIS1	ICIS0	BRSTRM	BRSTS1	BRSTS0	—	—	—
Initial value	1	1	0	1	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reserved
Only 0 should be written to these bits

Burst Cycle Select 0

0	Max. 4 words in burst access
1	Max. 8 words in burst access

Burst Cycle Select 1

0	Burst cycle comprises 1 state
1	Burst cycle comprises 2 states

Area 0 Burst ROM Enable

0	Basic bus interface
1	Burst ROM interface

Idle Cycle Insert 0

0	Idle cycle not inserted in case of successive external read and external write cycles
1	Idle cycle inserted in case of successive external read and external write cycles

Idle Cycle Insert 1

0	Idle cycle not inserted in case of successive external read cycles in different areas
1	Idle cycle inserted in case of successive external read cycles in different areas

Bit	7	6	5	4	3	2	1	0
	BRLE	BREQOE	EAE	—	—	—	—	WAITE
Initial value	0	0	1	1	1	1	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WAIT Pin Enable

0	Wait input by $\overline{\text{WAIT}}$ pin disabled
1	Wait input by $\overline{\text{WAIT}}$ pin enabled

Reserved
(Only 0 should be written to this bit.)

Reserved
(Only 1 should be written to these bit.)

External Address Enable

0	Addresses H'010000 to H'03FFFF[*2]: • H8S/2319 and H8S/2315: On-chip ROM • H8S/2318: On-chip ROM • H8S/2317: On-chip ROM at addresses H'010000 to H'01FFFF and reserved area[*1] at addresses H'020000 to H'03FFFF • H8S/2311, H8S/2313, and H8S/2316: Reserved area[*1]
1	Addresses H'010000 to H'03FFFF[*2]: • Expanded mode: External addresses • Single-chip mode: Reserved area[*1]

Notes: 1. Do not access a reserved area.
2. H'010000 to H'05FFFF in the H8S/2315, and H'010000 to H'07FFFF in the H8S/2319.

BREQO Pin Enable

0	$\overline{\text{BREQO}}$ output disabled
1	$\overline{\text{BREQO}}$ output enabled

Bus Release Enable

0	External bus release disabled
1	External bus release enabled

Bit :	7	6	5	4	3	2	1	0
	—	—	—	—	RAMS	RAM2	RAM1	RAM0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	—	—	—	—	R/W	R/W	R/W	R/W

RAM Select, Flash Memory Area Select

RAMS	RAM2	RAM1	RAM0	RAM Area	Block Name
0	*	*	*	H'FFDC00 to H'FFEBFF	RAM area, 4 kbytes
1	0	0	0	H'000000 to H'000FFF	EB0 (4 kbytes)
			1	H'001000 to H'001FFF	EB1 (4 kbytes)
		1	0	H'002000 to H'002FFF	EB2 (4 kbytes)
			1	H'003000 to H'003FFF	EB3 (4 kbytes)
	1	0	0	H'004000 to H'004FFF	EB4 (4 kbytes)
			1	H'005000 to H'005FFF	EB5 (4 kbytes)
		1	0	H'006000 to H'006FFF	EB6 (4 kbytes)
			1	H'007000 to H'007FFF	EB7 (4 kbytes)

*: Don't care

ISCRH

Bit	15	14	13	12	11	10	9	8
	IRQ7SCB	IRQ7SCA	IRQ6SCB	IRQ6SCA	IRQ5SCB	IRQ5SCA	IRQ4SCB	IRQ4SCA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IRQ7 to IRQ4 Sense Control A, B

ISCRL

Bit	7	6	5	4	3	2	1	0
	IRQ3SCB	IRQ3SCA	IRQ2SCB	IRQ2SCA	IRQ1SCB	IRQ1SCA	IRQ0SCB	IRQ0SCA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IRQ3 to IRQ0 Sense Control A, B

IRQnSCB	IRQnSCA	Interrupt Request Generation
0	0	$\overline{\text{IRQn}}$ input low level
	1	Falling edge of $\overline{\text{IRQn}}$ input
1	0	Rising edge of $\overline{\text{IRQn}}$ input
	1	Both falling and rising edges of $\overline{\text{IRQn}}$ input

(n = 7 to 0)

Bit	:	7	6	5	4	3	2	1	0
		IRQ7E	IRQ6E	IRQ5E	IRQ4E	IRQ3E	IRQ2E	IRQ1E	IRQ0E
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IRQn Enable

0	IRQn interrupt disabled
1	IRQn interrupt enabled

(n = 7 to 0)

Bit :	7	6	5	4	3	2	1	0
	IRQ7F	IRQ6F	IRQ5F	IRQ4F	IRQ3F	IRQ2F	IRQ1F	IRQ0F
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Indicate the status of IRQ7 to IRQ0 interrupt requests

Bit n IRQnF	**Description**
0	[Clearing conditions] (Initial value) • When 0 is written to IRQnF after reading IRQnF = 1 • When interrupt exception handling is executed while low-level detection is set (IRQnSCB = IRQnSCA = 0) and $\overline{\text{IRQn}}$ input is high • When IRQn interrupt exception handling is executed while falling, rising, or both-edge detection is set (IRQnSCB = 1 or IRQnSCA = 1) • When the DTC is activated by an IRQn interrupt and the DISEL bit in the DTC's MRB register is 0
1	[Setting conditions] • When $\overline{\text{IRQn}}$ input goes low while low-level detection is set (IRQnSCB = IRQnSCA = 0) • When a falling edge occurs in $\overline{\text{IRQn}}$ input while falling edge detection is set (IRQnSCB = 0, IRQnSCA = 1) • When a rising edge occurs in $\overline{\text{IRQn}}$ input while rising edge detection is set (IRQnSCB = 1, IRQnSCA = 0) • When a falling or rising edge occurs in $\overline{\text{IRQn}}$ input while both-edge detection is set (IRQnSCB = IRQnSCA = 1)

(n = 7 to 0)

Note: * Can only be written with 0 for flag clearing.

Bit :	7	6	5	4	3	2	1	0
	DTCE7	DTCE6	DTCE5	DTCE4	DTCE3	DTCE2	DTCE1	DTCE0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DTC Activation Enable

0	DTC activation by this interrupt is disabled [Clearing conditions] • When the DISEL bit is 1 and data transfer has ended • When the specified number of transfers have ended
1	DTC activation by this interrupt is enabled [Holding condition] When the DISEL bit is 0 and the specified number of transfers have not ended

Correspondence between Interrupt Sources and DTCER

	Bits							
Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DTCERA	IRQ0	IRQ1	IRQ2	IRQ3	IRQ4	IRQ5	IRQ6	IRQ7
DTCERB	—	ADI	TGI0A	TGI0B	TGI0C	TGI0D	TGI1A	TGI1B
DTCERC	TGI2A	TGI2B	TGI3A	TGI3B	TGI3C	TGI3D	TGI4A	TGI4B
DTCERD	—	—	TGI5A	TGI5B	CMIA0	CMIB0	CMIA1	CMIB1
DTCERE	—	—	—	—	RXI0	TXI0	RXI1	TXI1

Note: For DTCE bit setting, read/write operations must be performed using bit-manipulation instructions such as BSET and BCLR. For the initial setting only, however, when multiple activation sources are set at one time, it is possible to disable interrupts and write after executing a dummy read on the relevant register.

Bit :	7	6	5	4	3	2	1	0
	SWDTE	DTVEC6	DTVEC5	DTVEC4	DTVEC3	DTVEC2	DTVEC1	DTVEC0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Sets vector number for DTC software activation

DTC Software Activation Enable

0	DTC software activation is disabled [Clearing conditions] • When the DISEL bit is 0 and the specified number of transfers have not ended • When 0 is written to the SWDTE bit after a software activated data transfer end interrupt (SWDTEND) has been requested of the CPU
1	DTC software activation is enabled [Holding conditions] • When the DISEL bit is 1 and data transfer has ended • When the specified number of transfers have ended • During data transfer due to software activation

Note: * Bits DTVEC6 to DTVEC0 can be written to when SWDTE = 0.

Bit :	7	6	5	4	3	2	1	0
	SSBY	STS2	STS1	STS0	OPE	—	—	IRQ37S
Initial value :	0	0	0	0	1	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	—	—	R/W

IRQ37 Software Standby Clear Select

0	$\overline{IRQ3}$ to $\overline{IRQ7}$ cannot be used as software standby mode clearing sources
1	$\overline{IRQ3}$ to $\overline{IRQ7}$ can be used as software standby mode clearing sources

Output Port Enable

0	In software standby mode, address bus and bus control signals are high-impedance
1	In software standby mode, address bus and bus control signals retain output state

Standby Timer Select

0	0	0	Standby time = 8192 states
		1	Standby time = 16384 states
	1	0	Standby time = 32768 states
		1	Standby time = 65536 states
1	0	0	Standby time = 131072 states
		1	Standby time = 262144 states
	1	0	Reserved
		1	Standby time = 16 states*

Note: * Cannot be used in the F-ZTAT version.

Software Standby

0	Transition to sleep mode after execution of SLEEP instruction
1	Transition to software standby mode after execution of SLEEP instruction

Bit :	7	6	5	4	3	2	1	0
	—	—	INTM1	INTM0	NMIEG	LWROD	—	RAME
Initial value :	0	0	0	0	0	0	0	1
Read/Write :	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W

RAM Enable

0	On-chip RAM disabled
1	On-chip RAM enabled

Reserved
Only 0 should be written to this bit

LWR Output Disable

0	PF3 is designated as $\overline{\text{LWR}}$ output pin
1	PF3 is designated as I/O port, and does not function as $\overline{\text{LWR}}$ output pin

NMI Input Edge Select

0	Falling edge
1	Rising edge

Interrupt Control Mode Selection

0	0	Interrupt control mode 0
	1	Setting prohibited
1	0	Interrupt control mode 2
	1	Setting prohibited

Reserved
Only 0 should be written to this bit

Bit	7	6	5	4	3	2	1	0
	PSTOP	—	DIV	—	—	SCK2	SCK1	SCK0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	—	—	R/W	R/W	R/W

Division Ratio Select

Reserved
Only 0 should be written to this bit

System Clock Select

			DIV = 0	DIV = 1
0	0	0	Bus master is in high-speed mode	Bus master is in high-speed mode
		1	Medium-speed clock is ø/2	Clock supplied to entire chip is ø/2
	1	0	Medium-speed clock is ø/4	Clock supplied to entire chip is ø/4
		1	Medium-speed clock is ø/8	Clock supplied to entire chip is ø/8
1	0	0	Medium-speed clock is ø/16	—
		1	Medium-speed clock is ø/32	—
	1	—	—	—

ø Clock Output Control

PSTOP	Normal Operation	Sleep Mode	Software Standby Mode	Hardware Standby Mode
0	ø output	ø output	Fixed high	High impedance
1	Fixed high	Fixed high	Fixed high	High impedance

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	MDS2	MDS1	MDS0
Initial value	1	0	0	0	0	—*	—*	—*
Read/Write	—	—	—	—	—	R	R	R

Current mode pin operating mode

Note: * Determined by pins MD2 to MD0

MSTPCRH — Module Stop Control Register H H'FF3C Power-Down State
MSTPCRL — Module Stop Control Register L H'FF3D Power-Down State

	MSTPCRH								MSTPCRL							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Specifies module stop mode

0	Module stop mode cleared
1	Module stop mode set

MSTP Bits and On-Chip Supporting Modules

Register	Bits	Module
MSTPCRH	MSTP15	—
	MSTP14	DTC
	MSTP13	TPU
	MSTP12	8-bit timer
	MSTP11	—
	MSTP10	D/A
	MSTP9	A/D
	MSTP8	—
MSTPCRL	MSTP7	—
	MSTP6	SCI1
	MSTP5	SCI0
	MSTP4	—
	MSTP3	—
	MSTP2	—
	MSTP1	—
	MSTP0	—

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	FLSHE	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	—	—	—

Flash Memory Control Register Enable

0	Flash memory control register is not selected for area H'FFFFC8 to H'FFFFCB
1	Flash memory control register is selected for area H'FFFFC8 to H'FFFFCB

Reserved Register **H'FF44**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	—	—	—	—	—

Reserved
Only 0 should be written to these bits

PFCR1—Port Function Control Register 1 H'FF45

Bit	7	6	5	4	3	2	1	0
	CSS17	CSS36	PF1CC5S	PF0CS45	A23E	A22E	A21E	A20E
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address 20 Output Enable*1

0	P10DR is output when P10DDR = 1
1	A20 is output when P10DDR = 1

Address 21 Output Enable*1

0	P11DR is output when P11DDR = 1
1	A21 is output when P11DDR = 1

Address 22 Output Enable*1

0	P12DR is output when P12DDR = 1
1	A22 is output when P12DDR = 1

Address 23 Output Enable*1

0	P13DR is output when P13DDR = 1
1	A23 is output when P13DDR = 1

Port F0 chip select 4 select*1

0	PF0 is PF0/$\overline{\text{BREQ}}$/$\overline{\text{IRQ0}}$ pin
1	PF0 is PF0/$\overline{\text{BREQ}}$/$\overline{\text{IRQ0}}$/$\overline{\text{CS4}}$ pin. $\overline{\text{CS4}}$ output is enabled when BRLE = 0, CS25E = 1, and PF0DDR = 1

Port F1 chip select 5 select*1

0	PF1 is PF1/$\overline{\text{BACK}}$/$\overline{\text{IRQ1}}$ pin
1	PF1 is PF1/$\overline{\text{BACK}}$/$\overline{\text{IRQ1}}$/$\overline{\text{CS5}}$ pin. $\overline{\text{CS5}}$ output is enabled when BRLE = 0, CS25E = 1, and PF1DDR = 1

CS36 select*1, *3

0	PG1 is PG1/$\overline{\text{IRQ7}}$/$\overline{\text{CS3}}$ pin. $\overline{\text{CS3}}$ output is enabled when when CS25E = 1 and PG1DDR = 1
1	PG1 is PG1/$\overline{\text{IRQ7}}$/$\overline{\text{CS6}}$ pin. $\overline{\text{CS6}}$ output is enabled when CS167E = 1 and PG1DDR = 1

CS17 select*1, *2

0	PG3 is PG3/$\overline{\text{CS1}}$ pin. $\overline{\text{CS1}}$ output is enabled when CS167E = 1 and PG3DDR = 1
1	PG3 is PG3/$\overline{\text{CS7}}$ pin. $\overline{\text{CS7}}$ output is enabled when CS167E = 1 and PG3DDR = 1

Notes: 1. Valid in modes 4 to 6.
2. Clear PG3DDR to 0 before changing the CSS17 bit setting.
3. Clear PG1DDR to 0 before changing the CSS36 bit setting.

PORT1—Port 1 Register **H'FF50** **Port 1**

Bit	7	6	5	4	3	2	1	0
	P17	P16	P15	P14	P13	P12	P11	P10
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port 1 pins

Note: * Determined by the state of pins P17 to P10.

PORT2—Port 2 Register **H'FF51** **Port 2**

Bit	7	6	5	4	3	2	1	0
	P27	P26	P25	P24	P23	P22	P21	P20
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port 2 pins

Note: * Determined by the state of pins P27 to P20.

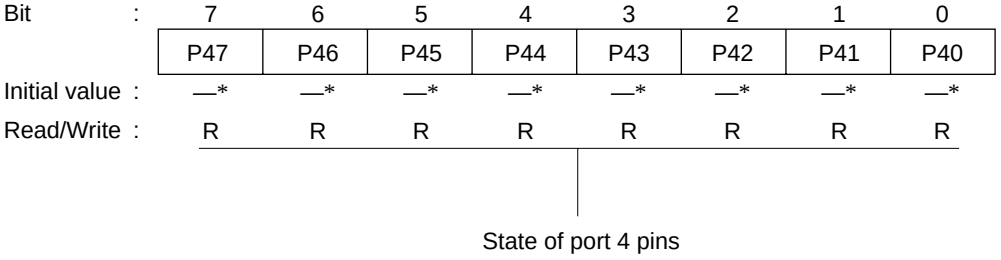
PORT3—Port 3 Register **H'FF52** **Port 3**

Bit	7	6	5	4	3	2	1	0
	—	—	P35	P34	P33	P32	P31	P30
Initial value	Undefined	Undefined	—*	—*	—*	—*	—*	—*
Read/Write	—	—	R	R	R	R	R	R

State of port 3 pins

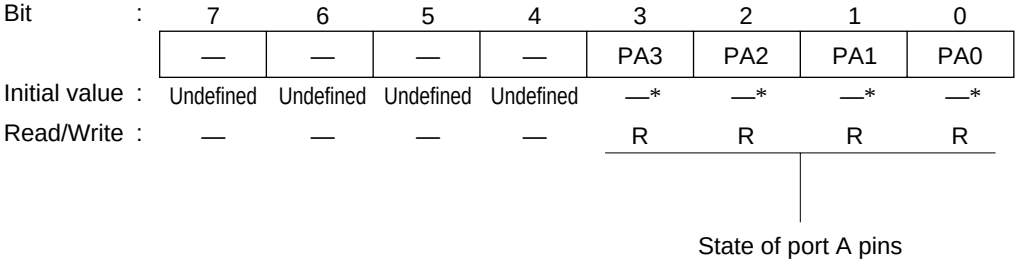
Note: * Determined by the state of pins P35 to P30.

PORT4—Port 4 Register **H'FF53** **Port 4**



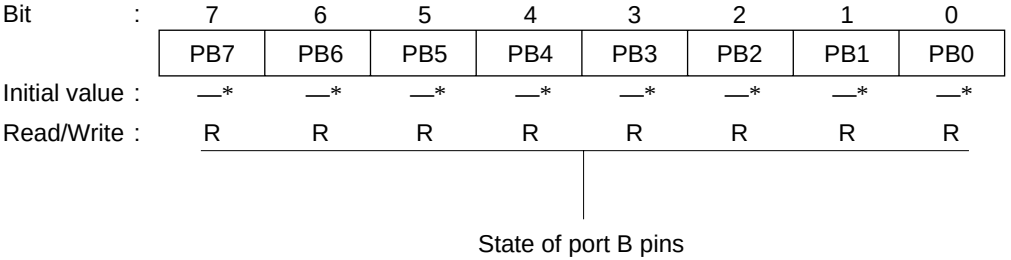
Note: * Determined by the state of pins P47 to P40.

PORTA—Port A Register **H'FF59** **Port A**



Note: * Determined by the state of pins PA3 to PA0.

PORTB—Port B Register **H'FF5A** **Port B**



Note: * Determined by the state of pins PB7 to PB0.

PORTC—Port C Register **H'FF5B** **Port C**

Bit :	7	6	5	4	3	2	1	0
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Initial value :	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write :	R	R	R	R	R	R	R	R

State of port C pins

Note: * Determined by the state of pins PC7 to PC0.

PORTD—Port D Register **H'FF5C** **Port D**

Bit :	7	6	5	4	3	2	1	0
	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Initial value :	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write :	R	R	R	R	R	R	R	R

State of port D pins

Note: * Determined by the state of pins PD7 to PD0.

PORTE—Port E Register **H'FF5D** **Port E**

Bit :	7	6	5	4	3	2	1	0
	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Initial value :	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write :	R	R	R	R	R	R	R	R

State of port E pins

Note: * Determined by the state of pins PE7 to PE0.

PORTF—Port F Register **H'FF5E** **Port F**

Bit	7	6	5	4	3	2	1	0
	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port F pins

Note: * Determined by the state of pins PF7 to PF0.

PORTG—Port G Register **H'FF5F** **Port G**

Bit	7	6	5	4	3	2	1	0
	—	—	—	PG4	PG3	PG2	PG1	PG0
Initial value	Undefined	Undefined	Undefined	—*	—*	—*	—*	—*
Read/Write	—	—	—	R	R	R	R	R

State of port G pins

Note: * Determined by the state of pins PG4 to PG0.

P1DR—Port 1 Data Register **H'FF60** **Port 1**

Bit	7	6	5	4	3	2	1	0
	P17DR	P16DR	P15DR	P14DR	P13DR	P12DR	P11DR	P10DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port 1 pins (P17 to P10)

P2DR—Port 2 Data Register **H'FF61** **Port 2**

Bit	7	6	5	4	3	2	1	0
	P27DR	P26DR	P25DR	P24DR	P23DR	P22DR	P21DR	P20DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port 2 pins (P27 to P20)

P3DR—Port 3 Data Register **H'FF62** **Port 3**

Bit	7	6	5	4	3	2	1	0
	—	—	P35DR	P34DR	P33DR	P32DR	P31DR	P30DR
Initial value	Undefined	Undefined	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port 3 pins (P35 to P30)

PADR—Port A Data Register **H'FF69** **Port A**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PA3DR	PA2DR	PA1DR	PA0DR
Initial value	Undefined	Undefined	Undefined	Undefined	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Stores output data for
port A pins (PA3 to PA0)

PBDR—Port B Data Register **H'FF6A** **Port B**

Bit	7	6	5	4	3	2	1	0
	PB7DR	PB6DR	PB5DR	PB4DR	PB3DR	PB2DR	PB1DR	PB0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port B pins (PB7 to PB0)

PCDR—Port C Data Register **H'FF6B** **Port C**

Bit	7	6	5	4	3	2	1	0
	PC7DR	PC6DR	PC5DR	PC4DR	PC3DR	PC2DR	PC1DR	PC0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port C pins (PC7 to PC0)

PDDR—Port D Data Register **H'FF6C** **Port D**

Bit	7	6	5	4	3	2	1	0
	PD7DR	PD6DR	PD5DR	PD4DR	PD3DR	PD2DR	PD1DR	PD0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port D pins (PD7 to PD0)

PEDR—Port E Data Register **H'FF6D** **Port E**

Bit	7	6	5	4	3	2	1	0
	PE7DR	PE6DR	PE5DR	PE4DR	PE3DR	PE2DR	PE1DR	PE0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port E pins (PE7 to PE0)

PFDR—Port F Data Register **H'FF6E** **Port F**

Bit	7	6	5	4	3	2	1	0
	PF7DR	PF6DR	PF5DR	PF4DR	PF3DR	PF2DR	PF1DR	PF0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port F pins (PF7 to PF0)

PGDR—Port G Data Register **H'FF6F** **Port G**

Bit	7	6	5	4	3	2	1	0
	—	—	—	PG4DR	PG3DR	PG2DR	PG1DR	PG0DR
Initial value	Undefined	Undefined	Undefined	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

Stores output data for port G pins (PG4 to PG0)

PAPCR—Port A MOS Pull-Up Control Register **H'FF70** **Port A**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PA3PCR	PA2PCR	PA1PCR	PA0PCR
Initial value	Undefined	Undefined	Undefined	Undefined	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Controls the MOS input pull-up function incorporated into port A on a bit-by-bit basis

PBPCR—Port B MOS Pull-Up Control Register **H'FF71** **Port B**

Bit	7	6	5	4	3	2	1	0
	PB7PCR	PB6PCR	PB5PCR	PB4PCR	PB3PCR	PB2PCR	PB1PCR	PB0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Controls the MOS input pull-up function incorporated into port B on a bit-by-bit basis

PCPCR—Port C MOS Pull-Up Control Register H'FF72 **Port C**

Bit	7	6	5	4	3	2	1	0
	PC7PCR	PC6PCR	PC5PCR	PC4PCR	PC3PCR	PC2PCR	PC1PCR	PC0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Controls the MOS input pull-up function incorporated into port C on a bit-by-bit basis

PDPCR—Port D MOS Pull-Up Control Register H'FF73 **Port D**

Bit	7	6	5	4	3	2	1	0
	PD7PCR	PD6PCR	PD5PCR	PD4PCR	PD3PCR	PD2PCR	PD1PCR	PD0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Controls the MOS input pull-up function incorporated into port D on a bit-by-bit basis

PEPCR—Port E MOS Pull-Up Control Register H'FF74 **Port E**

Bit	7	6	5	4	3	2	1	0
	PE7PCR	PE6PCR	PE5PCR	PE4PCR	PE3PCR	PE2PCR	PE1PCR	PE0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Controls the MOS input pull-up function incorporated into port E on a bit-by-bit basis

P3ODR—Port 3 Open Drain Control Register H'FF76 Port 3

Bit	7	6	5	4	3	2	1	0
	—	—	P35ODR	P34ODR	P33ODR	P32ODR	P31ODR	P30ODR
Initial value	Undefined	Undefined	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Controls the PMOS on/off status for each port 3 pin (P35 to P30)

PAODR—Port A Open Drain Control Register H'FF77 Port A

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PA3ODR	PA2ODR	PA1ODR	PA0ODR
Initial value	Undefined	Undefined	Undefined	Undefined	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Controls the PMOS on/off status for each port A pin (PA3 to PA0)

Bit	7	6	5	4	3	2	1	0
	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ø clock
	1	ø/4 clock
1	0	ø/16 clock
	1	ø/64 clock

Multiprocessor Mode

0	Multiprocessor function disabled
1	Multiprocessor format selected

Stop Bit Length

0	1 stop bit
1	2 stop bits

Parity Mode

0	Even parity*1
1	Odd parity*2

Notes: 1. When even parity is selected, the parity bit added to transmit data makes an even number of 1s in the transmitted character and parity bit combined. Receive data must have an even number of 1s in the received character and parity bit combined.
2. When odd parity is selected, the parity bit added to transmit data makes an odd number of 1s in the transmitted character and parity bit combined. Receive data must have an odd number of 1s in the received character and parity bit combined.

Parity Enable

0	Parity bit addition and checking disabled
1	Parity bit addition and checking enabled*

Notes: * When the PE bit is set to 1, the parity (even or odd) specified by the O/$\overline{E}$ bit is added to transmit data before transmission. In reception, the parity bit is checked for the parity (even or odd) specified by the O/$\overline{E}$ bit.

Character Length

0	8-bit data
1	7-bit data*

Note: * When 7-bit data is selected, the MSB (bit 7) of TDR is not transmitted. With 7-bit data, it is not possible to select LSB-first or MSB-first transfer.

Asynchronous Mode/Synchronous Mode Select

0	Asynchronous mode
1	Synchronous mode

Bit :	7	6	5	4	3	2	1	0
	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ø clock
	1	ø/4 clock
1	0	ø/16 clock
	1	ø/64 clock

Base Clock Pulse

BCP1	BCP0	Base Clock Pulse
0	0	32 clocks
	1	64 clocks
1	0	372 clocks
	1	256 clocks

Parity Mode

0	Even parity*1
1	Odd parity*2

Notes: 1. When even parity is selected, the parity bit added to transmit data makes an even number of 1s in the transmitted character and parity bit combined. Receive data must have an even number of 1s in the received character and parity bit combined.
2. When odd parity is selected, the parity bit added to transmit data makes an odd number of 1s in the transmitted character and parity bit combined. Receive data must have an odd number of 1s in the received character and parity bit combined.

Parity Enable
(Set to 1 when using the smart card interface)

0	Setting prohibited
1	Parity bit addition and checking enabled

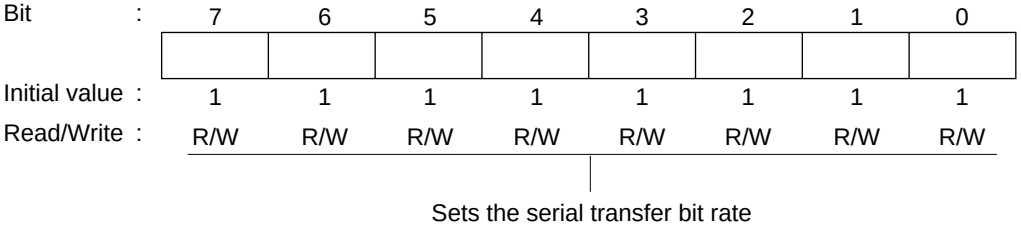
Block Transfer Mode Select

0	Normal smart card interface mode
1	Block transfer mode

GSM Mode

0	Normal smart card interface mode operation • TEND flag generated 12.5 etu (11.5 etu in block transfer mode) after beginning of start bit • Clock output on/off control only
1	GSM mode smart card interface mode operation • TEND flag generated 11.0 etu after beginning of start bit • Fixed high/low-level control possible (set in SCR) in addition to clock output on/off control

Note: etu (Elementary Time Unit): Interval for transfer of one bit



Note: For details, see section 11.2.8, Bit Rate Register (BRR), in the Hardware Manual.

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable

0	0	Asynchronous mode	Internal clock/SCK pin functions as I/O port
		Synchronous mode	Internal clock/SCK pin functions as serial clock output
	1	Asynchronous mode	Internal clock/SCK pin functions as clock output*1
		Synchronous mode	Internal clock/SCK pin functions as serial clock output
1	0	Asynchronous mode	External clock/SCK pin functions as clock input*2
		Synchronous mode	External clock/SCK pin functions as serial clock input
	1	Asynchronous mode	External clock/SCK pin functions as clock input*2
		Synchronous mode	External clock/SCK pin functions as serial clock input

Transmit End Interrupt Enable

0	Transmit-end interrupt (TEI) request disabled*3
1	Transmit-end interrupt (TEI) request enabled*3

Multiprocessor Interrupt Enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled*4 Receive-data-full interrupt (RXI) requests, receive-error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive Enable

0	Reception disabled*5
1	Reception enabled*6

Transmit Enable

0	Transmission disabled*7
1	Transmission enabled*8

Receive Interrupt Enable

0	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request disabled*9
1	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request enabled

Transmit Interrupt Enable

0	Transmit-data-empty interrupt (TXI) request disabled*10
1	Transmit-data-empty interrupt (TXI) request enabled

Notes:
1. Outputs a clock of the same frequency as the bit rate.
2. Inputs a clock with a frequency 16 times the bit rate.
3. TEI clearing can be performed by reading 1 from the TDRE flag in SSR, then clearing it to 0 and clearing the TEND flag to 0, or by clearing the TEIE bit to 0.
4. When receive data including MPB = 0 is received, receive data transfer from RSR to RDR, receive error detection, and setting of the RDRF, FER, and ORER flags in SSR , is not performed. When receive data including MPB = 1 is received, the MPB bit in SSR is set to 1, the MPIE bit is cleared to 0 automatically, and generation of RXI and ERI interrupts (when the TIE and RIE bits in SCR are set to 1) and FER and ORER flag setting is enabled.
5. Clearing the RE bit to 0 does not affect the RDRF, FER, PER, and ORER flags, which retain their states.
6. Serial reception is started in this state when a start bit is detected in asynchronous mode or serial clock input is detected in synchronous mode.
   SMR setting must be performed to decide the receive format before setting the RE bit to 1.
7. The TDRE flag in SSR is fixed at 1.
8. In this state, serial transmission is started when transmit data is written to TDR and the TDRE flag in SSR is cleared to 0.
   SMR setting must be performed to decide the transmit format before setting the TE bit to 1.
9. RXI and ERI interrupt requests can be cleared by reading 1 from the RDRF, FER, PER, or ORER flag, then clearing the flag to 0, or by clearing the RIE bit to 0.
10. TXI interrupt requests can be cleared by reading 1 from the TDRE flag, then clearing it to 0, or by clearing the TIE bit to 0.

Bit	:	7	6	5	4	3	2	1	0
		TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable
(When bit 7 of SMR is set to 1 in smart card interface mode)

SMCR	SMR	SCR setting		SCK pin function
SMIF	C/$\overline{A}$,GM	CKE1	CKE0	
0	See SCI specification			
1	0	0	0	Operates as port I/O pin
1	0	0	1	Clock output as SCK output pin
1	1	0	0	Fixed-low output as SCK output pin
1	1	0	1	Clock output as SCK output pin
1	1	1	0	Fixed-high output as SCK output pin
1	1	1	1	Clock output as SCK output pin

Transmit End Interrupt Enable

0	Transmit-end interrupt (TEI) request disabled*1
1	Transmit-end interrupt (TEI) request enabled*1

Multiprocessor Interrupt Enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled*2 Receive-data-full interrupt (RXI) requests, receive-error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive Enable

0	Reception disabled*3
1	Reception enabled*4

Transmit Enable

0	Transmission disabled*5
1	Transmission enabled*6

Receive Interrupt Enable

0	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request disabled*7
1	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request enabled

Transmit Interrupt Enable

0	Transmit-data-empty interrupt (TXI) request disabled*8
1	Transmit-data-empty interrupt (TXI) request enabled

Notes: 1. TEI clearing can be performed by reading 1 from the TDRE flag in SSR, then clearing it to 0 and clearing the TEND flag to 0, or by clearing the TEIE bit to 0.

2. When receive data including MPB = 0 is received, receive data transfer from RSR to RDR, receive error detection, and setting of the RDRF, FER, and ORER flags in SSR , is not performed. When receive data including MPB = 1 is received, the MPB bit in SSR is set to 1, the MPIE bit is cleared to 0 automatically, and generation of RXI and ERI interrupts (when the TIE and RIE bits in SCR are set to 1) and FER and ORER flag setting is enabled.
3. Clearing the RE bit to 0 does not affect the RDRF, FER, PER, and ORER flags, which retain their states.
4. Serial reception is started in this state when a start bit is detected in asynchronous mode or serial clock input is detected in synchronous mode.
   SMR setting must be performed to decide the receive format before setting the RE bit to 1.
5. The TDRE flag in SSR is fixed at 1.
6. In this state, serial transmission is started when transmit data is written to TDR and the TDRE flag in SSR is cleared to 0.
   SMR setting must be performed to decide the transmit format before setting the TE bit to 1.
7. RXI and ERI interrupt requests can be cleared by reading 1 from the RDRF, FER, PER, or ORER flag, then clearing the flag to 0, or by clearing the RIE bit to 0.
8. TXI interrupt requests can be cleared by reading 1 from the TDRE flag, then clearing it to 0, or by clearing the TIE bit to 0.

TDR0—Transmit Data Register 0 H'FF7B SCI0, Smart Card Interface 0

Bit :	7	6	5	4	3	2	1	0
Initial value :	1	1	1	1	1	1	1	1
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores data for serial transmission

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*1	R/(W)*1	R/(W)*1	R/(W)*1	R/(W)*1	R	R	R/W

Multiprocessor Bit Transfer

0	Data with a 0 multiprocessor bit is transmitted
1	Data with a 1 multiprocessor bit is transmitted

Multiprocessor Bit

0	[Clearing condition] When data with a 0 multiprocessor bit is received*2
1	[Setting condition] When data with a 1 multiprocessor bit is received

Transmit End

0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] • When the TE bit in SCR is 0 • When TDRE = 1 at transmission of the last bit of a 1-byte serial transmit character

Parity Error

0	[Clearing condition] When 0 is written to PER after reading PER = 1*3
1	[Setting condition] When, in reception, the number of 1 bits in the receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/E bit in SMR*4

Framing Error

0	[Clearing condition] When 0 is written to FER after reading FER = 1*5
1	[Setting condition] When the SCI checks the stop bit at the end of the receive data when reception ends, and the stop bit is 0*6

Overrun Error

0	[Clearing condition] When 0 is written to ORER after reading ORER = 1*7
1	[Setting condition] When the next serial reception is completed while RDRF = 1*8

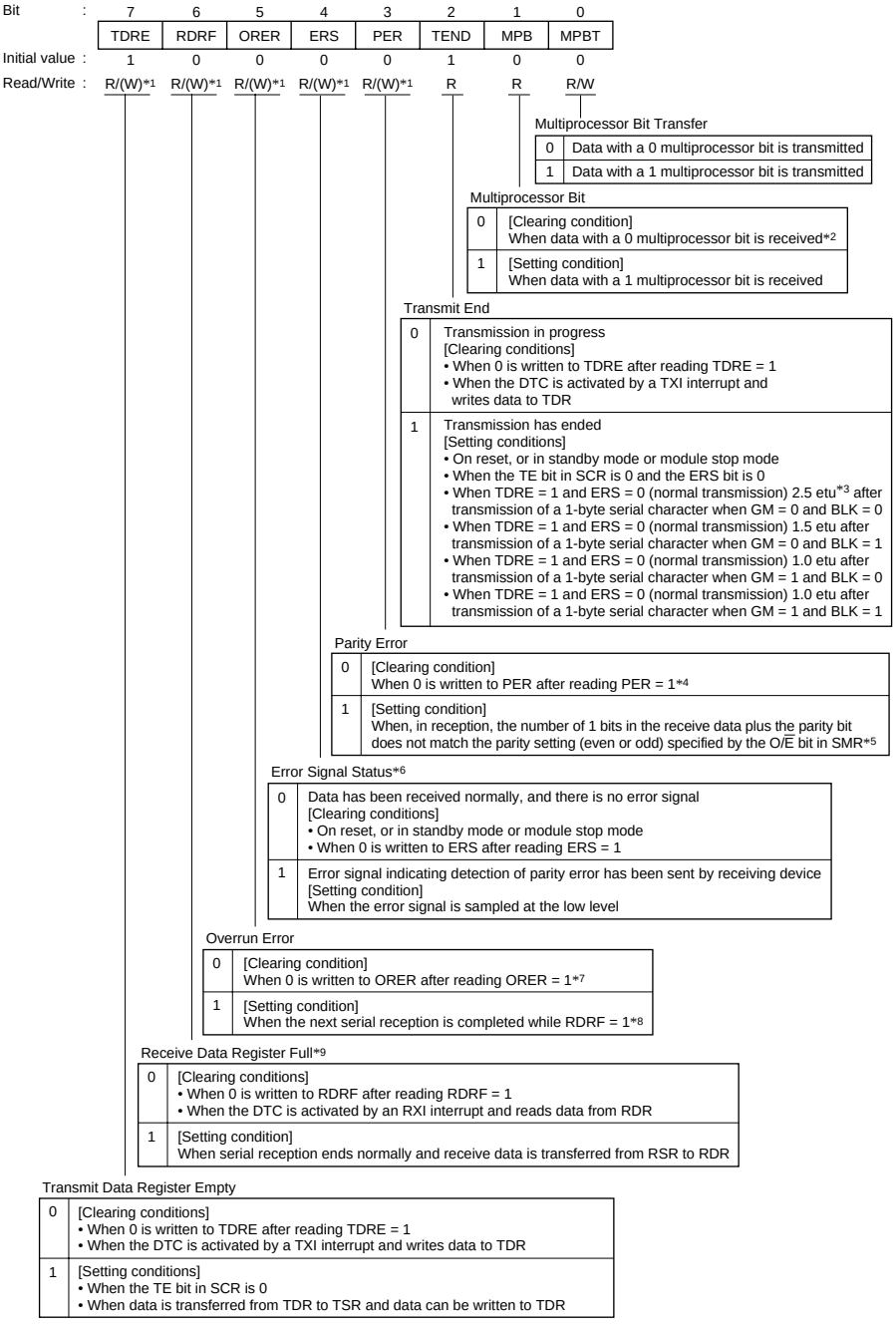
Receive Data Register Full*9

0	[Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When the DTC is activated by an RXI interrupt and reads data from RDR
1	[Setting condition] When serial reception ends normally and receive data is transferred from RSR to RDR

Transmit Data Register Empty

0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and data can be written to TDR

Notes:
1. Can only be written with 0 for flag clearing.
2. Retains its previous state when the RE bit in SCR is cleared to 0 with a multiprocessor format.
3. The PER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.
4. If a parity error occurs, the receive data is transferred to RDR but the RDRF flag is not set. Serial reception cannot be continued while the PER flag is set to 1. In synchronous mode, serial transmission is also disabled.
5. The FER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.
6. In 2-stop-bit mode, only the first stop bit is checked for a value of 1; the second stop bit is not checked. If a framing error occurs, the receive data is transferred to RDR but the RDRF flag is not set. Serial reception cannot be continued while the FER flag is set to 1. In synchronous mode, serial transmission is also disabled.
7. The ORER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.
8. The receive data prior to the overrun error is retained in RDR, and data received subsequently is lost. Serial reception cannot be continued while the ORER flag is set to 1. In synchronous mode, serial transmission is also disabled.
9. RDR and the RDRF flag are not affected and retain their previous values when an error is detected during reception or when the RE bit in SCR is cleared to 0.
   If reception of the next data is completed while the RDRF flag is still set to 1, an overrun error will occur and the receive data will be lost.


Bit : 7 6 5 4 3 2 1 0
TDRE RDRF ORER ERS PER TEND MPB MPBT
Initial value : 1 0 0 0 0 1 0 0
Read/Write : R/(W)*1 R/(W)*1 R/(W)*1 R/(W)*1 R/(W)*1 R R R/W
Multiprocessor Bit Transfer
0 Data with a 0 multiprocessor bit is transmitted
1 Data with a 1 multiprocessor bit is transmitted
Multiprocessor Bit
0 [Clearing condition] When data with a 0 multiprocessor bit is received*2
1 [Setting condition] When data with a 1 multiprocessor bit is received
Transmit End
0 Transmission in progress [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DTC is activated by a TXI interrupt and writes data to TDR
1 Transmission has ended [Setting conditions] • On reset, or in standby mode or module stop mode • When the TE bit in SCR is 0 and the ERS bit is 0 • When TDRE = 1 and ERS = 0 (normal transmission) 2.5 etu*3 after transmission of a 1-byte serial character when GM = 0 and BLK = 0 • When TDRE = 1 and ERS = 0 (normal transmission) 1.5 etu after transmission of a 1-byte serial character when GM = 0 and BLK = 1 • When TDRE = 1 and ERS = 0 (normal transmission) 1.0 etu after transmission of a 1-byte serial character when GM = 1 and BLK = 0 • When TDRE = 1 and ERS = 0 (normal transmission) 1.0 etu after transmission of a 1-byte serial character when GM = 1 and BLK = 1
Parity Error
0 [Clearing condition] When 0 is written to PER after reading PER = 1*4
1 [Setting condition] When, in reception, the number of 1 bits in the receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/E bit in SMR*5
Error Signal Status*6
0 Data has been received normally, and there is no error signal [Clearing conditions] • On reset, or in standby mode or module stop mode • When 0 is written to ERS after reading ERS = 1
1 Error signal indicating detection of parity error has been sent by receiving device [Setting condition] When the error signal is sampled at the low level
Overrun Error
0 [Clearing condition] When 0 is written to ORER after reading ORER = 1*7
1 [Setting condition] When the next serial reception is completed while RDRF = 1*8
Receive Data Register Full*9
0 [Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When the DTC is activated by an RXI interrupt and reads data from RDR
1 [Setting condition] When serial reception ends normally and receive data is transferred from RSR to RDR
Transmit Data Register Empty
0 [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DTC is activated by a TXI interrupt and writes data to TDR
1 [Setting conditions] • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and data can be written to TDR

Notes:
1. Can only be written with 0 for flag clearing.
2. Retains its previous state when the RE bit in SCR is cleared to 0 with a multiprocessor format.
3. etu (Elementary Time Unit): Interval for transfer of one bit
4. The PER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.
5. If a parity error occurs, the receive data is transferred to RDR but the RDRF flag is not set. Serial reception cannot be continued while the PER flag is set to 1. In synchronous mode, serial transmission is also disabled.
6. Clearing the TE bit in SCR to 0 does not affect the ERS flag, which retains its prior state.
7. The ORER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.
8. The receive data prior to the overrun error is retained in RDR, and data received subsequently is lost. Serial reception cannot be continued while the ORER flag is set to 1. In synchronous mode, serial transmission is also disabled.
9. RDR and the RDRF flag are not affected and retain their previous values when an error is detected during reception or when the RE bit in SCR is cleared to 0.
   If reception of the next data is completed while the RDRF flag is still set to 1, an overrun error will occur and the receive data will be lost.

RDR0—Receive Data Register 0 **H'FF7D** **SCI0, Smart Card Interface 0**

Bit	7	6	5	4	3	2	1	0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R	R	R	R	R	R	R	R

Stores received serial data

SCMR0—Smart Card Mode Register 0 **H'FF7E** **SCI0, Smart Card Interface 0**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	SDIR	SINV	—	SMIF
Initial value :	1	1	1	1	0	0	1	0
Read/Write :	—	—	—	—	R/W	R/W	—	R/W

Smart Card Interface Mode Select

0	Smart card interface function is disabled
1	Smart card interface function is enabled

Smart Card Data Invert

0	TDR contents are transmitted as they are Receive data is stored in RDR as it is
1	TDR contents are inverted before being transmitted Receive data is stored in RDR in inverted form

Smart Card Data Direction

0	TDR contents are transmitted LSB-first Receive data is stored in RDR LSB-first
1	TDR contents are transmitted MSB-first Receive data is stored in RDR MSB-first

Bit	7	6	5	4	3	2	1	0
	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ø clock
	1	ø/4 clock
1	0	ø/16 clock
	1	ø/64 clock

Multiprocessor Mode

0	Multiprocessor function disabled
1	Multiprocessor format selected

Stop Bit Length

0	1 stop bit
1	2 stop bits

Parity Mode

0	Even parity*1
1	Odd parity*2

Notes: 1. When even parity is selected, the parity bit added to transmit data makes an even number of 1s in the transmitted character and parity bit combined. Receive data must have an even number of 1s in the received character and parity bit combined.
2. When odd parity is selected, the parity bit added to transmit data makes an odd number of 1s in the transmitted character and parity bit combined. Receive data must have an odd number of 1s in the received character and parity bit combined.

Parity Enable

0	Parity bit addition and checking disabled
1	Parity bit addition and checking enabled*

Notes: * When the PE bit is set to 1, the parity (even or odd) specified by the O/$\overline{E}$ bit is added to transmit data before transmission. In reception, the parity bit is checked for the parity (even or odd) specified by the O/$\overline{E}$ bit.

Character Length

0	8-bit data
1	7-bit data*

Note: * When 7-bit data is selected, the MSB (bit 7) of TDR is not transmitted. With 7-bit data, it is not possible to select LSB-first or MSB-first transfer.

Asynchronous Mode/Synchronous Mode Select

0	Asynchronous mode
1	Synchronous mode

Bit	7	6	5	4	3	2	1	0
	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ø clock
	1	ø/4 clock
1	0	ø/16 clock
	1	ø/64 clock

Base Clock Pulse

BCP1	BCP0	Base Clock Pulse
0	0	32 clocks
	1	64 clocks
1	0	372 clocks
	1	256 clocks

Parity Mode
(Set to 1 when using the smart card interface)

0	Even parity*1
1	Odd parity*2

Notes: 1. When even parity is selected, the parity bit added to transmit data makes an even number of 1s in the transmitted character and parity bit combined. Receive data must have an even number of 1s in the received character and parity bit combined.
2. When odd parity is selected, the parity bit added to transmit data makes an odd number of 1s in the transmitted character and parity bit combined. Receive data must have an odd number of 1s in the received character and parity bit combined.

Parity Enable

0	Setting prohibited
1	Parity bit addition and checking enabled*

Notes: * When the PE bit is set to 1, the parity (even or odd) specified by the O/$\overline{E}$ bit is added to transmit data before transmission. In reception, the parity bit is checked for the parity (even or odd) specified by the O/$\overline{E}$ bit.

Block Transfer Mode Select

0	Normal smart card interface mode
1	Block transfer mode

GSM Mode

0	Normal smart card interface mode operation • TEND flag generated 12.5 etu (11.5 etu in block transfer mode) after beginning of start bit • Clock output on/off control only
1	GSM mode smart card interface mode operation • TEND flag generated 11.0 etu after beginning of start bit • Fixed high/low-level control possible (set in SCR) in addition to clock output on/off control

Note: etu (Elementary Time Unit): Interval for transfer of one bit

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sets the serial transfer bit rate

Note: For details, see section 11.2.8, Bit Rate Register (BRR), in the Hardware Manual.

Bit	:	7	6	5	4	3	2	1	0
		TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable

0	0	Asynchronous mode	Internal clock/SCK pin functions as I/O port
		Synchronous mode	Internal clock/SCK pin functions as serial clock output
	1	Asynchronous mode	Internal clock/SCK pin functions as clock output*1
		Synchronous mode	Internal clock/SCK pin functions as serial clock output
1	0	Asynchronous mode	External clock/SCK pin functions as clock input*2
		Synchronous mode	External clock/SCK pin functions as serial clock input
	1	Asynchronous mode	External clock/SCK pin functions as clock input*2
		Synchronous mode	External clock/SCK pin functions as serial clock input

Transmit End Interrupt Enable

0	Transmit-end interrupt (TEI) request disabled*3
1	Transmit-end interrupt (TEI) request enabled*3

Multiprocessor Interrupt Enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled*4 Receive-data-full interrupt (RXI) requests, receive-error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive Enable

0	Reception disabled*5
1	Reception enabled*6

Transmit Enable

0	Transmission disabled*7
1	Transmission enabled*8

Receive Interrupt Enable

0	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request disabled*9
1	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request enabled

Transmit Interrupt Enable

0	Transmit-data-empty interrupt (TXI) request disabled
1	Transmit-data-empty interrupt (TXI) request enabled*10

Notes:
1. Outputs a clock of the same frequency as the bit rate.
2. Inputs a clock with a frequency 16 times the bit rate.
3. TEI clearing can be performed by reading 1 from the TDRE flag in SSR, then clearing it to 0 and clearing the TEND flag to 0, or by clearing the TEIE bit to 0.
4. When receive data including MPB = 0 is received, receive data transfer from RSR to RDR, receive error detection, and setting of the RDRF, FER, and ORER flags in SSR , is not performed. When receive data including MPB = 1 is received, the MPB bit in SSR is set to 1, the MPIE bit is cleared to 0 automatically, and generation of RXI and ERI interrupts (when the TIE and RIE bits in SCR are set to 1) and FER and ORER flag setting is enabled.
5. Clearing the RE bit to 0 does not affect the RDRF, FER, PER, and ORER flags, which retain their states.
6. Serial reception is started in this state when a start bit is detected in asynchronous mode or serial clock input is detected in synchronous mode.
   SMR setting must be performed to decide the receive format before setting the RE bit to 1.
7. The TDRE flag in SSR is fixed at 1.
8. In this state, serial transmission is started when transmit data is written to TDR and the TDRE flag in SSR is cleared to 0.
   SMR setting must be performed to decide the transmit format before setting the TE bit to 1.
9. RXI and ERI interrupt requests can be cleared by reading 1 from the RDRF, FER, PER, or ORER flag, then clearing the flag to 0, or by clearing the RIE bit to 0.
10. TXI interrupt requests can be cleared by reading 1 from the TDRE flag, then clearing it to 0, or by clearing the TIE bit to 0.

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable
(When bit 7 of SMR is set to 1 in smart card interface mode)

SCMR	SMR	SCR setting		SCK pin function
SMIF	C/$\overline{A}$,GM	CKE1	CKE0	
0	See SCI specification			
1	0	0	0	Operates as port I/O pin
1	0	0	1	Clock output as SCK output pin
1	1	0	0	Fixed-low output as SCK output pin
1	1	0	1	Clock output as SCK output pin
1	1	1	0	Fixed-high output as SCK output pin
1	1	1	1	Clock output as SCK output pin

Transmit End Interrupt Enable

0	Transmit-end interrupt (TEI) request disabled*1
1	Transmit-end interrupt (TEI) request enabled*1

Multiprocessor Interrupt Enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled*2 Receive-data-full interrupt (RXI) requests, receive-error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive Enable

0	Reception disabled*3
1	Reception enabled*4

Transmit Enable

0	Transmission disabled*5
1	Transmission enabled*6

Receive Interrupt Enable

0	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request disabled*7
1	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request enabled

Transmit Interrupt Enable

0	Transmit-data-empty interrupt (TXI) request disabled*8
1	Transmit-data-empty interrupt (TXI) request enabled

Notes: 1. TEI clearing can be performed by reading 1 from the TDRE flag in SSR, then clearing it to 0 and clearing the TEND flag to 0, or by clearing the TEIE bit to 0.

2. When receive data including MPB = 0 is received, receive data transfer from RSR to RDR, receive error detection, and setting of the RDRF, FER, and ORER flags in SSR , is not performed. When receive data including MPB = 1 is received, the MPB bit in SSR is set to 1, the MPIE bit is cleared to 0 automatically, and generation of RXI and ERI interrupts (when the TIE and RIE bits in SCR are set to 1) and FER and ORER flag setting is enabled.
3. Clearing the RE bit to 0 does not affect the RDRF, FER, PER, and ORER flags, which retain their states.
4. Serial reception is started in this state when a start bit is detected in asynchronous mode or serial clock input is detected in synchronous mode.
   SMR setting must be performed to decide the receive format before setting the RE bit to 1.
5. The TDRE flag in SSR is fixed at 1.
6. In this state, serial transmission is started when transmit data is written to TDR and the TDRE flag in SSR is cleared to 0.
   SMR setting must be performed to decide the transmit format before setting the TE bit to 1.
7. RXI and ERI interrupt requests can be cleared by reading 1 from the RDRF, FER, PER, or ORER flag, then clearing the flag to 0, or by clearing the RIE bit to 0.
8. TXI interrupt requests can be cleared by reading 1 from the TDRE flag, then clearing it to 0, or by clearing the TIE bit to 0.

TDR1—Transmit Data Register 1 H'FF83 SCI1, Smart Card Interface 1

Bit :	7	6	5	4	3	2	1	0
Initial value :	1	1	1	1	1	1	1	1
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores data for serial transmission

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*1	R/(W)*1	R/(W)*1	R/(W)*1	R/(W)*1	R	R	R/W

Multiprocessor Bit Transfer

0	Data with a 0 multiprocessor bit is transmitted
1	Data with a 1 multiprocessor bit is transmitted

Multiprocessor Bit

0	[Clearing condition] When data with a 0 multiprocessor bit is received*2
1	[Setting condition] When data with a 1 multiprocessor bit is received

Transmit End

0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] • When the TE bit in SCR is 0 • When TDRE = 1 at transmission of the last bit of a 1-byte serial transmit character

Parity Error

0	[Clearing condition] When 0 is written to PER after reading PER = 1*3
1	[Setting condition] When, in reception, the number of 1 bits in the receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/$\overline{E}$ bit in SMR*4

Framing Error

0	[Clearing condition] When 0 is written to FER after reading FER = 1*5
1	[Setting condition] When the SCI checks the stop bit at the end of the receive data when reception ends, and the stop bit is 0*6

Overrun Error

0	[Clearing condition] When 0 is written to ORER after reading ORER = 1*7
1	[Setting condition] When the next serial reception is completed while RDRF = 1*8

Receive Data Register Full*9

0	[Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When the DTC is activated by an RXI interrupt and reads data from RDR
1	[Setting condition] When serial reception ends normally and receive data is transferred from RSR to RDR

Transmit Data Register Empty

0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and data can be written to TDR

Notes:
1. Can only be written with 0 for flag clearing.
2. Retains its previous state when the RE bit in SCR is cleared to 0 with a multiprocessor format.
3. The PER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.
4. If a parity error occurs, the receive data is transferred to RDR but the RDRF flag is not set. Serial reception cannot be continued while the PER flag is set to 1. In synchronous mode, serial transmission is also disabled.
5. The FER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.
6. In 2-stop-bit mode, only the first stop bit is checked for a value of 1; the second stop bit is not checked. If a framing error occurs, the receive data is transferred to RDR but the RDRF flag is not set. Serial reception cannot be continued while the FER flag is set to 1. In synchronous mode, serial transmission is also disabled.
7. The ORER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.
8. The receive data prior to the overrun error is retained in RDR, and data received subsequently is lost. Serial reception cannot be continued while the ORER flag is set to 1. In synchronous mode, serial transmission is also disabled.
9. RDR and the RDRF flag are not affected and retain their previous values when an error is detected during reception or when the RE bit in SCR is cleared to 0.
   If reception of the next data is completed while the RDRF flag is still set to 1, an overrun error will occur and the receive data will be lost.

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*1	R/(W)*1	R/(W)*1	R/(W)*1	R/(W)*1	R	R	R/W

Multiprocessor Bit Transfer

0	Data with a 0 multiprocessor bit is transmitted
1	Data with a 1 multiprocessor bit is transmitted

Multiprocessor Bit

0	[Clearing condition] When data with a 0 multiprocessor bit is received*2
1	[Setting condition] When data with a 1 multiprocessor bit is received

Transmit End

0	Transmission in progress [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DTC is activated by a TXI interrupt and writes data to TDR
1	Transmission has ended [Setting conditions] • On reset, or in standby mode or module stop mode • When the TE bit in SCR is 0 and the ERS bit is 0 • When TDRE = 1 and ERS = 0 (normal transmission) 2.5 etu*3 after transmission of a 1-byte serial character when GM = 0 and BLK = 0 • When TDRE = 1 and ERS = 0 (normal transmission) 1.5 etu after transmission of a 1-byte serial character when GM = 0 and BLK = 1 • When TDRE = 1 and ERS = 0 (normal transmission) 1.0 etu after transmission of a 1-byte serial character when GM = 1 and BLK = 0 • When TDRE = 1 and ERS = 0 (normal transmission) 1.0 etu after transmission of a 1-byte serial character when GM = 1 and BLK = 1

Parity Error

0	[Clearing condition] When 0 is written to PER after reading PER = 1*4
1	[Setting condition] When, in reception, the number of 1 bits in the receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/$\overline{E}$ bit in SMR*5

Error Signal Status*6

0	Data has been received normally, and there is no error signal [Clearing conditions] • On reset, or in standby mode or module stop mode • When 0 is written to ERS after reading ERS =1
1	Error signal indicating detection of parity error has been sent by receiving device [Setting condition] When the error signal is sampled at the low level

Overrun Error

0	[Clearing condition] When 0 is written to ORER after reading ORER = 1*7
1	[Setting condition] When the next serial reception is completed while RDRF = 1*8

Receive Data Register Full*9

0	[Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When the DTC is activated by an RXI interrupt and reads data from RDR
1	[Setting condition] When serial reception ends normally and receive data is transferred from RSR to RDR

Transmit Data Register Empty

0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and data can be written to TDR

Notes:
1. Can only be written with 0 for flag clearing.
2. Retains its previous state when the RE bit in SCR is cleared to 0 with a multiprocessor format.
3. etu (Elementary Time Unit): Interval for transfer of one bit
4. The PER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.
5. If a parity error occurs, the receive data is transferred to RDR but the RDRF flag is not set. Serial reception cannot be continued while the PER flag is set to 1. In synchronous mode, serial transmission is also disabled.
6. Clearing the TE bit in SCR to 0 does not affect the ERS flag, which retains its prior state.
7. The ORER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.
8. The receive data prior to the overrun error is retained in RDR, and data received subsequently is lost. Serial reception cannot be continued while the ORER flag is set to 1. In synchronous mode, serial transmission is also disabled.
9. RDR and the RDRF flag are not affected and retain their previous values when an error is detected during reception or when the RE bit in SCR is cleared to 0.
   If reception of the next data is completed while the RDRF flag is still set to 1, an overrun error will occur and the receive data will be lost.

RDR1—Receive Data Register 1 **H'FF85 SCI1, Smart Card Interface 1**

Bit	:	7	6	5	4	3	2	1	0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R	R	R	R	R	R	R	R

Stores received serial data

SCMR1—Smart Card Mode Register 1 **H'FF86 SCI1, Smart Card Interface 1**

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	SDIR	SINV	—	SMIF
Initial value	:	1	1	1	1	0	0	1	0
Read/Write	:	—	—	—	—	R/W	R/W	—	R/W

Smart Card Interface Mode Select

0	Smart card interface function is disabled
1	Smart card interface function is enabled

Smart Card Data Invert

0	TDR contents are transmitted as they are Receive data is stored in RDR as it is
1	TDR contents are inverted before being transmitted Receive data is stored in RDR in inverted form

Smart Card Data Direction

0	TDR contents are transmitted LSB-first Receive data is stored in RDR LSB-first
1	TDR contents are transmitted MSB-first Receive data is stored in RDR MSB-first

ADDRAH	**—**	**A/D Data Register AH**	**H'FF90**	**A/D Converter**
ADDRAL	**—**	**A/D Data Register AL**	**H'FF91**	**A/D Converter**
ADDRBH	**—**	**A/D Data Register BH**	**H'FF92**	**A/D Converter**
ADDRBL	**—**	**A/D Data Register BL**	**H'FF93**	**A/D Converter**
ADDRCH	**—**	**A/D Data Register CH**	**H'FF94**	**A/D Converter**
ADDRCL	**—**	**A/D Data Register CL**	**H'FF95**	**A/D Converter**
ADDRDH	**—**	**A/D Data Register DH**	**H'FF96**	**A/D Converter**
ADDRDL	**—**	**A/D Data Register DL**	**H'FF97**	**A/D Converter**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	—	—	—	—	—	—
Initial value	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Stores the results of A/D conversion

Analog Input Channel		A/D Data Register
Group 0	Group 1	
AN0	AN4	ADDRA
AN1	AN5	ADDRB
AN2	AN6	ADDRC
AN3	AN7	ADDRD

Bit	7	6	5	4	3	2	1	0
	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Channel Select

Note: These bits select the analog input channel(s). Ensure that conversion is halted (ADST = 0) before making a channel setting.

Group Selection	Channel Selection		Description	
CH2	CH1	CH0	Single Mode (SCAN = 0)	Scan Mode (SCAN = 1)
0	0	0	AN0 (Initial value)	AN0
		1	AN1	AN0, AN1
	1	0	AN2	AN0 to AN2
		1	AN3	AN0 to AN3
1	0	0	AN4	AN4
		1	AN5	AN4, AN5
	1	0	AN6	AN4 to AN6
		1	AN7	AN4 to AN7

Clock Select

ADCR Bit 3	Bit 3	Description
CKS1	CKS	
0	0	Conversion time = 530 states (max.)
	1	Conversion time = 68 states (max.)
1	0	Conversion time = 266 states (max.) (Initial value)
	1	Conversion time = 134 states (max.)

Scan Mode

0	Single mode
1	Scan mode

A/D Start

0	A/D conversion stopped
1	• Single mode: A/D conversion is started. Cleared to 0 automatically when conversion ends • Scan mode: A/D conversion is started. Conversion continues sequentially on the selected channels until ADST is cleared to 0 by software, a reset, or transition to standby mode or module stop mode

A/D Interrupt Enable

0	A/D conversion end interrupt request disabled
1	A/D conversion end interrupt request enabled

A/D End Flag

0	[Clearing conditions] • When 0 is written to the ADF flag after reading ADF = 1 • When the DTC is activated by an ADI interrupt, and ADDR is read
1	[Setting conditions] • Single mode: When A/D conversion ends • Scan mode: When A/D conversion ends on all specified channels

Note: * Can only be written with 0 for flag clearing.

Bit	7	6	5	4	3	2	1	0
	TRGS1	TRGS0	—	—	CKS1	—	—	—
Initial value	0	0	1	1	1	1	1	1
Read/Write	R/W	R/W	—	—	R/W	R/W	—	—

Reserved
(Only 1 should be written to this bit.)

Clock Select

Bit 3	ADCSR Bit 3	Description
CKS1	CKS	
0	0	Conversion time = 530 states (max.)
	1	Conversion time = 68 states (max.)
1	0	Conversion time = 266 states (max.) (Initial value)
	1	Conversion time = 134 states (max.)

Timer Trigger Select

TRGS1	TRGS1	Description
0	0	A/D conversion start by external trigger is disabled
	1	A/D conversion start by external trigger (TPU) is enabled
1	0	A/D conversion start by external trigger (8-bit timer) is enabled
	1	A/D conversion start by external trigger pin ($\overline{\text{ADTRG}}$) is enabled

DADR0—D/A Data Register 0 **H'FFA4** **D/A Converter**
DADR1—D/A Data Register 1 **H'FFA5** **D/A Converter**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores data for D/A conversion

Bit	:	7	6	5	4	3	2	1	0
		DAOE1	DAOE0	DAE	—	—	—	—	—
Initial value	:	0	0	0	1	1	1	1	1
Read/Write	:	R/W	R/W	R/W	—	—	—	—	—

D/A Output Enable 0

0	Analog output DA0 is disabled
1	Channel 0 D/A conversion is enabled Analog output DA0 is enabled

D/A Output Enable 1

0	Analog output DA1 is disabled
1	Channel 1 D/A conversion is enabled Analog output DA1 is enabled

D/A Conversion Control

DAOE1	DAOE0	DAE	Description
0	0	*	Channel 0 and 1 D/A conversion disabled
	1	0	Channel 0 D/A conversion enabled
			Channel 1 D/A conversion disabled
		1	Channel 0 and 1 D/A conversion enabled
1	0	0	Channel 0 D/A conversion disabled
			Channel 1 D/A conversion enabled
		1	Channel 0 and 1 D/A conversion enabled
	1	*	Channel 0 and 1 D/A conversion enabled

* : Don't care

Bit	7	6	5	4	3	2	1	0
	—	—	CS167E	CS25E	ASOD	—	—	—
Initial value	0	0	1	1	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R	R	R

Reserved
Only 0 should be written to these bits

AS Output Disable*1

0	PF6 is designated as $\overline{AS}$ output pin
1	PF6 is designated as I/O port, and does not function as $\overline{AS}$ output pin

CS25 Enable*1, *2

0	$\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$, and $\overline{CS5}$ output disabled (can be used as I/O ports)
1	$\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$, and $\overline{CS5}$ output enabled

CS167 Enable*1, *3

0	$\overline{CS1}$, $\overline{CS6}$, and $\overline{CS7}$ output disabled (can be used as I/O ports)
1	$\overline{CS1}$, $\overline{CS6}$, and $\overline{CS7}$ output enabled

Notes: 1. This bit is valid in modes 4 to 6.
2. Clear the DDR bits to 0 before changing the CS25E setting.
3. Clear the DDR bits to 0 before changing the CS167E setting.

Bit :	7	6	5	4	3	2	1	0
	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	0	Clock input disabled
		1	Internal clock: counted at falling edge of ø/8
	1	0	Internal clock: counted at falling edge of ø/64
		1	Internal clock: counted at falling edge of ø/8192
1	0	0	For channel 0: Count at TCNT1 overflow signal* For channel 1: Count at TCNT0 compare match A*
		1	External clock: counted at rising edge
	1	0	External clock: counted at falling edge
		1	External clock: counted at both rising and falling edges

Note: * If the count input of channel 0 is the TCNT1 overflow signal and that of channel 1 is the TCNT0 compare match signal, no incrementing clock is generated. Do not use this setting.

Counter Clear

0	0	Clear is disabled
	1	Clear by compare match A
1	0	Clear by compare match B
	1	Clear by rising edge of external reset input

Timer Overflow Interrupt Enable

0	OVF interrupt requests (OVI) are disabled
1	OVF interrupt requests (OVI) are enabled

Compare Match Interrupt Enable A

0	CMFA interrupt requests (CMIA) are disabled
1	CMFA interrupt requests (CMIA) are enabled

Compare Match Interrupt Enable B

0	CMFB interrupt requests (CMIB) are disabled
1	CMFB interrupt requests (CMIB) are enabled

TCSR0

Bit	7	6	5	4	3	2	1	0
	CMFB	CMFA	OVF	ADTE	OS3	OS2	OS1	OS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/W	R/W	R/W	R/W	R/W

TCSR1

Bit	7	6	5	4	3	2	1	0
	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0
Initial value	0	0	0	1	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	—	R/W	R/W	R/W	R/W

Output Select

0	0	No change when compare match A occurs
	1	0 is output when compare match A occurs
1	0	1 is output when compare match A occurs
	1	Output is inverted when compare match A occurs (toggle output)

Output Select

0	0	No change when compare match B occurs
	1	0 is output when compare match B occurs
1	0	1 is output when compare match B occurs
	1	Output is inverted when compare match B occurs (toggle output)

A/D Trigger Enable (TCSR0 only)

0	A/D converter start requests by compare match A are disabled
1	A/D converter start requests by compare match A are enabled

Timer Overflow Flag

0	[Clearing condition] When 0 is written to OVF after reading OVF = 1
1	[Setting condition] When TCNT overflows (changes from H'FF to H'00)

Compare Match Flag A

0	[Clearing conditions] • When 0 is written to CMFA after reading CMFA = 1 • When the DTC is activated by a CMIA interrupt, while the DISEL bit of MRB in DTC is 0
1	[Setting condition] When TCNT matches TCORA

Compare Match Flag B

0	[Clearing conditions] • When 0 is written to CMFB after reading CMFB = 1 • When the DTC is activated by a CMIB interrupt, while the DISEL bit of MRB in DTC is 0
1	[Setting condition] When TCNT matches TCORB

Note: * Only 0 can be written to bits 7 to 5, to clear these flags.

TCORA0—Time Constant Register A0 **H'FFB4** **8-Bit Timer Channel 0**
TCORA1—Time Constant Register A1 **H'FFB5** **8-Bit Timer Channel 1**

	TCORA0								TCORA1							
Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value :	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TCORB0—Time Constant Register B0 **H'FFB6** **8-Bit Timer Channel 0**
TCORB1—Time Constant Register B1 **H'FFB7** **8-Bit Timer Channel 1**

	TCORB0								TCORB1							
Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value :	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TCNT0—Timer Counter 0 **H'FFB8** **8-Bit Timer Channel 0**
TCNT1—Timer Counter 1 **H'FFB9** **8-Bit Timer Channel 1**

	TCNT0								TCNT1							
Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	OVF	WT/$\overline{IT}$	TME	—	—	CKS2	CKS1	CKS0
Initial value	0	0	0	1	1	0	0	0
Read/Write	R/(W)*1	R/W	R/W	—	—	R/W	R/W	R/W

Clock Select

CKS2	CKS1	CKS0	Clock	Overflow period* (when ø = 20 MHz)
0	0	0	ø/2 (Initial value)	25.6µs
		1	ø/64	819.2µs
	1	0	ø/128	1.6ms
		1	ø/512	6.6ms
1	0	0	ø/2048	26.2ms
		1	ø/8192	104.9ms
	1	0	ø/32768	419.4ms
		1	ø/131072	1.68s

Note: * The overflow period is the time from when TCNT starts counting up from H'00 until overflow occurs.

Timer Enable

0	TCNT is initialized to H'00 and halted
1	TCNT counts

Timer Mode Select

0	Interval timer mode: Sends the CPU an interval timer interrupt request (WOVI) when TCNT overflows
1	Watchdog timer mode: Generates the $\overline{WDTOVF}$ signal*2 when TCNT overflows

Overflow Flag

0	[Clearing condition] When 0 is written to OVF after reading OVF = 1
1	[Setting condition] When TCNT overflows from H'FF to H'00 in interval timer mode

Notes: The method for writing to TCSR is different from that for general registers to prevent accidental overwriting. For details, see section 10.2.4, Notes on Register Access, in the Hardware Manual.

1. Can only be written with 0 for flag clearing.
2. The $\overline{WDTOVF}$ pin function cannot be used in the F-ZTAT version.

TCNT—Timer Counter **H'FFBC (W) H'FFBD (R)** **WDT**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: The method for writing to TCNT different from that for general registers to prevent accidental overwritting. For details, see section 10.2.4, Notes on Register Access, in the Hardware Manual.

RSTCSR—Reset Control/Status Register **H'FFBE (W) H'FFBF (R)** **WDT**

Bit	7	6	5	4	3	2	1	0
	WOVF	RSTE	—	—	—	—	—	—
Initial value	0	0	0	1	1	1	1	1
Read/Write	R/(W)*	R/W	R/W	—	—	—	—	—

Reserved
This bit cannot be modified

Reset Enable

0	Reset signal is not generated if TCNT overflows*
1	Reset signal is generated if TCNT overflows

Note: * The modules in the chip are not reset, but TCNT and TCSR in WDT are reset.

Watchdog Timer Overflow Flag

0	[Clearing condition] When 0 is written to WOVF after reading WOVF = 1
1	[Setting condition] When TCNT overflows (changes from H'FF to H'00) during watchdog timer operation

Notes: The method for writing to RSTCSR is different from that for general registers to prevent accidental overwriting. For details, see section 10.2.4, Notes on Register Access, in the Hardware Manual.
* Can only be written with 0 for flag clearing.

Bit	7	6	5	4	3	2	1	0
	—	—	CST5	CST4	CST3	CST2	CST1	CST0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Counter Start

0	TCNTn count operation is stopped
1	TCNTn performs count operation

(n = 5 to 0)

Note: If 0 is written to the CST bit during operation with the TIOC pin designated for output, the counter stops but the TIOC pin output compare output level is retained. If TIOR is written to when the CST bit is cleared to 0, the pin output level will be changed to the set initial output value.

TSYR—Timer Synchro Register **H'FFC1** **TPU**

Bit	7	6	5	4	3	2	1	0
	—	—	SYNC5	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Timer Synchronization

0	TCNTn operates independently (TCNT presetting/ clearing is unrelated to other channels)
1	TCNTn performs synchronous operation TCNT synchronous presetting/synchronous clearing is possible

(n = 5 to 0)

Notes: 1. To set synchronous operation, the SYNC bits for at least two channels must be set to 1.
2. To set synchronous clearing, in addition to the SYNC bit , the TCNT clearing source must also be set by means of bits CCLR2 to CCLR0 in TCR.

Bit	7	6	5	4	3	2	1	0
	FWE	SWE	ESU	PSU	EV	PV	E	P
Initial value	1/0*1	0	0	0	0	0	0	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Program*2

0	Program mode cleared
1	Transition to program mode [Setting condition] When FWE = 1, SWE = 1, and PSU = 1

Erase*2

0	Erase mode cleared
1	Transition to erase mode [Setting condition] When FWE = 1, SWE = 1, and ESU = 1

Program-Verify*2

0	Program-verify mode cleared
1	Transition to program-verify mode [Setting condition] When FWE = 1 and SWE = 1

Erase-Verify*2

0	Erase-verify mode cleared
1	Transition to erase-verify mode [Setting condition] When FWE = 1 and SWE = 1

Program Setup*2

0	Program setup cleared
1	Program setup [Setting condition] When FWE = 1 and SWE = 1

Software Write Enable*2

0	Writes disabled
1	Writes enabled [Setting condition] When FWE = 1

Erase Setup*2

0	Erase setup cleared
1	Erase setup [Setting condition] When FWE = 1 and SWE = 1

Flash Write Enable

0	When a low level is input to the FWE pin (hardware-protected state)
1	When a high level is input to the FWE pin

Notes: 1. Determined by the state of the FWE pin.
2. Valid for addresses H'000000 to H'03FFFF in H8S/2318 F-ZTAT and H'000000 to H'05FFFF in H8S/2315 F-ZTAT.

Bit	7	6	5	4	3	2	1	0
	FWE	SWE1	ESU1	PSU1	EV1	PV1	E1	P1
Initial value	1	0	0	0	0	0	0	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Flash Write Enable
Always read as 1 and cannot be written to.

Software Write Enable 1*

0	Writes disabled
1	Writes enabled

Erase Setup 1*

0	Erase setup cleared
1	Erase setup [Setting condition] When SWE1 = 1

Program Setup 1*

0	Program setup cleared
1	Program setup [Setting condition] When SWE1 = 1

Erase-Verify 1*

0	Erase-verify mode cleared
1	Transition to erase-verify mode [Setting condition] When SWE1 = 1

Program-Verify 1*

0	Program-verify mode cleared
1	Transition to program-verify mode [Setting condition] When SWE1 = 1

Erase 1*

0	Erase mode cleared
1	Transition to erase mode [Setting condition] When SWE1 = 1 and ESU1 = 1

Program 1*

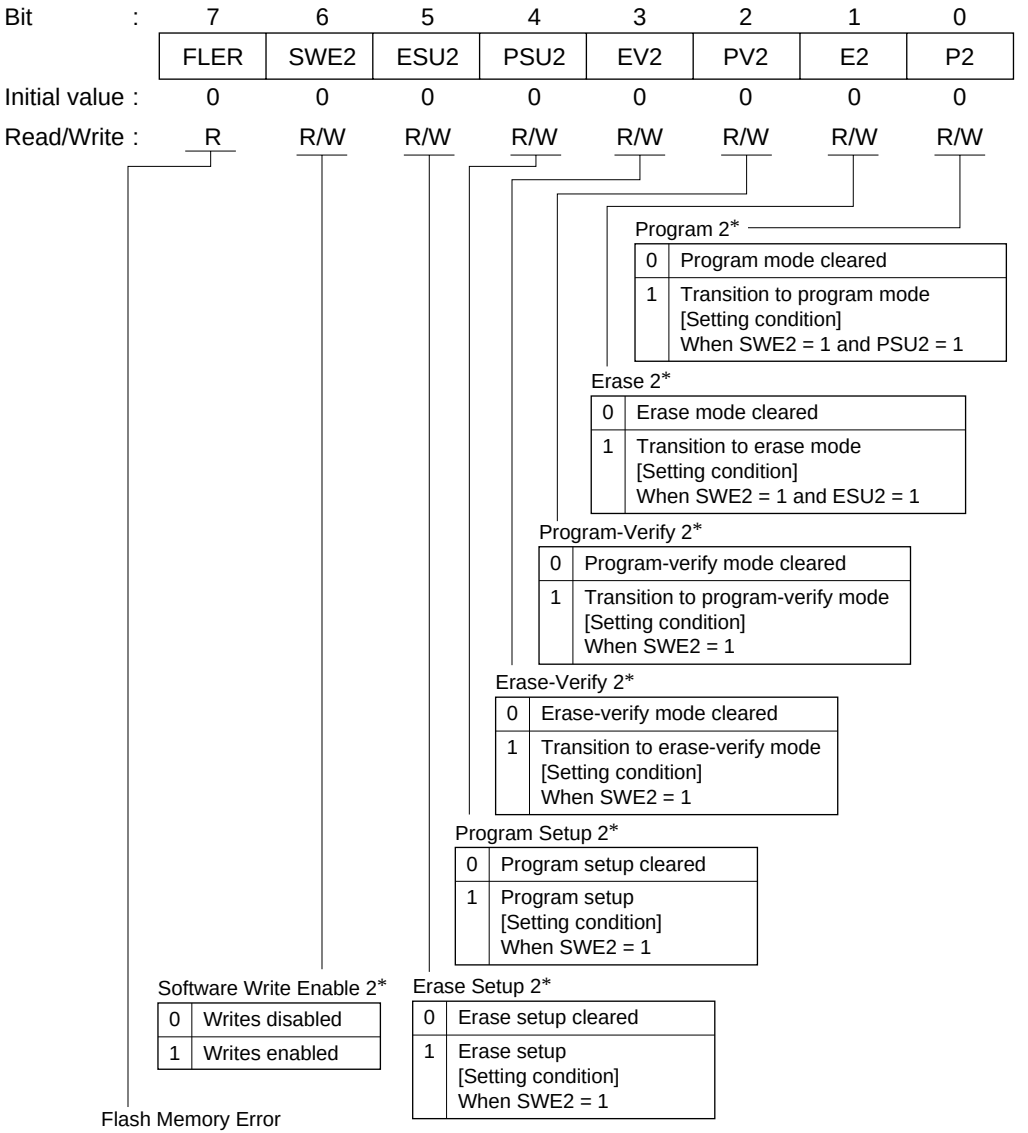
0	Program mode cleared
1	Transition to program mode [Setting condition] When SWE1 = 1 and PSU1 = 1

Note: * Valid for addresses H'000000 to H'03FFFF.

Bit	:	7	6	5	4	3	2	1	0
		FLER	—	—	—	—	—	—	—
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R	—	—	—	—	—	—	—

Flash Memory Error

0	Flash memory is operating normally Flash memory program/erase protection (error protection) is disabled [Clearing condition] Reset or hardware standby mode
1	An error has occurred during flash memory programming/erasing Flash memory program/erase protection (error protection) is enabled [Setting condition] See section 17.8.3, Error Protection, in the Hardware Manual.



Note: * Valid for addresses H'040000 to H'07FFFF.

Bit :	7	6	5	4	3	2	1	0
EBR1	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit :	7	6	5	4	3	2	1	0
EBR2	EB15*2	EB14*2	EB13*1	EB12*1	EB11	EB10	EB9	EB8
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W*2	R/W*2	R/W*1	R/W*1	R/W	R/W	R/W	R/W

Notes: 1. Valid in H8S/2319 F-ZTAT and H8S/2315 F-ZTAT versions.
2. Valid in H8S/2319 F-ZTAT version.

Bit :	7	6	5	4	3	2	1	0
	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Time Prescaler

0	0	0	Internal clock: counts on ø/1
		1	Internal clock: counts on ø/4
	1	0	Internal clock: counts on ø/16
		1	Internal clock: counts on ø/64
1	0	0	External clock: counts on TCLKA pin input
		1	External clock: counts on TCLKB pin input
	1	0	External clock: counts on TCLKC pin input
		1	External clock: counts on TCLKD pin input

Clock Edge

0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Note: The internal clock edge selection is valid when the input clock is ø/4 or slower. This setting is ignored if ø/1 or overflow/underflow on another channel is selected as the input clock.

Counter Clear

0	0	0	TCNT clearing disabled
		1	TCNT cleared by TGRA compare match/input capture
	1	0	TCNT cleared by TGRB compare match/input capture
		1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*1
1	0	0	TCNT clearing disabled
		1	TCNT cleared by TGRC compare match/input capture*2
	1	0	TCNT cleared by TGRD compare match/input capture*2
		1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*1

Notes: 1. Synchronous operation setting is performed by setting the SYNC bit in TSYR to 1.
2. When TGRC or TGRD is used as a buffer register, TCNT is not cleared because the buffer register setting has priority, and compare match/input capture does not occur.

Bit	7	6	5	4	3	2	1	0
	—	—	BFB	BFA	MD3	MD2	MD1	MD0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

* : Don't care

Notes: 1. MD3 is a reserved bit. In a write, it should always be written with 0.
2. Phase counting mode cannot be set for channels 0 and 3. In this case, 0 should always be written to MD2.

TGRA Buffer Operation

0	TGRA operates normally
1	TGRA and TGRC used together for buffer operation

TGRB Buffer Operation

0	TGRB operates normally
1	TGRB and TGRD used together for buffer operation

Bit :	7	6	5	4	3	2	1	0
	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR0A I/O Control

0	0	0	0	TGR0A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR0A is input capture register	Capture input source is TIOCA0 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/ count-down

* : Don't care

TGR0B I/O Control

0	0	0	0	TGR0B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR0B is input capture register	Capture input source is TIOCB0 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/ count-down*1

* : Don't care

Note: 1. When bits TPSC2 to TPSC0 in TCR1 are set to B'000, and ø/1 is used as the TCNT1 count clock, this setting is invalid and input capture does not occur.

Bit	7	6	5	4	3	2	1	0
	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR0C I/O Control

0	0	0	0	TGR0C is output compare register*	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR0C is input capture register*	Capture input source is TIOCC0 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/ count-down

* : Don't care

Note: When the BFA bit in TMDR0 is set to 1 and TGR0C is used as a buffer register, this setting is invalid and input capture/output compare does not occur.

TGR0D I/O Control

0	0	0	0	TGR0D is output compare register *2	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR0D is input capture register *2	Capture input source is TIOCD0 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/ count-down*1

* : Don't care

Notes:
1. When bits TPSC2 to TPSC0 in TCR1 are set to B'000, and ø/1 is used as the TCNT1 count clock, this setting is invalid and input capture does not occur.
2. When the BFB bit in TMDR0 is set to 1 and TGR0D is used as a buffer register, this setting is invalid and input capture/output compare does not occur.

Note: When TGRC or TGRD is designated for buffer operation, this setting is invalid and the register operates as a buffer register.

Bit	7	6	5	4	3	2	1	0
	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Initial value	0	1	0	0	0	0	0	0
Read/Write	R/W	—	—	R/W	R/W	R/W	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

TGR Interrupt Enable C

0	Interrupt request (TGIC) by TGFC bit disabled
1	Interrupt request (TGIC) by TGFC bit enabled

TGR Interrupt Enable D

0	Interrupt request (TGID) by TGFD bit disabled
1	Interrupt request (TGID) by TGFD bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit	7	6	5	4	3	2	1	0
	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	—	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Input Capture/Output Compare Flag C

0	[Clearing conditions] • When DTC is activated by TGIC interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFC after reading TGFC = 1
1	[Setting conditions] • When TCNT = TGRC while TGRC is functioning as output compare register • When TCNT value is transferred to TGRC by input capture signal while TGRC is functioning as input capture register

Input Capture/Output Compare Flag D

0	[Clearing conditions] • When DTC is activated by TGID interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFD after reading TGFD = 1
1	[Setting conditions] • When TCNT = TGRD while TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal while TGRD is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (changes from H'FFFF to H'0000)

Note: * Can only be written with 0 for flag clearing.

TCNT0—Timer Counter 0 **H'FFD6** **TPU0**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up-counter

TGR0A—Timer General Register 0A **H'FFD8** **TPU0**
TGR0B—Timer General Register 0B **H'FFDA** **TPU0**
TGR0C—Timer General Register 0C **H'FFDC** **TPU0**
TGR0D—Timer General Register 0D **H'FFDE** **TPU0**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Time Prescaler

0	0	0	Internal clock: counts on ø/1
		1	Internal clock: counts on ø/4
	1	0	Internal clock: counts on ø/16
		1	Internal clock: counts on ø/64
1	0	0	External clock: counts on TCLKA pin input
		1	External clock: counts on TCLKB pin input
	1	0	Internal clock: counts on ø/256
		1	Counts on TCNT2 overflow/underflow

Note: This setting is ignored when channel 1 is in phase counting mode.

Clock Edge*

0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Note: This setting is ignored when channel 1 is in phase counting mode. The internal clock edge selection is valid when the input clock is ø/4 or slower. This setting is ignored if ø/1 or overflow/underflow on another channel is selected as the input clock.

Counter Clear

0	0	TCNT clearing disabled
	1	TCNT cleared by TGRA compare match/input capture
1	0	TCNT cleared by TGRB compare match/input capture
	1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*

Note: * Synchronous operation setting is performed by setting the SYNC bit in TSYR to 1.

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	MD3	MD2	MD1	MD0
Initial value	:	1	1	0	0	0	0	0	0
Read/Write	:	—	—	—	—	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

* : Don't care

Note: MD3 is a reserved bit. In a write, it should always be written with 0.

Bit	:	7	6	5	4	3	2	1	0
		IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR1A I/O Control

0	0	0	0	TGR1A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR1A is input capture register	Capture input source is TIOCA1 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is TGR0A compare match/ input capture	Input capture at generation of channel 0/TGR0A compare match/ input capture

* : Don't care

TGR1B I/O Control

0	0	0	0	TGR1B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR1B is input capture register	Capture input source is TIOCB1 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is TGR0C compare match/ input capture	Input capture at generation of TGR0C compare match/input capture

* : Don't care

Bit	7	6	5	4	3	2	1	0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Initial value	0	1	0	0	0	0	0	0
Read/Write	R/W	—	R/W	R/W	—	—	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

Underflow Interrupt Enable

0	Interrupt request (TCIU) by TCFU disabled
1	Interrupt request (TCIU) by TCFU enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit	7	6	5	4	3	2	1	0
	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	R	—	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (changes from H'FFFF to H'0000)

Underflow Flag

0	[Clearing condition] When 0 is written to TCFU after reading TCFU = 1
1	[Setting condition] When the TCNT value underflows (changes from H'0000 to H'FFFF)

Count Direction Flag

0	TCNT counts down
1	TCNT counts up

Note: * Can only be written with 0 for flag clearing.

TCNT1—Timer Counter 1 **H'FFE6** **TPU1**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up/down-counter*

Note: * This timer counter can be used as an up/down-counter only in phase counting mode or when performing overflow/underflow counting on another channel. In other cases it functions as an up-counter.

TGR1A—Timer General Register 1A **H'FFE8** **TPU1**
TGR1B—Timer General Register 1B **H'FFEA** **TPU1**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Time Prescaler

0	0	0	Internal clock: counts on ø/1
		1	Internal clock: counts on ø/4
	1	0	Internal clock: counts on ø/16
		1	Internal clock: counts on ø/64
1	0	0	External clock: counts on TCLKA pin input
		1	External clock: counts on TCLKB pin input
	1	0	External clock: counts on TCLKC pin input
		1	Internal clock: counts on ø/1024

Note: This setting is ignored when channel 2 is in phase counting mode.

Clock Edge*

0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Note: This setting is ignored when channel 2 is in phase counting mode. The internal clock edge selection is valid when the input clock is ø/4 or slower. This setting is ignored if ø/1 or overflow/underflow on another channel is selected as the input clock.

Counter Clear

0	0	TCNT clearing disabled
	1	TCNT cleared by TGRA compare match/input capture
1	0	TCNT cleared by TGRB compare match/input capture
	1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*

Note: * Synchronous operation setting is performed by setting the SYNC bit in TSYR to 1.

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	MD3	MD2	MD1	MD0
Initial value	:	1	1	0	0	0	0	0	0
Read/Write	:	—	—	—	—	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

* : Don't care

Note: MD3 is a reserved bit. In a write, it should always be written with 0.

Bit	7	6	5	4	3	2	1	0
	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR2A I/O Control

0	0	0	0	TGR2A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	*	0	0	TGR2A is input capture register	Capture input source is TIOCA2 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges

* : Don't care

TGR2B I/O Control

0	0	0	0	TGR2B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	*	0	0	TGR2B is input capture register	Capture input source is TIOCB2 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges

* : Don't care

Bit	7	6	5	4	3	2	1	0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Initial value	0	1	0	0	0	0	0	0
Read/Write	R/W	—	R/W	R/W	—	—	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

Underflow Interrupt Enable

0	Interrupt request (TCIU) by TCFU disabled
1	Interrupt request (TCIU) by TCFU enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit	7	6	5	4	3	2	1	0
	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	R	—	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (changes from H'FFFF to H'0000)

Underflow Flag

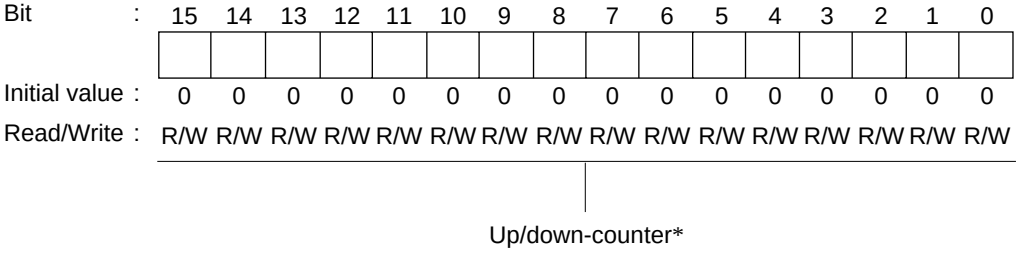
0	[Clearing condition] When 0 is written to TCFU after reading TCFU = 1
1	[Setting condition] When the TCNT value underflows (changes from H'0000 to H'FFFF)

Count Direction Flag

0	TCNT counts down
1	TCNT counts up

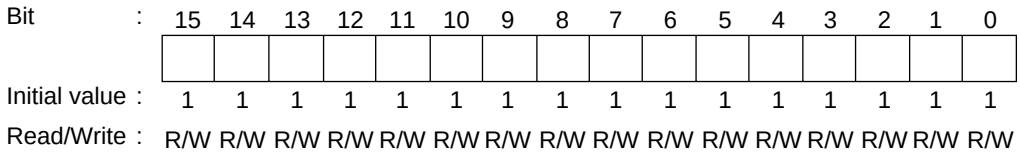
Note: * Can only be written with 0 for flag clearing.

TCNT2—Timer Counter 2 **H'FFF6** **TPU2**



Note: * This timer counter can be used as an up/down-counter only in phase counting mode or when performing overflow/underflow counting on another channel. In other cases it functions as an up-counter.

TGR2A—Timer General Register 2A **H'FFF8** **TPU2**
TGR2B—Timer General Register 2B **H'FFFA** **TPU2**



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