2M×36 DRAM SIMM Memory Module
(This SIMM is the ×36 built on ×40 board)

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM5362000BH-6	60ns	15ns	110ns
KMM5362000BH-7	70ns	20ns	130ns
KMM5362000BH-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V ± 10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**

GENERAL DESCRIPTION

The Samsung KMM5362000BH is a 1M bits×36 Dynamic RAM high density memory module. The Samsung KMM5362000BH consists of eighteen CMOS 1M×4 bit DRAMs in 20-pin SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each DRAM.

The KMM5362000BH is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

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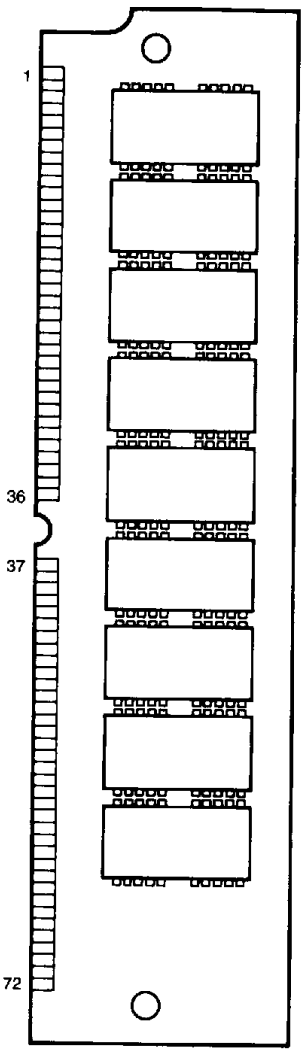
PIN CONFIGURATIONS (Front View)

Pin	Symbol	Pin	Symbol
1	V_{SS}	37	DQ_{19}
2	DQ_0	38	DQ_{20}
3	DQ_1	39	V_{SS}
4	DQ_2	40	$\overline{CAS}_0$
5	DQ_3	41	NC
6	DQ_4	42	NC
7	DQ_5	43	$\overline{CAS}_1$
8	DQ_6	44	$\overline{RAS}_0$
9	DQ_7	45	$\overline{RAS}_1$
10	V_{CC}	46	DQ_{21}
11	NC	47	$\overline{W}$
12	A_0	48	V_{SS}
13	A_1	49	DQ_{22}
14	A_2	50	DQ_{23}
15	A_3	51	DQ_{24}
16	A_4	52	DQ_{25}
17	A_5	53	DQ_{26}
18	A_6	54	DQ_{27}
19	$\overline{OE}$	55	DQ_{28}
20	DQ_8	56	DQ_{39}
21	DQ_9	57	DQ_{30}
22	DQ_{10}	58	DQ_{31}
23	DQ_{11}	59	V_{CC}
24	DQ_{12}	60	DQ_{32}
25	DQ_{13}	61	DQ_{33}
26	DQ_{14}	62	DQ_{34}
27	DQ_{15}	63	DQ_{35}
28	A_7	64	NC
29	DQ_{16}	65	NC
30	V_{CC}	66	NC
31	A_8	67	PD_1
32	A_9	68	PD_2
33	NC	69	PD_3
34	NC	70	PD_4
35	DQ_{17}	71	NC
36	DQ_{18}	72	V_{SS}



PIN NAMES

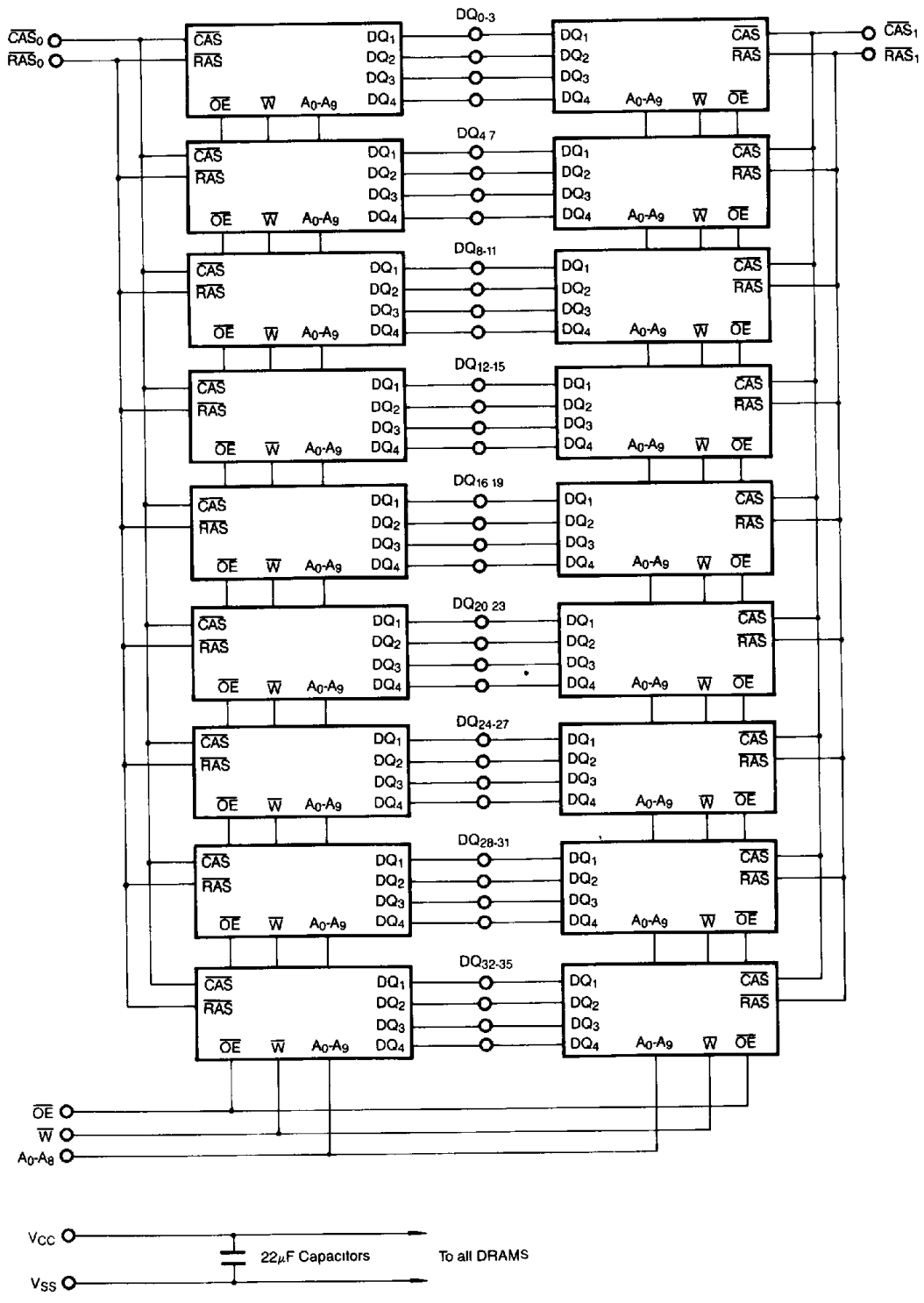
Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_0-DQ_{35}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_0$-$\overline{RAS}_1$	Row Address Strobe
$\overline{CAS}_0$-$\overline{CAS}_1$	Column Address Strobe
$\overline{OE}$	Output Enable
PD_1-PD_4	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

Presence Detect Pins (Optional)

Pin	60ns	70ns	80ns
PD_1	NC	NC	NC
PD_2	NC	NC	NC
PD_3	NC	Vss	NC
PD_4	NC	NC	Vss

* Pin Connection Changing Available

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{STG}	−55 to +150	°C
Power Dissipation	P_D	10.8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Part No.	Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	KMM5362000BH-6 KMM5362000BH-7 KMM5362000BH-8	I_{CC1}	— — —	963 873 783	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	36	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KMM5362000BH-6 KMM5362000BH-7 KMM5362000BH-8	I_{CC3}	— — —	963 873 783	mA mA mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=min.)	KMM5362000BH-6 KMM5362000BH-7 KMM5362000BH-8	I_{CC4}	— — —	738 648 558	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		I_{CC5}	—	18	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KMM5362000BH-6 KMM5362000BH-7 KMM5362000BH-8	I_{CC6}	— — —	963 873 783	mA mA mA
Input Leakage Current (Any input 0<V_{IN}<6.5V, all other pins not under test=0V)		I_{IL}	−180	180	μA
Output Leakage Current (Data out is disabled, 0V<V_{OUT}<5.5V)		I_{OL}	−20	20	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE (T_A = 25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance [A_0-A_9]	C_{IN1}	—	118	pF
Input Capacitance [$\overline{W}$, $\overline{OE}$]	C_{IN2}	—	136	pF
Input Capacitance [$\overline{RAS}_{0-1}$, $\overline{CAS}_{0-1}$]	C_{IN3}	—	73	pF
Input/Output Capacitance [DQ_{0-35}]	C_{DQ1}	—	29	pF

AC CHARACTERISTICS (0°C < T_A < 70°C, V_{CC} = 5.0V ± 10%. See notes 1, 2.)

Standard Operation	Symbol	KMM5362000BH-6		KMM5362000BH-7		KMM5362000BH-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3, 4
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3, 4, 5
Access time from column address	t_{AA}		30		35		40	ns	3, 11
CAS to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	50		55		60		ns	6
Write command pulse width	t_{WP}	15		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KMM5362000BH-6		KMM5362000BH-7		KMM5362000BH-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	30		35		40		ns	

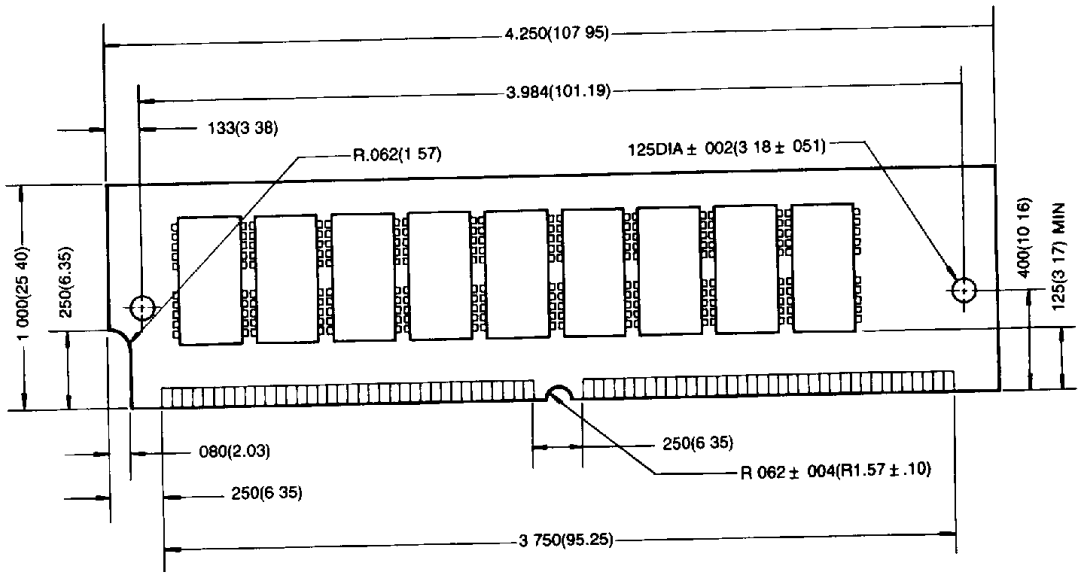
NOTES

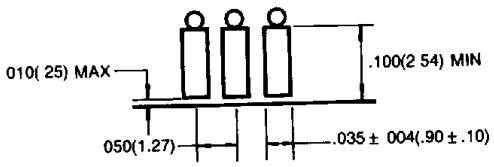
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS} is non restrictive operating parameters. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

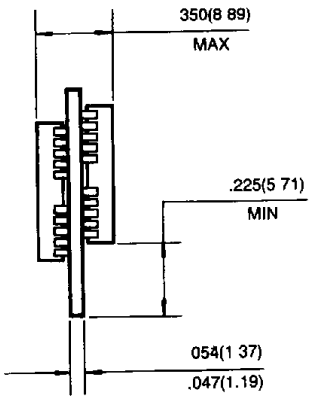
Please refer to attached Timing Chat Ⅱ

PACKAGE DIMENSIONS

Units: Inches (millimeters)







Tolerances: ± .005(.13) unless otherwise specified