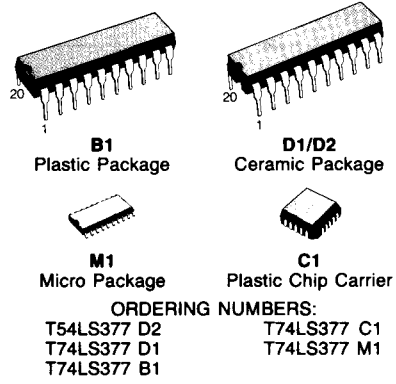




OCTAL D FLIP-FLOP WITH COMMON ENABLE AND CLOCK

DESCRIPTION

The T54LS377/T74LS377 is an 8-Bit register built using advanced Low Power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common clock enable. The device is packaged in the space-saving (0.3 inch row spacing) 20 pin package.



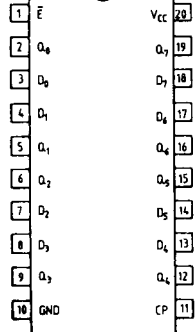
- 8-BIT HIGH SPEED PARALLEL REGISTERS
- POSITIVE EDGE-TRIGGERED D-TYPE FLIP-FLOP
- FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

\bar{E}	Enable (Active LOW) Input
D ₀ -D ₇	Data Inputs
CP	Clock (Active HIGH Going Edge) Input
Q ₀ -Q ₇	True Outputs

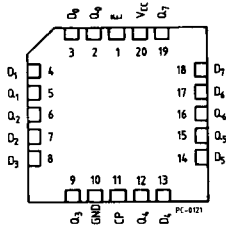
PIN CONNECTION (top view)

DUAL IN LINE



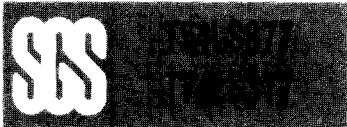
PC-4155

CHIP CARRIER



PC-4121

NC = No Internal Connection



TRUTH TABLE

E	CP	D _n	Q _n
H	┌	X	No Change
L	┌	H	H
L	┌	L	L

L = LOW Voltage Level
 H = HIGH Voltage Level
 X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to 7	V
V _I	Input Voltage, Applied to Input	-0.5 to 15	V
V _O	Output Voltage, Applied to Output	-0.5 to 10	V
I _I	Input Current, Into Inputs	-30 to 5	mA
I _O	Output Current, Into Outputs	50	mA

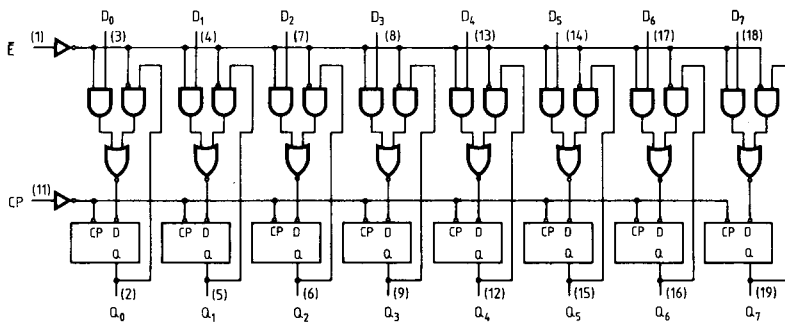
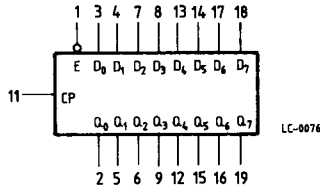
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS377D2	4.5 V	5.0 V	5.5 V	-55°C to +125°C
T74LS377XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

LOGIC SYMBOL AND LOGIC DIAGRAM



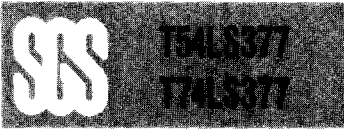
LC-0161

V_{CC} = Pin 20
 GND = Pin 10
 () = Pin numbers

FUNCTIONAL DESCRIPTION

The LS377 consists of eight edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable input (\bar{E}) are common to all flip-flops.

When \bar{E} is LOW, new data is entered into the register on the next LOW-to-HIGH transition of (CP). When \bar{E} is HIGH, the register will retain the present data independent of the CP.



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)	Units	
			Min.	Typ.	Max.			
V _{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V	
V _{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V	
		74			0.8			
V _{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V _{CC} = MIN, I _{IN} = -18mA	V	
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V _{CC} = MIN, I _{OH} = -400μA, V _{IN} = V _{IH} or V _{IL} per Truth Table	V	
		74	2.7	3.5				
V _{OL}	Output LOW Voltage	54,74		0.25	0.4	I _{OL} = 4.0mA	V _{CC} = MIN, V _{IN} = V _{IH} or V _{IL} per Truth Table	V
		74		0.35	0.5	I _{OL} = 8.0mA		
I _{IH}	Input HIGH Current				20 0.1	V _{CC} = MAX, V _{IN} = 2.7V V _{CC} = MAX, V _{IN} = 7.0V	μA mA	
I _{IL}	Input LOW Current				-0.4	V _{CC} = MAX, V _{IN} = 0.4V	mA	
I _{OS}	Output Short Circuit Current (Note 2)		-20		-100	V _{CC} = MAX, V _{OUT} = 0V	mA	
I _{CC}	Power Supply Current			18	28	V _{CC} = MAX	mA	

AC CHARACTERISTICS: T_A = 25°C

Symbol	Parameter		Limits			Test Conditions	Units
			Min.	Typ.	Max.		
f _{MAX}	Minimum Input Clock Frequency		30	40		Fig. 1	ns
t _{PLH}	Propagation Delay Clock to Output			17	27	Fig. 1 V _{CC} = 5.0V CL = 15pF R _L = 2kΩ	ns
t _{PHL}	Propagation Delay Clock to Output			18	27		ns

Notes:

- 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
- 2) Not more than one output should be shorted at a time.
- 3) Typical values are at V_{CC} = 5.0V, T_A = 25°C



AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
$t_w(\text{CP})$	Minimum Clock Pulse Width	20			Fig. 1	ns
t_s	Set-up Data to Clock (HIGH or LOW)	20			Fig. 1	ns
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			Fig. 1	ns
t_{sH}	Set-up Time HIGH Enable to Clock	10			Fig. 1	ns
t_{hH}	Hold Time HIGH Enable to Clock	5			Fig. 1	ns
t_{sL}	Set-up Time LOW Enable to Clock	25			Fig. 1	ns
t_{hL}	Hold Time Enable to Clock	5			Fig. 1	ns

$V_{CC} = 5.0\text{V}$
 $C_L = 15\text{pF}$
 $R_L = 2\text{k}\Omega$

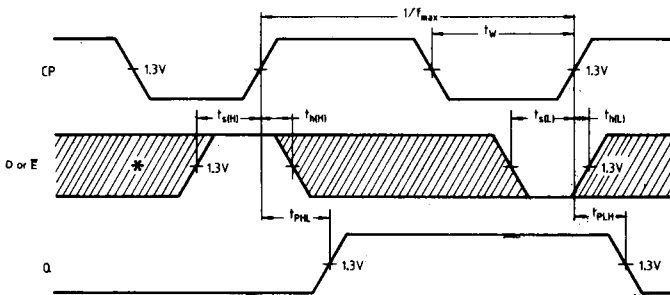
DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS

Fig. 1 Clock to Output Delays,
 Clock Pulse Width, Frequency,
 Set-up and Hold Times Data or Enable to Clock



SC0147

* The shaded areas indicate when the input is permitted to change for predictable output performance.