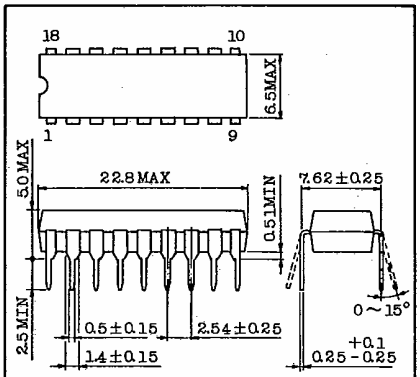
Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.18 leads.

JEDEC	—
TOSHIBA	3D18A-P

TC9122P HIGH-SPEED BCD PROGRAMMABLE COUNTER

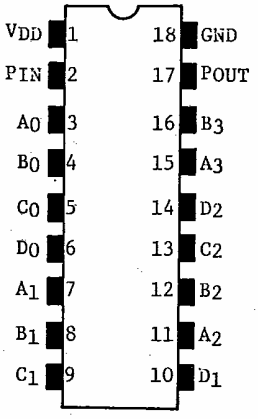
TC9122P is high-speed programmable counter of C-MOS structure developed for PLL circuits and various frequency dividers, and is provided with the following features.

- Permits epoch-making high-speed operation for C-MOS structure.

  f_{max} = 15MHz (V_{DD}=7.5V, Ta=−30 ∿ 75°C, V_{IN}=2.0Vp-p)

- Program data are input by means of BCD code, allowing frequency division of 8 ∿ 3999.
- Built-in self-bias type amplifier for divided frequency signal input is capable of operation by small signal in combination with capacitor.
- C-MOS structure provides wide range of operational supply voltage (4.5 ∿ 8.5V) and simplification of design.

PIN CONNECTION



MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3 ∿ 10	V
Input Voltage	V_{IN}	−0.3∿V_{DD}+0.3	V
Operating Temp.	T_{opr}	−30 ∿ 75	°C
Storage Temperature	T_{stg}	−55 ∿ 125	°C

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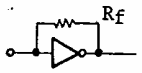
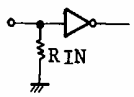
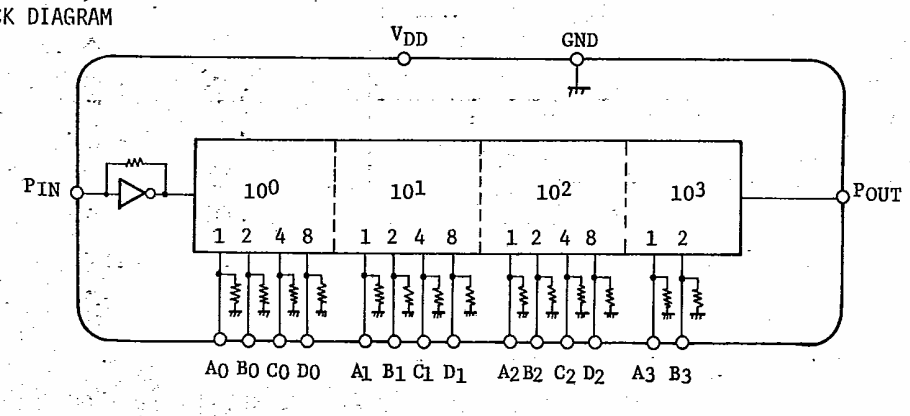
FUNCTIONAL DESCRIPTION OF EACH TERMINAL

PIN NO.	SYMBOL	NAME	FUNCTIONAL DESCRIPTION	REMARKS
2	P_{IN}	Programmable counter input terminal	Divided frequency signal input terminal of programmable counter. Built-in self-bias amplifier is capable of operation by small signal in combination with capacitor.	Built-in amplifier 
3∿16	$A_0 \sim D_0$	$\times 10^0$	Input terminals to establish frequency division ratio N by BCD. Program data allow frequency division of 8∿3999 by $3\frac{1}{2}$-digit BCD. The following frequency division ratio combinatios are inhibited.	Pull/down resistor contained in each terminal. 
	$A_1 \sim D_2$	$\times 10^1$		
	$A_2 \sim D_2$	$\times 10^2$ Program input terminal		
	A_3, B_3	$\times 10^3$		
17	P_{OUT}	Programmable counter output terminal	Output terminal of programmable counter. This terminal is for 1/N frequency output of P_{IN} input frequency. Pulse width is for 5 bits of input.	
1,18	V_{DD} GND		Terminal to which supply voltage is applied.	

A_0	B_0	C_0	D_0	A_1	B_1	C_1	D_1	A_2	B_2	C_2	D_2	A_3	A_3
1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Unless otherwise specified Ta=25°C, V_{DD}=7.5V)

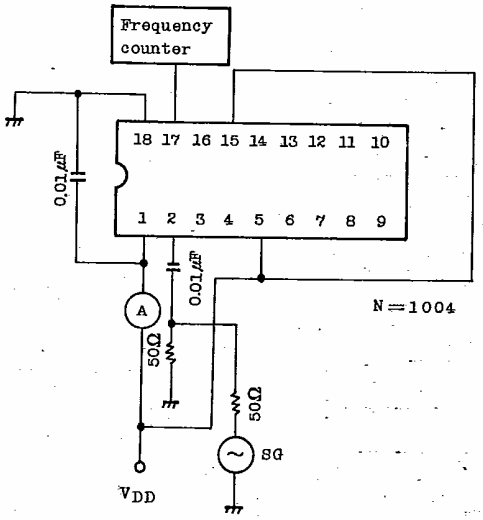
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage		V_{DD}	-	-	4.5	∿	8.5	V
Operating Input Amplitude		V_{IN}	-	-	2.0	∿	7.0	Vp-p
Operating Supply Current		I_{DD}	1	f_{IN}=15MHz, V_{IN}=2.0Vp-p	-	15	30	mA
Input Voltage	"H" Level	V_{IH}	-	-	5.5	-	-	V
	"L" Level	V_{IL}	-	-	-	-	2.0	V
Output Voltage	"H" Level	V_{OH}	-	I_{OH}=-0.5mA	6.5	-	-	V
	"L" Level	V_{OL}	-	I_{OL}=0.5mA	-	-	1.0	V
Operating Frequency Range		f_{opr}	1	(Note 1)	1	∿	15	MHz
Input Pull Down Resistance		R_{IN}	-	-	20	-	80	kΩ
Amp. Feedback Resistance		R_f	-	-	100	-	500	kΩ

(Note 1) This operational frequency satisfies the specification during the following conditions.

V_{DD} = 7.5V ± 10%, V_{IN} = 2.0Vp-p, Ta = -30∿75°C

TEST CIRCUIT 1

I_{DD}, f_{opr}



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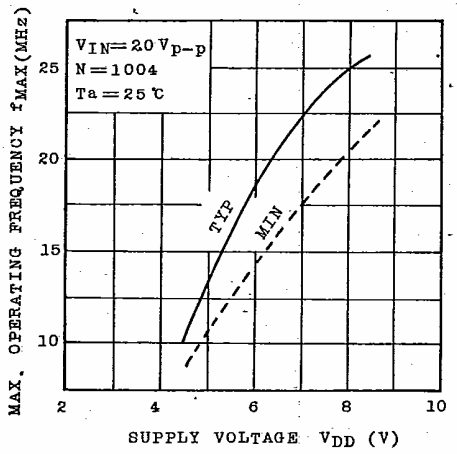
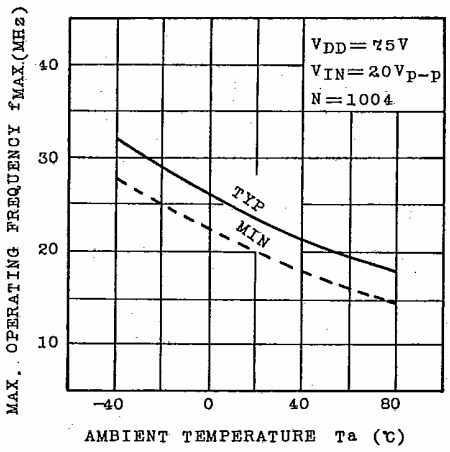
V_{DD} – f_{MAX}



Ta – f_{MAX}



V_{DD} – I_{DD}