128Kx24 SRAM 3.3 Volt

FEATURES

- 128Kx24 bit CMOS Static
- Random Access Memory Array
  - Fast Access Times: 10, 12, and 15ns
  - Master Output Enable and Write Control
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- Surface Mount Package
  - 119 Lead BGA (JEDEC MO-163), No. 391
  - Small Footprint, 14mm x 22mm
  - Multiple Ground Pins for Maximum
- Noise Immunity
- Single +3.3V (±5%) Supply Operation
- DSP Memory Solution
- Motorola DSP5630xTM
- Analog Devices SHARCTM

DESCRIPTION

The EDI8L24129VxxBC is a 3.3V, three megabit SRAM constructed with three 128Kx8 die mounted on a multi-layer laminate substrate. With 10 to 15ns access times, x24 width and a 3.3V operating voltage, the EDI8L24129V is ideal for creating a single chip memory solution for the Motorola DSP5630x (Figure 3) or a two chip solution for the Analog Devices SHARCTM DSP (Figure 4).

The single or dual chip memory solutions offer improved system performance by reducing the length of board traces and the number of board connections compared to using multiple monolithic devices. For example, the capacitance load on the data lines for the BGA package is 58% less than a monolithic SOJ solution.

The JEDEC Standard 119 lead BGA provides a 44% space savings over using 128Kx8, 300mil wide SOJs and the BGA package has a maximum height of 100 mils compared to 148 mils for the SOJ packages. The BGA package also allows the use of the same manufacturing and inspection techniques as the Motorola DSP, which is also in a BGA package.

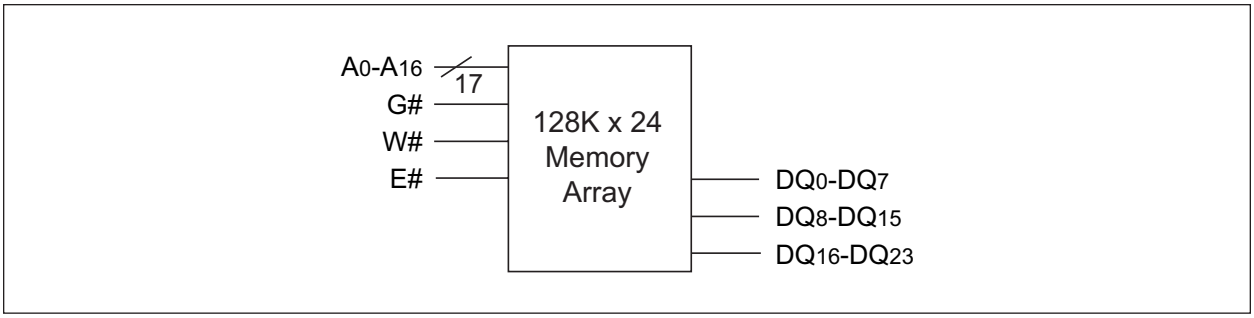
PIN CONFIGURATION

	1	2	3	4	5	6	7
A	NC	AO	A1	A2	A3	A4	NC
B	NC	A5	A6	E#	A7	A8	NC
C	I/012	NC	NC	NC	NC	NC	I/00
D	I/013	V_{CC}	GND	GND	GND	V_{CC}	I/01
E	I/014	GND	V_{CC}	GND	VCC	GND	I/02
F	I/015	V_{CC}	GND	GND	GND	V_{CC}	I/03
G	I/016	GND	V_{CC}	GND	V_{CC}	GND	I/04
H	I/017	V_{CC}	GND	GND	GND	V_{CC}	I/05
I	NC	GND	V_{CC}	GND	V_{CC}	GND	NC
J	I/018	V_{CC}	GND	GND	GND	V_{CC}	I/06
K	I/019	GND	V_{CC}	GND	V_{CC}	GND	I/07
L	I/020	V_{CC}	GND	GND	GND	V_{CC}	I/08
M	I/021	GND	V_{CC}	GND	V_{CC}	GND	I/09
N	I/022	V_{CC}	GND	GND	GND	V_{CC}	I/010
O	I/023	NC	NC	NC	NC	NC	I/011
P	NC	A9	A10	W#	A11	A12	NC
Q	NC	A13	A14	G#	A15	A16	NC

PIN NAMES

AØ-A16	Address Inputs
E#	Chip Enable
W#	Master Write Enable
G#	Master Output Enable
DQØ-DQ23	Common Data Input/Output
V_{CC}	Power (3.3V±5%)
GND	Ground
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS}	-0.5V to 4.6V
Operating Temperature TA (Ambient) Commercial Industrial	 0°C to + 70°C -40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	1.5 Watts
Output Current.	50 mA
Junction Temperature, TJ	175°C

** Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3	–	0.8	V

TRUTH TABLE

G#	E#	W#	Mode	Output	Power
X	H	X	Standby	High Z	I_{CC2},I_{CC3}
H	L	H	Output Deselect	High Z	I_{CC1}
L	L	H	Read	DOUT	I_{CC1}
X	L	L	Write	DIN	I_{CC1}

CAPACITANCE

f=1.0MHz, V_{IN}=V_{CC} or V_{SS}

Parameter	Sym	Max	Unit
Address Lines	CA	8	pF
Data Lines	CD/Q	10	pF
Write & Output Enable Lines	W#, G#	8	pF
Chip Enable Lines	EØ#-E2#	8	pF

These parameters are sampled, not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	Min	Max		Units
				10ns	12-15ns	
Operating Power Supply Current	I_{CC1}	W#= V_{IL}, II/O = 0mA, Min Cycle		420	360	mA
Standby (TTL) Supply Current	I_{CC2}	E# > V_{IH}, V_{IN} < V_{IL} or V_{IN} > V_{IH}, f=ØMHz		90	75	mA
Full Standby CMOS Supply Current	I_{CC3}	E# > V_{CC}-0.2V V_{IN} > V_{CC}-0.2V or V_{IN} < 0.2V		10	10	mA
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}		±10	±10	µA
Output Leakage Current	I_{LO}	V I/O = 0V to V_{CC}		±10	±10	µA
Output High Volltage	V_{OH}	I_{OH} = -4.0mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		0.4	0.4	V

AC TEST CIRCUIT

Figure 1

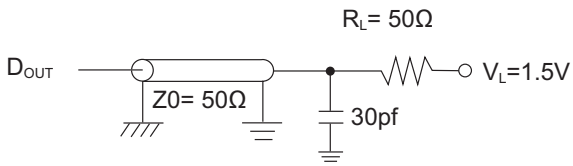
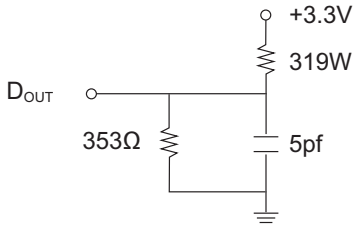


Figure 2



AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

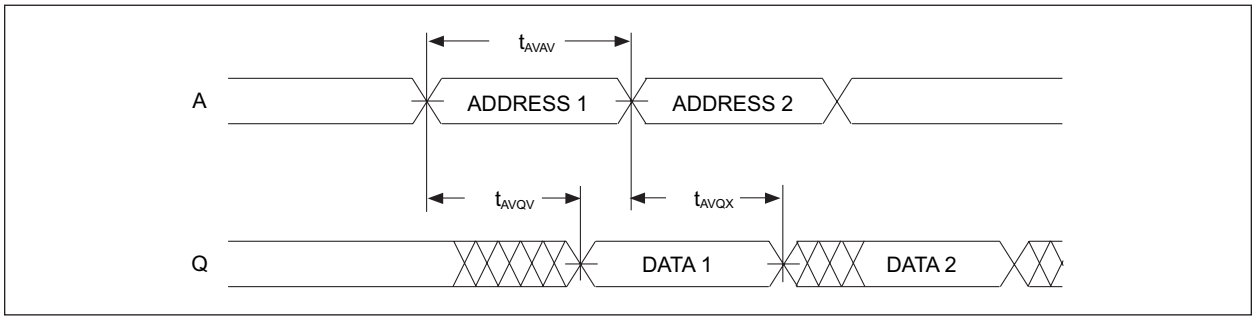
(NOTE: For t_{EHQZ},t_{GHQZ} and t_{WLQZ}, Figure 2)

AC CHARACTERISTICS – READ CYCLE

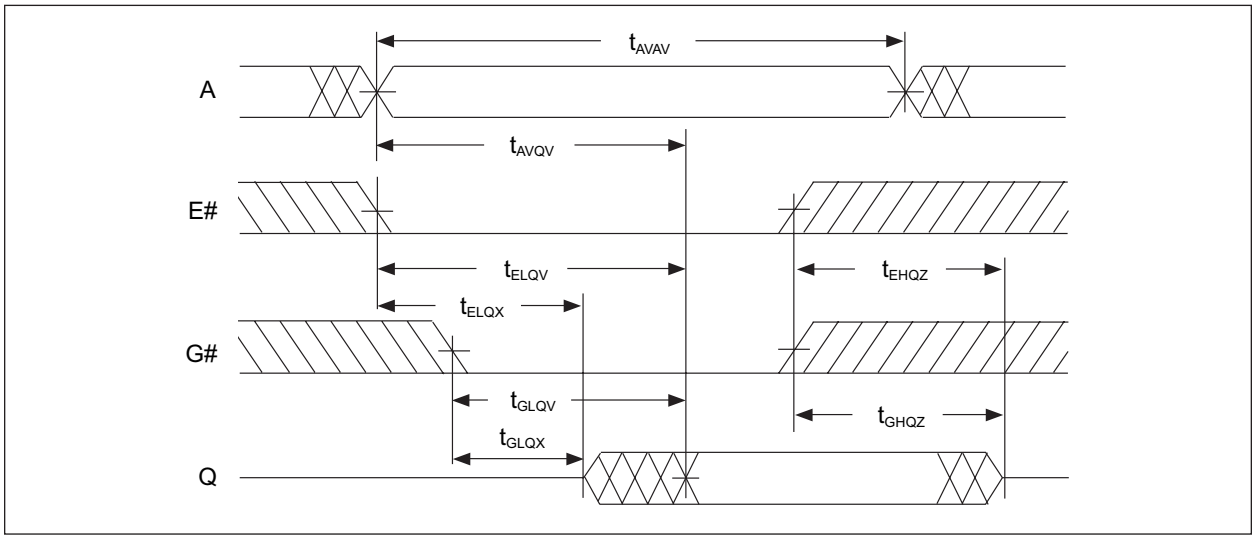
Parameter	Symbol		10ns		12ns		15ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	10		12		15		ns
Address Access Time	t_{AVQV}	t_{AA}		10		12		15	ns
Chip Enable Access Time	t_{ELQV}	t_{ACS}		10		12		15	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	3		3		3		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}		5		6		7	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	3		3		3		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		5		6		7	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	0		0		0		ns
Output Disable to Output in High Z(1)	t_{GHQZ}	t_{OHZ}		5		6		7	ns

Note 1: Parameter guaranteed, but not tested.

READ CYCLE – W# HIGH, G#, E# LOW



READ CYCLE 2 – W# HIGH

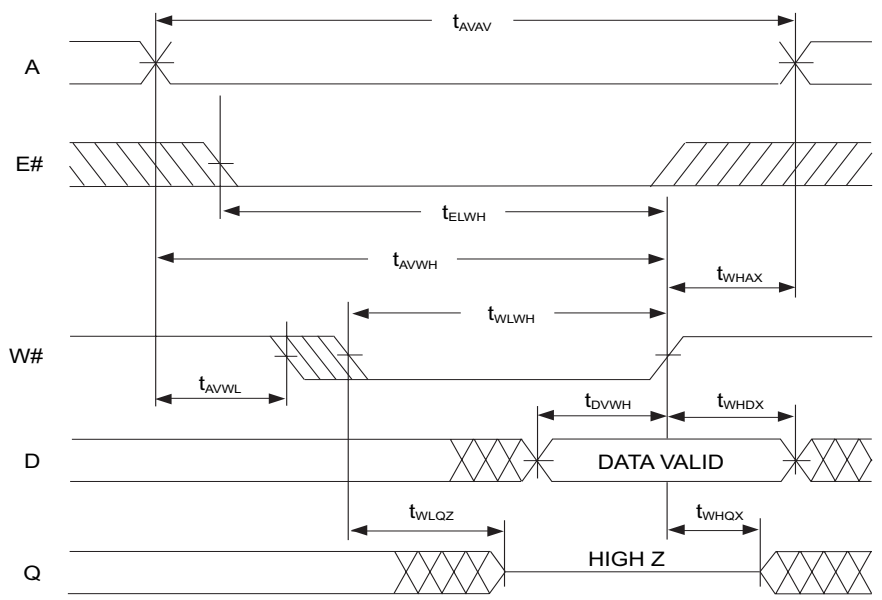


AC CHARACTERISTICS – WRITE CYCLE

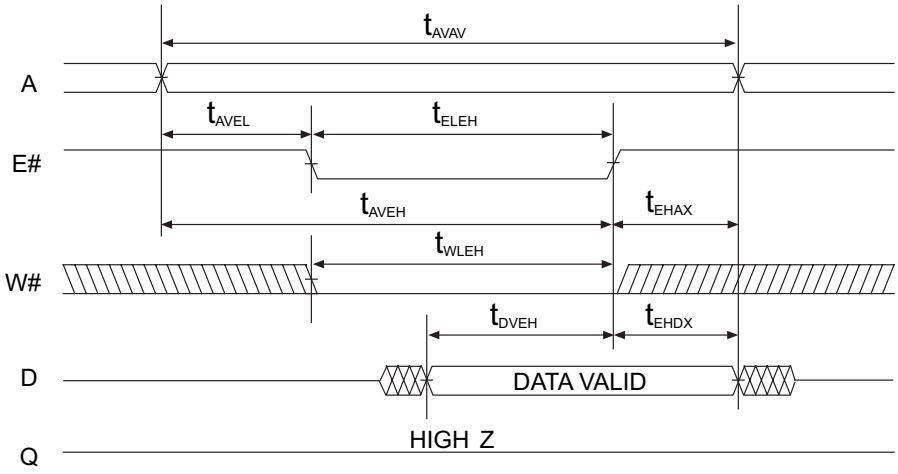
Parameter	Symbol		10ns		12ns		15ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	10		12		15		ns
Chip Enable to End of Write	t_{ELWH} t_{ELEH}	t_{CW} t_{CW}	8 8		9 9		9 9		ns ns
Address Setup Time	t_{AVWL} t_{AVEL}	t_{AS} t_{AS}	0 0		0 0		0 0		ns ns
Address Valid to End of Write	t_{AVWH} t_{AVEH}	t_{AW} t_{AW}	8 8		9 9		10 10		ns ns
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	8 8		10 10		11 11		ns ns
Write Recovery Time	t_{WHAX} t_{EHAX}	t_{WR} t_{WR}	0 0		0 0		0 0		ns ns
Data Hold Time	t_{WHDX} t_{EHDX}	t_{DH} t_{DH}	0 0		0 0		0 0		ns ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	5	0	6	0	7	ns
Data to Write Time	t_{DVWH} t_{DVEH}	t_{DW} t_{DW}	6 6		6 6		7 7		ns ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

WRITE CYCLE – W# CONTROLLED

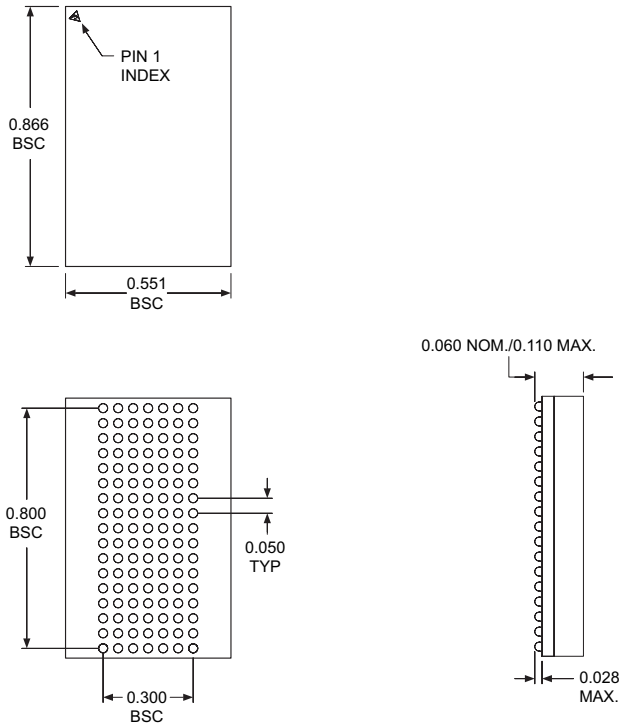


WRITE CYCLE 2 – E# CONTROLLED



PACKAGE DESCRIPTION

Package No. 391
119 Lead BGA
JEDEC MO-163



ORDERING INFORMATION

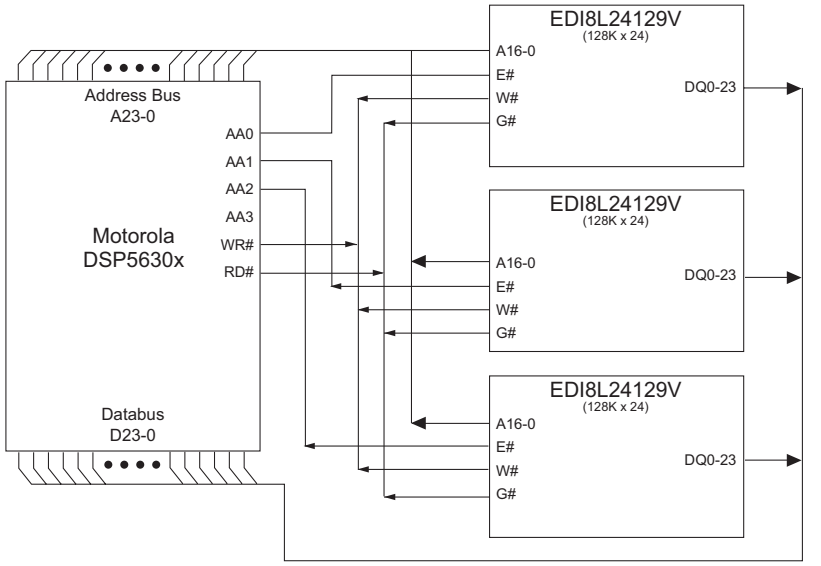
Commercial (0°C to +70°C)

Part Number	Speed (ns)	Package No.
EDI8L24129V10BC	10	391
EDI8L24129V12BC	12	391
EDI8L24129V15BC	15	391

Industrial (-40°C to +85°C)

Part Number	Speed (ns)	Package No.
EDI8L24129V10BI	10	391
EDI8L24129V12BI	12	391
EDI8L24129V15BI	15	391

FIGURE 3 – INTERFACING THE MOTOROLA DSP5630X DSP FAMILY WITH THE EDI8L24129V (128KX24)



NOTES:

1. In this example three 128K x 24 external memory arrays are shown, one for X data, one for Y data and one for Program. Specific applications may require one, two or all three arrays.
2. Any combination of AA0-AA3 may be used as chip selects. However, each chip select may only be used to select one memory array.

FIGURE 4 – INTERFACING THE 21060L OR THE 21062L TO THE EDI8L24129V, 119 BGA (CREATING A 128KX48 MEMORY ARRAY)