

**PRELIMINARY**  
 Note : This is not a final specification  
 Some parametric limits are subject to change

MITSUBISHI LSIs

# M5M51R16AWG -10LI, -12LI, -15LI, -10HI, -12HI, -15HI

1048576-BIT(65536-WORD BY 16-BIT)CMOS STATIC RAM

## DESCRIPTION

The M5M51R16AWG is a 1048576-bit CMOS static RAM organized as 65536 words by 16-bits, which are fabricated using high-performance CMOS technology. The use of CMOS cells and periphery results in a high density and low power static RAM.

The M5M51R16AWG can achieve low stand-by current and low operation current and ideal for the battery back-up application.

The M5M51R16AWG is packaged in a 48-pin chip scale package which is a high reliability and high density surface mount device (SMD). Using this type of devices, it becomes very easy to design a small system.

The M5M51R16AWG is fully compatible with the M5M51R16WG.

## FEATURE

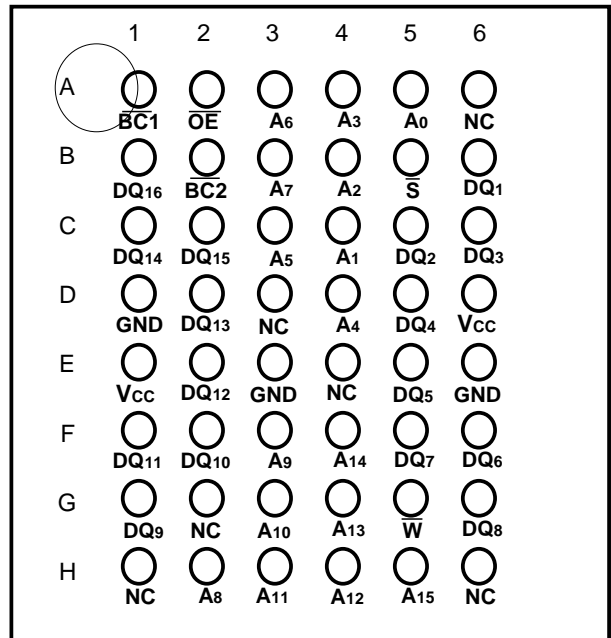
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51R16AWG- 10LI M5M51R16AWG- 12LI M5M51R16AWG- 15LI	100ns 120ns 150ns	10mA (1MHz)	4μA
M5M51R16AWG- 10HI M5M51R16AWG- 12HI M5M51R16AWG- 15HI	100ns 120ns 150ns		2μA

- Single +1.8V~2.7V power supply
- Low power down current 0.05μA(typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by  $\overline{S}$ ,  $\overline{BC1}$  and  $\overline{BC2}$
- Data hold on +1.0V power supply
- Three-state outputs : OR-tie capability
- $\overline{OE}$  prevents data contention in the I/O bus
- Common data I/O
- Separate control of lower and upper bytes by  $\overline{BC1}$  and  $\overline{BC2}$
- Package
  - 48-pin chip scale package(CSP)
  - Ball pitch : 0.75mm
  - Package size: 7.0mm x 8.5mm

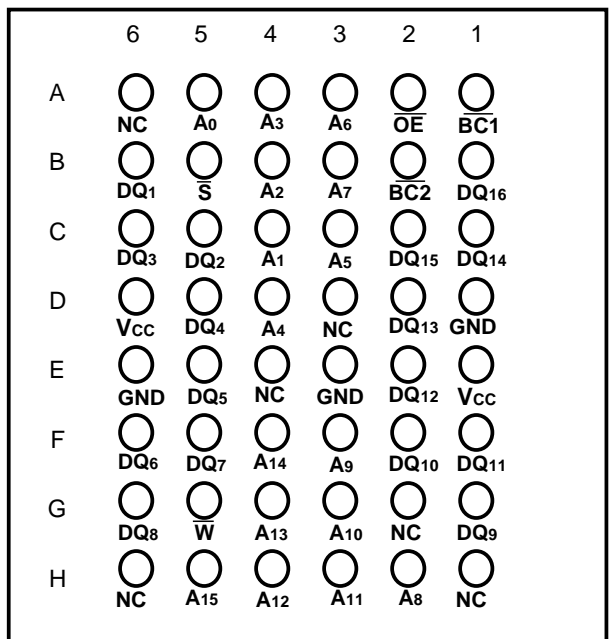
## APPLICATION

Small capacity memory units.

## PIN CONFIGURATION (TOP VIEW)



## PIN CONFIGURATION (BOTTOM VIEW)



Outline 48FJA

NC : NO CONNECTION

**FUNCTION**

The operation mode of the M5M51R16A series are determined by a combination of the device control inputs  $\bar{S}$ ,  $\bar{W}$ ,  $\bar{OE}$ ,  $\bar{BC1}$  and  $\bar{BC2}$ . Each mode is summarized in the function table.

A write cycle is executed whenever the low level  $\bar{W}$  overlaps with the low level  $\bar{BC1}$  and/or  $\bar{BC2}$  and the low level  $\bar{S}$ . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of  $\bar{W}$ ,  $\bar{BC1}$ ,  $\bar{BC2}$  or  $\bar{S}$ , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input  $\bar{OE}$  directly controls the output stage. Setting the  $\bar{OE}$  at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting  $\bar{W}$  at a high level and  $\bar{OE}$  at a low level while  $\bar{BC1}$  and/or  $\bar{BC2}$  and  $\bar{S}$  are in an active state. ( $\bar{BC1}$  and/or  $\bar{BC2}=L$ ,  $\bar{S}=L$ )

When setting  $\bar{BC1}$  at a high level and the other pins are in an active state, upper-Byte are in a selectable mode in which both reading and writing are enabled, and lower -Byte are in a non-selectable mode. And when setting  $\bar{BC2}$  at a high level and the other pins are in an active state, lower-Byte are in a selectable mode in which both reading and writing are enabled, and upper -Byte are in a non-selectable mode.

When setting  $\bar{BC1}$  and  $\bar{BC2}$  at a high level or  $\bar{S}$  at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled.

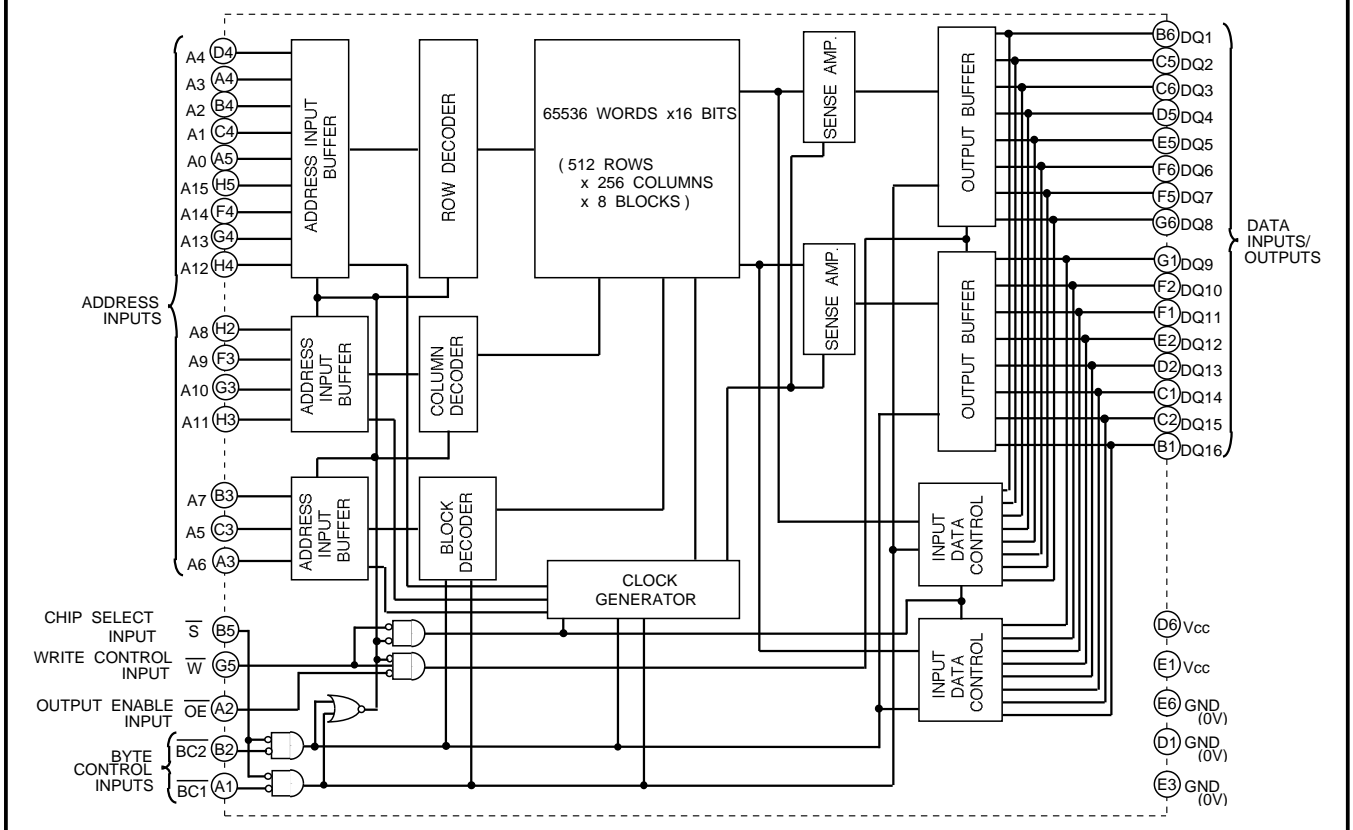
In this mode, the output stage is in a high-impedance state, allowing  $\bar{OR}$ -tie with other chips and memory expansion by  $\bar{BC1}$ ,  $\bar{BC2}$  and  $\bar{S}$ .  $\bar{S}$ ,  $\bar{BC1}$  and  $\bar{BC2}$  control the power down feature. When  $\bar{S}$ ,  $\bar{BC1}$  and  $\bar{BC2}$  go high, the power supply current is reduced as low as the stand-by current which is specified as  $I_{cc3}$  or  $I_{cc4}$ , and the memory data can be held at +1.0V power supply, enabling battery back-up operation during power-failure or power-down operation in the non-selected mode.

**FUNCTION TABLE**

$\bar{S}$	$\bar{W}$	$\bar{OE}$	$\bar{BC1}$	$\bar{BC2}$	Mode	DQ1~8	DQ9~16	Icc
L	H	L	L	L	Word Read	Dout	Dout	Active
L	H	L	H	L	Upper-Byte Read (Lower-Byte Non selection)	High-Z	Dout	Active
L	H	L	L	H	Lower-Byte Read (Upper-Byte Non selection)	Dout	High-Z	Active
L	L	X	L	L	Word Write	Din	Din	Active
L	L	X	H	L	Upper-Byte Write (Lower-Byte Non selection)	High-Z	Din	Active
L	L	X	L	H	Lower-Byte Write (Upper-Byte Non selection)	Din	High-Z	Active
L	H	H	X	X	Output disable	High-Z	High-Z	Active
X	X	X	H	H	Non selection	High-Z	High-Z	Stand-by
H	X	X	X	X	Non selection	High-Z	High-Z	Stand-by

(High-Z=High-impedance)

**BLOCK DIAGRAM**



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**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>cc</sub>	Supply voltage	With respect to GND	-0.2 ~ 4.6	V
V <sub>i</sub>	Input voltage		-0.2* ~ V <sub>cc</sub> +0.2(max.4.6V)	V
V <sub>o</sub>	Output voltage		0 ~ V <sub>cc</sub>	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> =25°C	1	W
T <sub>opr</sub>	Operating temperature		-40 ~ 85	°C
T <sub>stg</sub>	Storage temperature		-65 ~ 150	°C

\* -1.0V in case of AC ( Pulse width 30ns )

**DC ELECTRICAL CHARACTERISTICS** ( T<sub>a</sub> = - 40~85°C, V<sub>cc</sub> = 1.8V~2.7V, unless otherwise noted )

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V <sub>IH</sub>	High-level input voltage		0.7 x V <sub>cc</sub>		V <sub>cc</sub> +0.2V	V
V <sub>IL</sub>	Low-level input voltage		-0.2*		0.4	V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -0.1mA	1.6			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 0.1mA			0.2	V
I <sub>i</sub>	Input current	V <sub>i</sub> = 0 ~ V <sub>cc</sub>			±1	µA
I <sub>o</sub>	Output current in off-state	$\overline{BC1}$ and $\overline{BC2}$ = V <sub>IH</sub> or $\overline{S}$ = V <sub>IH</sub> or OE = V <sub>IH</sub> , V <sub>I/O</sub> = 0~ V <sub>cc</sub>			±1	µA
I <sub>cc1W</sub>	Word operation(16bit) Active supply current (AC,TTL level)	$\overline{BC1}$ and $\overline{BC2}$ = V <sub>IL</sub> , $\overline{S}$ = V <sub>IL</sub> other inputs = V <sub>IH</sub> or V <sub>IL</sub> Output-open(duty 100%)	Min cycle	15	25	mA
I <sub>cc2W</sub>			1MHz	7	10	mA
I <sub>cc1B</sub>	Byte operation(8bit) Active supply current (AC,TTL level)	( $\overline{BC1}$ = V <sub>IH</sub> and $\overline{BC2}$ = V <sub>IL</sub> ) or ( $\overline{BC1}$ = V <sub>IL</sub> and $\overline{BC2}$ = V <sub>IH</sub> ), $\overline{S}$ = V <sub>IL</sub> , other inputs = V <sub>IH</sub> or V <sub>IL</sub> Output-open(duty 100%)	Min cycle	10	15	mA
I <sub>cc2B</sub>			1MHz	5	8	mA
I <sub>cc3</sub>	Stand-by current	1) $\overline{S}$ V <sub>cc</sub> -0.2V, other inputs = 0~V <sub>cc</sub> 2) $\overline{BC1}$ and $\overline{BC2}$ V <sub>cc</sub> -0.2V, $\overline{S}$ 0.2V, other inputs = 0~V <sub>cc</sub>	-LI		4	µA
			-HI		2	µA
I <sub>cc4</sub>	Stand-by current	$\overline{BC1}$ and $\overline{BC2}$ = V <sub>IH</sub> or $\overline{S}$ = V <sub>IH</sub> , other inputs = 0~V <sub>cc</sub>			0.3	mA

\* -1.0V in case of AC ( Pulse width 30ns )

**CAPACITANCE** ( T<sub>a</sub> = - 40 ~85°C, V<sub>cc</sub> = 1.8V~2.7V, unless otherwise noted )

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
C <sub>i</sub>	Input capacitance	V <sub>i</sub> =GND, V <sub>i</sub> =25mVrms, f=1MHz			6	pF
C <sub>o</sub>	Output capacitance	V <sub>o</sub> =GND, V <sub>o</sub> =25mVrms, f=1MHz			10	pF

Note 1: Direction for current flowing into an IC is positive (no mark).

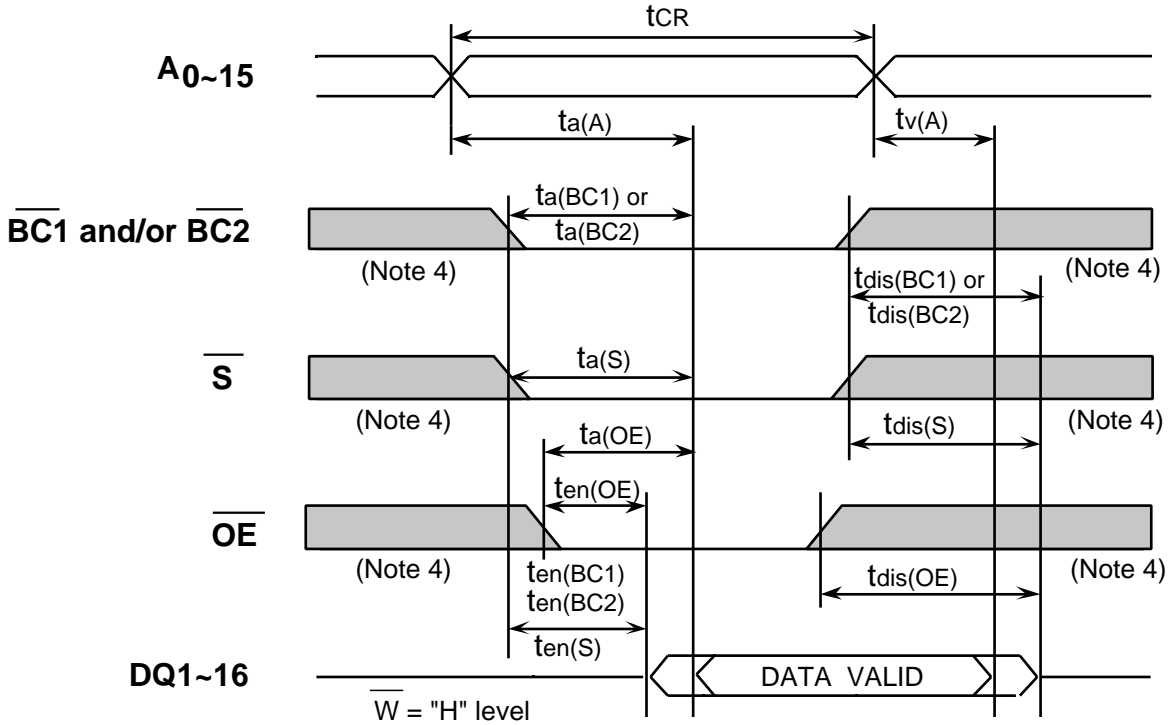
Note 2: Typical value is V<sub>cc</sub> = 2.0V, T<sub>a</sub> = 25°C

Note 3: C<sub>i</sub>,C<sub>o</sub> are periodically sampled and are not 100% tested.

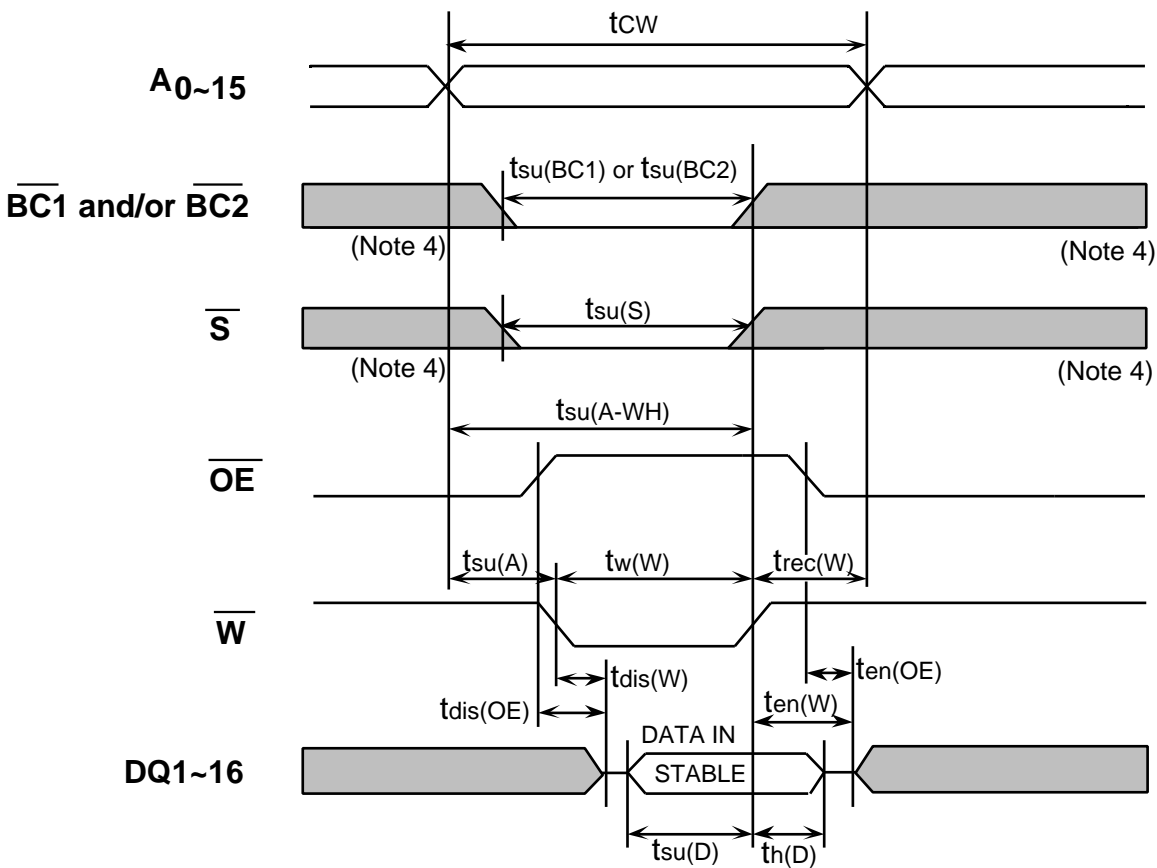


**(4) TIMING DIAGRAMS**

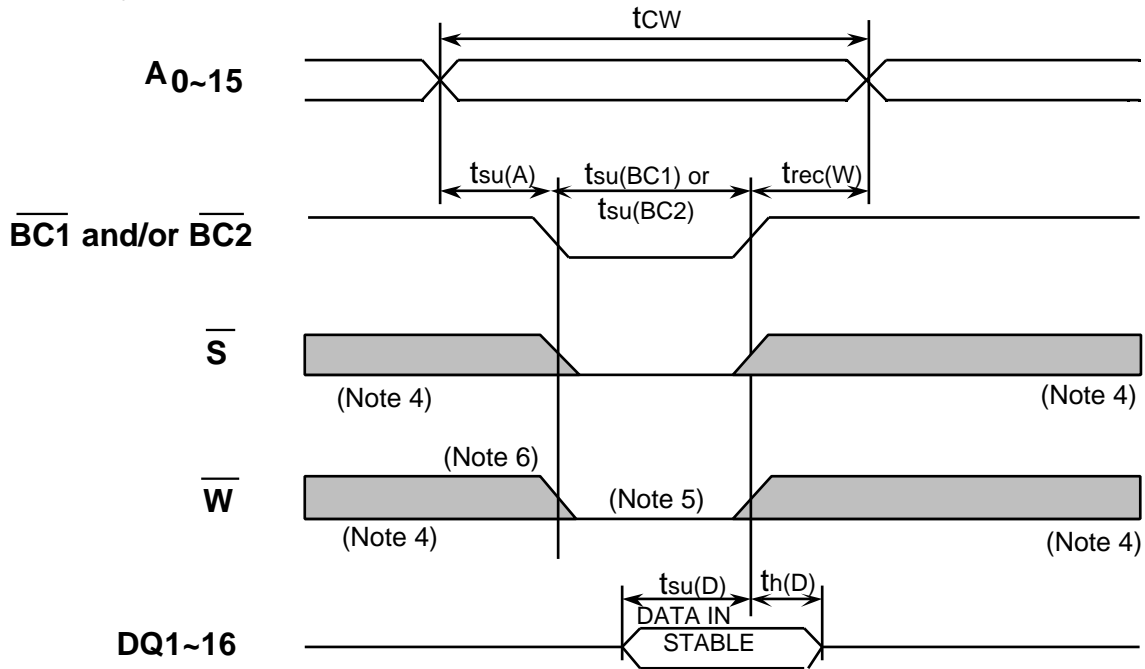
**Read cycle**



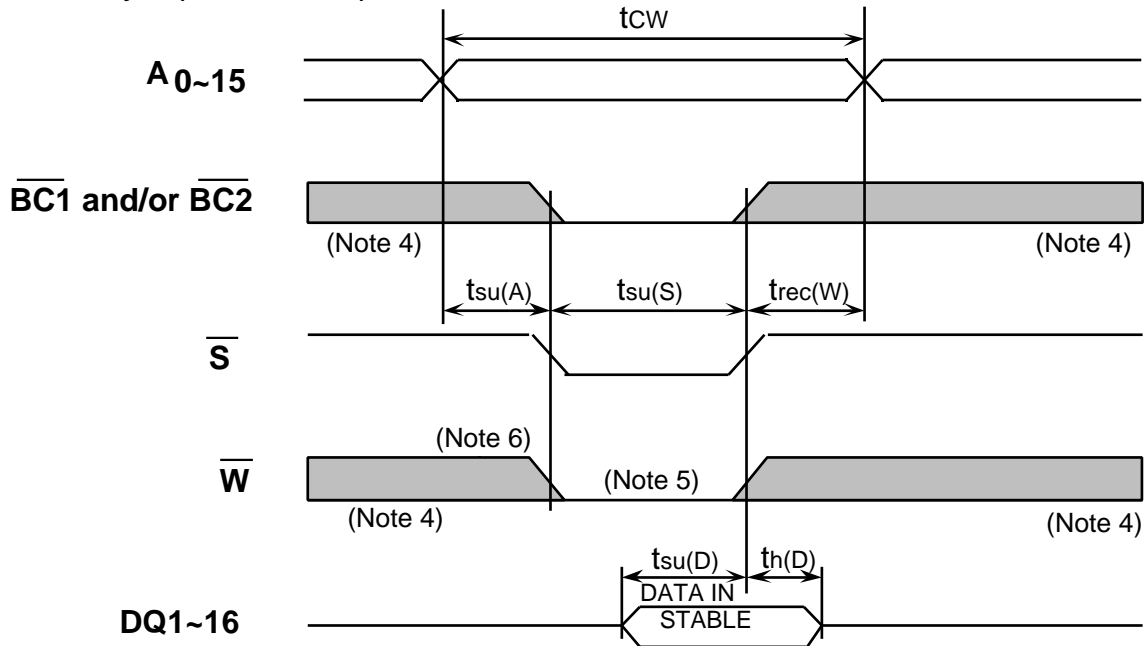
**Write cycle ( $\overline{W}$  control mode)**



**Write cycle ( $\overline{BC1}$ ,  $\overline{BC2}$  control mode)**



**Write cycle ( $\overline{S}$  control mode)**



Note 4: Hatching indicates the state is "don't care".

Note 5: Writing is executed while  $\overline{S}$  low overlaps  $\overline{BC1}$  and/or  $\overline{BC2}$  low and  $\overline{W}$  low.

Note 6: When the falling edge of  $\overline{W}$  is simultaneously or prior to the falling edge of  $\overline{BC1}$  and/or  $\overline{BC2}$  or falling edge of  $\overline{S}$ , the outputs are maintained in the high impedance state.

Note 7: Don't apply inverted phase signal externally when DQ pin is output mode.

Note 8:  $t_{en}$ ,  $t_{dis}$  are periodically sampled and are not 100% tested.

Note 9:  $t_{CR}$  (Read cycle time) is defined as whole time from reading address set up to this address change under read mode set condition by  $\overline{S}$ ,  $\overline{W}$ ,  $\overline{OE}$ ,  $\overline{BC1}$  and/or  $\overline{BC2}$ .

Note 10:  $t_{CW}$  (Write cycle time) is defined as whole time from writing address set up to this address change under write mode set condition by  $\overline{S}$ ,  $\overline{W}$ ,  $\overline{BC1}$  and/or  $\overline{BC2}$ .

**POWER DOWN CHARACTERISTICS**

**(1) ELECTRICAL CHARACTERISTICS** (Ta = - 40~85°C, unless otherwise noted )

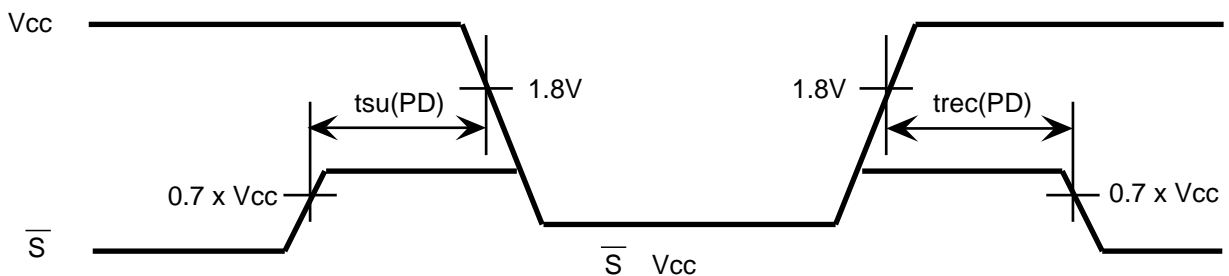
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V <sub>cc(PD)</sub>	Power down supply voltage		1.0			V
V <sub>I(S)</sub>	Chip select input $\bar{S}$	1.8V V <sub>cc(PD)</sub>	0.7 x V <sub>cc</sub>			V
		1.0V V <sub>cc(PD)</sub> 1.8V		V <sub>cc(PD)</sub>		
V <sub>I(BC)</sub>	Byte control inputs $\bar{BC}1$ and $\bar{BC}2$	1.8V V <sub>cc(PD)</sub>	0.7 x V <sub>cc</sub>			V
		1.0V V <sub>cc(PD)</sub> 1.8V		V <sub>cc(PD)</sub>		
I <sub>cc(PD)</sub>	Power down supply current	V <sub>cc</sub> = 2.0V 1) $\bar{S}$ V <sub>cc</sub> - 0.2V other inputs = 0~V <sub>cc</sub>	-LI		2	μA
		2) $\bar{BC}1$ and $\bar{BC}2$ V <sub>cc</sub> - 0.2V $\bar{S}$ 0.2V, other inputs = 0~V <sub>cc</sub>	-HI	0.05	1	

**(2) TIMING REQUIREMENTS** (Ta = - 40 ~85°C, unless otherwise noted )

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
tsu(PD)	Power down set up time		0			ns
trec(PD)	Power down recovery time		5			ms

**(3) POWER DOWN CHARACTERISTICS**

**$\bar{S}$  control mode**



**$\bar{BC}1$  and  $\bar{BC}2$  control mode**

