100BASE-X Fiber Physical Layer With 5-bit Interface

GENERAL DESCRIPTION

The ML6695 implements the physical layer of the Fast Ethernet 100BASE-X standard for fiber media. The device provides the 5-bit (or symbol) interface for interface to upper-layer silicon. The ML6695 integrates the data quantizer and the LED driver, allowing the use of low cost optical PMD components.

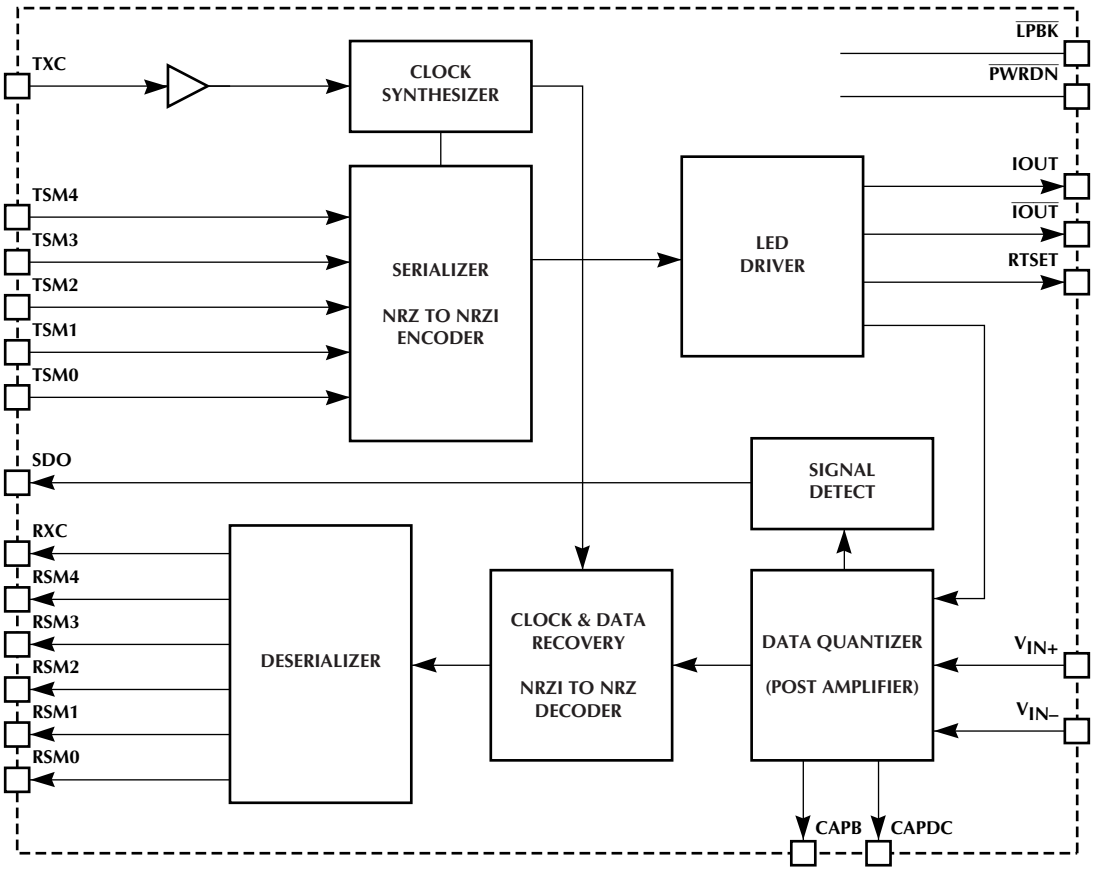
The ML6695 includes 125MHz clock recovery/clock generation, an LED driver, and a data quantizer (post amplifier). The device also offers a power down mode which results in total power consumption of less than 20mA.

The ML6695 is suitable for the current 100BASE-FX IEEE 803.2u standard defined using 1300nm optics, as well as for the *proposed* 100BASE-SX standard defined using lower cost 820nm optics.

FEATURES

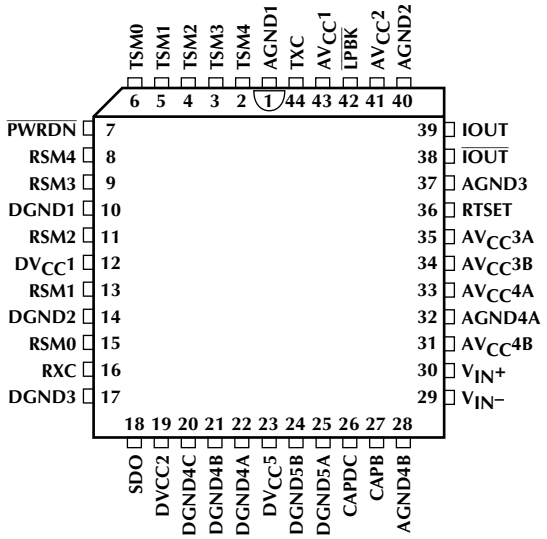
- 100BASE-FX physical layer with 5-bit interface
- Optimal 100BASE-SX solution (draft standard)
- Integrated data quantizer (post-amplifier)
- Integrated LED driver
- 125MHz clock generation and recovery
- Power-down mode

BLOCK DIAGRAM



PIN CONFIGURATION

ML6695
44-Pin PLCC (Q44)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	$A_{GND}1$	Analog ground
2	TSM4	Transmit data TTL inputs. TSM 0-4 inputs accept TX data symbols from the MII. Data appearing at TSM 0-4 are clocked into the ML6695 on the rising edge of TXCLK .
3	TSM3	Transmit data TTL inputs. TSM 0-4 inputs accept TX data symbols from the MII. Data appearing at TSM 0-4 are clocked into the ML6695 on the rising edge of TXC.
4	TSM2	Transmit data TTL inputs. TSM 0-4 inputs accept TX data symbols from the MII. Data appearing at TSM 0-4 are clocked into the ML6695 on the rising edge of TXC.
5	TSM1	Transmit data TTL inputs. TSM 0-4 inputs accept TX data symbols from the MII. Data appearing at TSM 0-4 are clocked into the ML6695 on the rising edge of TXC.
6	TSM0	Transmit data TTL inputs. TSM 0-4 inputs accept TX data symbols from the MII. Data appearing at TSM 0-4 are clocked into the ML6695 on the rising edge of TXC.
7	$\overline{PWRDN}$	Powerdown TTL input. Driving this pin low, or floating the pin, powers the ML6695 down to a low-current, inoperative state. Driving $\overline{PWRDN}$ high enables the ML6695.
8	RSM4	Receive data TTL outputs. RSM 0-4 output may be sampled synchronously with RXC's rising edge.

PIN DESCRIPTION (Continued)

PIN	NAME	FUNCTION
9	RSM3	Receive data TTL outputs. RSM 0-4 output may be sampled synchronously with RXC's rising edge.
10	DGND1	Digital ground
11	RSM2	Receive data TTL outputs. RSM 0-4 output may be sampled synchronously with RXC's rising edge.
12	$DV_{CC}1$	Digital positive power supply
13	RSM1	Receive data TTL outputs. RSM 0-4 output may be sampled synchronously with RXC's rising edge.
14	DGND2	Digital ground
15	RSM0	Receive data TTL outputs. RSM 0-4 output may be sampled synchronously with RXC's rising edge.
16	RXC	Recovered receive symbol clock TTL output. This 25MHz clock is phase-aligned with the internal 125MHz bit clock recovered from the signal received at $V_{IN+/-}$. Receive data are clocked out at RSM 0-4 on the falling edges of this clock.
17	DGND3	Digital ground
18	SDO	Signal Detect TTL output. This output goes high when the signal at VIN+/- exceeds the preset amplitude threshold.
19	$DV_{CC}2$	Digital positive power supply
20	DGND4C	Digital ground
21	DGND4B	Digital ground
22	DGND4	Digital ground
23	$DV_{CC}5$	Digital positive power supply
24	DGND5B	Digital ground
25	DGND5A	Digital ground
26	CAPDC	Data quantizer offset-correction loop, offset-storage capacitor input pin. The capacitor tied between this pin and AV_{CC} stores the amplified data quantizer offset voltage and also sets the dominant pole in the offset-correction loop. A 0.1µF surface mount is recommended.
27	CAPB	Data quantizer input bias bypass capacitor input. The capacitor tied between this pin and AV_{CC} filters the quantizer's internal input bias reference. A 0.1µF surface-mount capacitor is recommended.
28	AGND4B	Analog ground
29	$V_{IN}-$	Receive quantizer input. This differential input pair receives 100BASE-FX NRZI signals from the network opto-coupler.
30	$V_{IN}+$	Receive quantizer input. This differential input pair receives 100BASE-FX NRZI signals from the network opto-coupler.
31	$AV_{CC}4B$	Analog positive power supply
32	AGND4A	Analog ground
33	$AV_{CC}4A$	Analog positive power supply
34	$AV_{CC}3B$	Analog positive power supply
35	$AV_{CC}3A$	Analog positive power supply
36	RTSET	Transmit level bias resistor. For 100BASE-FX, an external 2.32kΩ, 1% resistor connected between RTSET and AGND3 sets a precision constant bias current that gives a nominal output "on" current of 75mA at I_{OUT}.
37	AGND3	Analog ground
38	$\overline{IOUT}$	Transmit LED output. This pin connects through an external 15Ω resistor to AV_{CC} when the part is used to drive a network LED.

PIN DESCRIPTION (Continued)

PIN	NAME	FUNCTION
39	IOUT	Transmit LED output. This open-collector current output drives NRZI waveforms into an LED. Output current can be set externally by choosing RTSET value.
40	AGND2	Analog ground
41	$AV_{CC}2$	Analog positive power supply
42	$\overline{LPBK}$	Loopback TTL input pin. Tying this pin to ground places the part in loopback mode; data at TSM0 0-4 are serialized, then sent to the quantizer, followed by the receive PLL for clock recovery, and finally to the RSM<4:07> outputs. Floating this pin or tying it to V_{CC} places the part in its normal mode of operation.
43	$AV_{CC}1$	Analog positive power supply
44	TXC	Transmit clock TTL input. This 25MHz clock is phase-aligned with the internal 125MHz TX bit clock. Data appearing at Tsm<4:0> are clocked into the ML6695 on the rising edge of this clock.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} Supply Voltage Range ..... –0.3V to 6V
Input Voltage Range
  Digital Inputs ..... –0.3V to V_{CC}
  VIN+, VIN-,TXC, CAPDC, CAPB ..... –0.3V to V_{CC}
Output Current
  IOUT, $\overline{IOUT}$ 90mA
  All Other Outputs 10mA

Junction Temperature ..... 0ºC to 125ºC
Storage Temperature ..... –65ºC to 150ºC
Lead Temperature (Soldering, 10 sec) 260ºC
Thermal Resistance (θ_{JA})
  PLCC ..... 53°C/W

OPERATING CONDITIONS

Temperature Range ..... 0ºC to 70ºC
V_{CC} Supply Voltage ..... 5V ±5%
  All V_{CC} supply pins *must* be within 0.1V of each other.
  All GND pins *must* be within 0.1V of each other.

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC} = 5V ±5%, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TTL INPUTS (TSM<4:0>, $\overline{LPBK}$, TXC, $\overline{PWRDN}$)						
V_{IL}	Input Low Voltage	I_{IL} = –400µA	–0.3		0.8	V
V_{IH}	Input High Voltage	I_{IH} = 100µA	2.0		V_{CC}+0.3	V
I_{IL}	Input Low Current	V_{IN} = 0.4V	–200			µA
I_{IH}	Input High Current	V_{IN} = 2.4V			100	µA
TTL OUTPUTS (RSM<4:0>, RXC, SDO)						
V_{OL}	Output Low Voltage	I_{OL} = 4mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4			
RECEIVER						
V_{ICM}	V_{IN}+/- input common-mode voltage	V_{CC} = 5V		2.5		$\bar{V}$
V_{ID}	V_{IN}+/- differential input voltage range		3.5		1700	mV_{P-P}
R_{IDR}	V_{IN}+/- differential input resistance		500		1k	Ω
V_{SDA}	Signal detect assertion threshold	peak-to-peak non-idle signal level at V_{IN}+/- for SDO assertion	8		12	mV_{P-P}
A_{HYST}	Input hysteresis		1.5		2	dB
I_{RT}	RTSET input current	RTSET = 2.32kΩ ±1%	486	540	594	µA
TRANSMITTER						
I_{LEDH}	I_{OUT} high output current (Note 2)	RTSET = 2.32kΩ ±1%	67.5	75	82.5	mA
I_{LEDL}	I_{OUT}/I_{OUT} low output current	RTSET = 2.32kΩ ±1%			0.1	mA
POWER SUPPLY CURRENT						
I_{CC}	Supply Current, 100BASE-FX operation, transmitting	Current into all V_{CC} pins, V_{CC} = 5.25V		200	295	mA
I_{PD}	Supply Current, Powerdown Mode				20	mA

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC} = 5V ±5%, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER (NOTE 8)						
$t_{TR/F}$	I_{OUT} rise/fall time	Note 3			2	ns
t_{TDC}	I_{OUT} output duty cycle distortion	Note 3	-0.5		0.5	ns
SIGNAL DETECT						
t_{AS}	SDO assert time (SDO low to high)	VIN>8mV_{P-P}			100	µs
t_{ANS}	SDO deassert time (SDO high to low)	VIN<8mV_{P-P}	350			µs
DATA INTERFACE						
X_{NTOL}	TX input clock frequency tolerance	25MHz frequency	–50		50	ppm
t_{TPWH}	TXC pulse width HIGH		14		ns	
t_{TPWL}	TXC pulse width LOW		14		ns	
t_{RPWH}	RXC pulse width HIGH		14		ns	
t_{RPWL}	RXC pulse width LOW		14		ns	
t_{TPS}	Setup time, TSM 0-4 data valid to TXC rising edge (1.4V point)		13			ns
t_{TPH}	Hold time, TSM 0-4 data valid after TXC rising edge (1.4V point)		3			ns
t_{RCS}	Time that RSM0-4 data are valid before RXC falling edge (1.4V point)		10			ns
t_{RCH}	Time that RSM0-4 data are valid after RXC falling edge (1.4V point)		10			ns
t_{RPCR}	RXC 10%-90% rise time				6	ns
t_{RPCF}	RXC 90%-10% fall time				6	ns

Note 1. Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

Note 2. Output current amplitude is I_{OUT} = 207V/RTSET.

Note 3. Using the test load shown in Figure 1, transmitting "H" symbols.

FUNCTIONAL DESCRIPTION

TRANSMIT SECTION

The ML6695 transmit section accepts parallel NRZ data nibbles, creates a serial NRZI data stream using the internal 125MHz clock multiplier, and provides an open-collector output IOUT to directly drive an LED. $\overline{IOUT}$ must be connected to V_{CC} through a 15Ω resistor. The internal clock multiplier accepts an external 25MHz clock input.

The LED driver at IOUT is a current mode switch which develops the output light by sinking current through the network LED into IOUT. RTSET'S value determines the output current:

$$RTSET = \left(\frac{1.25V}{IOUT}\right) \times 140\Omega \qquad (1)$$

where IOUT is the desired output current.

RECEIVE SECTION

The ML6695 receive section includes a fiber optic quantizer and a 125MHz receive clock recovery circuit. The quantizer is a wide-bandwidth limiting amplifier with DC offset correction. The quantizer output drives a data comparator with a controlled slicing threshold. The comparator provides a large-amplitude receive signal. The clock recovery circuit extracts 125MHz receive clock from the large-amplitude signal, and provides the clock for the parallel data output registers. Received NRZ data nibbles appear at the RSM outputs synchronously with RXC falling edges. Received signals exceeding the preset signal detect amplitude threshold for more than 5µs cause the SDO output to go high. Received signals that fall below the preset threshold for more than 5µs cause SDO to go low.

OTHER MODES

The ML6695 will enter a power down mode when the $\overline{PWRDN}$ pin is tied low. In this state the ML6695 powers down to a low-current (less than 20mA), inoperative state. Driving it high enables normal operation of the ML6695.

Loopback mode is entered when the $\overline{LPBK}$ is tied to ground. In this mode, the data at TSM0-4 are serialized, then sent to the quantizer, followed by the receive PLL for clock recovery, and finally to the RSM0-4 outputs. Tying $\overline{LPBK}$ to V_{CC} places the ML6695 in its normal mode of operation.

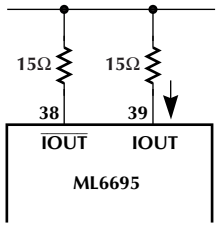
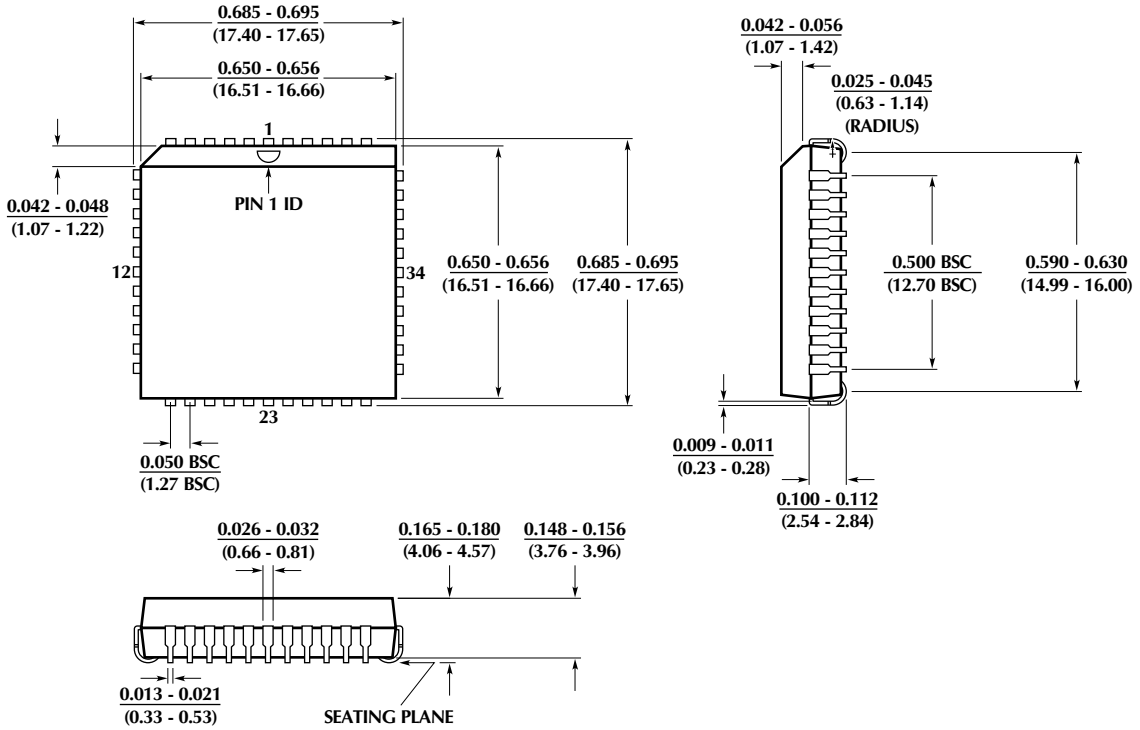


Figure 1. Test Load

PHYSICAL DIMENSIONS inches (millimeters)

Package: Q44
44-Pin PLCC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6695CQ	0°C to 70°C	44-Pin PLCC (Q44)

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