MN673794

1. Overview

This IC is used to process a variety of items including the following ones: NTSC/PAL signal (Y/C and composite video) I/O, 3D Y/C separation, TBC, DD conversion, frame sync, sync/clock generation, Rec 656 I/O.

■ Features

- Analog input block
  Composite video/Component Y input (10 bits at 27.0 MHz)
  Component C input (10 bits at 27.0 MHz)

- Analog control block
  AGC (Auto Gain Control), clamp control, ACC (Auto Color Control)

- Digital I/O block
  Digital video I/O (ITU-R Rec 656: Y/Cr/Cb multiple, 8 bits at 27 MHz)
  Digital video input clock must be synchronized with the system clock of 27 MHz.

- Signal processing block
  3D Y/C separation (image movement adaptive processing: NTSC), 2D Y/C separation (PAL)
  TBC (Time Base Corrector) processing (velocity error correction/jitter correction)
  Frame sync processing (See Note.)
  NR processing (Y/C recursive NR)
  Y/C separation is performed only in two dimensions (due to memory sharing) when the NR function is in use.

- Copyright VBLK detection
  Macrovision (AGC pulse and color stripe) detection
  VBID detection
  Closed caption detection
  WSS detection

Note: This IC uses a 27-MHz fixed clock. Therefore, input signals into the IC are not synchronized with output signals from the IC. Therefore, a frame-skip or frame-hold occurs to standard and nonstandard signals, the frequency of occurrence of which varies with the difference in frame frequency between input signals and the 27-MHz fixed clock.
If the user does not want the occurrence of any frame-skip or frame-hold to standard signals, externally generate 27-MHz clock pulses synchronized with the frames of the input signals, and input the clock pulses into the IC.
A frame-skip refers to loss of the image in a single frame.
A frame-hold refers to the duplicated output of the image in the previous frame. *1

2. Specifications

2.1 Electrical Characteristics

(1) Processor
0.25-µm, four-layer aluminum DRAM-embedded processor

(2) Maximum operating frequency
27.0 MHz

(3) Operating supply voltage
3.0 V to 3.6 V (Analog power supply)
3.0 V to 3.6 V (Digital I/O power supply 1)
1.65 V to 1.95 V (Internal digital power supply)
2.3 V to 2.7 V (Internal DRAM power supply)

(4) Ambient temperature
-20°C to +80°C

(5) Package
208-pin QFP with 28-mm square (0.5-mm pitch)
(Package code No. LQFP208-P-2828)

2.2 Pin Descriptions

Table 2.2 shows the explanation of the pins of the IC.

Table 2.2 Pin Descriptions (1/4)

Pin No.	Pin name	I/O	Voltage	Type	Drive	Function	Clock	BST
1	CLK18O2	O	3.3 V	CMOS	4 mA	Test output	-	-
2	VDD3	Power supply	3.3 V	-	-	Digital I/O (3.3 V) use	-	-
3	CLK45I	I		Crystal interface	-	Test input (VSS)	-	-
4	VSS	GND	-	-	-	Digital use	-	-
5	VDDI	Power supply	1.8 V	-	-	Internal digital use	-	-
6	DSF7	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (open or VSS)	-	YES
7	DSF6	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (open or VSS)	-	YES
8	VSS	GND	-	-	-	Digital use	-	-
9	DSF5	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (open or VSS)	-	YES
10	DSF4	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (open or VSS)	-	YES
11	VDD2	Power supply	3.3 V	-	-	Digital I/O (3.3 V) use	-	-
12	DSF3	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (open or VSS)	-	YES
13	DSF2	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (open or VSS)	-	YES
14	VSS	GND	-	-	-	Digital use	-	-
15	DSF1	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (open or VSS)	-	YES
16	DSF0	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (open or VSS)	-	YES
17	VDD2	Power supply	3.3 V	-	-	Digital I/O (3.3 V) use	-	-
18	CASHD	O	3.3 V	CMOS	2 mA	Test output	-	YES
19	CASVD	O	3.3 V	CMOS	2 mA	Test output	-	YES
20	VSS	GND	-	-	-	Digital use	-	-
21	CLK188	O	3.3 V	CMOS	2 mA	Clock	-	-
22	CLK450	O	3.3 V	CMOS	2 mA	Clock	-	-
23	VDD2	Power supply	3.3 V	-	-	Digital I/O (3.3 V) use	-	-
24	CLK18O1	O	3.3 V	CMOS	4 mA	Test output	-	-
25	VSS	GND	-	-	-	Digital use	-	-
26	AVSS1	GND	-	-	-	Analog use	-	-
27	TPLL	I/O	-	Analog	-	Test use	-	-
28	AVDD1	Power supply	3.3 V	-	-	Analog use	-	-
29	AVSS2	GND	3.3 V	-	-	Analog use	-	-
30	VREFCK	I	-	Analog	-	Test use (AVSS)	-	-
31	IREFCK	I	-	Analog	-	Test use (AVSS)	-	-
32	COMPCK	I	-	Analog	-	Test use (AVDD)	-	-
33	CK45O	O	-	Analog	-	Test output	-	-
34	AVDD2	Power supply	3.3 V	-	-	D/A (CLK) use	-	-
35	AVSS3	GND	3.3 V	-	-	Analog use	-	-
36	VREFC	I	-	Analog	-	Test use (AVSS)	-	-
37	IREFC	I	-	Analog	-	Test use (AVSS)	-	-
38	COMPC	I	-	Analog	-	Test use (AVDD)	-	-
39	TESTI	O	-	Analog	-	Test output	-	-
40	AVDD3	Power supply	3.3 V	-	-	Analog use	-	-
41	AVSS4	GND	-	-	-	Analog use	-	-
42	VREFY	I	-	Analog	-	Test use (AVSS)	-	-
43	IREFY	I	-	Analog	-	Test use (AVSS)	-	-
44	COMPY	I	-	Analog	-	Test use (AVDD)	-	-
45	TESTK	O	-	Analog	-	Test output	-	-
46	AVDD4	Power supply	3.3 V	-	-	Analog use	-	-
47	AGCO	O	-	Analog	-	AGC control output	1 MHz	-
48	AVSS5	GND	-	-	-	Voltage dividing resistor DAC (ACC, CLAMP, and AGC) use	-	-
49	CLPOS	O	-	Analog	-	Clamp control output (for sync tip clamp use)	1 MHz	-
50	VREFMA	I	-	Analog	-	Reference voltage input for voltage dividing resistor DAC use (Capacitance coupling to AVSS)	-	-
51	AVDD5	Power supply	3.3 V	-	-	Voltage dividing resistor DAC (ACC, CLAMP, and AGC) use	-	-
52	ACCO	O	-	Analog	-	ACC control output	1 MHz	-

Table 2.2 Pin Descriptions (2/4)

Pin No.	Pin name	I/O	Voltage	Type	Drive	Function	Clock	BST
53	AVDD6	Power supply	3.3 V	Analog	-	A/D (C) use	-	-
54	CIN	I	-	Analog	-	C input (analog)	27 MHz	-
55	AVSS6	GND	-	-	-	A/D (C) use	-	-
56	VREFLC	I	-	Analog	-	A/D (C) reference voltage low-level input	-	-
57	VREFMLC	I	-	Analog	-	A/D (C) intermediate reference potential input (Capacitance coupling to AVSS)	-	-
58	VREFMC	I	-	Analog	-	A/D (C) intermediate reference potential input (Capacitance coupling to AVSS)	-	-
59	VREFHMC	I	-	Analog	-	A/D (C) intermediate reference potential input (Capacitance coupling to AVSS)	-	-
60	VREFHC	I	-	Analog	-	A/D (C) reference voltage high-level input	-	-
61	AVSS7	GND	-	-	-	A/D (C) use	-	-
62	AVDD7	Power supply	3.3 V	Analog	-	A/D (C) use	-	-
63	AVDD8	Power supply	3.3 V	-	-	A/D (Y and composite) use	-	-
64	VIDEO	I	-	Analog	-	Composite video input (analog)	27 MHz	-
65	AVSS8	GND	-	-	-	A/D (Y and composite) use	-	-
66	VREFLY	I	-	Analog	-	A/D (Y and composite) reference voltage low-level input	-	-
67	VREFMLY	I	-	Analog	-	A/D (Y and composite) intermediate reference potential input (Capacitance coupling to AVSS)	-	-
68	VREFMY	I	-	Analog	-	A/D (Y and composite) intermediate reference potential input (Capacitance coupling to AVSS)	-	-
69	VREFHMY	I	-	Analog	-	A/D (Y and composite) intermediate reference potential input (Capacitance coupling to AVSS)	-	-
70	VREFHY	I	-	Analog	-	A/D (Y and composite) reference voltage high-level input	-	-
71	AVSS9	GND	-	-	-	A/D (Y and composite) use	-	-
72	AVDD9	Power supply	3.3 V	-	-	A/D (Y and composite) use	-	-
73	VSS	GND	-	-	-	Digital use	-	-
74	ANACLK	O	3.3 V	CMOS	2 mA	6.75-MHz output	-	-
75	VDD3	Power supply	3.3 V	-	-	Digital I/O (3.3 V) use	-	-
76	GCP	O	3.3 V	CMOS	2 mA	Clamp pulse (sync chip) output	27 MHz	-
77	TESTIO9	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (MSB) (open or VSS)	-	-
78	TESTIO8	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (open or VSS)	-	-
79	VSS	GND	-	-	-	Digital use	-	-
80	TESTIO7	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (open or VSS)	-	-
81	TESTIO6	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (open or VSS)	-	-
82	VDDI	Power supply	1.8 V	-	-	Internal digital use	-	-
83	TESTIO5	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (open or VSS)	-	-
84	TESTIO4	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (open or VSS)	-	-
85	VSS	GND	-	-	-	Digital use	-	-
86	VDDDRAM0	Power supply	2.5 V	-	-	DRAM (5 Mbits) use	-	-
87	VSSDRAM0	GND	-	-	-	Digital use	-	-
88	TESTIO3	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (open or VSS)	-	-
89	TESTIO2	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (open or VSS)	-	-
90	VDD3	Power supply	3.3 V	-	-	Digital I/O (3.3 V) use	-	-
91	TESTIO1	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (open or VSS)	-	-
92	TESTIO0	I/O	3.3 V	CMOS-100 kΩ PD	4 mA	Test I/O (LSB) (open or VSS)	-	-
93	VSS	GND	-	-	-	Digital use	-	-
94	TCK	I	3.3 V	CMOS-100 kΩ PD	-	Boundary scan clock input	-	-
95	TDO	O	3.3 V	3-state CMOS	2 mA	Boundary scan data output	-	-
96	VDDI	Power supply	1.8 V	-	-	Internal digital use	-	-
97	TDI	I	3.3 V	CMOS-100 kΩ PU	-	Boundary scan data input	-	-
98	TRST	I	3.3 V	CMOS-100 kΩ PU	-	Boundary scan reset input (VSS or RST when not used)	-	-
99	TMS	I	3.3 V	CMOS-100 kΩ PU	-	Boundary scan mode input	-	-
100	VSS	GND	-	-	-	Digital use	-	-
101	TEST5	I	3.3 V	CMOS-100 kΩ PD	-	Test mode (MSB) (open or VSS)	-	-
102	TEST4	I	3.3 V	CMOS-100 kΩ PD	-	Test mode (open or VSS)	-	-
103	TEST3	I	3.3 V	CMOS-100 kΩ PD	-	Test mode (open or VSS)	-	-
104	TEST2	I	3.3 V	CMOS-100 kΩ PD	-	Test mode (open or VSS)	-	-

When the boundary scan function is not used, set the TRST pin (pin 98) to reset input or VSS. *2

Table 2.2 Pin Descriptions (3/4)

Pin No.	Pin name	I/O	Voltage	Type	Drive	Function	Clock	BST
105	TEST1	I	3.3 V	CMOS-100 kΩ PD	-	Test mode (open or VSS)	-	-
106	TEST0	I	3.3 V	CMOS-100 kΩ PD	-	Test mode (LSB) (open or VSS)	-	-
107	VDDI	Power supply	1.8 V	-	-	Internal digital use	-	-
108	VSS	GND	-	-	-	Digital use	-	-
109	MINTC1	I	3.3 V	CMOS	-	Test input（VSS)	-	-
110	MINTIN1	I	3.3 V	CMOS	-	Test input（VSS)	-	-
111	MINTEST	I	3.3 V	CMOS-30 kΩ PD	-	Test input（open or VSS)	-	-
112	VDD3	Power supply	3.3 V	-	-	Digital I/O (3.3 V) use	-	-
113	PDRAM0	I	3.3 V	CMOS-100 kΩ PD	-	DRAM test input (open or VSS)	-	-
114	PDRAM1	I	3.3 V	CMOS-100 kΩ PD	-	DRAM test input (open or VSS)	-	-
115	VSSDRAM1	GND	-	-	-	Digital use	-	-
116	VDDDRAM1	Power supply	2.5 V	-	-	DRAM (5 Mbits) use	-	-
117	NTDRAM	I	3.3 V	CMOS-100 kΩ PD	-	DRAM test input (open or VSS)	-	-
118	VSS	GND	-	-	-	Digital use	-	-
119	VDDI	Power supply	1.8 V	-	-	Internal digital use	-	-
120	CLK27I	I	3.3 V	CMOS	-	27-MHz clock for Rec 656 input (VSS when not used)	27 MHz	-
121	VSS	GND	-	-	-	Digital use	-	-
122	R656IN7	I	3.3 V	CMOS-100 kΩ PD	-	Digital video (Rec 656) input (MSB) (open or VSS when not used)	27 MHz	YES
123	R656IN6	I	3.3 V	CMOS-100 kΩ PD	-	Digital video (Rec 656) input (open or VSS when not used)	27 MHz	YES
124	VDD3	Power supply	3.3 V	-	-	Digital I/O (3.3 V) use	-	-
125	R656IN5	I	3.3 V	CMOS-100 kΩ PD	-	Digital video (Rec 656) input (open or VSS when not used)	27 MHz	YES
126	R656IN4	I	3.3 V	CMOS-100 kΩ PD	-	Digital video (Rec 656) input (open or VSS when not used)	27 MHz	YES
127	VSS	GND	-	-	-	Digital use	-	-
128	VDDDRAM2	Power supply	2.5 V	-	-	DRAM (7 Mbits) use	-	-
129	VSSDRAM2	GND	-	-	-	Digital use	-	-
130	R656IN3	I	3.3 V	CMOS-100 kΩ PD	-	Digital video (Rec 656) input (open or VSS when not used)	27 MHz	YES
131	R656IN2	I	3.3 V	CMOS-100 kΩ PD	-	Digital video (Rec 656) input (open or VSS when not used)	27 MHz	YES
132	VDD3	Power supply	3.3 V	-	-	Digital I/O (3.3 V) use	-	-
133	R656IN1	I	3.3 V	CMOS-100 kΩ PD	-	Digital video (Rec 656) input (open or VSS when not used)	27 MHz	YES
134	R656IN0	I	3.3 V	CMOS-100 kΩ PD	-	Digital video (Rec 656) input (LSB) (open or VSS when not used)	27 MHz	YES
135	VSS	GND	-	-	-	Digital use	-	-
136	CLK27O	O	3.3 V	CMOS	4 mA	27-MHz clock output	27 MHz	-
137	VDDI	Power supply	1.8 V	-	-	Internal digital use	-	-
138	R656OUT7	O	3.3 V	CMOS	4 mA	Digital video (Rec 656) output (MSB)	27 MHz	YES
139	R656OUT6	O	3.3 V	CMOS	4 mA	Digital video (Rec 656) output	27 MHz	YES
140	VSS	GND	-	-	-	Digital use	-	-
141	R656OUT5	O	3.3 V	CMOS	4 mA	Digital video (Rec 656) output	27 MHz	YES
142	R656OUT4	O	3.3 V	CMOS	4 mA	Digital video (Rec 656) output	27 MHz	YES
143	VDD3	Power supply	3.3 V	-	-	Digital I/O (3.3 V) use	-	-
144	R656OUT3	O	3.3 V	CMOS	4 mA	Digital video (Rec 656) output	27 MHz	YES
145	R656OUT2	O	3.3 V	CMOS	4 mA	Digital video (Rec 656) output	27 MHz	YES
146	VSS	GND	-	-	-	Digital use	-	-
147	R656OUT1	O	3.3 V	CMOS	4 mA	Digital video (Rec 656) output	27 MHz	YES
148	R656OUT0	O	3.3 V	CMOS	4 mA	Digital video (Rec 656) output (LSB)	27 MHz	YES
149	VDDI	Power supply	1.8 V	-	-	Internal digital use	-	-
150	VSS	GND	-	-	-	Digital use	-	-
151	HD	I/O	3.3 V	CMOS-100 kΩ PU	4 mA	Test I/O (open or VDD3)	27 MHz	YES
152	VD	I/O	3.3 V	CMOS-100 kΩ PU	4 mA	Test I/O (open or VDD3)	27 MHz	YES
153	VDD3	Power supply	3.3 V	-	-	Digital I/O (3.3 V) use	-	-
154	APCE	O	3.3 V	3-state CMOS	2 mA	Phase error output	27 MHz	-
155	VSS	GND	-	-	-	Digital use	-	-
156	CSYNCO	O	3.3 V	CMOS	2 mA	Composite sync detection output	27 MHz	YES

Table 2.2 Pin Descriptions (4/4)

Pin No.	Pin name	I/O	Voltage	Type	Drive	Function	Clock	BST
157	MICONRWW	O	3.3 V	CMOS	2 mA	Microcontroller interrupt (write) sync signal output	27 MHz	YES
158	VDD3	Power supply	3.3 V	-	-	Digital I/O (3.3 V) use	-	-
159	MICONRWR	O	3.3 V	CMOS	2 mA	Microcontroller interrupt (read) sync signal output	27 MHz	YES
160	VSSDRAM3	GND	-	-	-	Digital use	-	-
161	VDDDRAM3	Power supply	2.5 V	-	-	DRAM (7 Mbits) use	-	-
162	RST	I	3.3 V	CMOS-100 kΩ PU	-	Reset input	-	-
163	VSS	GND	-	-	-	Digital use	-	-
164	CLK27XI	I	-	Crystal interface	-	27-MHz clock (crystal) input	27 MHz	-
165	CLK27XO	O	-	Crystal interface	-	27-MHz clock (crystal) output	27 MHz	-
166	VDDI	Power supply	1.8 V	-	-	Internal digital use	-	-
167	VSS	GND	-	-	-	Digital use	-	-
168	MAD6	I/O	3.3 V	Schmitt CMOS	4 mA	Microcontroller interface data/address input (MSB)	-	YES
169	MAD5	I/O	3.3 V	Schmitt CMOS	4 mA	Microcontroller interface data/address input	-	YES
170	MAD4	I/O	3.3 V	Schmitt CMOS	4 mA	Microcontroller interface data/address input	-	YES
171	VDD3	Power supply	3.3 V	-	-	Digital I/O (3.3 V) use	-	-
172	MAD3	I/O	3.3 V	Schmitt CMOS	4 mA	Microcontroller interface data/address input	-	YES
173	MAD2	I/O	3.3 V	Schmitt CMOS	4 mA	Microcontroller interface data/address input	-	YES
174	MAD1	I/O	3.3 V	Schmitt CMOS	4 mA	Microcontroller interface data/address input	-	YES
175	MAD0	I/O	3.3 V	Schmitt CMOS	4 mA	Microcontroller interface data/address input (LSB)	-	YES
176	VSS	GND	-	-	-	Digital use	-	-
177	MDA15	I/O	3.3 V	CMOS	8 mA	Microcontroller interface data/address I/O (MSB)	-	YES
178	MDA14	I/O	3.3 V	CMOS	8 mA	Microcontroller interface data/address I/O	-	YES
179	VDDI	Power supply	1.8 V	-	-	Internal digital use	-	-
180	MDA13	I/O	3.3 V	CMOS	8 mA	Microcontroller interface data/address I/O	-	YES
181	MDA12	I/O	3.3 V	CMOS	8 mA	Microcontroller interface data/address I/O	-	YES
182	VSS	GND	-	-	-	Digital use	-	-
183	MDA11	I/O	3.3 V	CMOS	8 mA	Microcontroller interface data/address I/O	-	YES
184	MDA10	I/O	3.3 V	CMOS	8 mA	Microcontroller interface data/address I/O	-	YES
185	VDD3	Power supply	3.3 V	-	-	Digital I/O (3.3 V) use	-	-
186	MDA9	I/O	3.3 V	CMOS	8 mA	Microcontroller interface data/address I/O	-	YES
187	MDA8	I/O	3.3 V	CMOS	8 mA	Microcontroller interface data/address I/O	-	YES
188	VSS	GND	-	-	-	Digital use	-	-
189	MDA7	I/O	3.3 V	CMOS	8 mA	Microcontroller interface data/address I/O	-	YES
190	MDA6	I/O	3.3 V	CMOS	8 mA	Microcontroller interface data/address I/O	-	YES
191	VDDI	Power supply	1.8 V	-	-	Internal digital use	-	-
192	MDA5	I/O	3.3 V	CMOS	8 mA	Microcontroller interface data/address I/O	-	YES
193	MDA4	I/O	3.3 V	CMOS	8 mA	Microcontroller interface data/address I/O	-	YES
194	VSS	GND	-	-	-	Digital use	-	-
195	MDA3	I/O	3.3 V	CMOS	8 mA	Microcontroller interface data/address I/O	-	YES
196	MDA2	I/O	3.3 V	CMOS	8 mA	Microcontroller interface data/address I/O	-	YES
197	VDD3	Power supply	3.3 V	-	-	Digital I/O (3.3 V) use	-	-
198	MDA1	I/O	3.3 V	CMOS	8 mA	Microcontroller interface data/address I/O	-	YES
199	MDA0	I/O	3.3 V	CMOS	8 mA	Microcontroller interface data/address I/O (LSB)	-	YES
200	VSS	GND	-	-	-	Digital use	-	-
201	MCSALE	I/O	3.3 V	Schmitt CMOS	-	Microcontroller interface chip select input	-	YES
202	MNRE	I/O	3.3 V	Schmitt CMOS	-	Microcontroller interface read input	-	YES
203	MNWENBW	I/O	3.3 V	Schmitt CMOS	-	Microcontroller interface write input	-	YES
204	MICOMSEL	I/O	3.3 V	Schmitt CMOS	-	Microcontroller interface selection input	-	YES
205	NC3	I/O	3.3 V	Schmitt CMOS	-	Microcontroller interface mode selection input (Normal mode: VSS)	-	-
206	VDDI	Power supply	1.8 V	-	-	Internal digital use	-	-
207	INF	I	3.3 V	CMOS-100 kΩ PD	-	Test input (open or VSS)	-	YES
208	FRP	O	3.3 V	CMOS	4 mA	Test output	-	YES

2.3 Pin Assignment

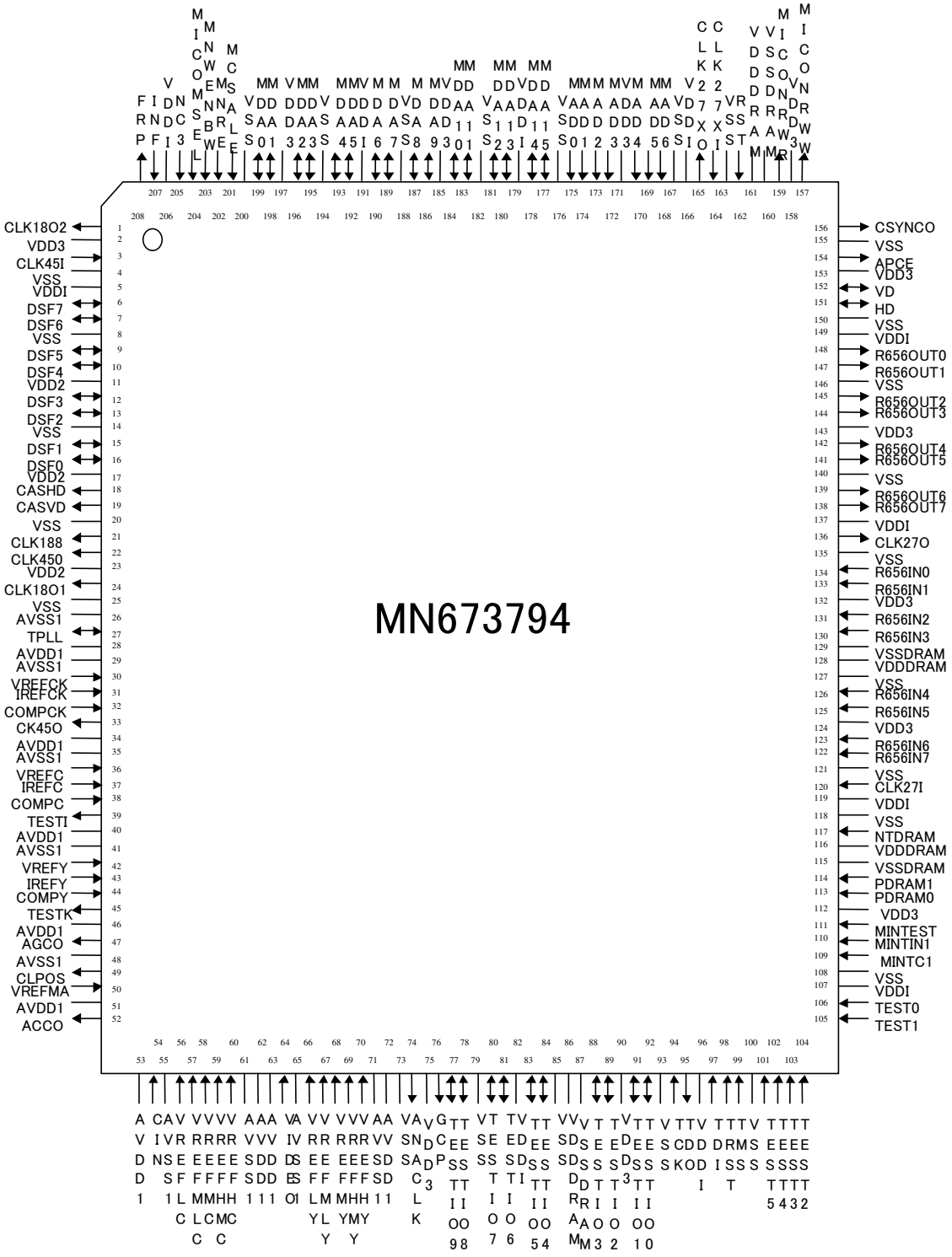


Figure 2.3 Pin Assignment

2.4 Block Diagram

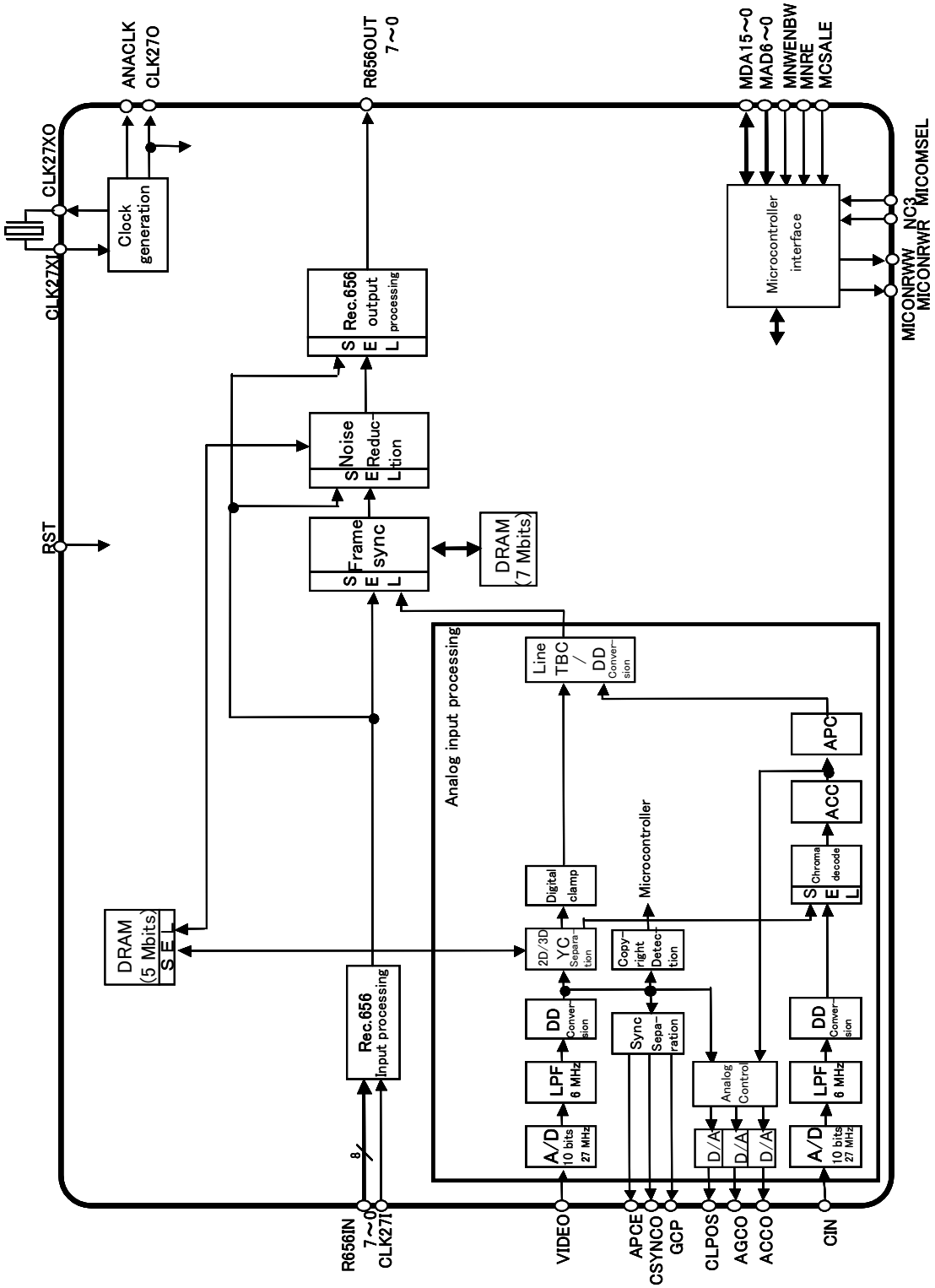


Figure 2.4 Block Diagram

3. Microcontroller Interface

(1) Overview

Data is written to and read from the internal registers of the IC through microcontroller interfaces. A microcontroller to be connected to the IC has two types of interfaces in consideration of two cases, where the address, data, and control line are synchronous with the system clock of the IC and where they are not synchronous with the system clock. The two types of interfaces are available in both cases. One of them is an address/data multiple bus interface, which enables the data bus to be overlapped with addresses, and the other is an interface for address/data bus separation. These cases and types are selectable with the external pins of the IC as shown in table 3.1.

Table 3.1 Protocol Settings for Microcontroller Interface

Pin setting (Pin number)		Protocol	
No. 204 (MICOMSEL)	No. 205 (NC3)	Sync/Async with system clock	Separation/Multiple address data bus
0	0	Async	Separation
0	1	Sync	Separation
1	0	Async	Multiple
1	1	Sync	Multiple

(2) Microcontroller Interface Signals

Table 3.2 shows the respective microcontroller interface signals and corresponding pins that appear in the microcontroller timing chart.

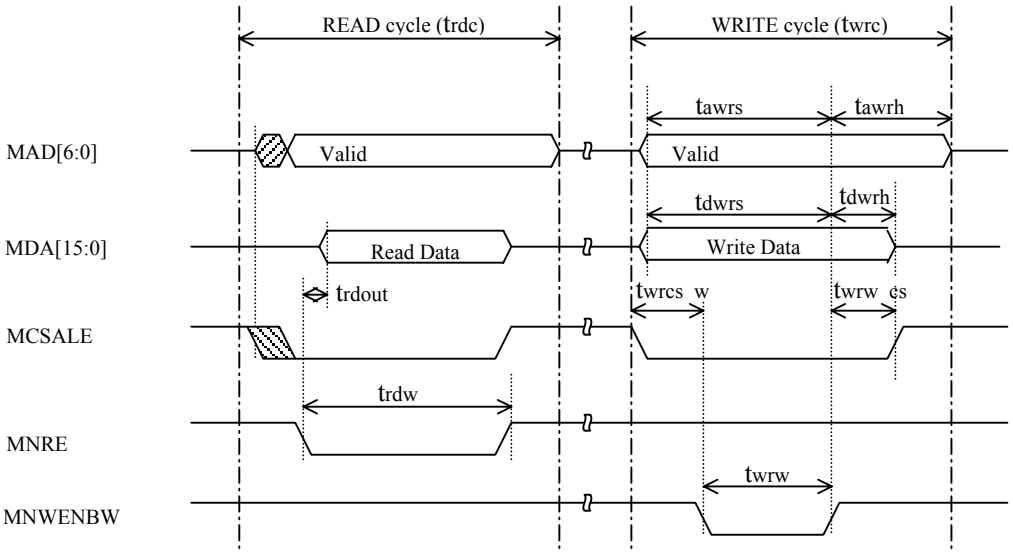
Table 3.2 Interface Signals and Corresponding Pins

Signal	Interface (separation/multiple) signals not synchronous with system clock	Interface (separation/multiple) signals synchronous with system clock
Address	MAD	Adress
Data	MDA	Data
CS (chip select)	MCSALE	CS
WE (write enable)	MNWENBW	WE
RE (read enable)	MNRE	RE

(3) Timing

[a] System Clock Async/Separation Bus Interface

Figure 3.3 (a) is the timing chart of the interface.



Timing		[ns]	
		Min	Max
trdc	Read cycle	148	–
trdout	Read data valid	–	30
twrc	Write cycle	148	–
trdw	Read pulse (MNRE) width	74	–
twrw	Write pulse (MNWENBW) width	74	–
twrcs_w	CS enable after WE active	10	–
twrw_cs	WE negate after CS disable	10	–
tdwrs	Write data setup	twrw	–
tdwrh	Write data hold	0	–
tawrs	Write address setup	twrw	–
tawrh	Write address hold	10	–

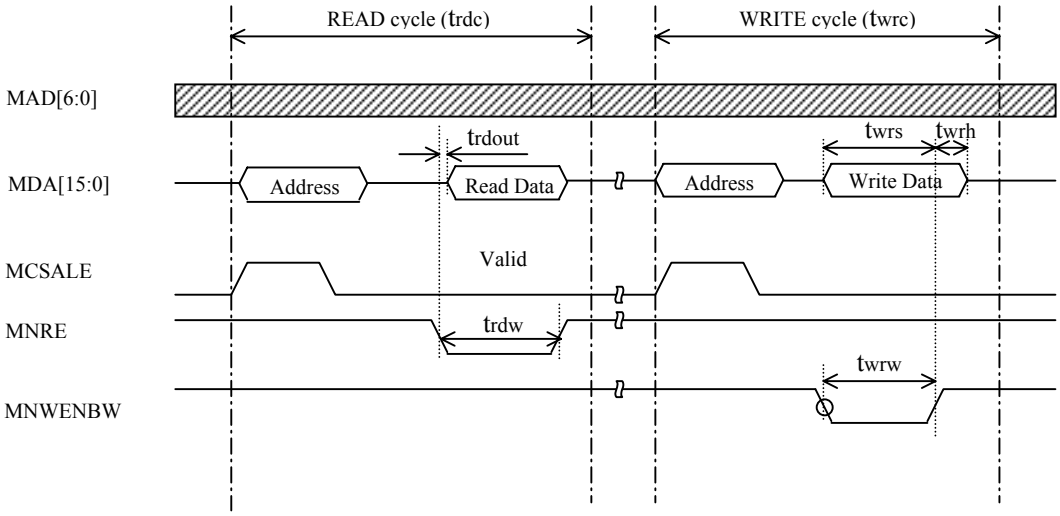
Figure 3.3 (a) Microcontroller Interface Timing 1

∗ Note)

- When the signal timing changes to the read cycle from the write cycle, data reading must start at least 50 ns after the write cycle completes.
- In the case of continuous data writing, a minimum of 148 ns is required between the falling edge of the present write enable (MNWENBW) and that of the next write enable.

[b] System Clock Async/Multiple Bus Interface

Figure 3.3 (b) is the timing chart of the interface.

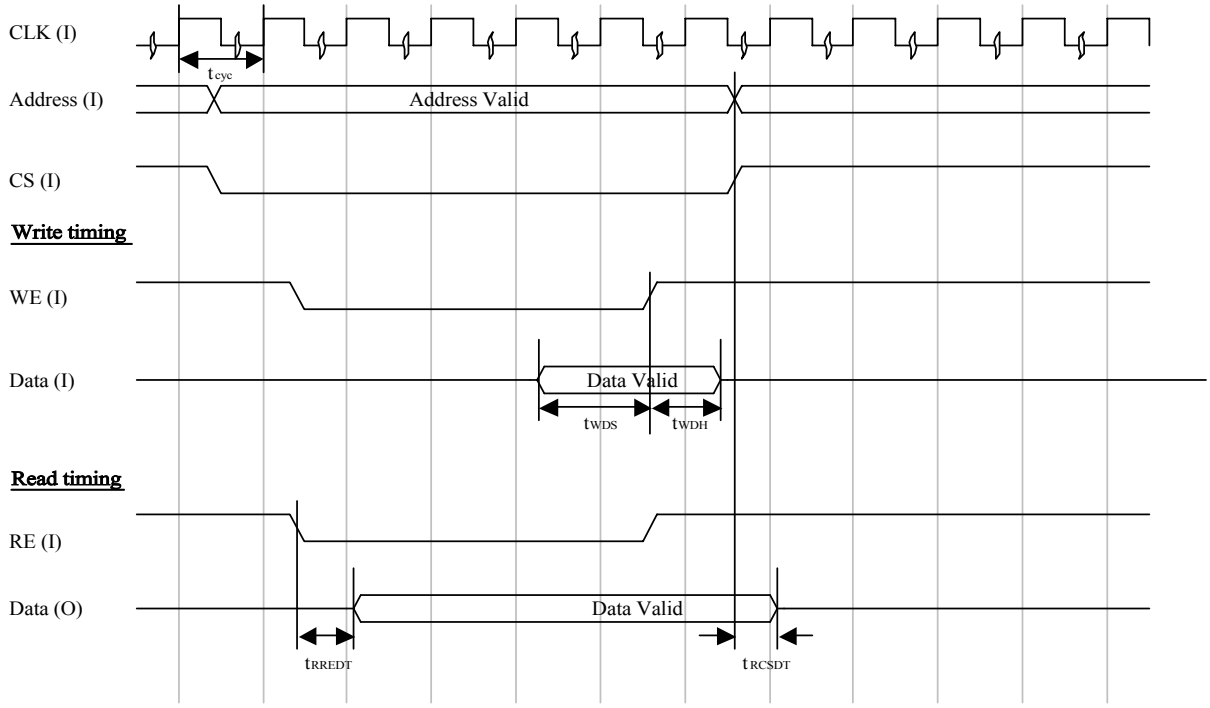


Timing		[ns]	
		Min	Max
trdc	Read cycle	148	–
trdout	Read data valid	–	30
twrc	Write cycle	148	–
trdw	Read pulse (MNRE) width	74	–
twrw	Write pulse (MNWENBW) width	74	–
twrs	Write data setup	twrw	–
twrh	Write data hold	10	–

Figure 3-3 (b) Microcontroller Interface Timing 2

[c] System Clock Sync/Separation Bus Interface

Figure 3.3 (c) is the timing chart of the interface.



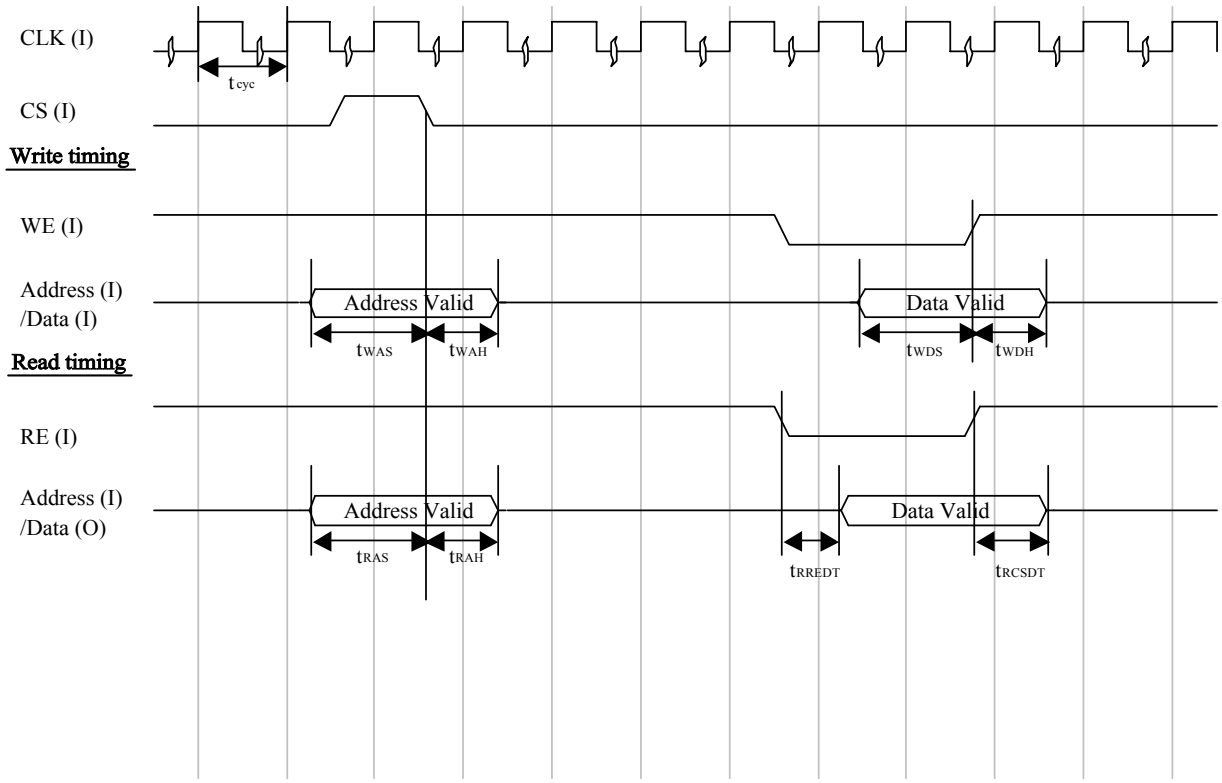
Parameter	Symbol	Min	Typ	Max	Unit
27-MHz clock cycle	tCYC		37		ns
Write data setup （based on rising edge of write enable WE）	tWDS	tCYC			ns
Write data hold (based on rising edge of write enable WE)	tWDH	tCYC			ns
Read data delay (based on falling edge of read enable RE)	tRREDT	0		tCYC	ns
Read data hold (based on rising edge of chip select CS)	tRCSDT	0			ns

Figure 3.3 (c) Microcontroller Interface Timing 3

- Address, Data, CS, WE, and RE input signals are input, not synchronizing with the CLK clock signal.
- The CS must be disabled (i.e., set to high) whenever data is read from or written to any address.

[d] System Clock Async/Multiple Bus Interface

Figure 3.4 (d) is the timing chart of the interface.



Parameter	Symbol	Min	Typ	Max	Unit
27-MHz clock cycle	tCYC		37		ns
Write address setup (based on falling edge of address latch enable ALE)	tWAS	tCYC			ns
Write address hold (based on falling edge of address latch enable ALE)	tWAH	tCYC			ns
Read address setup (based on falling edge of address latch enable ALE)	tRAS	tCYC			ns
Read address hold (based on falling edge of address latch enable ALE)	tRAH	tCYC			ns
Write data setup (based on rising edge of write enable WE)	tWDS	tCYC			ns
Write data hold (based on rising edge of write enable WE)	tWDH	tCYC			ns
Read data delay (based on falling edge of read enable RE)	tRREDT	0		tCYC	ns
Read data hold (based on rising edge of chip select CS)	tRCSDT	0			ns

Figure 3.3 (d) Microcontroller Interface Timing 4

* Address, Data, CS, WE, and RE input signals are input, not synchronizing with the CLK clock signal.

(4) Microcontroller Registers

[a] Read/Write

Addresses 0040h to 0046h, 0048h, and 004Ah are read-only registers.
Data can be written to and read from addresses with register marks if they are not read-only registers.
Although data can be written to addresses with no register marks, the accuracy of data read from such addresses is not guaranteed.

[b] Special Registers

Addresses 0043h and 0044h are registers, the functions of which vary with the signal mode settings for the registers.

- NTSC mode: Register for VBID detection
- PAL mode: Register for WSS detection (The register table in WSS mode is different.)

[c] Video Signal Mode Settings

A video signal mode is set with three bits. These bits have the following meanings.

Bit	Meaning	0	1
[2]	Line	525-line mode	625-line mode
[1]	Processing frequency (4fsc)	14 MHz line	17 MHz line
[0]	Phase Alt	No	Yes

Make the following settings for the respective signal modes.

[2:0]	System
000	NTSC
001	PAL-M
010	NTSC443
011	(PAL-60)
100	–
101	PAL-N
110	–
111	PAL

Make sigmod 0000h [2:0] settings for the signal modes of the analog input processing block, frame sync processing block, Rec 656 input processing block, and Rec 656 output processing block.

[d] Write Registers

Figure 3.4 shows the block diagram for the write registers.

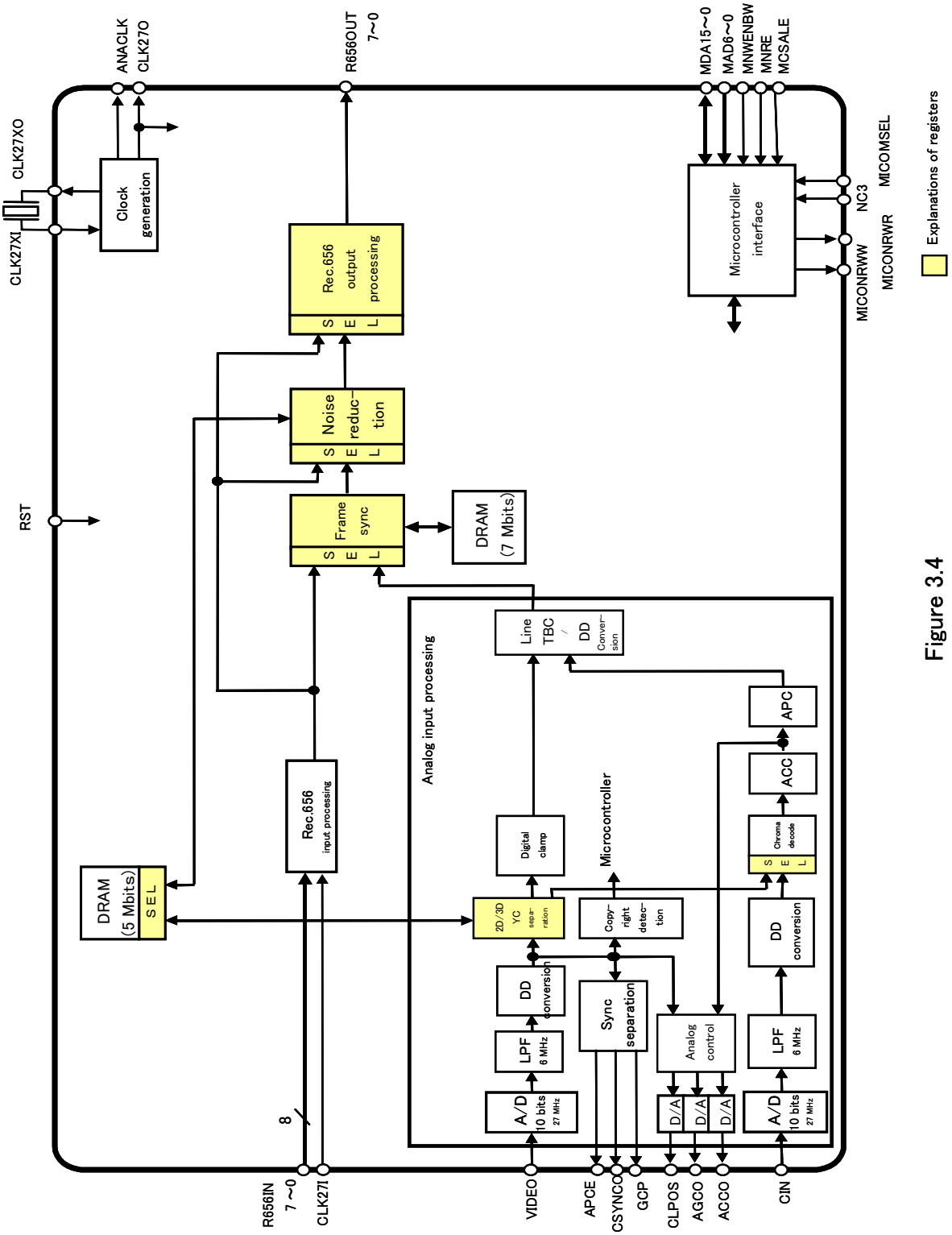


Figure 3.4

1. Control system

Register name	Address	Description	Default (Recommended value)
cpsh	0000h[15]	Used to select the mode of the analog input processing block. 0: Component input 1: Composite input	1
fsinsel	0000h[13:12]	Used to select the input of the frame sync block. 00: Analog input 01: Rec656 input 10: Test use 11: Not used	00
r656outsel	0000h[11]	Used to select the input of the Rec656 output processing block. 0: Noise reduction output 1: Rec656 input	0
sigmod	0000h[2:0]	Used to set the signal modes of the analog input processing block, frame sync processing block, Rec656 input processing block, and Rec656 output processing block. 000: NTSC 001: PAL-M 010: NTSC443 011: PAL-60 100: - 101: PAL-N 110: - 111: PAL	000
pvs_pll_sell	0004h[1:0]	Used to set the sync output of the sync separation block 00: Normal sync output mode 01: Prohibited 10: AFCV mode (pseudo V-AFC) 11: AFCV-still detection mode (pseudo V-AFC-still detection)	11 (00)
tbcmod	0012h[1:0]	Used to set the mode of the TBC block 00: Normal (DD conversion + jitter correction + velocity error correction) 01: Velocity error correction off (DD conversion + jitter correction) 10: Jitter correction / velocity error correction off (DD conversion only) 11: Prohibited	00
rpclamp[4:2]	0014h[4:2]	Used to set the hold range of the DCLP (digital clamp) block (8 steps) 000: Thru 001: ±2 010: ±4 011: ±6 110: ±8 101: ±10 110: ±14 111: ±16	000 (001)
rpclamp[0]	0014h[0]	Used to set the operation of the DCLP (digital clamp) block 0: Off 1: On	1
clpreg[5:4]	0025h[5:4]	Used to set the error output of the clamp control block 00: Center fixed 01:Max. fixed 10:Min. fixed 11: Normal	11
agcreg1 [11:10]	0022h[11:10]	Used to set the error output of the AGC control block 00: Center fixed 01:Max. fixed 10:Min. fixed 11: Normal	11
SideLock Sel	0003h[1]	Used to set the AFCH pseudo lock reset of the sync separation block 0: Not available 1: Available	0
paravsep pll	0004h[5:2]	AFCV response characteristics	1110 (0100)
parajdet pls	000Fh[13:12]	Used to set the TBC sync separation	11 (00)
misfmv	0020h[5:0]	Used to set the lower limit of MV judgment level of the MV detection block	100000 (100001)
tdir2516	0029h[3:1]	Used to set the sync separation block	000 (011)

2. Y/C separation

Register name	Address	Description	Default (Recommend-ed value)
HYOZI	0008h[6]	The detected movement area is displayed dark (for evaluation). 0: Normal 1: Movement detection display	0
F3DSEL	0008h[5:3]	A threshold value to determine movement with two-frame differential movement detected. (Compared with the 9-bit absolute value converted from the 10-bit difference between the 9-bit input signal and 2-frame, 9-bit delay signal.) 000: 3D fixed 001: 4 or more 010: 8 or more 011: 12 or more 100: 16 or more 101: 20 or more 110: 24 or more 111: 28 or more (To fix the setting to 3D, set the F3DSEL register to 000 and the F2DSEL register to 000. To fix the setting to 2D, set the F3DSEL to any value other than 000 and set the F2DSEL to 000.)	100
F2DSEL	0008h[2:0]	A threshold value to determine movement with one-frame differential movement detected. (Compared with the 9-bit absolute value converted from the 10-bit difference between the 9-bit input signal and 1-frame, 9-bit delay signal.) 000: 3D fixed 001: 4 or more 010: 8 or more 011: 12 or more 100: 16 or more 101: 20 or more 110: 24 or more 111: 28 or more (To fix the setting to 3D, set the F3DSEL register to 000 and the F2DSEL register to 000. To fix the setting to 2D, set the F3DSEL to any value other than 000 and set the F2DSEL to 000.)	100

3. Y/C delay adjustment

Register name	Address	Description	Default (Recommend-ed value)
cdly2	0009h[7:6]	Used to adjust the delay of the component C signal (in 4fsc increments). (DD conversion output of C signal of analog input processing block) 00: No delay 01: +1 clock 10: -2 clock 11: -1 clock	00
cdly1	0009h[5]	Used to adjust the delay of the component C signal (in 27 MHz increments). (LPF output of C signal of analog input processing block) 00: No delay 01: +1 clock	0
tbccdly	0009h[9:8]	Used to adjust the delay of the CbCr multiple signal (in 4fsc increments). (Before TBC input into the analog input processing block) 00: No delay 01: +1 clock 10: -2 clock 11: -1 clock	00 (11)
cflgdly	0029h[0]	Used to reverse the polarity of the CbCr separation flag for the CbCr multiple signal. If the tint is reversed with tbccdly delay adjustments, invert this flag. (Before TBC input into the analog input processing block) 0: No reversion 1: Reversion	0 (1)

4. Color setting

Register name	Address	Description	Default (Recommend -ed value)
apcerr2deg	0006h[12:8]	Used to set the gain of the APC frequency pull-in (loop filter first term) (0 to 31) 00001: Large gain 00111: Default 01101: Small gain	00111 (00101)
sekilmt	0006h[7:5]	Used to set the burst lock range of the APC block 000: Narrow 011: Default 100: Wide	011
apcerr1deg	0006h[4:0]	Used to set the gain of the APC phase pull-in (loop filter zero term) (0 to 31) 11000: Small gain 11100: Default 11110: Large gain	11100
raccoff	000Ah[15]	Used to set the On/Off of the FFACC (Digital feed forward ACC) block 0: Off 1: On	0
racc	000Ah[14:8]	Used to set the gain of the FFACC block 0: Default (72) Other than 0: racc[6:0]X2	0000000
sacc	000Bh[15]	Used to set the control DAC output of the FBACC (Analog feedback ACC) block 0: Center fixed 1: Normal (error output)	1 (0)
racc	000Bh[12:8]	Used to set the saturation (except burst) of the FFACC block 00000: Small 10000: Default 11111: Large	10000
rapcon	000Ch[6]	Used to set the hue compensation of the APC block 0: Off 1: On	0
rphadj	000Ch[5:0]	Used to set the hue compensation of the APC block 100000: Large (-) 00000: Off 011111: Large (+)	00000

5. Rec656 output

Register name	Address	Description	Default (Recommend -ed value)
VideoOutsel	002Eh[1:0]	Used to switch over the valid pixels of the Rec656 output signal to blue or black background. 0X: Normal 10: Black background 11: Blue background	00

6. Noise Reduction (NR)

Figure 3.6-1 shows the block diagram of noise reduction.
The input signal will be output with the NR-ROM output signal subtracted.
Furthermore, the output signal will be delayed in fields or frames, and the difference from the input signal will be input into the NR-ROM. This is called recursive noise reduction with a variable recursive coefficient.
Figure 3.6-2 shows the characteristics of the NR-ROM.
The field/frame differential signal contains a movement or noise signal.
When the field/frame differential signal is high, the signal is considered a movement signal. When the signal is low, it is considered a noise signal. The strength or gain of the filed/frame differential signal for noise reduction can be changed by register settings.
Figure 3.6-3 shows the characteristics of noise reduction.
For details, refer to the table of registers.

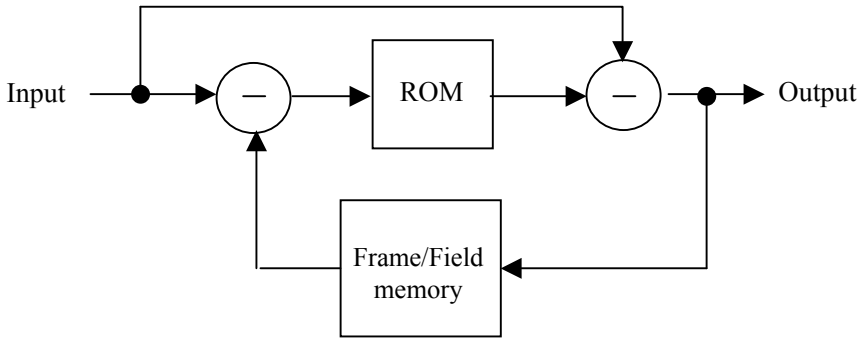


Fig. 3.6-1 NR Block Diagram

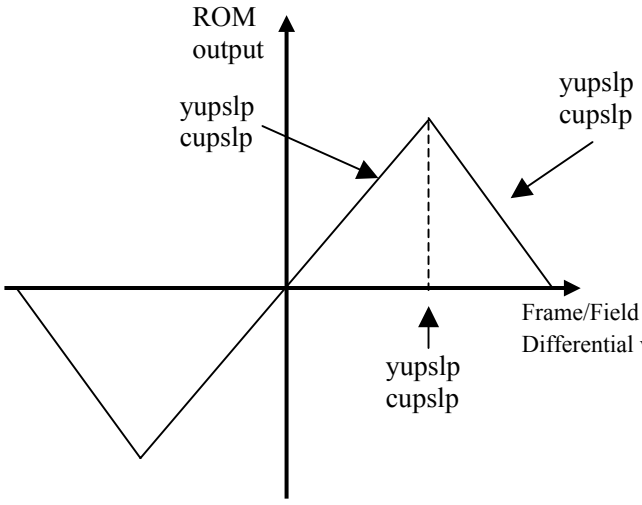


Fig. 3.6-2 NR-ROM characteristics

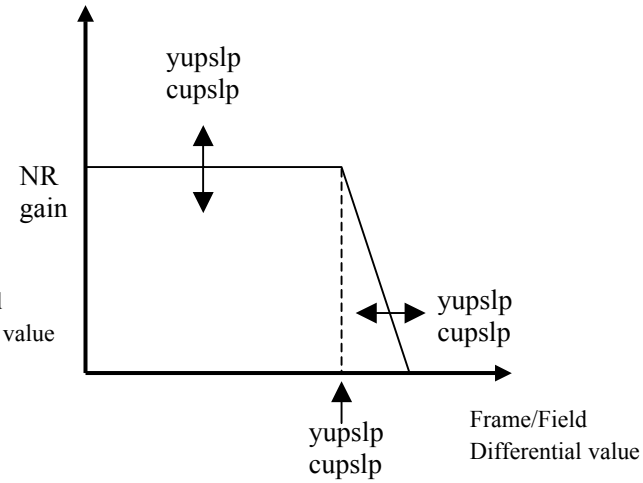


Fig. 3.6-3 NR characteristics

Register name	Address	Description	Default (Recommend-ed value)
Setnrin	003Ch[15]	Used to switch over the input into the noise reduction block. 0: Frame sync output 1: Rec656 input	0
SetTof	003Ch[14:13]	Used to make through/NR setting in the noise reduction block. 0X: NR block through 10: NR OFF 11: NR ON	00
Set3dnr	003Ch[12]	Used to set the recursive 3D control. 0: Frame recursive NR 1: Field recursive NR	0
SetMdet	003Ch[9:5]	A threshold value to disable the noise reduction of the C signal by using the Y frame/field differential signal. The color frame/field differential signal has narrow band range. Therefore, higher precision can be obtained in edge portions by using the Y differential signal. If the threshold value is larger, the influence of the differential signal of Y will be less, and the NR of the C will be enabled by the color differential signal. If the threshold value is smaller, the NR of the C will not be enabled when the Y differential signal is high. Threshold value = SetMdet [6:2]×2 Example: If SetMdet is 01000, the threshold value is 16.	01000
	003Ch[4:3]	A width where the noise reduction of C is disabled by the frame/field differential signal of Y. Area to disable the noise reduction of C: Number of clocks. 00: 1 clock (The differential signal of Y is used as it is) 01: -1 to +1 clock (The differential signal of Y is widened left and right for one clock each.) 10: -2 to +2 clock (The differential signal of Y is widened left and right for two clocks each.) 11: -3 to +3 clock (The differential signal of Y is widened left and right for three clocks each.)	01
SetMvVi	003Ch[2]	The detected movement area is displayed dark (for evaluation). 0: Normal 1: Movement detection display	0
Ydnslp	003Dh[12:10]	Used to make negative slope settings for a high Y frame/field differential signal range. If the differential signal is higher than the Yudchg value, the differential signal is considered a movement signal. Then the amount of noise reduction will be attenuated. Set the attenuation gain in the register. Large value: Quickly attenuated according to the differential signals. Small value: Slowly attenuated according to the differential signals. (For the characteristics, refer to NR-ROM and NR characteristics.)	010
Yupslp	003Dh[9:6]	Used to make positive slope setting for a low Y frame/field differential signal range. If the positive slope setting is larger, the gain will be high to enable NR high. If the positive slope setting is smaller, the gain will be less to enable NR low. Gain=yupslp[3:00]/16 (For the characteristics, refer to NR-ROM and NR characteristics.)	10000
Yudchg	003Dh[5:0]	Used to set the change point between the above ydnslp (negative slope) and the yupslp (positive slope). If the differential signal is higher than the change point, the differential signal is considered a movement signal. Then the amount of NR will be attenuated. (For the characteristics, refer to NR-ROM and NR characteristics.)	010000
Cdnslp	003Eh[12:10]	Used to set the negative slope of the maximum C frame/field differential value. (Same as Y in characteristics.)	010
Cupslp	003Eh[9:6]	Used to set the positive slope of the minimum C frame/field differential value. Gain=cupslp[3:0]/16 (Same as Y in characteristics.)	1110
Cudchg	003Eh[5:0]	Used to set the change point between the above cdnslp (negative slope) and cupslp (positive slope). (Same as Y in characteristics.)	100000

7. Frame sync

Register name	Address	Description	Default (Recommend -ed value)
wr_offset	0017h[4:0]	Frame sync, write line start position offset (23 lines + offset value)	00000

8. Analog power down (Possible to reduce the power consumption of the corresponding functions when the functions are not in use.)

Register name	Address	Description	Default (Recommend -ed value)
yadpdwn	0039h[8]	Used to power down the component Y/composite Y (analog input) ADC. 0: Normal 1: Power down	0
cadpdwn	0039h[7]	Used to power down the component C (analog output) ADC. 0: Normal 1: Power down	0
Test0dapdwn	0039h[6]	Used to power down the DAC for test use. 0: Normal 1: Power down	0 (1)
Test1dapdwn	0039h[5]	Used to power down the DAC for test use. 0: Normal 1: Power down	0 (1)
Test2dapdwn	0039h[4]	Used to power down the DAC for test use. 0: Normal 1: Power down	0 (1)
agcdapdwn	0039h[3]	Used to power down the AGC control DAC. 0: Normal 1: Power down	0
accdapdwn	0039h[2]	Used to power down the ACC control DAC. 0: Normal 1: Power down	0
clpdapdwn	0039h[1]	Used to power down the clamp control DAC. 0: Normal 1: Power down	0
testpllpdwn	0039h[0]	Used to power down the PLL for test use 0: Normal 1: Power down	0 (1)

[e] Read registers

1. Macrovision

Register name	Address	Description	Default
immvh	0041h[15]	Result of AGC pulse detection 0: No 1: Yes	—
spiso	0041h[14:13]	Result of color stripe phase detection 00: 0° 01: 90° 10: 180° 11: 270°	—
spgcnt	0041h[12:8]	Result of detection of the number of color stripe groups per field	—
sppos	0041h[7:6]	Result of detection of the color stripe split position 00: No 01: Latter half 10: First half 11: Indefinite	—
spcnt	0041h[5:0]	Result of detection of the number of color stripe lines per field (Implement the spcnt/spgcnt based on the result of spcnt and spgcnt detection. Then determine if the 4- or 2-line mode is set.)	—
agcflg	0042h[9:8]	Result of detection of sync reduction 00: V=H 01: H>V 11: V>H	—

2. VBID

Register name	Address	Description	Default
imdatavw	0043h[13:0]	Detection data First data=0043h[0]	—
immidvw1	0044h[13:9]	Number of data items the intermediate values of which are detected (from the 600 kHz LPF signal) (Number of bits out of the 14 data bits)	—
immidvw2	0044h[8:4]	Number of data items the intermediate values of which are detected (from the 6 MHz LPF signal) (Number of bits out of the 14 data bits)	—
imvwlno	0044h[3:2]	The number of line where the data is detected 00: Not detected 01: 19(282)H 10: 20(283)H 11: 21(284)H	—
imvwdet	0044h[0]	Result of reference pulse detection 0: Not detected 1: Detected	—
imvwok	0044h[1]	Reliability of the detection result 0: Not good 1: OK (The imvwdet bit is set to 1 and all data fixed with CRC added.)	—

3. WSS

Register name	Address	Description	Default
imdatavw	0043h[13:0]	Detection data First data=0043h[0]	—
immidvw1	0044h[13:9]	Number of data items the intermediate values of which are detected (from the 1 MHz LPF signal)	—
immidvw2	0044h[8:4]	Number of data items the intermediate values of which are detected (from the 6 MHz LPF signal)	—
imvwlno	0044h[3:2]	The number of line where the data is detected 00: Not detected 01: 19(282)H 10: 20(283)H 11: 21(284)H	—
imvwdet	0044h[0]	Result of Clock Run-In detection 0: Not detected 1: Detected	—
imvwok	0044h[1]	Reliability of the detection result 0: Not good 1: OK (The imvwdet bit is set to 1 and start code and bi-phase acceptable)	—

4. Closed caption

Register name	Address	Description	Default
imdatacc	0045h[15:0]	Detection data First data=0045h[0]	—
immidcc1	0046h[12:9]	Number of data items the intermediate values of which are detected (from the 600 kHz LPF signal)	—
immidcc2	0046h[7:4]	Number of data items the intermediate values of which are detected (from the 6 MHz LPF signal)	—
imcclno	0046h[3:2]	The number of line where the data is detected 00: Not detected 01: 20(283)H 10: 21(284)H 11: 22(285)H	—
imccdet	0046h[0]	Result of Clock Run-In detection 0: Not detected 1: Detected	—
imccok	0046h[1]	Reliability of the detection result 0: Not good 1: OK (The imccdet bit is set to 0 and all data fixed)	—

5. Others

Register name	Address	Description	Default
bg32cnt	0040h[7:4]	Color killer use 1/4 of the number of lines with no burst gate generated during a period of 128H.	—
ckreg	0040h[3:0]	Color killer use The total number (absolute value) of APC errors resulted during a period of 128H.	—
imjack	0042h[7:0]	Result of detection of weak electromagnetic field sync noise (The number of pulses in the sliced and binary-coded Csync in a single field)	—
NSTD	0046h[15]	Standard signal discrimination (Discriminated as a standard signal if the number of clocks per 1H period is within a range of 910±7.) 0: Standard 1: Nonstandard	—
odev	0048h[5]	Field discrimination 0: Second field (even) 1: First field (odd)	—
ghsfew	0048h[4]	Signal detection result 0: Detected 1: Not detected	—
lownoise	0049h[15:8]	Result of weak electromagnetic field detection The integrated noise value (0 to 255) in a period of 6H V-blanking.	—
frmchg_skip	004Ah[1]	Discrimination of frame skipping in the frame sync block 0: No skip 1: Skipped	—
frmchg_hold	004Ah[0]	Discrimination of frame hold in the frame sync block 0: No hold 1: Hold	—

[f] Register map

Tables 3.4-1 to 3.4-4 show the register maps.

Table 3.4-1 Read Register Map

	0000h	0003h	0004h	0006h	0008h	0009h	000Ah	000Bh
D[15]	cpsh						raccoff	sacc
D[14]							racc [6:0]	
D[13]	fsinsel [1:0]							
D[12]				apcerr 2deg [5:0]				rlvl adj [4:0]
D[11]	r656out sel							
D[10]								
D[9]						tbccdly [1:0]		
D[8]								
D[7]				seki lmt [2:0]		cdly2 [1:0]		
D[6]					HYOZI			
D[5]			parav seppll [3:0]		F3DSEL [2:0]	cdly1		
D[4]				apcerr 1deg [4:0]				
D[3]								
D[2]	sigmod [2:0]				F2DSEL [2:0]			
D[1]		sidelo cksel	pvs_pll _sell [1:0]					
D[0]								

Table 3.4-2 Read Register Map

	000Ch	000Fh	0014h	0017h	0020h	0022h	0025h	0029h	002Eh
D[15]									
D[14]									
D[13]		paraj detpls [1:0]							
D[12]									
D[11]						agc reg1 [11:10]			
D[10]									
D[9]									
D[8]									
D[7]									
D[6]	rapcon								
D[5]	rphadj [5:0]				mis fmv [5:0]		clp reg [5:4]		
D[4]			rp clamp [2:0]	wr_ offset [4:0]					
D[3]								tdir 2516 [2:0]	
D[2]									
D[1]									video out sel
D[0]			rp clamp [2:0]					cflg dly	

Table 3.4-3 Read Register Map

	0039h	003Ch	003Dh	003Eh
D[15]		set nrin		
D[14]		set tof		
D[13]				
D[12]		set 3dnr	ydn slp [2:0]	cdn slp [2:0]
D[11]				
D[10]				
D[9]		set mdet [6:0]	yup slp [3:0]	cup slp [3:0]
D[8]	yad pdwn			
D[7]	cad pdwn			
D[6]	test0da Pdwn			
D[5]	test1da pdwn		yud chg [5:0]	cud chg [5:0]
D[4]	test2da pdwn			
D[3]	agcda pdwn			
D[2]	accda pdwn	set mvvi		
D[1]	clpda pdwn			
D[0]	testpll pdwn			

Table 3.4-4 Write Register Map

	0040h	0041h	0042h	0043h	0044h	0045h	0046h	0048h	004Ah
D[15]		immvh				im data cc [15:0]	NSTD		
D[14]		spiso [1:0]							
D[13]				im data vw [13:0]	immid vw1 [4:0]				
D[12]		spg cnt [4:0]					immid cc1 [3:0]		
D[11]									
D[10]									
D[9]			agcflg [1:0]						
D[8]					immid vw2 [4:0]				
D[7]	bg32 cnt [4:0]	sppos [1:0]	im jack [7:0]				immid cc2 [3:0]		
D[6]									
D[5]		sp cnt [5:0]						odev	
D[4]								ghs few	
D[3]	ckreg [3:0]				imvw lno [1:0]		imcc lno [1:0]	low noise [3:0]	
D[2]									
D[1]					imvw ok		im ccok		frmchg skip
D[0]					imvw det		im ccdet		frmchg hold

A. Absolute Maximum Ratings

(V_{SS}= 0 V)

Parameter		Symbol	Rating	Unit
A1	External supply voltage	V_{DD}	-0.3 to 4.6	V
A2	Internal supply voltage	V_{DDI}	-0.3 to 3.6	
A3	Input pin voltage	V_I	-0.3 to V_{DD}+0.3 (Upper limit: 4.6)	
A4	Output pin voltage	V_O	-0.3 to V_{DD}+0.3 (Upper limit: 4.6)	
A5	Output current (TYPE-HL2)	I_O	±6	mA
A6	Output current (TYPE-HL4)	I_O	±12	
A7	Output current (TYPE-HL8)	I_O	±24	
A8	Power dissipation	P_D	1920	mW
A9	Operating ambient temperature	T_{OPR}	-20 to +80	℃
A10	Storage temperature	T_{STG}	-40 to 125	

TYPE-HL2 pins: CASHD, CASVD, CLK188, CLK450, ANACLK, GCP, CSYNCO, MICONRWW, MICONRWR, APCE, TDO

TYPE-HL4 pins: CLK27O, CLK18O2, CLK18O1, R656OUT7 to R656OUT0, FRP, HD, VD, TESTIO9 to TESTIO0, DSF7 to DSF0, MAD6 to MAD0, MCSALE, MNR, MNWENBW, MICOMSEL, NC3

TYPE-HL8 pins: MDA15 to MDA0

Note)

(1) The external supply pins are V_{DD3}, V_{DD2}, and AV_{DD} pins and the internal supply pins are V_{DDI} and V_{DDDRAM} pins.

(2) The absolute maximum ratings are the limit values beyond which the IC may be broken. They do not assure operations.

(3) Connect all V_{DD} pins externally and directly to the power supply. Connect all V_{SS} pins externally and directly to ground.

(4) Connect one or more bypass capacitors of 0.1 µF or larger between the power supply pin and ground.

(5) Connect MINTEST pin to V_{SS} pin.

B. Recommended Operating Conditions

(V_{SS}= 0 V)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
B1	Supply voltage (External 1)	V_{DD3}		3.0	3.3	3.6	V
B2	Supply voltage (External 2)	V_{DD2}		2.0	2.2	2.4	V
B3	Supply voltage (Internal)	V_{DDI}		1.65	1.8	1.95	V
B4	Supply voltage (Internal DRAM)	V_{DDDRAM}		2.3	2.5	2.7	V
B5	Supply voltage (Analog)	AV_{DD}		3.0	3.3	3.6	V
B6	Ambient temperature	Ta		-20		80	℃
B7	Oscillator frequency	f_{OSC}	CLK27XI pin		27		MHz
B8	Clock 1 input frequency	f_{IN1}	CLK27I		27		MHz
B9	Clock 2 input frequency	f_{IN2}	CLK45I		4.5		MHz

C. Pin Capacitance

C1	Input pin	C_{IN}	V_{DD}=V_I=0 V		7	8	pF
C2	Output pin	C_{OUT}	f_{in}=1 MHz		7	8	pF
C3	I/O pin	C_{IO}	Ta=25℃		7	8	pF

D. Electrical Characteristics

(1) DC Characteristics

(V_{SS}=AV_{SS}=V_{SSDRAM}=0 V, Ta=-20℃ to 80℃)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
D1	Operating supply current	I_{DDI}	V_{DD3}=AV_{DD}=3.6 V V_{DD2}=2.4 V V_{DDI}=1.95 V V_{DDDRAM}=2.7 V V_I=V_{DD} or V_{SS} f_{IN1}=27 MHz f_{IN2}=4.5 MHz f_{OSC1}=27 MHz Output: Open			300	mA
D2	Operating supply current	I_{DDDRAM}	V_{DD3}=AV_{DD}=3.6 V V_{DD2}=2.4 V V_{DDI}=1.95 V V_{DDDRAM}=2.7 V V_I=V_{DD} or V_{SS} f_{IN1}=27 MHz f_{IN2}=4.5 MHz f_{OSC1}=27 MHz Output: Open			80	mA
D3	Operating supply current	I_{DDANA}	V_{DD3}=AV_{DD}=3.6 V V_{DD2}=2.4 V V_{DDI}=1.95 V V_{DDDRAM}=2.7 V V_I=V_{DD} or V_{SS} f_{IN1}=27 MHz f_{IN2}=4.5 MHz f_{OSC1}=27 MHz Output: Open			302	mA

	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
	<Input: CMOS level> CLK27I						
D4	High-level input voltage	V_{IH3}		V_{DD3} ×0.7		V_{DD3}	V
D5	Low-level input voltage	V_{IL3}		0		V_{DD3} ×0.3	V
D6	Input leakage current	I_{LIPD3}	V_I=V_{DD3} or V_{SS}			±5	µA
	<Input: CMOS level with pull-up resistor> RST, TDI, TRST, TMS						
D7	High-level input voltage	V_{IH4}		V_{DD3} ×0.7		V_{DD3}	V
D8	Low-level input voltage	V_{IL4}		0		V_{DD3} ×0.3	V
D9	Input leakage current	I_{LIPD4}	V_I=V_{DD3}			±10	µA
D10	Pull-up resistor	R_{PU4}	V_{DD3}=0.0 V	33	100	300	kΩ
	<Input: CMOS level with pull-down resistor> TCK, TEST5 to TEST0, PDRAM1, PDRAM0, NTDRAM, R656IN7 to R656IN0, INF						
D11	High-level input voltage	V_{IH5}		V_{DD3} ×0.7		V_{DD3}	V
D12	Low-level input voltage	V_{IL5}		0		V_{DD3} ×0.3	V
D13	Input leakage current	I_{LIPD5}	V_I=V_{SS}			±10	µA
D14	Pull-up resistor	R_{PD5}	V_{DD3}=3.3 V	33	100	300	kΩ
	<Input: CMOS level with pull-down resistor> MINTEST						
D15	High-level input voltage	V_{IH6}		V_{DD3} ×0.7		V_{DD3}	V
D16	Low-level input voltage	V_{IL6}		0		V_{DD3} ×0.3	V
D17	Input leakage current	I_{LIPD6}	V_I=V_{SS}			±10	µA
D18	Pull-up resistor	R_{PD6}	V_{DD3}=3.3 V	10	30	90	kΩ

	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
	<Input: CMOS level> MINTC1, MINTIN1						
D19	High-level input voltage	V_{IH7}		V_{DD3} ×0.7		V_{DD3}	V
D20	Low-level input voltage	V_{IL7}		0		V_{DD3} ×0.3	V
D21	Input leakage current	I_{LIPD7}	V_I=V_{DD3} or V_{SS}			±5	µA

	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
	<Output: Normal buffer> ANACLK, GCP, CSYNCO, MICONRWW, MICONRWR						
D22	High-level output voltage	V_{OH9}	I_{OH}=-2 mA,V_I=V_{DD3} or V_{SS}	V_{DD3} -0.6			V
D23	Low-level output voltage	V_{OL9}	I_{OL}=2 mA,V_I=V_{DD3} or V_{SS}			0.4	V
	<Output: Normal buffer> CLK27O, CLK18O2, R656OUT7 to R656OUT0, FRP						
D24	High-level output voltage	V_{OH10}	I_{OH}=-4 mA,V_I=V_{DD3} or V_{SS}	V_{DD3} -0.6			V
D25	Low-level output voltage	V_{OL10}	I_{OL}=4 mA,V_I=V_{DD3} or V_{SS}			0.4	V
	<Output: Tri-state buffer> APCE, TDO						
D26	High-level output voltage	V_{OH11}	I_{OH}=-2 mA,V_I=V_{DD3} or V_{SS}	V_{DD3} -0.6			V
D27	Low-level output voltage	V_{OL11}	I_{OL}=2 mA,V_I=V_{DD3} or V_{SS}			0.4	V
D28	Output leakage current	I_{OZ11}	V_O=Hi-z state V_I=V_{DD3} or V_{SS} V_O=V_{DD3} or V_{SS}			±5	µA
	<Output: Normal buffer> CASHD, CASVD, CLK188, CLK450						
D29	High-level output voltage	V_{OH12}	I_{OH}=-0.5 mA,V_I=V_{DD2} or V_{SS}	V_{DD2} -0.4			V
D30	Low-level output voltage	V_{OL12}	I_{OL}=0.5 mA,V_I=V_{DD2} or V_{SS}			0.4	V
	<Output: Normal buffer> CLK18O1						
D31	High-level output voltage	V_{OH13}	I_{OH}=-1.0 mA,V_I=V_{DD2} or V_{SS}	V_{DD2} -0.4			V
D32	Low-level output voltage	V_{OL13}	I_{OL}=1.0 mA,V_I=V_{DD2} or V_{SS}			0.4	V

	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
	<Output: Tri-state buffer / Input: CMOS level>			MDA15 to MDA0			
D33	High-level input voltage	V_{IH14}		V_{DD3} ×0.7		V_{DD3}	V
D34	Low-level input voltage	V_{IL14}		0		V_{DD3} ×0.3	V
D35	High-level output voltage	V_{OH14}	I_{OH}=-8 mA,V_I=V_{DD3} or V_{SS}	V_{DD3} -0.6			V
D36	Low-level output voltage	V_{OL14}	I_{OL}=8 mA,V_I=V_{DD3} or V_{SS}			0.4	V
D37	Output leakage current	I_{OZ14}	V_O=Hi-z state V_I=V_{DD3} or V_{SS} V_O=V_{DD3} or V_{SS}			±5	µA
	<Output: Tri-state buffer / Input: CMOS level with pull-up resistor>			HD, VD			
D38	High-level input voltage	V_{IH15}		V_{DD3} ×0.7		V_{DD3}	V
D39	Low-level input voltage	V_{IL115}		0		V_{DD3} ×0.3	V
D40	Input pull-up resistor	R_{PU15}	V_I=0.0 V	33	100	300	kΩ
D41	High-level output voltage	V_{OH15}	I_{OH}=-4 mA,V_I=V_{DD3} or V_{SS}	V_{DD3} -0.6			V
D42	Low-level output voltage	V_{OL15}	I_{OL}=4 mA,V_I=V_{DD3} or V_{SS}			0.4	V
D43	Output leakage current	I_{OZ15}	V_O=pull-up state V_I=V_{DD3} or V_{SS} V_O=V_{DD3}			±10	µA

Parameter	Symbol	Conditions	Limits			Unit
			Min	Typ	Max	

<Output: Tri-state buffer / Input: CMOS level with pull-down resistor>

TESTIO9 to TESTIO0

D44	High-level input voltage	V_{IH16}		V_{DD3} ×0.7		V_{DD3}	V
D45	Low-level input voltage	V_{IL116}		0		V_{DD3} ×0.3	V
D46	Input pull-down resistor	R_{PD16}	$V_I=V_{DD3}$	33	100	300	kΩ
D47	High-level output voltage	V_{OH16}	I_{OH}=-4 mA,$V_I=V_{DD3}$ or V_{SS}	V_{DD3} -0.6			V
D48	Low-level output voltage	V_{OL16}	I_{OL}=4 mA,$V_I=V_{DD3}$ or V_{SS}			0.4	V
D49	Output leakage current	I_{OZ16}	V_O=pull-down state $V_I=V_{DD3}$ or V_{SS} $V_O=V_{SS}$			±10	µA

<Output: Tri-state buffer / Input: CMOS level schmitt>

MAD6 to MAD0, MCSALE, MNRE, MNWENBW, MICOMSEL, NC3

D50	High-level output voltage	V_{OH17}	I_{OH}=-4 mA,$V_I=V_{DD3}$ or V_{SS}	V_{DD3} -0.6			V
D51	Low-level output voltage	V_{OL17}	I_{OL}=4 mA,$V_I=V_{DD3}$ or V_{SS}			0.4	V
D52	Output leakage current	I_{OZ17}	V_O=Hi-z state $V_I=V_{DD3}$ or V_{SS} $V_O=V_{DD3}$ or V_{SS}			±5	µA

	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
	<Output: Tri-state buffer / Input: CMOS level with pull-down resistor>						
	DSF7 to DSF0						
D53	High-level input voltage	V_{IH18}		V_{DD2} ×0.7		V_{DD2}	V
D54	Low-level input voltage	V_{IL118}		0		V_{DD2} ×0.3	V
D55	Input pull-down resistor	R_{PD18}	$V_I=V_{DD3}$	33	100	300	kΩ
D56	High-level output voltage	V_{OH18}	I_{OH}=-1.0 mA,$V_I=V_{DD2}$ or V_{SS}	V_{DD2} -0.4			V
D57	Low-level output voltage	V_{OL18}	I_{OL}=1.0 mA,$V_I=V_{DD2}$ or V_{SS}			0.4	V
D58	Output leakage current	I_{OZ18}	V_O=pull-down state $V_I=V_{DD3}$ or V_{SS} $V_O=V_{DD3}$			±10	μA
	<Oscillator circuit>						
	CLK27XO						
D59	Internal feedback resistor	R_{f7}	$V_I=V_{DD3}$ or V_{SS} V_{DD3}=3.3 V	0.33	1.00	3.00	MΩ

(2) AC Characteristics

(Under the recommended operating conditions)

	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
	<R656 digital video input> R656IN7 to R656IN0						
D60	Input setup time	t_{S1}	Fig. 3-1	10.0			ns
D61	Input hold time	t_{H1}		5.0			ns
	<R656 digital video output> R656OUT to R656OUT0						
D62	Output delay time	t_{D2}	Fig. 3-1	5.0		27.0	ns
	<DV video input> DSF7 to DSF0						
D63	Input setup time	t_{S3}	Fig. 3-2	10.0			ns
D64	Input hold time	t_{H3}		5.0			ns
	<DV control signal input> CASHD, CASVD						
D65	Output delay time	t_{D4}	Fig. 3-2	5.0		45.0	ns
	<DV control signal input> FRP						
D66	Output delay time	t_{D5}	Fig. 3-2	5.0		45.0	ns

E. Analog Characteristics

(AV_{DD} = 3.3 V, AV_{SS} = 0 V, Ta = 25℃)

	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
	<10-bit A/D converter> VIDEO, CIN						
E1	Low-level reference voltage	V_{REFL1}		AV_{SS}	0.5		V
E2	High-level reference voltage	V_{REFH1}			2.5	AV_{DD}	V
E3	Integral nonlinearity	NLE1	f_{ADCK1}=27.0 MHz V_{REFH}=2.5 V V_{REFL}=0.5 V		±6.0	±8.0	LSB
E4	Differential nonlinearity	DNLE1	f_{ADCK1}=27.0 MHz V_{REFH}=2.5 V V_{REFL}=0.5 V		±2.0	±4.0	LSB
E5	Clock frequency	f_{ADCK1}				27	MHz
	<10-bit high-speed D/A converter>						
E6	Zero-scale output voltage	V_{ZS2}	V_{REF}=1.235 V D9 to D0＝ALL "L"		0		V[p-p]
E7	Full-scale output voltage	V_{FS2}	V_{REF}=1.235 V D9 to D0＝ALL "H"		1.0		V[p-p]
E8	Integral nonlinearity	NLE2	f_{ADCK2}=27 MHz V_{REF}=1.235 V		±1.5	±3.0	LSB
E9	Differential nonlinearity	DNLE2	f_{ADCK2}=27 MHz V_{REF}=1.235 V		±1.0	±3.0	LSB
E10	Clock frequency	f_{ADCK2}				27	MHz

(AV_{DD} = 3.3 V, AV_{SS} = 0 V, Ta = 25℃)

	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
	<10-bit voltage dividing type D/A converter>						
E11	Zero-scale output voltage	V_{ZS3}	D9 to D0＝ALL "L"	-0.1	0	0.1	V
E12	Full-scale output voltage	V_{FS3}	D9 to D0＝ALL "H"	3.1	3.2	3.3	V
E13	Integral nonlinearity	NLE3	f_{ADCK3}=1 MHz		±1.0	±3.0	LSB
E14	Differential nonlinearity	DNLE3	f_{ADCK3}=1 MHz		±1.0	±2.0	LSB
E15	Clock frequency	f_{ADCK3}				1	MHz

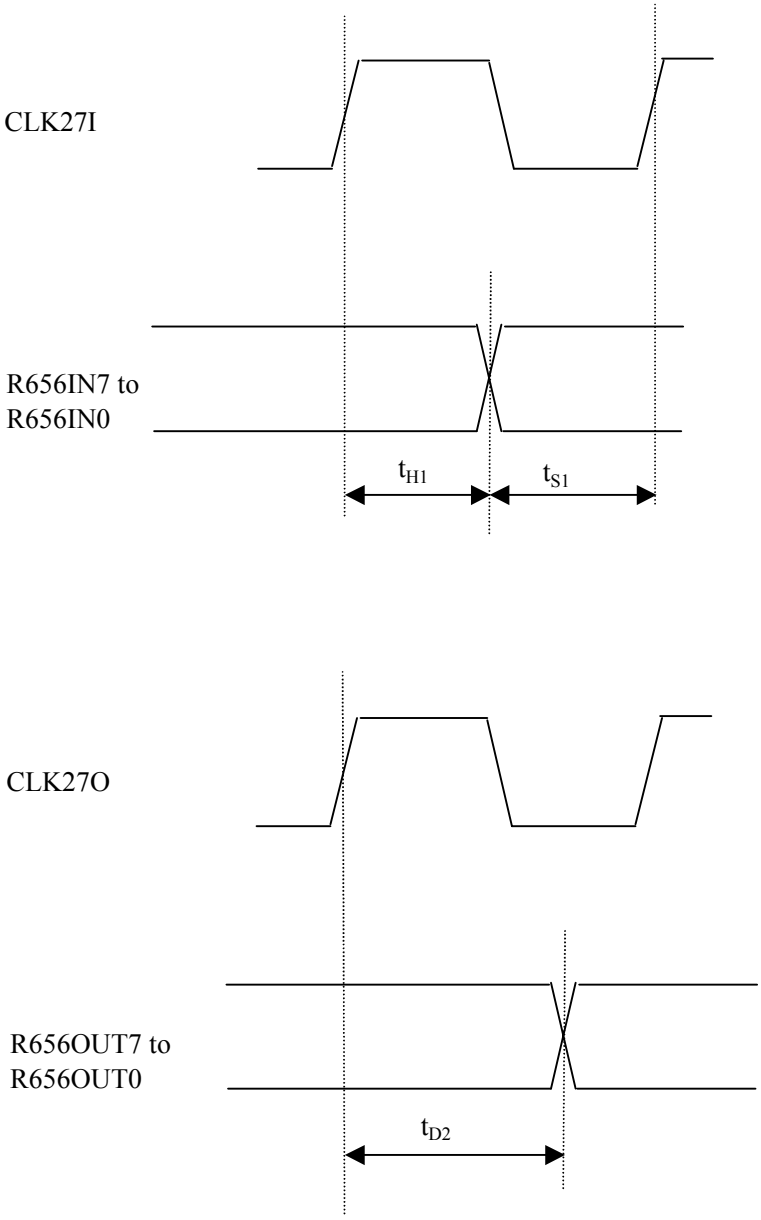


Fig. 3-1 I/O signal timing

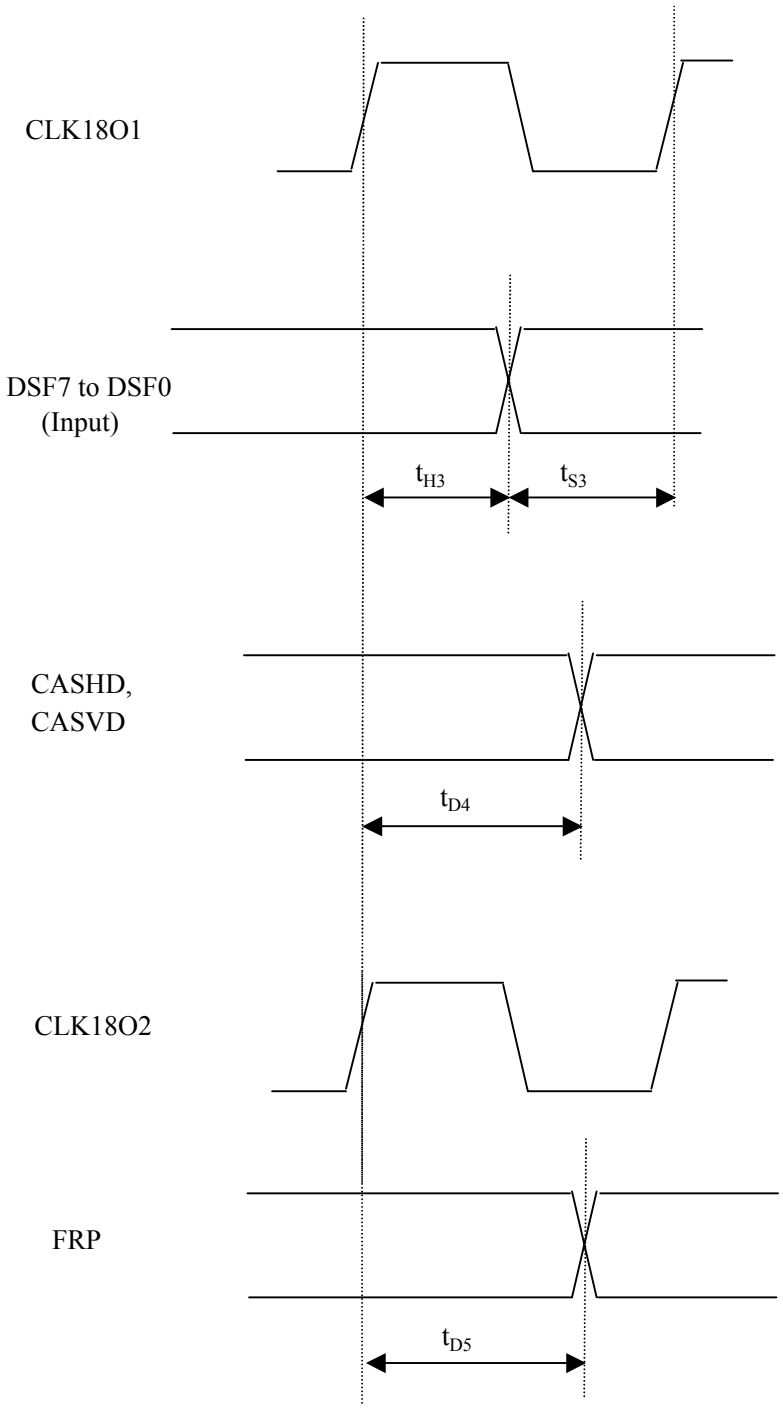


Fig. 3-2 I/O signal timing

Package Dimensions (Unit: mm)

LQFP208-P-2828 (Lead-free package)