

# DATA SHEET

## **P5Z22V10**

**5V zero power, TotalCMOS™,  
universal PLD device**

Product specification  
Supersedes data of 1997 Apr 04  
IC27 Data Handbook

1997 May 02

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# 5V zero power, TotalCMOS™, universal PLD device

# P5Z22V10

## FEATURES

- Industry's first TotalCMOS™ 22V10 – both CMOS design and process technologies
- Fast Zero Power (FZP™) design technique provides ultra-low power and high speed
  - Static current of less than 75µA
  - Dynamic current 1/10 to 1/1000 that of competing devices
  - Pin-to-pin delay of only 7.5ns
- True Zero Power device with no turbo bits or power down schemes
- Function/JEDEC map compatible with Bipolar UVCMOS EECMOS 22V10s
- Multiple packaging options featuring PCB-friendly flow-through pinouts (SOL and TSSOP)
  - 24-pin TSSOP—uses 93% less in-system space than a 28-pin PLCC
  - 24-pin SOL
  - 28-pin PLCC with standard JEDEC pin-out
- Available in commercial and industrial operating ranges
- Advanced 0.5µ E<sup>2</sup>CMOS process
- 1000 erase/program cycles guaranteed
- 20 years data retention guaranteed
- Varied product term distribution with up to 16 product terms per output for complex functions

- Programmable output polarity
- Synchronous preset/asynchronous reset capability
- Security bit prevents unauthorized access
- Electronic signature for identification
- Design entry and verification using industry standard CAE tools
- Reprogrammable using industry standard device programmers

## DESCRIPTION

The P5Z22V10 is the first SPLD to combine high performance with low power, without the need for “turbo bits” or other power down schemes. To achieve this, Philips Semiconductors has used their FZP™ design technique, which replaces conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates. This results in the combination of low power and high speed that has previously been unattainable in the PLD arena. For 3V operation, Philips Semiconductors offers the P3Z22V10 that offers high speed and low power in a 3V implementation.

The P5Z22V10 uses the familiar AND/OR logic array structure, which allows direct implementation of sum-of-products equations. This device has a programmable AND array which drives a fixed OR array. The OR sum of products feeds an “Output Macro Cell” (OMC), which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback.

## ORDERING INFORMATION

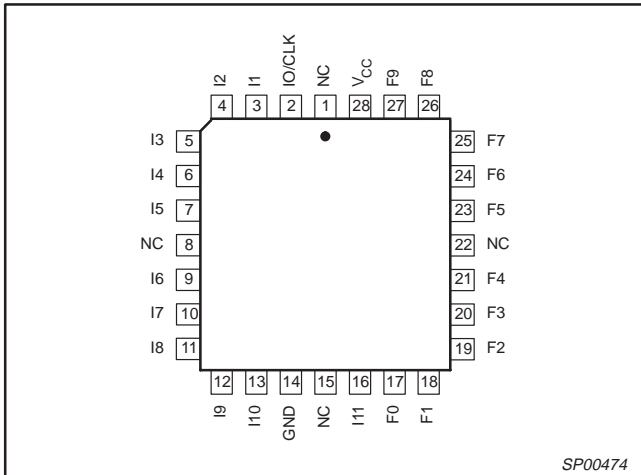
ORDER CODE	PACKAGE	PROPAGATION DELAY	TEMPERATURE RANGE	OPERATING RANGE	DRAWING NUMBER
P5Z22V10-7A	28-pin PLCC	7.5ns	0 to +70°C	V <sub>CC</sub> = 5.0V ±5%	SOT261-3
P5Z22V10-7D	24-pin SOL	7.5ns	0 to +70°C	V <sub>CC</sub> = 5.0V ±5%	SOT137-1
P5Z22V10-7DH	24-pin TSSOP	7.5ns	0 to +70°C	V <sub>CC</sub> = 5.0V ±5%	SOT355-1
P5Z22V10-DA	28-pin PLCC	10ns	0 to +70°C	V <sub>CC</sub> = 5.0V ±5%	SOT261-3
P5Z22V10-DD	24-pin SOL	10ns	0 to +70°C	V <sub>CC</sub> = 5.0V ±5%	SOT137-1
P5Z22V10-DDH	24-pin TSSOP	10ns	0 to +70°C	V <sub>CC</sub> = 5.0V ±5%	SOT355-1
P5Z22V10IDA	28-pin PLCC	10ns	-40 to +85°C	V <sub>CC</sub> = 5.0V ±10%	SOT261-3
P5Z22V10IDD	24-pin SOL	10ns	-40 to +85°C	V <sub>CC</sub> = 5.0V ±10%	SOT137-1
P5Z22V10IDDH	24-pin TSSOP	10ns	-40 to +85°C	V <sub>CC</sub> = 5.0V ±10%	SOT355-1

# 5V zero power, TotalCMOS™, universal PLD device

P5Z22V10

## PIN CONFIGURATIONS

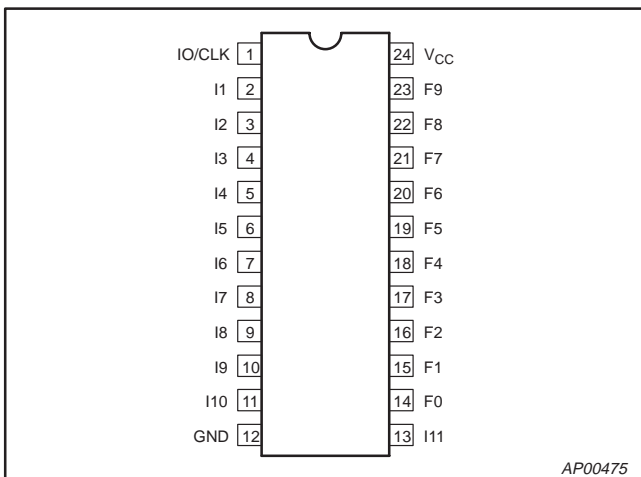
### 28-Pin PLCC



### PIN DESCRIPTIONS

PIN LABEL	DESCRIPTION
I1 – I11	Dedicated Input
NC	Not Connected
F0 – F9	Macrocell Input/Output
IO/CLK	Dedicated Input/Clock Input
V <sub>CC</sub>	Supply Voltage
GND	Ground

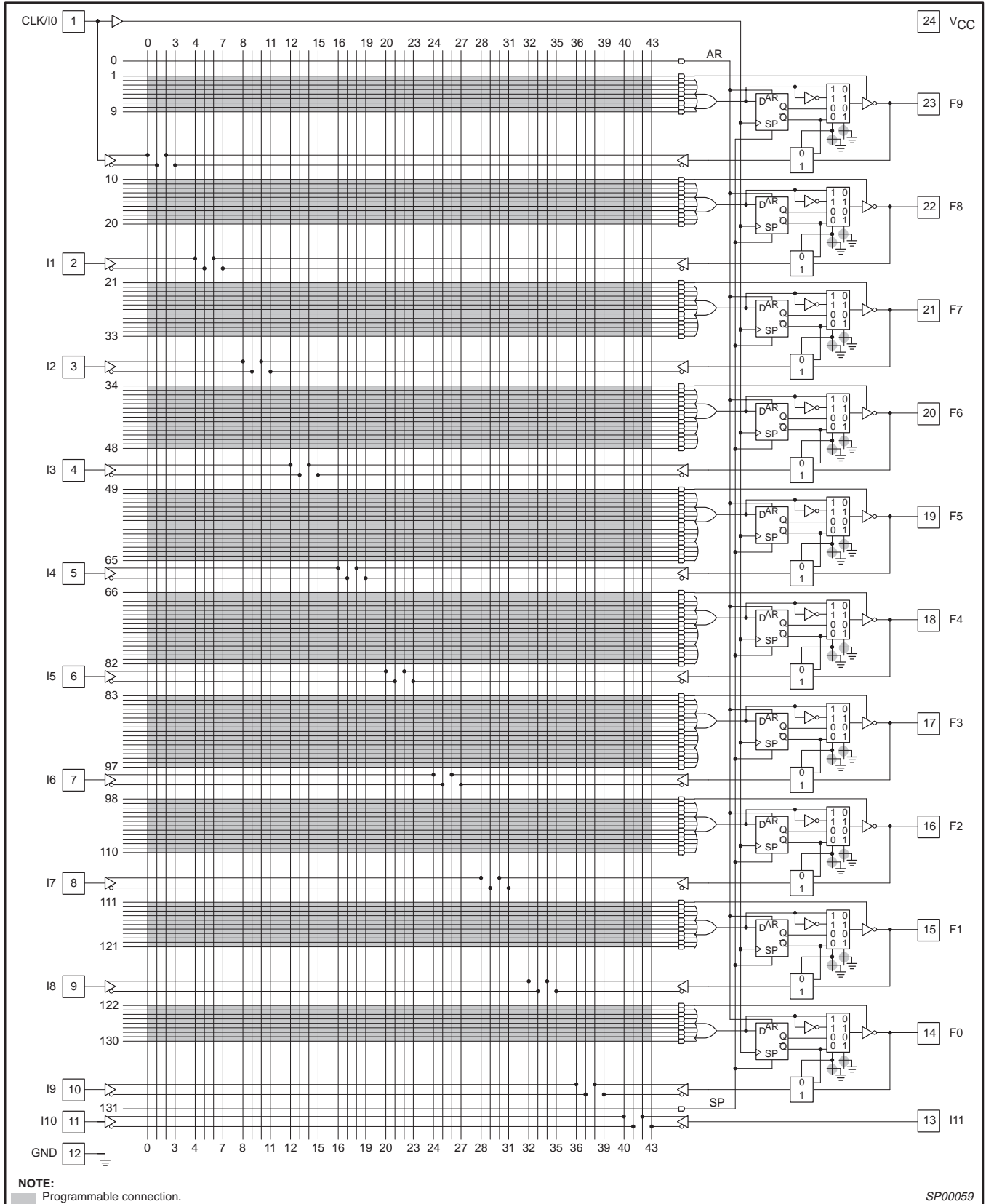
### 24-Pin SOL and 24-Pin TSSOP



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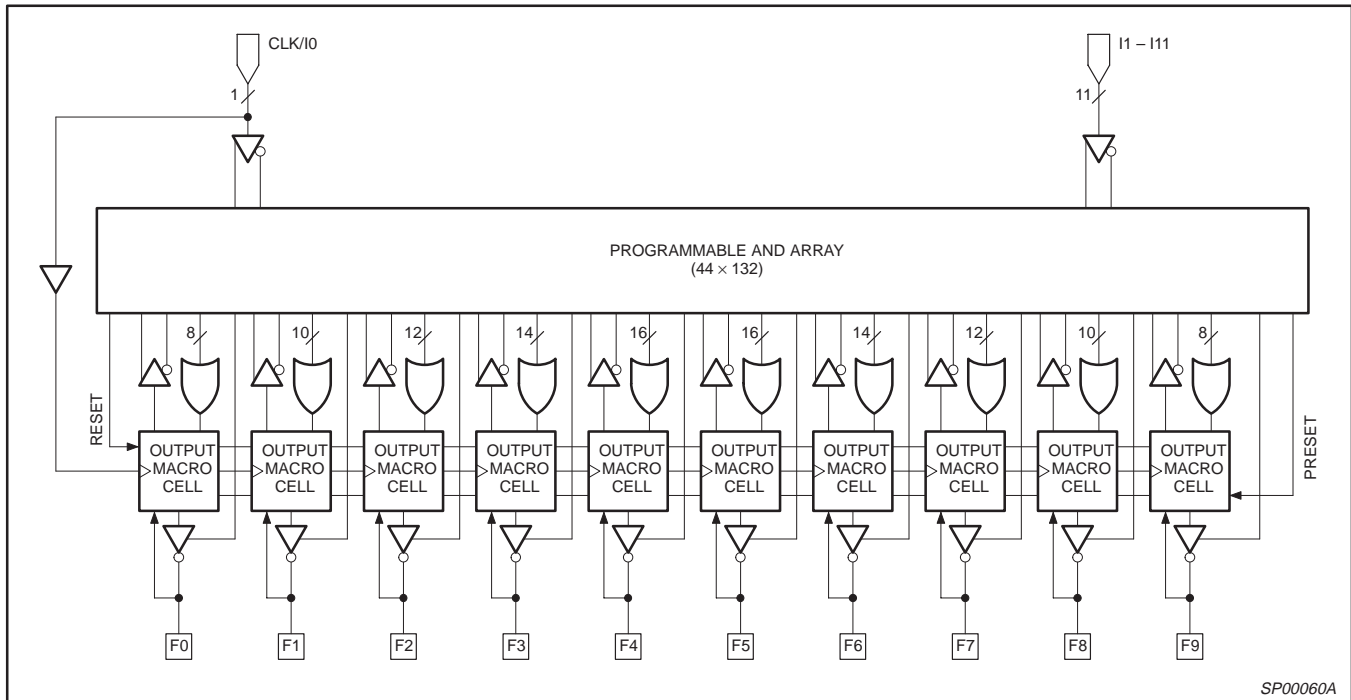
## P5Z22V10

### LOGIC DIAGRAM



# 5V zero power, TotalCMOS™, universal PLD device

# P5Z22V10



**Figure 1. Functional Diagram**

## FUNCTIONAL DESCRIPTION

The P5Z22V10 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

## ARCHITECTURE OVERVIEW

The P5Z22V10 architecture is illustrated in Figure 1. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed-OR array. With this structure, the P5Z22V10 can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 4 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions with either Active-High or Active-Low polarity.

### AND/OR Logic Array

The programmable AND array of the P5Z22V10 (shown in the Logic Diagram) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 input lines:

- 24 input lines carry the True and Complement of the signals applied to the 12 input pins
- 20 additional lines carry the True and Complement values of feedback or input signals from the 10 I/Os

132 product terms:

- 120 product terms (arranged in 2 groups of 8, 10, 12, 14, and 16) used to form logical sums
- 10 output enable terms (one for each I/O)
- 1 global synchronous preset product term
- 1 global asynchronous clear product term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the True and Complement of an input signal will always be FALSE, and thus will not affect the OR function that it drives. When all the connections on a product term are opened, a Don't Care state exists and that term will always be TRUE.

### Variable Product Term Distribution

The P5Z22V10 provides 120 product terms to drive the 10 OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see Logic Diagram). This distribution allows optimum use of device resources.

5V zero power, TotalCMOS™, universal PLD device

P5Z22V10

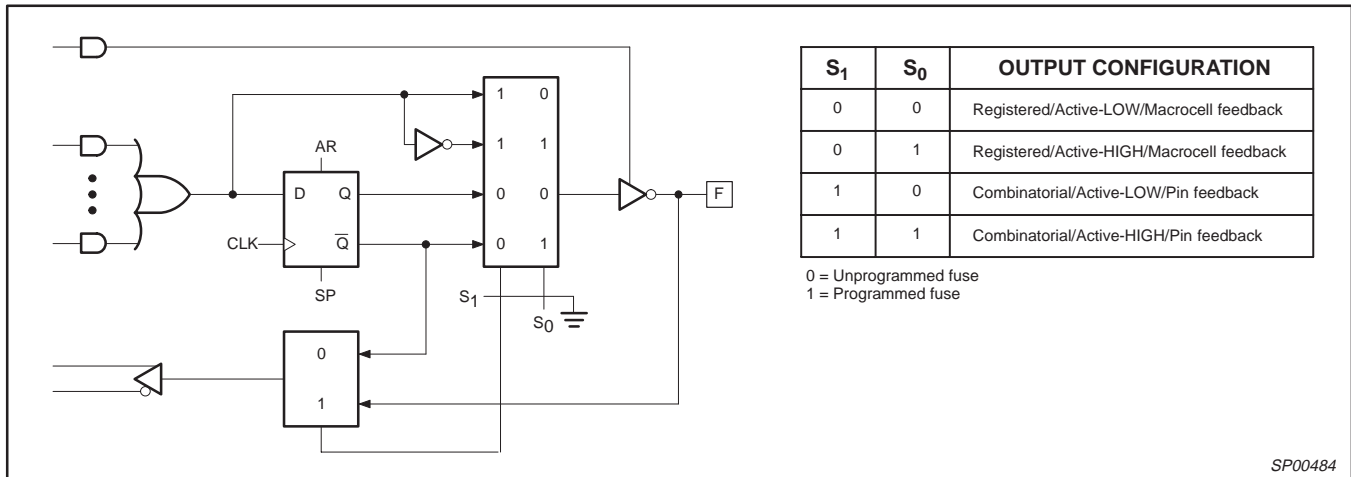


Figure 2. Output Macro Cell Logic Diagram

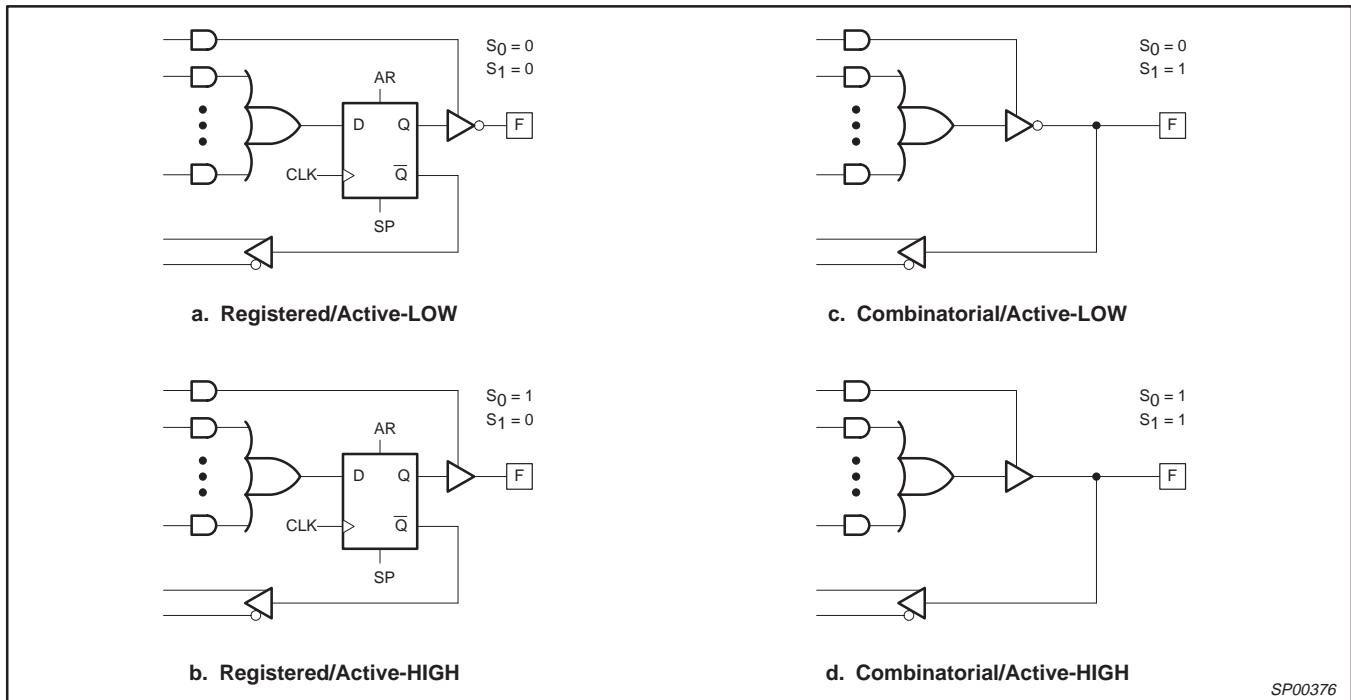


Figure 3. Output Macro Cell Configurations

**Programmable I/O Macrocell**

The output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the P5Z22V10 to the precise requirements of their designs.

**Macrocell Architecture**

Each I/O macrocell, as shown in Figure 2, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell of the P5Z22V10 is determined by the two EEPROM bits controlling these multiplexers. These bits determine output polarity, and output type (registered or non-registered). Equivalent circuits for the macrocell configurations are illustrated in Figure 3.

**Output type**

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

# 5V zero power, TotalCMOS™, universal PLD device

# P5Z22V10

### Program/Erase Cycles

The P5Z22V10 is 100% testable, erases/programs in seconds, and guarantees 1000 program/erase erase cycles.

### Output Polarity

Each macrocell can be configured to implement Active-High or Active-Low logic. Programmable polarity eliminates the need for external inverters.

### Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically FALSE and the I/O will function as a dedicated input.

### Register Feedback Select

When the I/O macrocell is configured to implement a registered function (S1 = 0) (Figures 3a or 3b), the feedback signal to the AND array is taken from the Q output.

### Bi-directional I/O Select

When configuring an I/O macrocell to implement a combinatorial function (S1 = 1) (Figures 3c or 3d), the feedback signal is taken from the I/O pin. In this case, the pin can be used as a dedicated input, a dedicated output, or a bi-directional I/O.

### Power-On Reset

To ease system initialization, all flip-flops will power-up to a reset condition and the Q output will be low. The actual output of the P5Z22V10 will depend on the programmed output polarity. The V<sub>CC</sub> rise must be monotonic.

### Design Security

The P5Z22V10 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set, it is impossible to verify (read) or program the P5Z22V10 until the entire device has first been erased with the bulk-erase function.

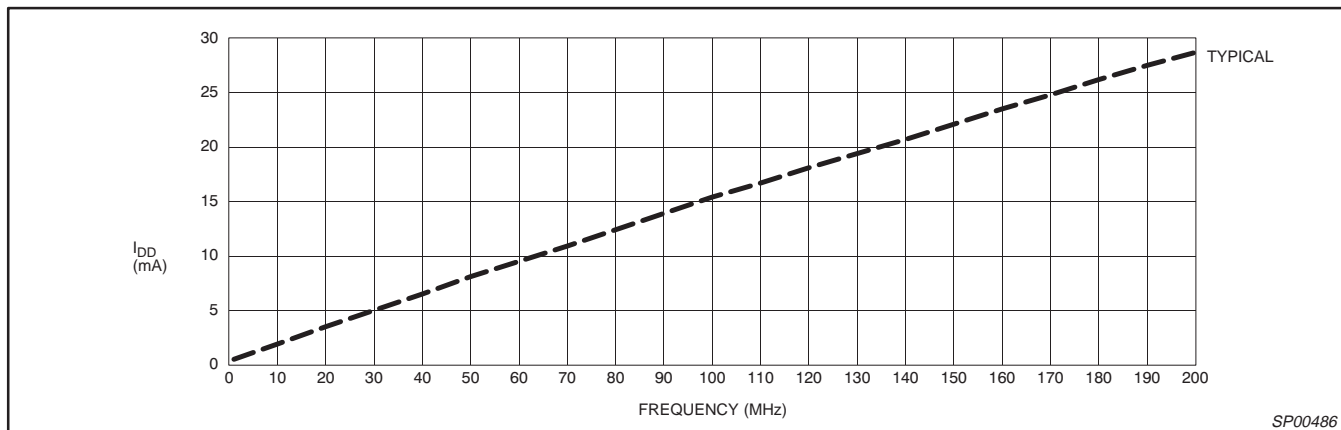
### TotalCMOS™ Design Technique for Fast Zero Power

Philips is the first to offer a TotalCMOS™ SPLD, both in process technology and design technique. Philips employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Philips to offer SPLDs which are both high performance and low power, breaking the paradigm that to have low power, you must accept low performance. Refer to Figure 4 and Table 1 showing the I<sub>DD</sub> vs. Frequency of our P5Z22V10 TotalCMOS™ SPLD.

**Table 1. Typical I<sub>DD</sub> vs. Frequency**

V<sub>DD</sub> = 5V @ 25°C

FREQUENCY (MHz)	TYPICAL I <sub>DD</sub> (mA)
1	0.5
10	1.9
20	3.5
30	5.0
40	6.5
50	8.1
60	9.5
70	10.9
80	12.4
90	13.9
100	15.4
110	16.7
120	18.1
130	19.4
140	20.7
150	22.1
160	23.5
170	24.8
180	26.2
190	27.5
200	28.7



**Figure 4. Typical I<sub>DD</sub> vs. Frequency @ V<sub>DD</sub> = 5V, 25°C (10-bit counter)**

## 5V zero power, TotalCMOS™, universal PLD device

P5Z22V10

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
V <sub>DD</sub>	Supply voltage	-0.5	7.0	V
V <sub>I</sub>	Input voltage	-1.2	V <sub>DD</sub> + 0.5	V
V <sub>OUT</sub>	Output voltage	-0.5	V <sub>DD</sub> + 0.5	V
I <sub>IN</sub>	Input current	-30	30	mA
I <sub>OUT</sub>	Output current	-100	100	mA
T <sub>R</sub>	Allowable thermal rise ambient to junction	0	75	°C
T <sub>J</sub>	Junction temperature range	-40	150	°C
T <sub>STG</sub>	Storage temperature range	-65	150	°C
ESD	Static discharge voltage (human body)		1000	V

**NOTE:**

- Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

**OPERATING RANGE**

PRODUCT GRADE	TEMPERATURE	VOLTAGE
Commercial	0 to +70°C	5.0 ± 5% V
Industrial	-40 to +85°C	5.0 ± 10% V



## 5V zero power, TotalCMOS™, universal PLD device

P5Z22V10

**DC ELECTRICAL CHARACTERISTICS FOR COMMERCIAL GRADE DEVICES**Commercial:  $0^{\circ}\text{C} \leq T_{\text{amb}} \leq +70^{\circ}\text{C}$ ;  $4.75 \leq V_{\text{DD}} \leq 5.25\text{V}$ 

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
$V_{\text{IL}}$	Input voltage low	$V_{\text{DD}} = 4.75\text{V}$			0.8	V
$V_{\text{IH}}$	Input voltage high	$V_{\text{DD}} = 5.25\text{V}$	2			V
$V_{\text{I}}$	Input clamp voltage	$V_{\text{DD}} = 4.75\text{V}$ ; $I_{\text{IN}} = -18\text{mA}$			-1.2	V
$V_{\text{OL}}$	Output voltage low	$V_{\text{DD}} = 4.75\text{V}$ ; $I_{\text{OL}} = 8\text{mA}$			0.5	V
$V_{\text{OH}}$	Output voltage high	$V_{\text{DD}} = 4.75\text{V}$ ; $I_{\text{OL}} = -4\text{mA}$	2.4			V
$I_{\text{I}}$	Input leakage current	$V_{\text{IN}} = 0$ to $V_{\text{DD}}$	-10		10	$\mu\text{A}$
$I_{\text{OZ}}$	3-States output leakage current	$V_{\text{IN}} = 0$ to $V_{\text{DD}}$	-10		10	$\mu\text{A}$
$I_{\text{DDQ}}$	Standby current	$V_{\text{DD}} = 5.25\text{V}$ ; $T_{\text{amb}} = 0^{\circ}\text{C}$		60	75	$\mu\text{A}$
$I_{\text{DDD}}^1$	Dynamic current	$V_{\text{DD}} = 5.25\text{V}$ ; $T_{\text{amb}} = 0^{\circ}\text{C}$ @ 1MHz		1	2	mA
		$V_{\text{DD}} = 5.25\text{V}$ ; $T_{\text{amb}} = 0^{\circ}\text{C}$ @ 50MHz		10	15	mA
$I_{\text{SC}}$	Short circuit output current	1 pin/time for no longer than 1 second	-30		-100	mA
$C_{\text{IN}}$	Input pin capacitance	$T_{\text{amb}} = 25^{\circ}\text{C}$ ; $f = 1\text{MHz}$			10	pF
$C_{\text{CLK}}$	Clock input capacitance	$T_{\text{amb}} = 25^{\circ}\text{C}$ ; $f = 1\text{MHz}$	5		12	pF
$C_{\text{I/O}}$	I/O pin capacitance	$T_{\text{amb}} = 25^{\circ}\text{C}$ ; $f = 1\text{MHz}$			10	pF

**NOTE:**

- These parameters measured with a 10-bit up counter, with all outputs enabled and unloaded. Inputs are tied to  $V_{\text{DD}}$  or ground. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where current may be affected.

**AC ELECTRICAL CHARACTERISTICS FOR COMMERCIAL GRADE DEVICES**Commercial:  $0^{\circ}\text{C} \leq T_{\text{amb}} \leq +70^{\circ}\text{C}$ ;  $4.75 \leq V_{\text{DD}} \leq 5.25\text{V}$ 

SYMBOL	PARAMETER	-7		D		UNIT
		MIN.	MAX.	MIN.	MAX.	
$t_{\text{PD}}$	Input or feedback to non-registered output		7.5		10	ns
$t_{\text{SU}}$	Setup time from input, feedback or SP to Clock	3		4		ns
$t_{\text{CO}}$	Clock to output		6.75		8	ns
$t_{\text{CF}}$	Clock to feedback <sup>1</sup>		2		3	ns
$t_{\text{H}}$	Hold time		0		0	ns
$t_{\text{AR}}$	Asynchronous Reset to registered output		15		15	ns
$t_{\text{ARW}}$	Asynchronous Reset width	5		5		ns
$t_{\text{ARR}}$	Asynchronous Reset recovery time		5		5	ns
$t_{\text{SPR}}$	Synchronous Preset recovery time		5		5	ns
$t_{\text{WL}}$	Width of Clock LOW	3		3		ns
$t_{\text{WH}}$	Width of Clock HIGH	3		3		ns
$t_{\text{R}}$	Input rise time		20		20	ns
$t_{\text{F}}$	Input fall time		20		20	ns
$f_{\text{MAX1}}$	Maximum internal frequency <sup>2</sup> $1/(t_{\text{SU}} + t_{\text{CF}})$	200		143		MHz
$f_{\text{MAX2}}$	Maximum external frequency <sup>1</sup> $1/(t_{\text{SU}} + t_{\text{CO}})$	103		83		MHz
$f_{\text{MAX3}}$	Maximum clock frequency <sup>1</sup> $1/(t_{\text{WL}} + t_{\text{WH}})$	167		167		MHz
$t_{\text{EA}}$	Input to Output Enable		9		10	ns
$t_{\text{ER}}$	Input to Output Disable		9		10	ns
<b>Capacitance</b>						
$C_{\text{IN}}$	Input pin capacitance		10		10	pF
$C_{\text{OUT}}$	Output capacitance		12		12	pF

**NOTES:**

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## 5V zero power, TotalCMOS™, universal PLD device

P5Z22V10

**DC ELECTRICAL CHARACTERISTICS FOR INDUSTRIAL GRADE DEVICES**Industrial:  $-40^{\circ}\text{C} \leq T_{\text{amb}} \leq +85^{\circ}\text{C}$ ;  $4.5 \leq V_{\text{DD}} \leq 5.5\text{V}$ 

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
$V_{\text{IL}}$	Input voltage low	$V_{\text{DD}} = 4.5\text{V}$			0.8	V
$V_{\text{IH}}$	Input voltage high	$V_{\text{DD}} = 5.5\text{V}$	2			V
$V_{\text{I}}$	Input clamp voltage	$V_{\text{DD}} = 4.5\text{V}$ ; $I_{\text{IN}} = -18\text{mA}$			-1.2	V
$V_{\text{OL}}$	Output voltage low	$V_{\text{DD}} = 4.5\text{V}$ ; $I_{\text{OL}} = 8\text{mA}$			0.5	V
$V_{\text{OH}}$	Output voltage high	$V_{\text{DD}} = 4.5\text{V}$ ; $I_{\text{OL}} = -4\text{mA}$	2.4			V
$I_{\text{I}}$	Input leakage current	$V_{\text{IN}} = 0$ to $V_{\text{DD}}$	-10		10	$\mu\text{A}$
$I_{\text{OZ}}$	3-States output leakage current	$V_{\text{IN}} = 0$ to $V_{\text{DD}}$	-10		10	$\mu\text{A}$
$I_{\text{DDQ}}$	Standby current	$V_{\text{DD}} = 5.5\text{V}$ ; $T_{\text{amb}} = -40^{\circ}\text{C}$		70	95	$\mu\text{A}$
$I_{\text{DDD}}^1$	Dynamic current	$V_{\text{DD}} = 5.5\text{V}$ ; $T_{\text{amb}} = -40^{\circ}\text{C}$ @ 1MHz		1	3	mA
		$V_{\text{DD}} = 5.5\text{V}$ ; $T_{\text{amb}} = -40^{\circ}\text{C}$ @ 50MHz		10	20	mA
$I_{\text{SC}}$	Short circuit output current	1 pin/time for no longer than 1 second	-30		-100	mA
$C_{\text{IN}}$	Input pin capacitance	$T_{\text{amb}} = 25^{\circ}\text{C}$ ; $f = 1\text{MHz}$			10	pF
$C_{\text{CLK}}$	Clock input capacitance	$T_{\text{amb}} = 25^{\circ}\text{C}$ ; $f = 1\text{MHz}$	5		12	pF
$C_{\text{I/O}}$	I/O pin capacitance	$T_{\text{amb}} = 25^{\circ}\text{C}$ ; $f = 1\text{MHz}$			10	pF

**NOTE:**

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SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
$t_{\text{PD}}$	Input or feedback to non-registered output		10	ns
$t_{\text{SU}}$	Setup time from input, feedback or SP to Clock	5		ns
$t_{\text{CO}}$	Clock to output		8.5	ns
$t_{\text{CF}}$	Clock to feedback <sup>1</sup>		4	ns
$t_{\text{H}}$	Hold time		0	ns
$t_{\text{AR}}$	Asynchronous Reset to registered output		15	ns
$t_{\text{ARW}}$	Asynchronous Reset width	5		ns
$t_{\text{ARR}}$	Asynchronous Reset recovery time		5	ns
$t_{\text{SPR}}$	Synchronous Preset recovery time		5	ns
$t_{\text{WL}}$	Width of Clock LOW	3		ns
$t_{\text{WH}}$	Width of Clock HIGH	3		ns
$t_{\text{R}}$	Input rise time		20	ns
$t_{\text{F}}$	Input fall time		20	ns
$f_{\text{MAX1}}$	Maximum internal frequency <sup>2</sup> $1/(t_{\text{SU}} + t_{\text{CF}})$	111		MHz
$f_{\text{MAX2}}$	Maximum external frequency <sup>1</sup> $1/(t_{\text{SU}} + t_{\text{CO}})$	74		MHz
$f_{\text{MAX3}}$	Maximum clock frequency <sup>1</sup> $1/(t_{\text{WL}} + t_{\text{WH}})$	167		MHz
$t_{\text{EA}}$	Input to Output Enable		11	ns
$t_{\text{ER}}$	Input to Output Disable		11	ns
<b>Capacitance</b>				
$C_{\text{IN}}$	Input pin capacitance		10	pF
$C_{\text{OUT}}$	Output capacitance		12	pF

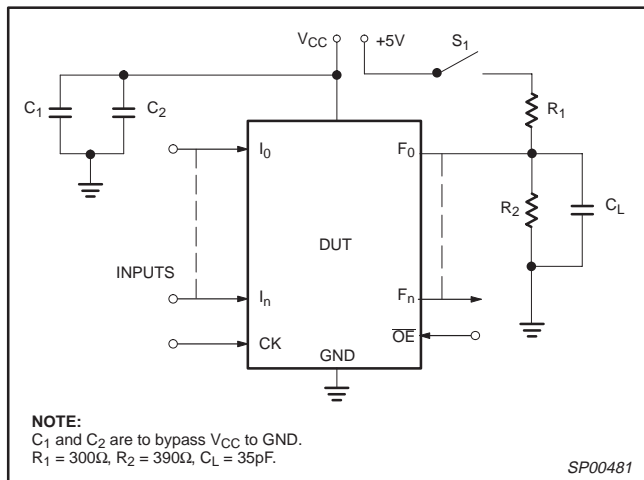
**NOTES:**

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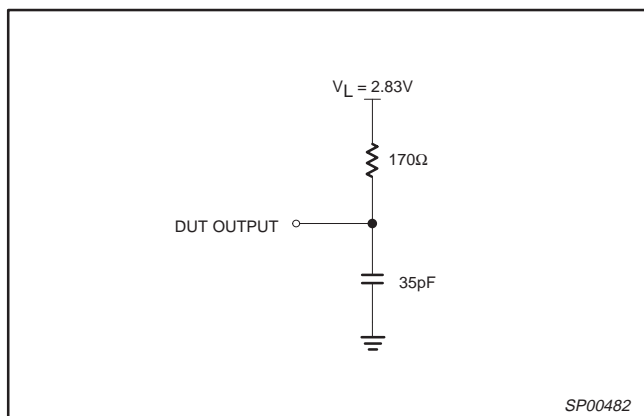
# 5V zero power, TotalCMOS™, universal PLD device

P5Z22V10

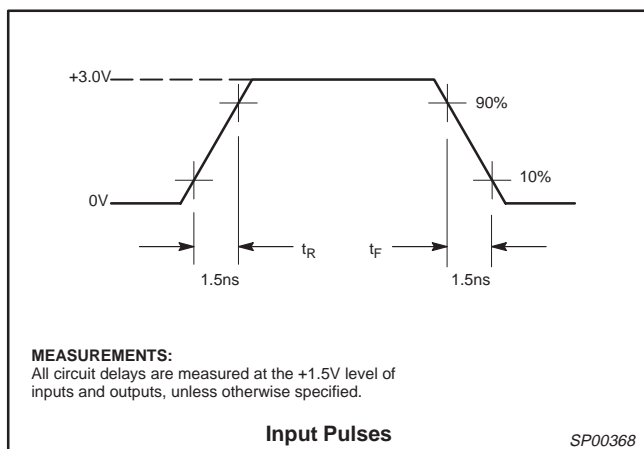
## TEST LOAD CIRCUIT



## THEVENIN EQUIVALENT



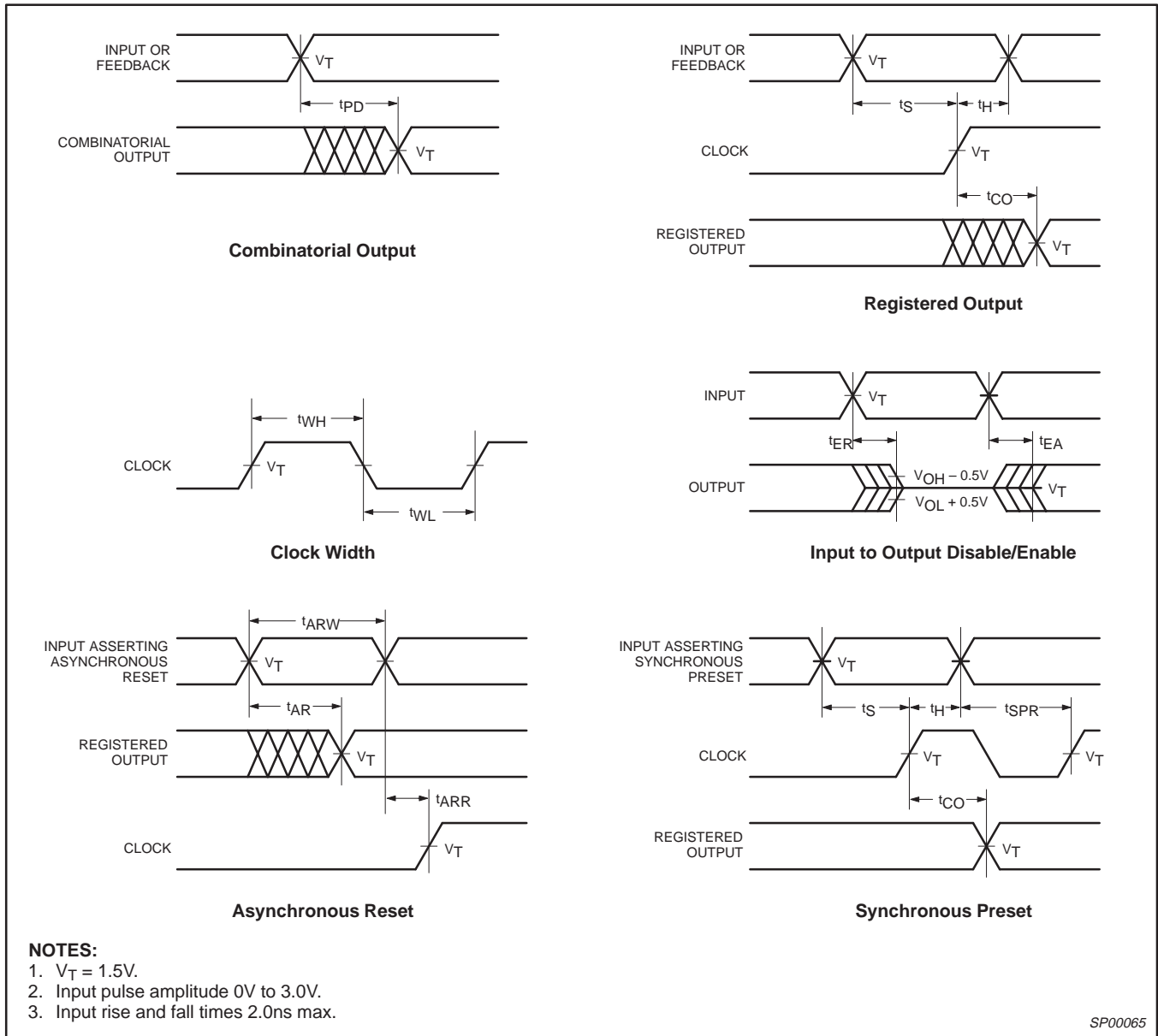
## VOLTAGE WAVEFORM



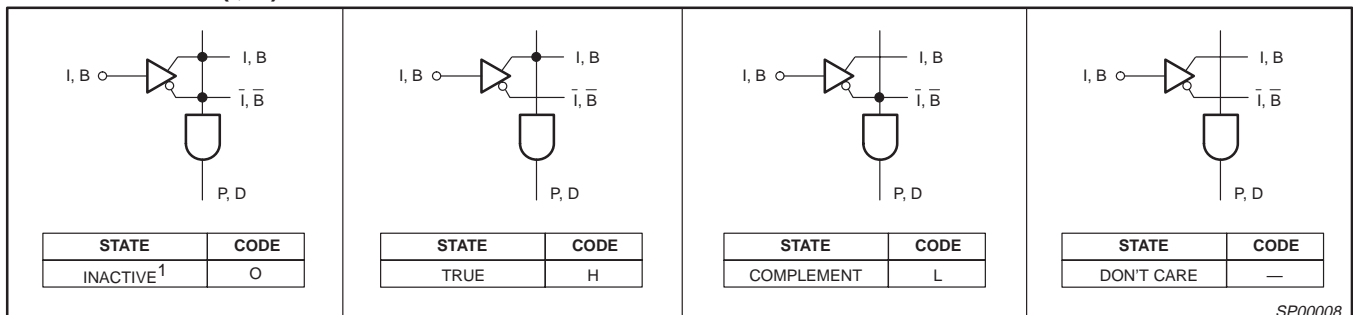
5V zero power, TotalCMOS™, universal PLD device

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SWITCHING WAVEFORMS



“AND” ARRAY – (I, B)



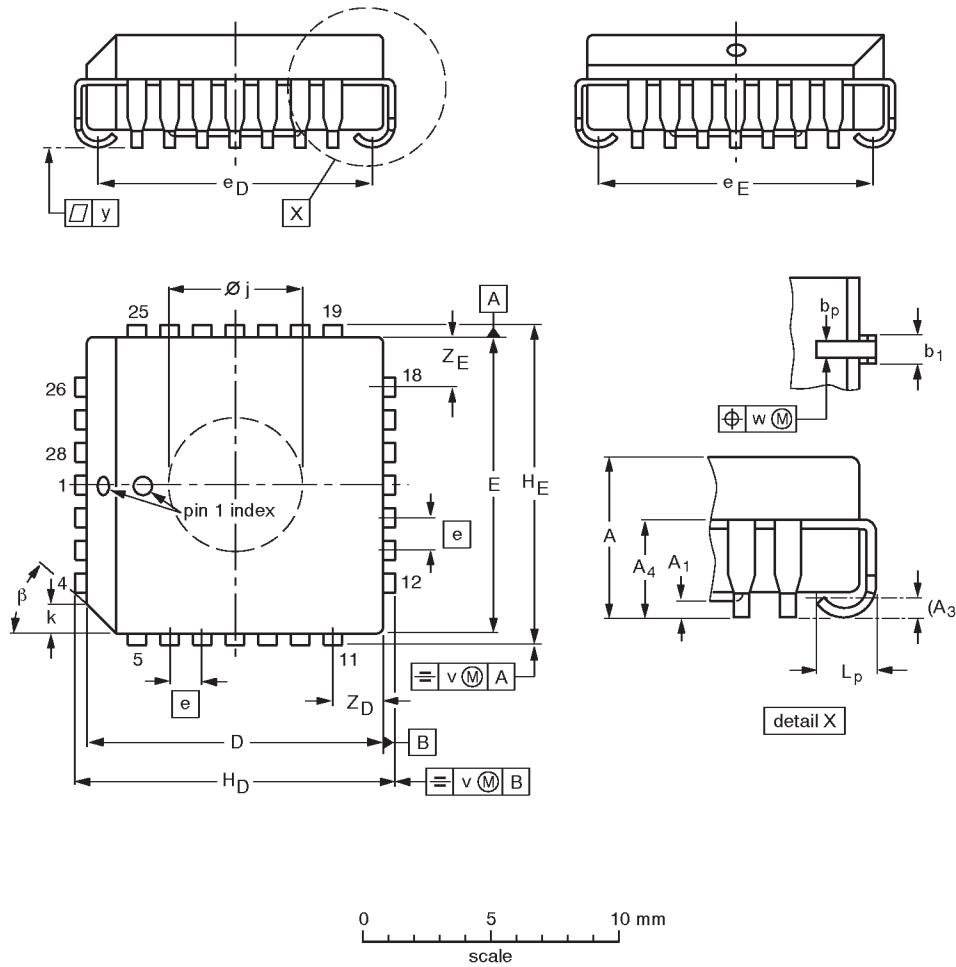
**NOTE:**  
1. This is the initial state.

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P5Z22V10

PLCC28: plastic leaded chip carrier; 28 leads; pedestal

SOT261-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A <sub>1</sub> min.	A <sub>3</sub>	A <sub>4</sub> max.	b <sub>p</sub>	b <sub>1</sub>	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>D</sub>	e <sub>E</sub>	H <sub>D</sub>	H <sub>E</sub>	k	∅ <sub>j</sub>	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup> max.	Z <sub>E</sub> <sup>(1)</sup> max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	5.69 5.54	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.224 0.218	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

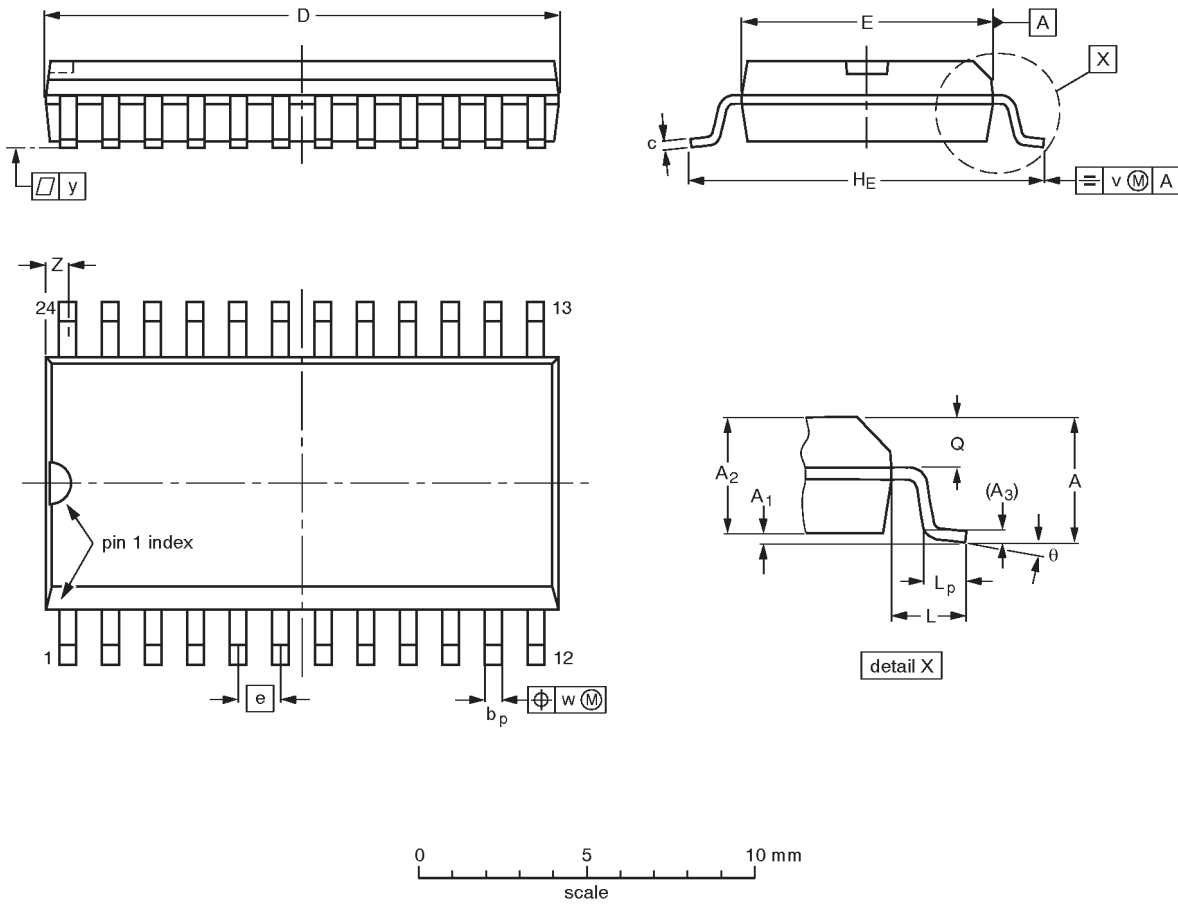
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT261-3		MO-047AB				92-11-17 95-02-25

5V zero power, TotalCMOS™, universal PLD device

P5Z22V10

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	HE	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

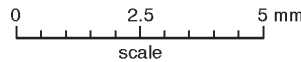
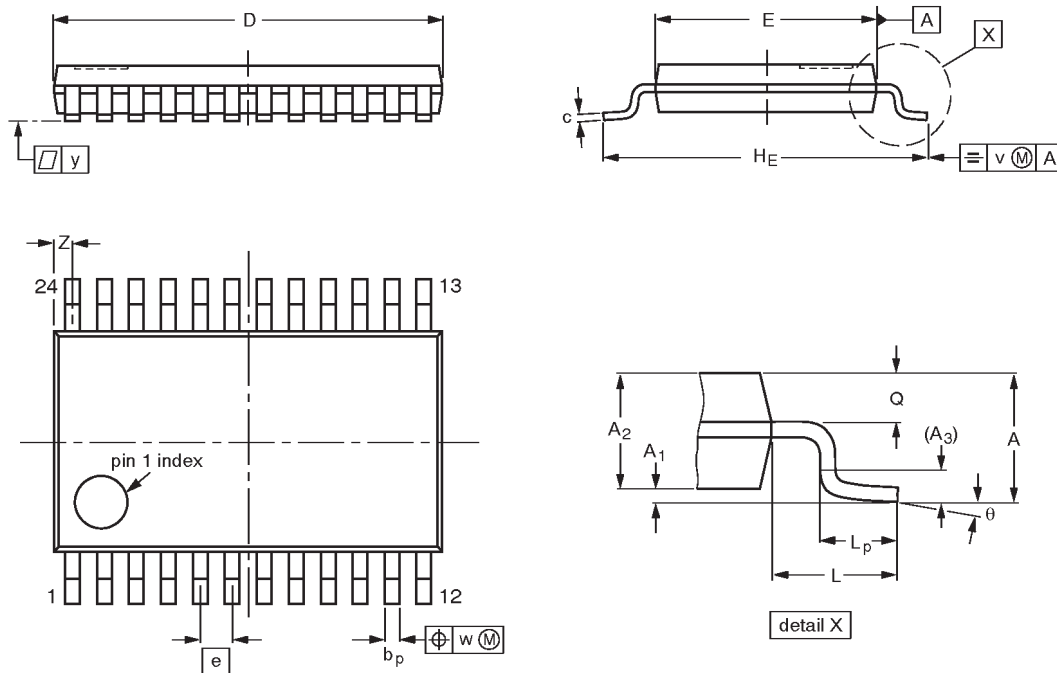
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				-92-11-17 95-01-24

5V zero power, TotalCMOS™, universal PLD device

P5Z22V10

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



**DIMENSIONS** (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				93-06-16 95-02-04

## 5V zero power, TotalCMOS™, universal PLD device

P5Z22V10

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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