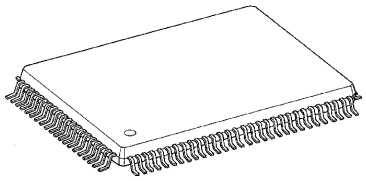
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC90A18AF

TIME COMPRESSION LSI FOR EDTV-II WIDE-SCREEN TVs

TC90A18AF is a time-compression LSI for wide-screen TVs. With a compression ratio of 0.5 to 2, the device can display a 4:3 aspect ratio NTSC / PAL signal on a 16:9 aspect ratio TV screen.
Using horizontal 16-point variable compression, this LSI can realize digital super live mode.
Among the wide range of functions offered by the LSI are EDTV-II broadcast detection, letterbox detection, and caption detection.



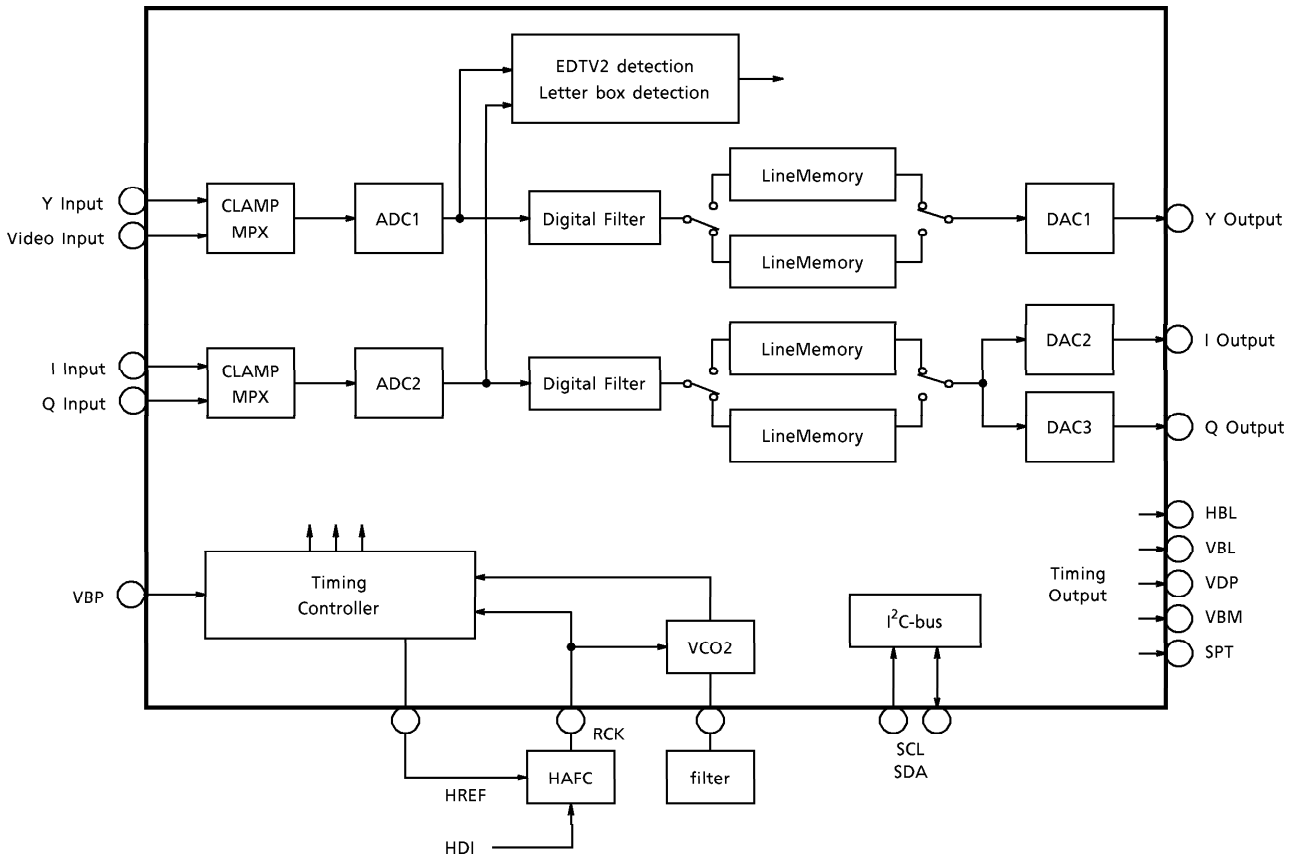
QFP100-P-1420-0.65A

Weight : 1.6 g (Typ.)

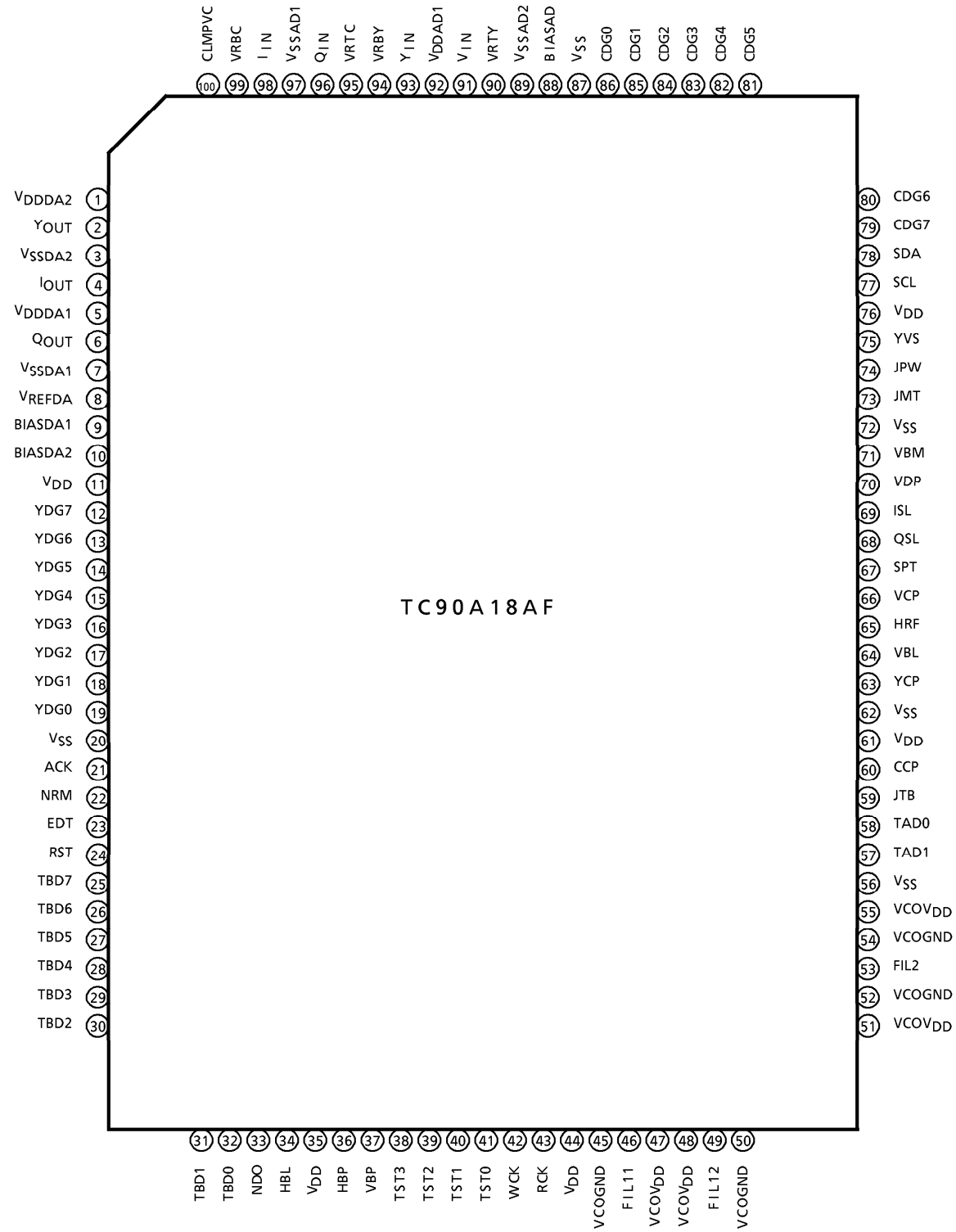
FEATURES

- Fixed ratio compression processing
  - 0.5 to 1 × fixed ratio compression (64 steps)
  - 1 to 1.5 × fixed ratio expansion (32 steps)
  - 2 × expansion
- Digital super live mode
  - Compression and expansion with specified ratio within a horizontal period (16 points settable)
- EDTV-II
  - NRZ pattern detection
  - DC offset detection
  - Top and bottom blank portion detection
- Letterbox detection
- Caption detection
- Incorporates two 8-bit ADCs for Y / V and I / Q inputs
- Incorporates three 8-bit DACs for Y, I, and Q outputs
- Incorporates 1368fHVCO
- I^2C bus control (slave address : 40H)
- 3.3 V single power supply

BLOCK DIAGRAM



TERMINAL CONNECTION DIAGRAM



TERMINAL FUNCTION

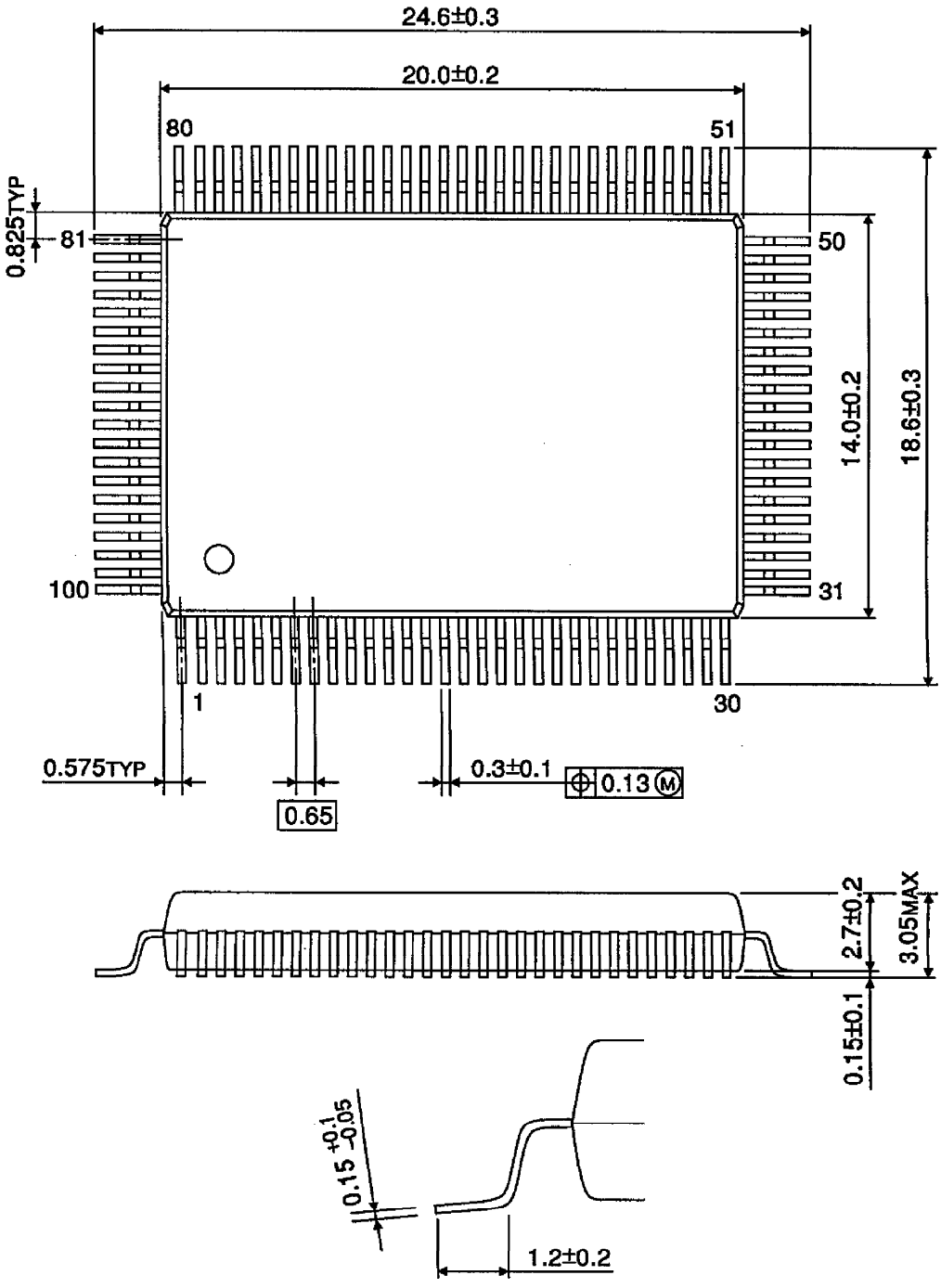
PIN No.	PIN NAME	I / O	FUNCTION	OPERATING CONDITIONS
1	V_{DDDA2}	—	Analog power supply	+3.3 V
2	Y_{OUT}	—	Luminance signal analog output	D range : V_{DD} to V_{REFDA}
3	V_{SSDA2}	—	Analog GND	—
4	I_{OUT}	—	I signal analog output	D range : V_{DD} to V_{REFDA}
5	V_{DDDA1}	—	Analog power supply	+3.3 V
6	Q_{OUT}	—	Q signal analog output	D range : V_{DD} to V_{REFDA}
7	V_{SSDA1}	—	Analog GND	—
8	V_{REFDA}	—	DAC reference voltage supply pin	V_{DD} − 1.5 V
9	BIASDA1	—	DAC bias voltage pin 1	—
10	BIASDA2	—	DAC bias voltage pin 2	—
11	V_{DD}	I	Digital power supply	+3.3 V
12	YDG7	I	Test input (normally connect to V_{SS})	—
13	YDG6	I	Test input (normally connect to V_{SS})	—
14	YDG5	I	Test input (normally connect to V_{SS})	—
15	YDG4	I	Test input (normally connect to V_{SS})	—
16	YDG3	I	Test input (normally connect to V_{SS})	—
17	YDG2	I	Test input (normally connect to V_{SS})	—
18	YDG1	I	Test input (normally connect to V_{SS})	—
19	YDG0	I	Test input (normally connect to V_{SS})	—
20	V_{SS}	—	Digital GND	—
21	ACK	O	Test output	—
22	NRM	O	I^2C bus subaddress 30H : NRM contents output (data from microcontroller)	—
23	EDT	O	Unmatch output of ED2 signal NRZ pattern (for each field, unmatch : L, match : H)	—
24	RST	I	System reset input (normal : H, reset : L)	—
25	TBD7	I	Test input (normally connect to V_{SS})	—
26	TBD6	I	Test input (normally connect to V_{SS})	—
27	TBD5	I	Test input (normally connect to V_{SS})	—
28	TBD4	I	Test input (normally connect to V_{SS})	—
29	TBD3	I	Test input (normally connect to V_{SS})	—
30	TBD2	I	Test input (normally connect to V_{SS})	—
31	TBD1	I	Test input (normally connect to V_{SS})	—
32	TBD0	I	Test input (normally connect to V_{SS})	—
33	NDO	O	Test output	—
34	HBL	O	Horizontal blanking signal output	—
35	V_{DD}	—	Digital power supply	—
36	HBP	I	Horizontal sync signal input	—
37	VBP	I	Vertical sync signal input	—
38	TST3	I	Test mode setting (normally connect to V_{DD})	—
39	TST2	I	Test mode setting (normally connect to V_{SS})	—
40	TST1	I	Test mode setting (normally connect to V_{DD})	—

PIN No.	PIN NAME	I / O	FUNCTION	OPERATING CONDITIONS
41	TST0	I	Test mode setting (normally connect to V_{DD})	—
42	WCK	I	Test input (normally connect to V_{SS})	—
43	RCK	I	Memory read clock input (1824fH)	—
44	V_{DD}	—	Digital power supply	+3.3 V
45	VCOGND	—	VCO GND	—
46	FIL11	—	External filter pin 1 for VCO1	—
47	$VCOV_{DD}$	—	VCO power supply	+3.3 V
48	$VCOV_{DD}$	—	VCO power supply	+3.3 V
49	FIL12	—	External filter pin 2 for VCO1	—
50	VCOGND	—	VCO GND	—
51	$VCOV_{DD}$	—	VCO power supply	+3.3 V
52	VCOGND	—	VCO GND	—
53	FIL2	—	External filter pin for VCO2	—
54	VCOGND	—	VCO GND	—
55	$VCOV_{DD}$	—	VCO power supply	+3.3 V
56	V_{SS}	—	Digital GND	—
57	TAD1	O	Test output	—
58	TAD0	O	Test output	—
59	JTB	O	Timing signal for caption position	—
60	CCP	O	I^2C bus acknowledge output (active H)	—
61	V_{DD}	—	Digital power supply	+3.3 V
62	V_{SS}	—	Digital GND	—
63	YCP	O	Clamp pulse position output for luminance	—
64	VBL	O	Vertical blanking signal output	—
65	HRF	O	Horizontal AFC reference signal output	—
66	VCP	O	Clamp pulse position output for video	—
67	SPT	O	Side panel position output	—
68	QSL	O	684fH output	—
69	ISL	O	684fH output (QSL reverse output)	—
70	VDP	O	Vertical drive pulse output	—
71	VBM	O	Timing signal for vertical black masking	—
72	V_{SS}	—	Digital GND	—
73	JMT	O	Caption detection signal (caption : H, no caption : L)	—
74	JPW	O	PWM output	—
75	YVS	O	Video / luminance switching signal output (22H, 285H)	—
76	V_{DD}	—	Digital power supply	—
77	SCL	I	I^2C bus clock input	—
78	SDA	I / O	I^2C bus data input / output	—

PIN No.	PIN NAME	I / O	FUNCTION	OPERATING CONDITIONS
79	CDG7	I	Test input (normally connect to V_{SS})	—
80	CDG6	I	Test input (normally connect to V_{SS})	—
81	CDG5	I	Test input (normally connect to V_{SS})	—
82	CDG4	I	Test input (normally connect to V_{SS})	—
83	CDG3	I	Test input (normally connect to V_{SS})	—
84	CDG2	I	Test input (normally connect to V_{SS})	—
85	CDG1	I	Test input (normally connect to V_{SS})	—
86	CDG0	—	Test input (normally connect to V_{SS})	—
87	V_{SS}	—	Digital GND	—
88	BIASAD	—	ADC bias voltage pin	—
89	V_{SSAD2}	—	Analog GND	—
90	VRTY	—	Video / luminance ADC reference voltage (H side)	208LSB
91	V_{IN}	—	Video signal input	Pedestal clamp
92	V_{DDAD1}	—	Analog power supply	+ 3.3 V
93	Y_{IN}	—	Luminance signal input	Pedestal clamp
94	VRBY	—	Video / luminance ADC reference voltage (L side)	64LSB
95	VRTC	—	I / Q ADC reference voltage (H side)	208LSB
96	Q_{IN}	—	Q signal input	—
97	V_{SSAD1}	—	Analog GND	—
98	I_{IN}	—	I signal input	—
99	VRBC	—	I / Q ADC reference voltage (L side)	64LSB
100	CLMPVC	—	I / Q clamp pin	—

PACKAGE DIMENSIONS

QFP100-P-1420-0.65A Unit : mm



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