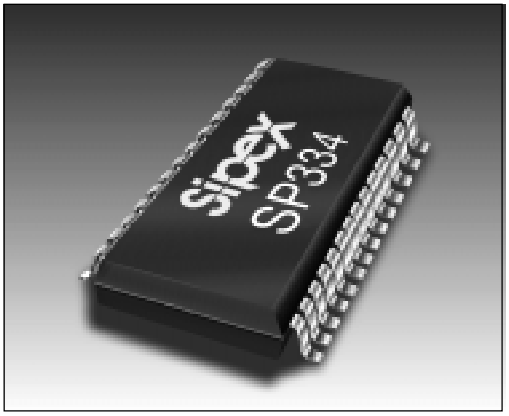
Programmable RS-232/RS-485 Transceiver

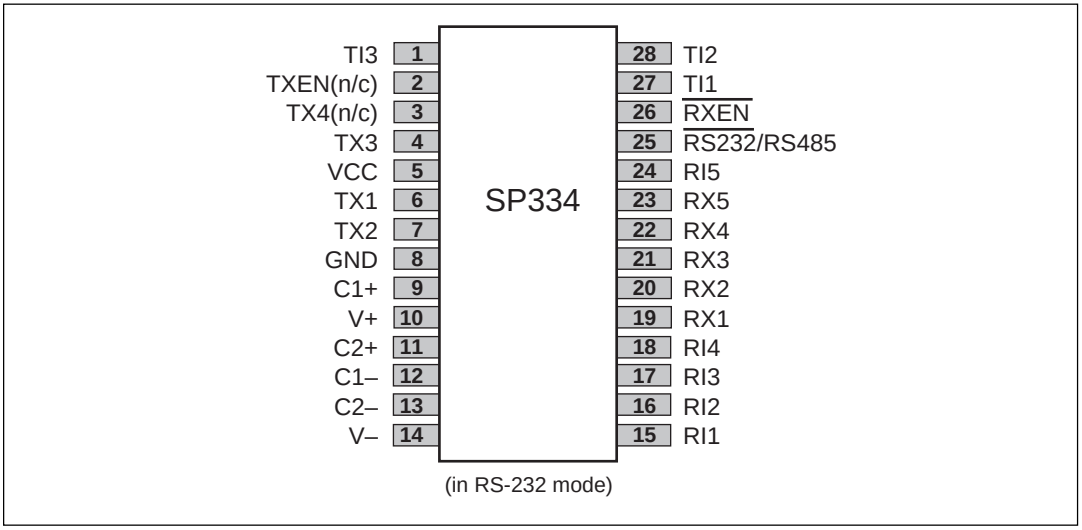
- +5V Only Operation
- Software Programmable RS-232 or RS-485 Selection
- Three RS-232 Drivers and Five Receivers in RS-232 Mode
- Two RS-485 Full-Duplex Transceivers in RS-485 Mode
- Full Differential Driver Tri-State (Hi-Z) Control
- Receiver Output Tri-State Control



DESCRIPTION…

The **SP334** is a programmable RS-232 and/or RS-485 transceiver IC. The **SP334** contains three drivers and five receivers when selected in RS-232 mode; and two drivers and two receivers when selected in RS-485 mode.

The RS-232 transceivers can typically operate at 230kbps while adhering to the RS-232 specifications. The RS-485 transceivers can operate up to 10Mbps while adhering to the RS-485 specifications. The RS-485 drivers can be disabled (High-Z output) by the TXEN enable pin. The RS-232 and RS-485 receiver outputs can be disabled by the $\overline{\text{RXEN}}$ enable pin.



(in RS-232 mode)

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC}.....+7V
Storage Temperature.....-65˚C to +150˚C
Power Dissipation
28-pin Plastic DIP.....1000mW
28-pin Plastic SOIC.....1000mW

Package Derating:
28-pin Plastic DIP
$ø_{JA}$.....40 °C/W
28-pin Plastic SOIC
$ø_{JA}$.....40 °C/W

SPECIFICATIONS

Typically 25°C @ Vcc = +5V unless otherwise noted.

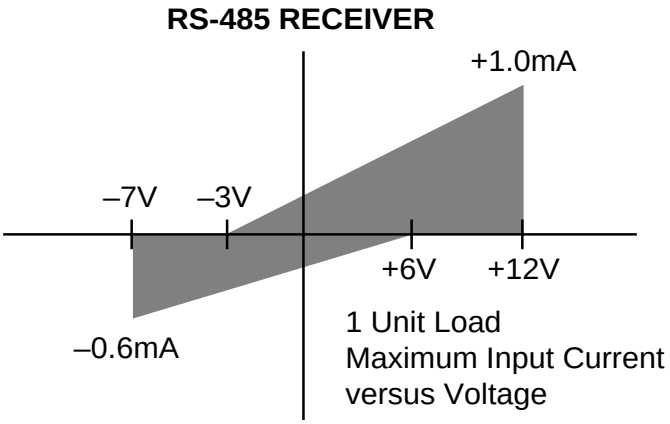
	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
LOGIC OUTPUTS					
V_{OL}			0.4	Volts	I_{OUT}= -3.2mA
V_{OH}	2.4			Volts	I_{OUT}= 1.0mA
Output Tri-state Leakage		10		µA	0.4V ≤ V_{OUT} ≤ +2.4V
RS-232 DRIVER					
DC Characteristics					
HIGH Level Output	+5.0		+15	Volts	R_L=3kΩ, V_{IN}=0.8V
LOW Level Output	–15.0		–5.0	Volts	R_L=3kΩ, V_{IN}=2.0V
Open Circuit Voltage	–15		+15	Volts	
Short Circuit Current			±100	mA	V_{OUT} = 0V
Power Off Impedance	300			Ω	V_{cc} = 0V, V_{out} = ±2.0V
AC Characteristics					
Slew Rate			30	V/µs	R_L=3kΩ, C_L= 50pF V_{CC} = +5.0V, T_A @ +25°C
Transition Time			1.56	µs	R_L=3kΩ, C_L=2500pF ; between ±3V, T_A @ +25°C
Maximum Data Rate	120	235		kbps	R_L=3kΩ, C_L=2500pF
Propagation Delay					
t_{PHL}		2	8	µs	Measured from 1.5V of V_{IN}
t_{PLH}		2	8	µs	to 50% of V_{OUT}; R_L=3kΩ
RS-232 RECEIVER					
DC Characteristics					
HIGH Threshold		1.7	3.0	Volts	
LOW Threshold	0.8	1.2		Volts	
Receiver Open Circuit Bias			+2.0	Volts	
Input Impedance	3	5	7	kΩ	V_{IN} = +15V to –15V
AC Characteristics					
Maximum Data Rate	120	235		kbps	
Propagation Delay					
t_{PHL}		0.25	1	µs	Measured from 50% of V_{IN}
t_{PLH}		0.25	1	µs	to 1.5V of V_{OUT}.
RS-485 DRIVER					
DC Characteristics					
Open Circuit Voltage			6.0	Volts	
Differential Output	1.5		5.0	Volts	R_L=54Ω, C_L=50pF

SPECIFICATIONS

Typically 25°C @ Vcc = +5V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-485 DRIVER					
Balance			±0.2	Volts	$\|V_T\| - \|\overline{V_T}\|$
Common-Mode Output			3.0	Volts	
Output Current	28.0			mA	R_L=54Ω
Short Circuit Current			±250	mA	Terminated in –7V to +10V
AC Characteristics					
Maximum Data Rate	10			Mbps	R_L=54Ω
Output Transition Time		30		ns	Rise/fall time, 10%–90%
Propagation Delay					See Figures 3A & 5
t_{PHL}		80	120	ns	R_{DIFF}=54Ω, C_{L1}=C_{L2}=100pF
t_{PLH}		80	120	ns	R_{DIFF}=54Ω, C_{L1}=C_{L2}=100pF
Driver Output Skew		5	20	ns	per figure 5, t_{SKEW} = $\|t_{DPLH} - t_{DPHL}\|$
RS-485 RECEIVER					
DC Characteristics					
Inputs					
Common Mode Range	–7.0		+12.0	Volts	
Receiver Sensitivity			±0.2	Volts	$–7V \le V_{CM} \le +12V$
Input Impedance	12	15		kΩ	$–7V \le V_{CM} \le +12V$
AC Characteristics					
Maximum Data Rate	10			Mbps	
Propagation Delay					See Figures 3A & 7
t_{PHL}		130	200	ns	R_{DIFF}=54Ω, C_{L1}=C_{L2}=100pF
t_{PLH}		130	200	ns	R_{DIFF}=54Ω, C_{L1}=C_{L2}=100pF
Differential Receiver Skew		10	20	ns	t_{SKEW}= $\|t_{PLH} – t_{PHL}\|$; R_{DIFF}=54Ω, C_{L1}=C_{L2}=100pF, see Figure 8
ENABLE TIMING					
RS-485 Driver					
Enable Time					See Figures 4 & 6
Enable to Low		100	150	ns	C_L=15pF, S_1 Closed
Enable to High		100	150	ns	C_L=15pF, S_2 Closed
Disable Time					See Figures 4 & 6
Disable From Low		100	120	ns	C_L=15pF, S_1 Closed
Disable From High		100	120	ns	C_L=15pF, S_2 Closed
RS-485 Receiver					
Enable Time					See Figures 2 & 8
Enable to Low		100	150	ns	C_L=15pF, S_1 Closed
Enable to High		100	150	ns	C_L=15pF, S_2 Closed
Disable Time					See Figures 2 & 8
Disable From Low		100	120	ns	C_L=15pF, S_1 Closed
Disable From High		100	120	ns	C_L=15pF, S_2 Closed
POWER REQUIREMENTS					
Supply Voltage V_{CC}	+4.75		+5.25	Volts	
Supply Current I_{CC}					
No Load (T_x Disabled)		12	20	mA	TXEN = 0V
No Load (RS-232 Mode)		20	50	mA	$\overline{RS232}$/RS485 = 0V
No Load (RS-485 Mode)		15	50	mA	$\overline{RS232}$/RS485 = +5V
ENVIRONMENTAL					
Operating Temperature					
Commercial (..C..)	0		+70	°C	
Industrial (..E..)	–40		+85	°C	
Storage Temperature	–65		+150	°C	

RECEIVER INPUT GRAPH



TEST CIRCUITS

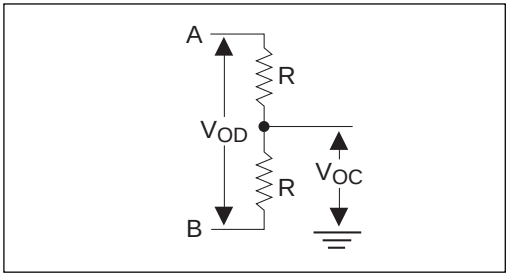


Figure 1. Driver DC Test Load Circuit

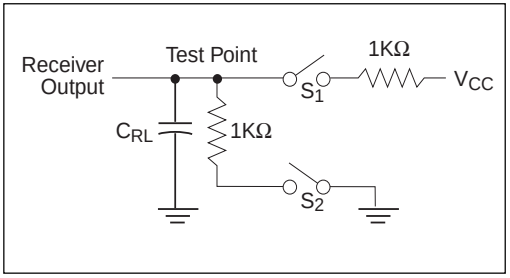


Figure 2. Receiver Timing Test Load Circuit

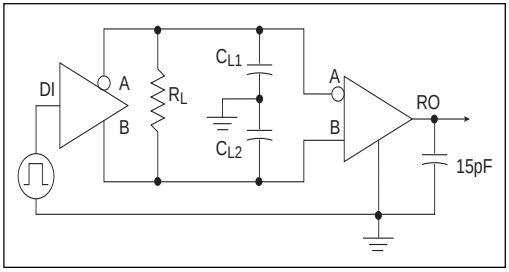


Figure 3a. Driver/Receiver Timing Test Circuit

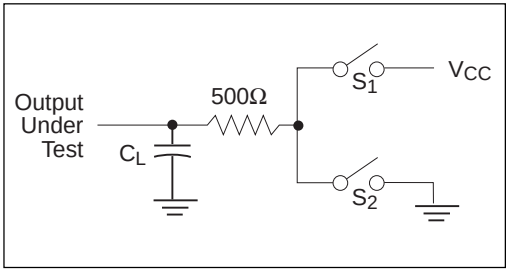


Figure 4. Driver Timing Test Load #2 Circuit

SWITCHING WAVEFORMS

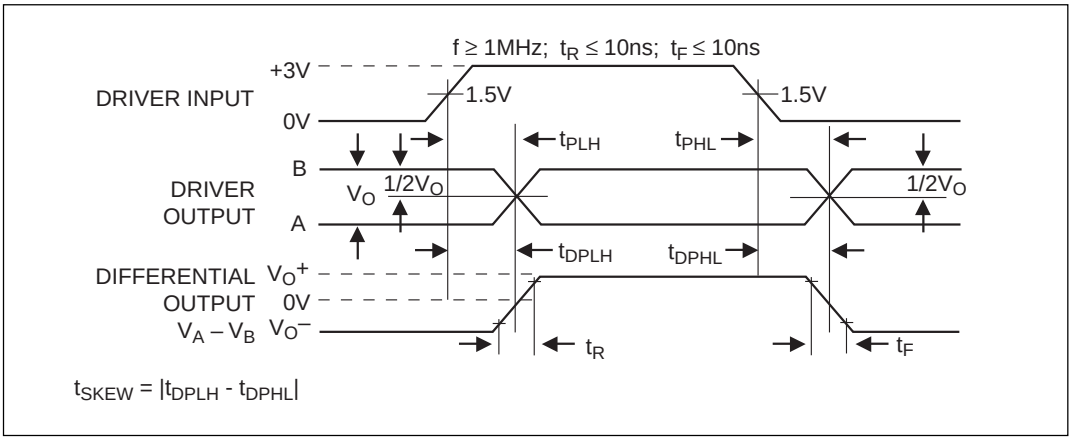


Figure 5. Driver Propagation Delays

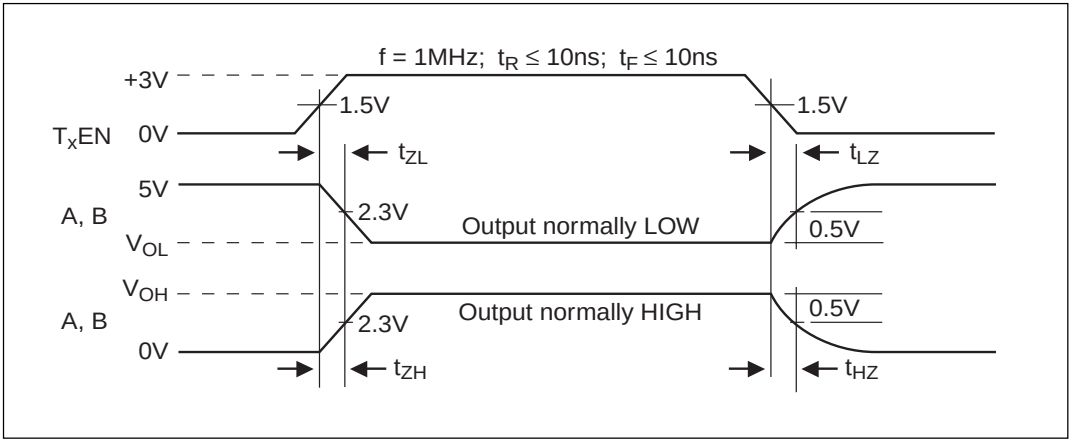


Figure 6. Driver Enable and Disable Times

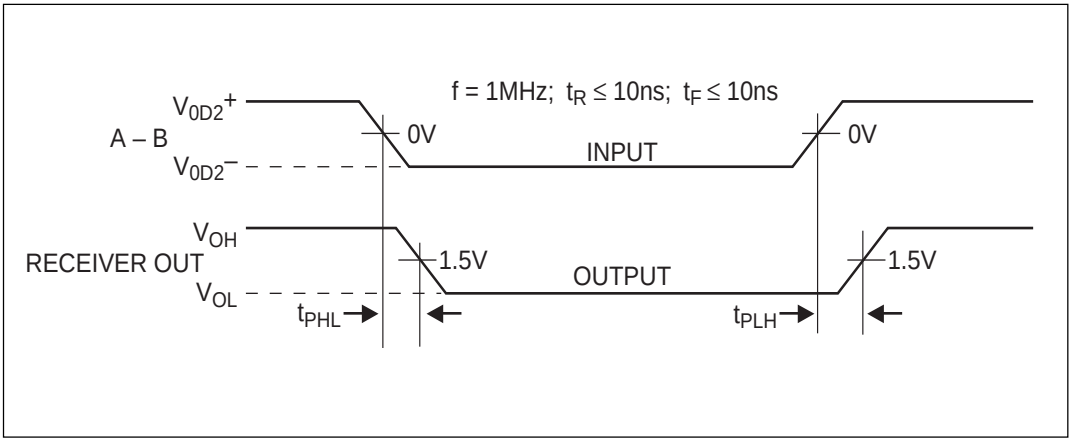


Figure 7. Receiver Propagation Delays

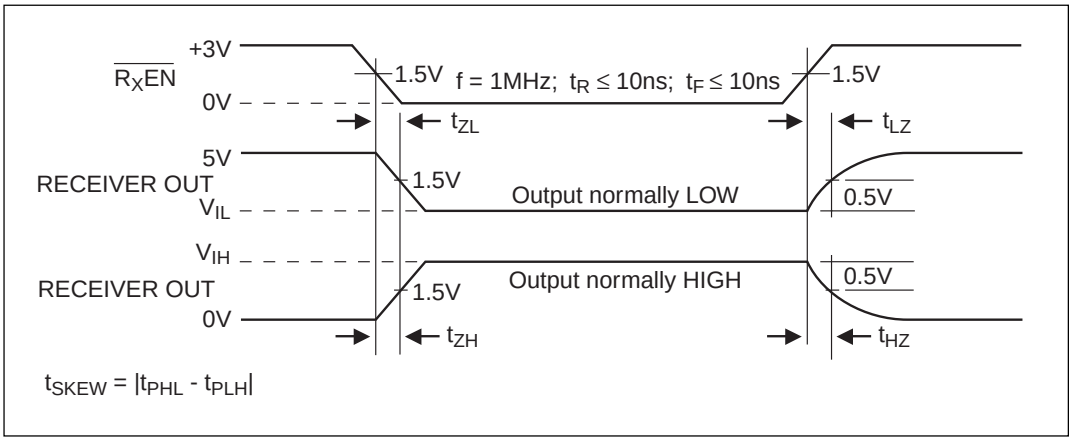


Figure 8. Receiver Enable and Disable Times

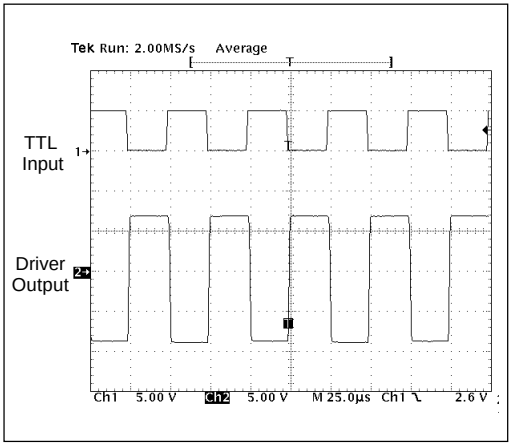


Figure 9. Typical RS-232 Driver Output

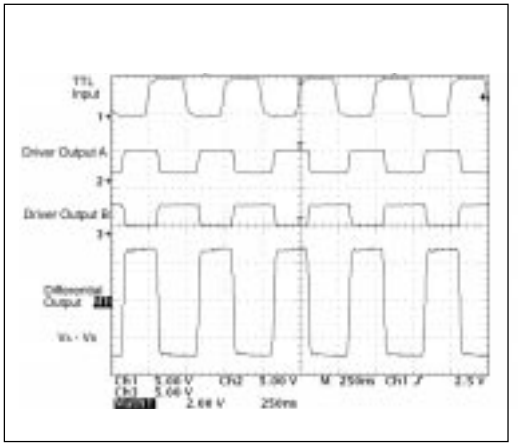


Figure 10. Typical RS-485 Driver Output

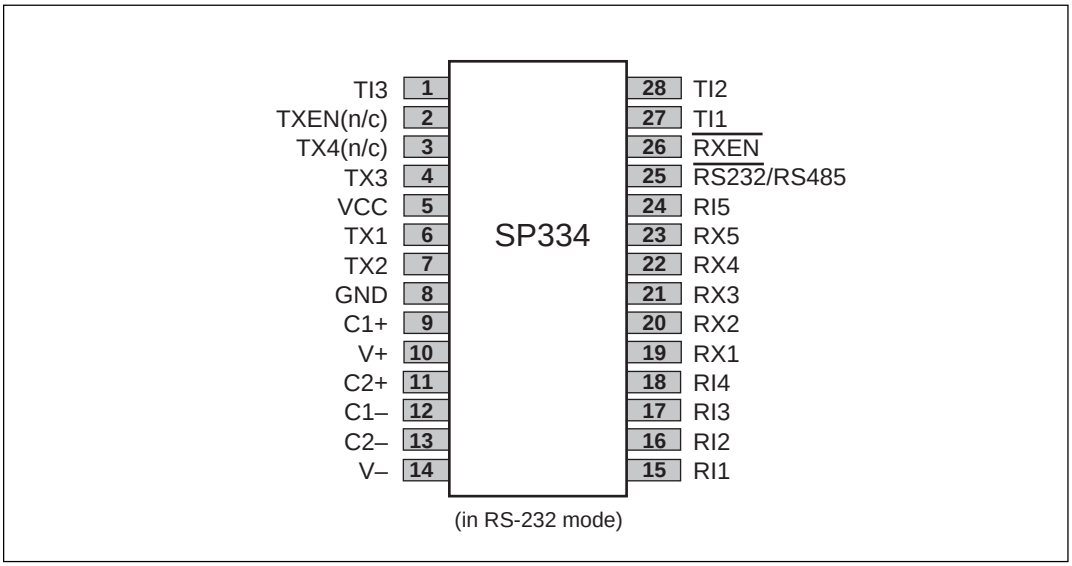


Figure 11. SP334 Pinout

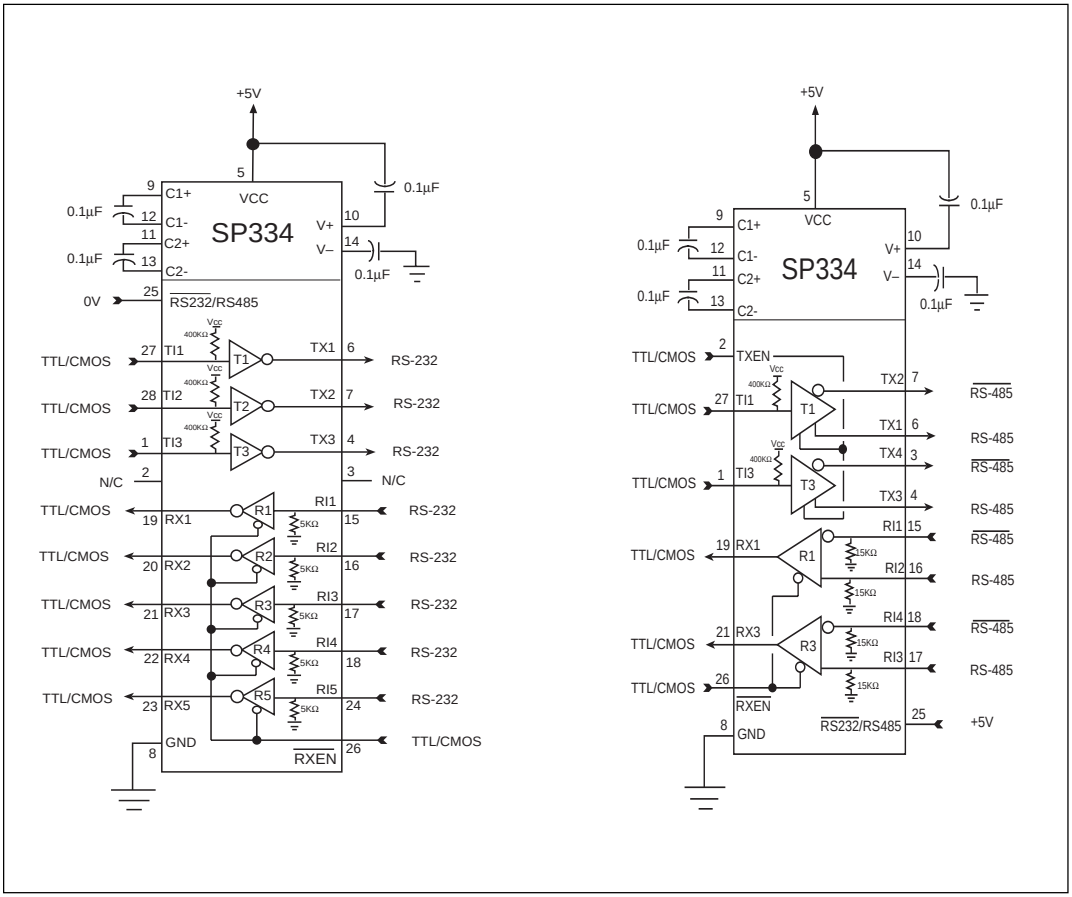


Figure 12. Typical Operating Circuit

THEORY OF OPERATION

The **SP334** is made up of four separate circuit blocks — the charge pump, drivers, receivers, and decoder. Each of these circuit blocks is described in more detail below.

Charge–Pump

The charge pump is a **Sipex**–patented design (U.S. 5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 10V power supplies. Figure 17(a) shows the waveform found on the positive side of capcitor C2, and figure 17(b) shows the negative side of capcitor C2. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage —During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. C_1^+ is then switched to ground and charge on C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated –l0V to C_3. Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces –5V in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at +5V, the voltage potential across C_2 is l0V.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to ground and transfers the generated l0V across C_2 to C_4, the V_{DD} storage capacitor. Again, simultaneously with this, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V+ and V– are separately generated from V_{CC} in a no–load condition, V+ and V– will be symmetrical. Older charge pump approaches that generate V– from V+ will show a decrease in the magnitude of V– compared to V+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors must be a minimum of 0.1µF with a 16V breakdown rating.

External Power Supplies

For applications that do not require +5V only, external supplies can be applied at the V+ and V– pins. The value of the external supply voltages must be no greater than ±l0V. The current drain for the ±10V supplies is used for RS232. For the RS-232 driver the current requirement will be 3.5mA per driver. The external power supplies should provide a power supply sequence of :+l0V, then +5V, followed by –l0V.

Drivers

The **SP334** has three independent RS-232 single-ended drivers and two differential RS-485 drivers. Control for the mode selection is done by the $\overline{\text{RS-232}}$/RS-485 select pin. The drivers are pre-arranged such that for each mode of

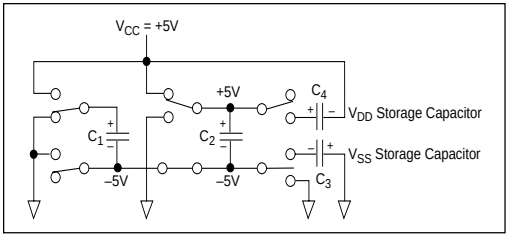


Figure 13. Charge Pump Phase 1.

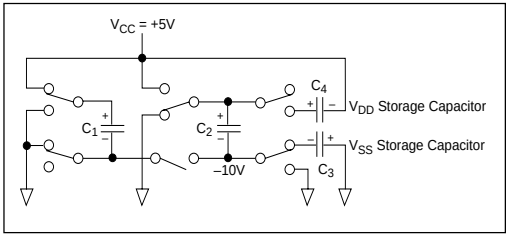


Figure 14a. Charge Pump Phase 2.

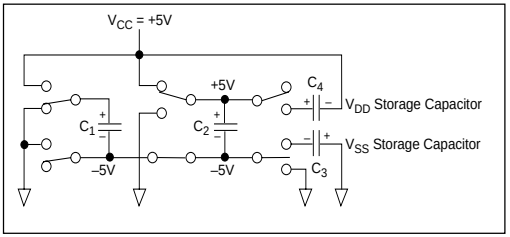


Figure 15. Charge Pump Phase 3.

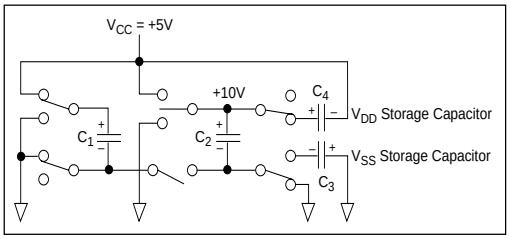


Figure 16. Charge Pump Phase 4.

operation the relative position and functionality of the drivers are set up to accommodate the selected interface mode. As the mode of the drivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line signal levels. Unused driver inputs can be left floating; however, to ensure a desired state with no input signal, pull–up resistors to +5V or pull–down resistors to ground are suggested. Since the driver inputs are both TTL or CMOS compatible, any value resistor less than 100kΩ will suffice.

When in RS-232 mode, the single-ended RS-232 drivers produce compliant RS-232E and ITU V.28 signals. Each of the three drivers output single-ended bipolar signals in excess of ±5V with a full load of 3kΩ and 2500pF applied as specified. These drivers can also operate at least 120kbps.

When programmed to RS-485 mode, the differential RS-485 drivers produce complaint RS-485 signals. Each RS-485 driver outputs a unipolar signal on each output pin with a magnitude of at least 1.5V while loaded with a worst case of 54Ω between the driver's two output pins. The signal levels and drive capability of the RS-485 drivers allow the drivers to also comply with RS-422 levels. The transmission rate for the differential drivers is 10Mbps.

Receivers

The **SP334** has five single-ended receivers when programmed for RS-232 mode and two differential receivers when programmed for RS-485 mode.

Control for the mode selection is done by the same select pin as the drivers. As the operating mode of the receivers is changed, the electrical characteristics will change to support the requirements of the appropriate serial standard. Unused receiver inputs can be left floating without causing oscillation. To ensure a desired state of the receiver output, a pull–up resistor of 100kΩ to +5V should be connected to the inverting input for a logic low, or the non–inverting input for a logic high. For single-ended receivers, a pull–down resistor to ground of 5kΩ is internally connected, which will ensure a logic high output.

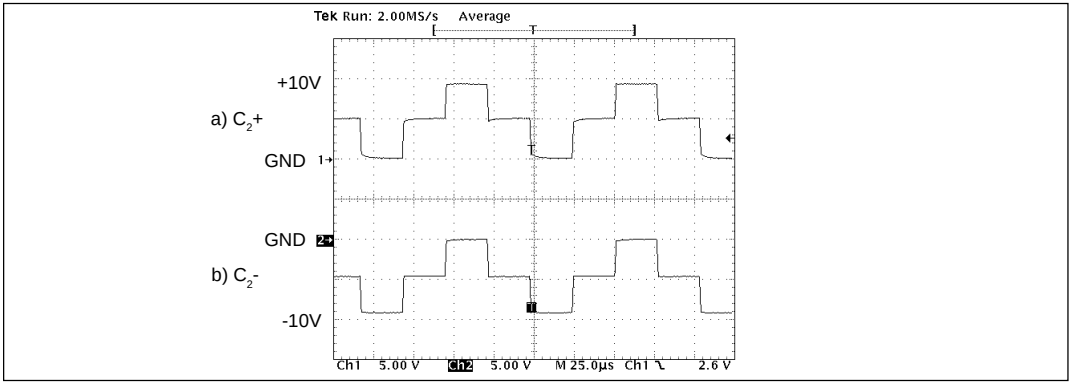


Figure 17. Charge Pump Waveforms

The RS-232 receiver has a single–ended input with a threshold of 0.8V to 2.4V. The RS-232 receiver has an operating voltage range of ±15V and can receive signals up to 120kbps. RS-232 receivers are used in RS-232 mode for all signal types include data, clock, and control lines of the RS-232 serial port.

The differential RS-485 receiver has an input impedance of 15kΩ and a differential threshold of ±200mV. Since the characteristics of an RS-422 receiver are actually subsets of RS485, the receivers for RS-422 requirements are identical to the RS-485 receivers. All of the differential receivers can receive data up to 10Mbps.

Enable Pins

The **SP334** drivers can be enabled by use of the TXEN pin. A logic HIGH will enable the driver outputs and a logic LOW will tri-state the outputs. The drivers can only be tri-stated in RS-485 mode. The drivers are always active in RS-232 mode.

The receiver outputs can also be tri-stated by use of the $\overline{\text{RXEN}}$ pin. A logic LOW will enable the receiver outputs and a logic HIGH will tri-state the outputs. The receiver tri-state capability is offered for both RS-232 and RS-485 modes. The input impedance if the receivers during tri-state is at least 12kΩ.

Applications

The **SP334** allows the user flexibility in having a RS-232 or RS-485 serial port without using two different discrete active ICs. *Figure 18* shows a connection to a standard DB-9 RS-232 connector. In RS-485 mode, the **SP334** is a full duplex transceiver, however, a half duplex configuration can be made by connecting the driver outputs to the receiver inputs.

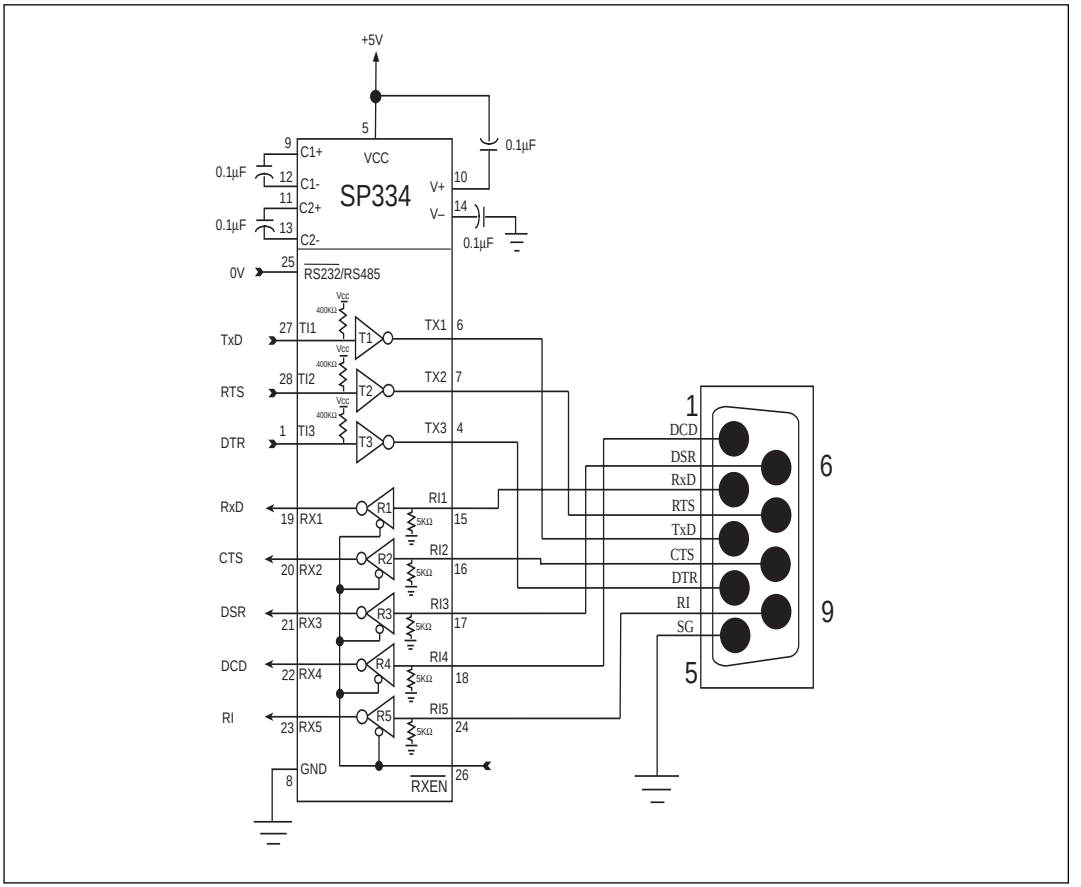
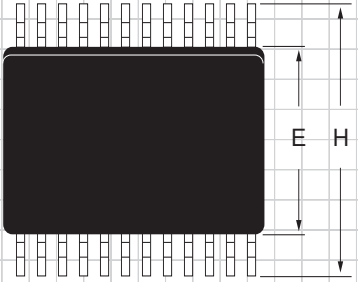
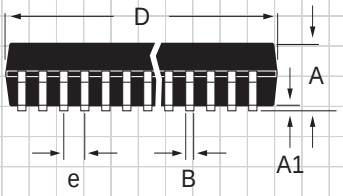
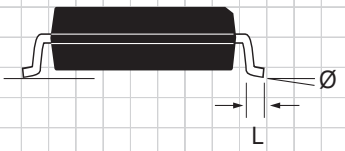


Figure 18. SP334 Configuration to a DB-9 Serial Port

PACKAGE: 28-PIN PLASTIC SMALL OUTLINE (SOIC)







DIMENSIONS (Inches) Minimum/Maximum (mm)	28–PIN
A	0.093/0.104 (2.352/2.649)
A1	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)
D	0.698/0.706 (17.73/17.93)
E	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP334CT	0°C to +70°C	28-pin Plastic SOIC
SP334ET	-40°C to +85°C	28-pin Plastic SOIC

Please consult the factory for pricing and availability on a Tape-On-Reel option.

SIGNAL PROCESSING EXCELLENCE

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