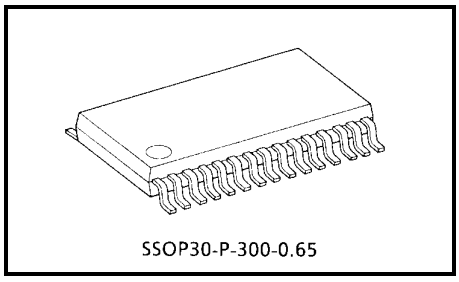
TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB2132FNG

3-V AM/FM/TV Single Chip Tuner IC with On-Chip PLL

The TB2132FNG is an IC suitable for 3-V headphone radio and radio cassette application. It has FM/TV front end, FM IF, FM stereo decoder, AM function and PLL function on a single chip. The FM/TV front end is designed to lower the oscillation voltage of the FM/TV local oscillator, enabling this IC to meet the new FCC standards.



Weight: 0.17 g (typ.)

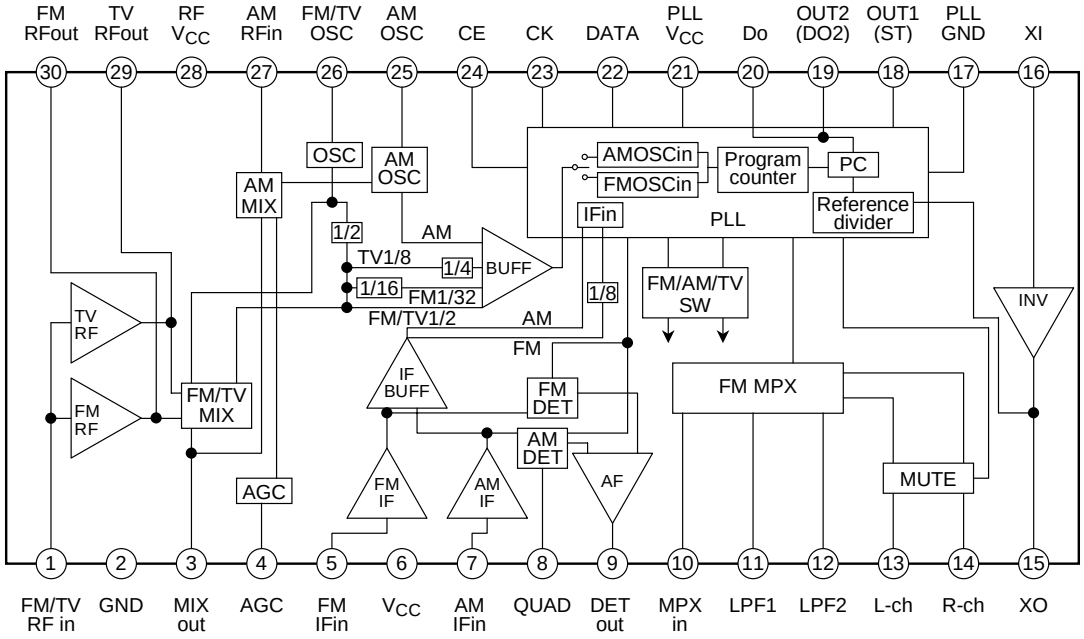
Features

- Low supply current (V_{CC} = 3 V, Ta = 25°C)
  FM: I_{CC} = 18 mA (typ.)
  AM: I_{CC} = 7.5 mA (typ.)
- Operating supply voltage range
  : V_{CC} = 1.8 to 5.5 V (Ta = 25°C)
- Tuner block
  - Can be used for TV band.
  - Enable to meet the new FCC standards.
  - Adjustment-free FM quad detector due to ceramic discriminator
  - On-chip FM MPX VCO circuit
- PLL block
  - Reference frequency: 1 kHz , 1.5625 kHz, 3 kHz, 3.125 kHz, 5 kHz, 6.25 kHz, 12.5 kHz, 25 kHz
  - Data transfer is performed with synchronous three-line bus, using pins CE (Chip Enable), CK (Clock) and DATA (DATA).
  - Crystal oscillation frequency: 75 kHz
  - IF count method: On-chip 20-bit counter

Note: The TB2132FNG is mounted with lead-free soldering alloys.

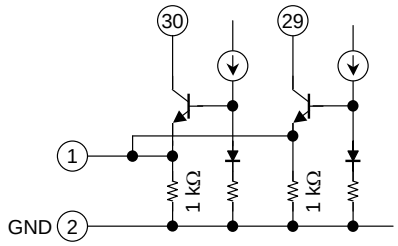
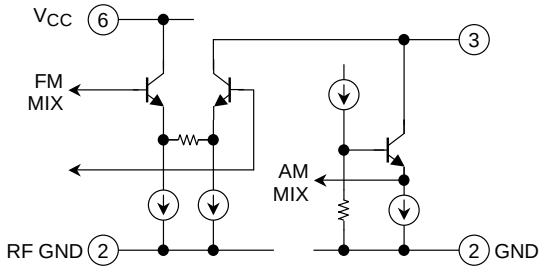
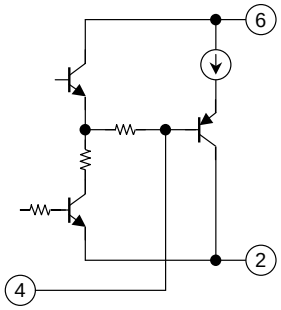
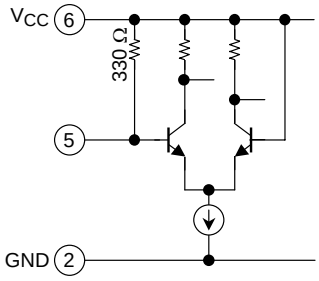
Pin 26 (FM/TV OSC) is sensitive to electrostatic discharge. Take care when handling.

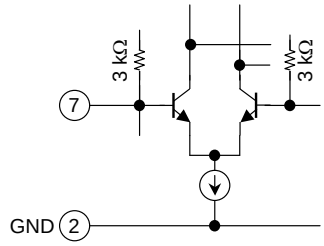
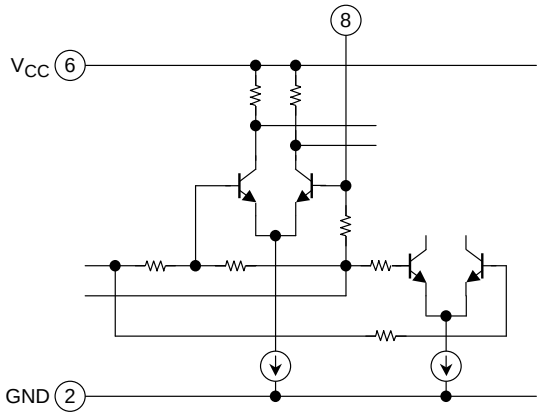
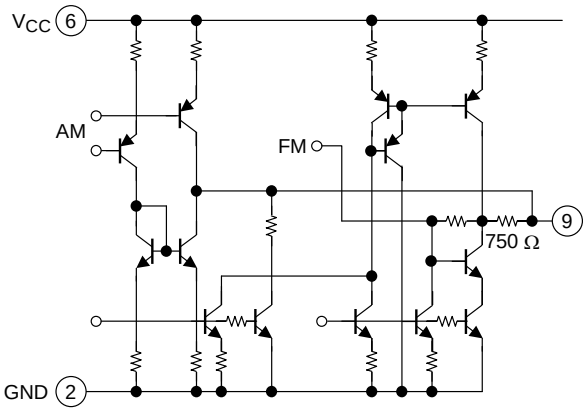
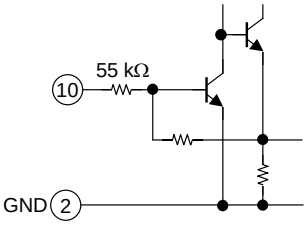
Block Diagram

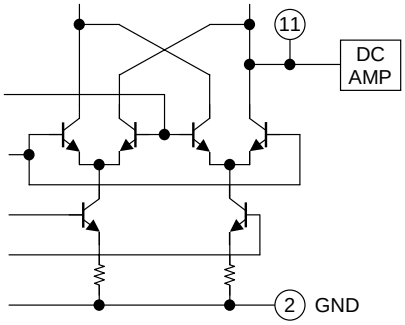
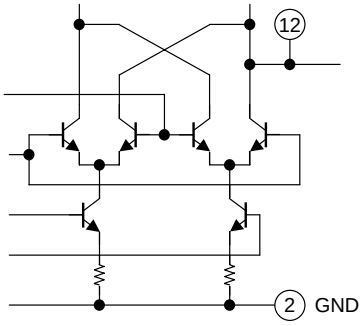
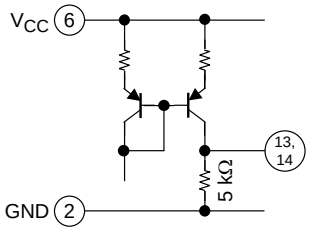
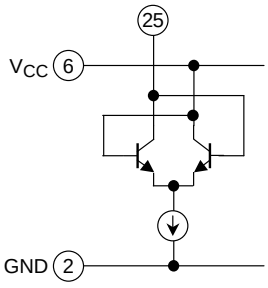


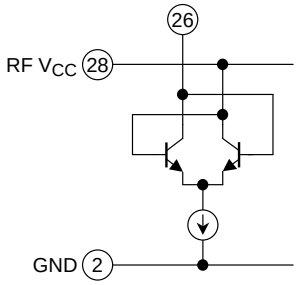
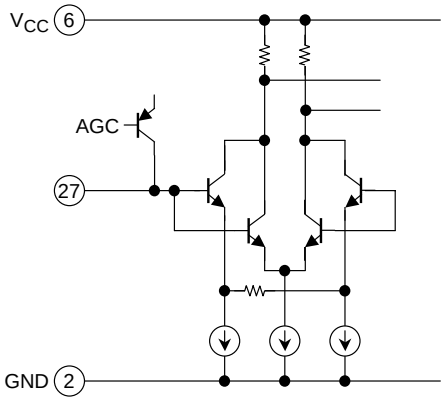
Pin Description

1. Tuner Block

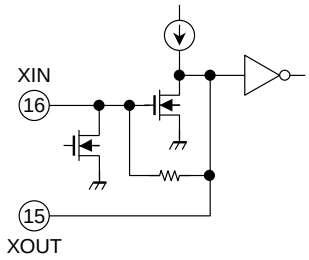
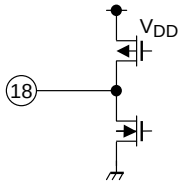
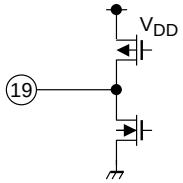
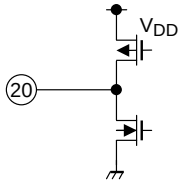
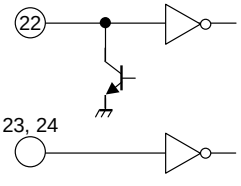
Pin No.	Characteristics	Internal Circuit	Pin Voltage (typ.) (V)	
			AM	FM
1	FM/TV RFin		0	0.8
2	GND	—	0	0
3	MIX OUT		3.0	3.0
4	AGC		0	0
5	FM IF IN		3.0	3.0
6	VCC (VCC for FM IF and MPX)	—	3.0	3.0

Pin No.	Characteristics	Internal Circuit	Pin Voltage (typ.) (V)	
			AM	FM
7	AM IF IN		2.3	2.5
8	QUOD		2.5	2.2
9	DET OUT		1.0	0.9
10	MPX IN		0.7	0.7

Pin No.	Characteristics	Internal Circuit	Pin Voltage (typ.) (V)	
			AM	FM
11	LPF1 • LPF pin for synchronous detector		0.7	2.4
12	LPF2 • LPF pin for phase detector		0	2.2
13 14	L-OUT R-OUT		1.2	1.2
25	AM OSC		3.0	3.0

Pin No.	Characteristics	Internal Circuit	Pin Voltage (typ.) (V)	
			AM	FM
26	FM/TV OSC		3.0	3.0
27	AM RFin		3.0	3.0
28	RF V_{CC} (V_{CC} for FM RF)	—	3.0	3.0
29	TV RF OUT	Refer to the internal circuit of pin 1.	3.0	3.0
30	FM RFout	Refer to the internal circuit of pin 1.	3.0	3.0

2. PLL Block

Pin No.	Symbol	Pin Name	Description	Equivalent Circuit
15	XOUT	Crystal oscillator pin	These pins are used for a crystal oscillator. A 75-kHz reference crystal oscillator is connected to the pins XIN and XOUT.	
16	XIN			
17	PLL GND	Power supply input pin	This is a power supply input pin for the PLL block.	
18	OUT1 (ST)	General-purpose output port (ST port)	This port can be switched between general-purpose output port and ST output using STC bit of serial data. Note: Upon power-on or power-on reset, pin 18 is configured as an output (the OUT1 output will be low). Thus, If an LED is connected to pin 18 for stereo display, it is illuminated at these times.	
19	OUT2 (DO2)	General-purpose output port (DO output)	This port can be switched between general-purpose output port and DO output using DO2 bit of serial data.	
20	DO	Phase comparator output	This is a phase comparator output pin for the PLL block with tri-state output. When the divided-down clock from the programmable counter is higher than the reference frequency, it will be in High-level. When it is lower, it will be in Low-level. If it matches the reference frequency, it will be in high-impedance state. The output is held at Low in Standby Mode.	
21	PLL V_{CC}	Power supply input pin	This is a power supply input pin for the PLL block.	
22, 23, 24	DATA CK CE	Serial data I/O	These are serial data I/O pins.	

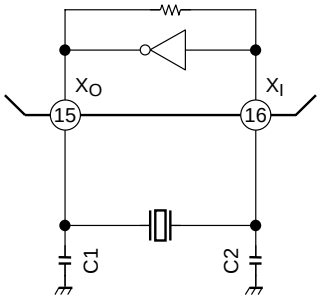
Application Note

1. Power Supply Line

This IC has two voltage supply pins, V_{CC} (for stages of AM, FM IF and MPX) and RF V_{CC} (for FM RF stage). Please keep the potential difference between these power supply pins at 0.4 V (typ.) or less. Otherwise, it may cause the IC to malfunction.
Also, please keep the potential difference between the V_{CC} (tuner power supply) and the V_{DD} (PLL power supply) at 1 V or less. Otherwise, due to improper interaction between analog and digital blocks, a malfunction may occur.

2. Crystal Oscillator External Constant

When the constants of external components C1 and C2 are determined, please show the IC with the final layout of the board to a crystal oscillator manufacturer and test it to confirm the constants.
If you need an IC to adjust parameter values to compensate for variables in layout, ask Toshiba.
Please use a crystal oscillator with lower CI value

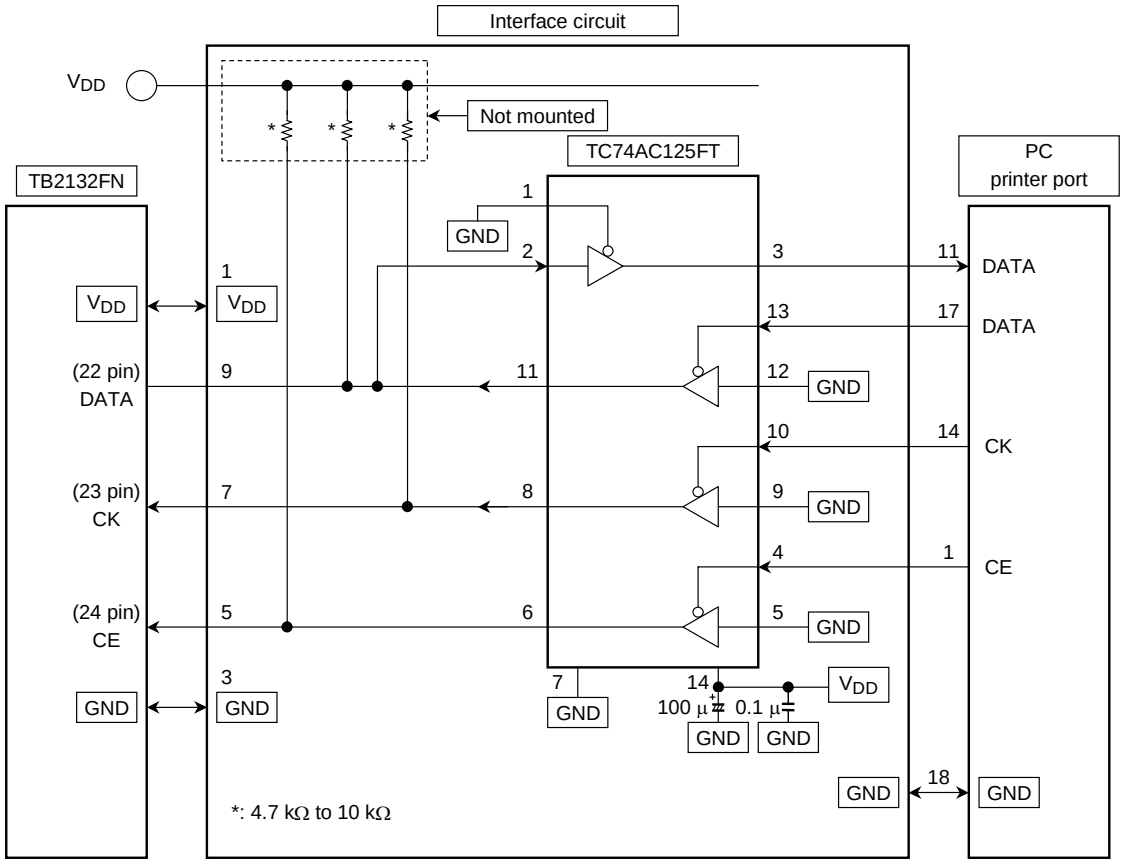


Toshiba tested a crystal oscillator from DAISHINKU CORP. (CI value is 30 kΩ max) using a Toshiba evaluation board.

3. Miscellaneous

1) We offer information on software programs to control the TB2132FNG on Windows 95/98. For details, contact us.
   (Also contact us if you are using Windows 2000/NT.)
2) We offer an interface board to run the TB2132FNG under software control on Windows 95/98.

<Interface circuit diagram>

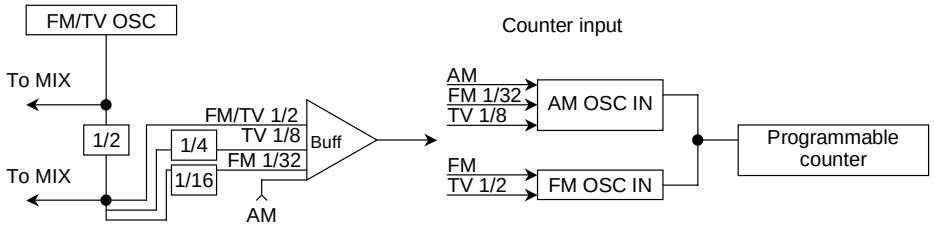


4. Resistor in Interface Block

- When tuner power supply > Microcontroller power supply
  CE, CK and DATA should be connected to the tuner power supply via pull-up resistors.
  (Depending on a microcontroller specification, these pins should be connected directly to the tuner power supply, or the interface board should be inserted as shown above.)
- When tuner power supply ≦ Microcontroller power supply
  Only DATA should be connected to the microcontroller power supply via a pull-up resistor.

Configuration of Local Oscillator and Programmable Counter

Operate the FM/TV local oscillator at approximately 200 MHz and select the counter input using the following settings of the bits. Then determine reference frequency and minimum step frequency.



Mode	BAND0	BAND1	Divide by 16	PW	Interna VCO IN	Input Frequency Range	Recommended Reference Frequency	Minimum Step Frequency
AM	1	0	*	0	AM OSC IN	0.1 MHz~40 MHz	1 k, 3 k, 5 k	1 k, 3 k, 5 k
FM 1/32	0	0	0	0			3.125 k	50 kHz
TV 1/8	0	1	0	0			6.25 k	50 kHz
FM	0	0	1	1	FM OSC IN	30 MHz~230 MHz	25 kHz	25 kHz
TV 1/2	0	1	1	1			12.5 kHz	25 kHz

How to Set the Divisor

A divisor of the programmable counter is set in binary using the bits P0 to P16.

1. FM OSC IN: Pulse swallow mode (set the PW bit)
   Pulse swallow mode (17 bits: FM and TV 1/2 Modes). Please set as shown below.

MSB LSB

P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

2^{17} — 2^{0}

Divisor range n: 528~131072 (210H to 1FFFH)

2. AM OSC IN (clear the PW bit)
   Direct divide mode (12 bits: AM, FM 1/32, TV 1/8) please set P4 to P16 as shown below.

MSB LSB

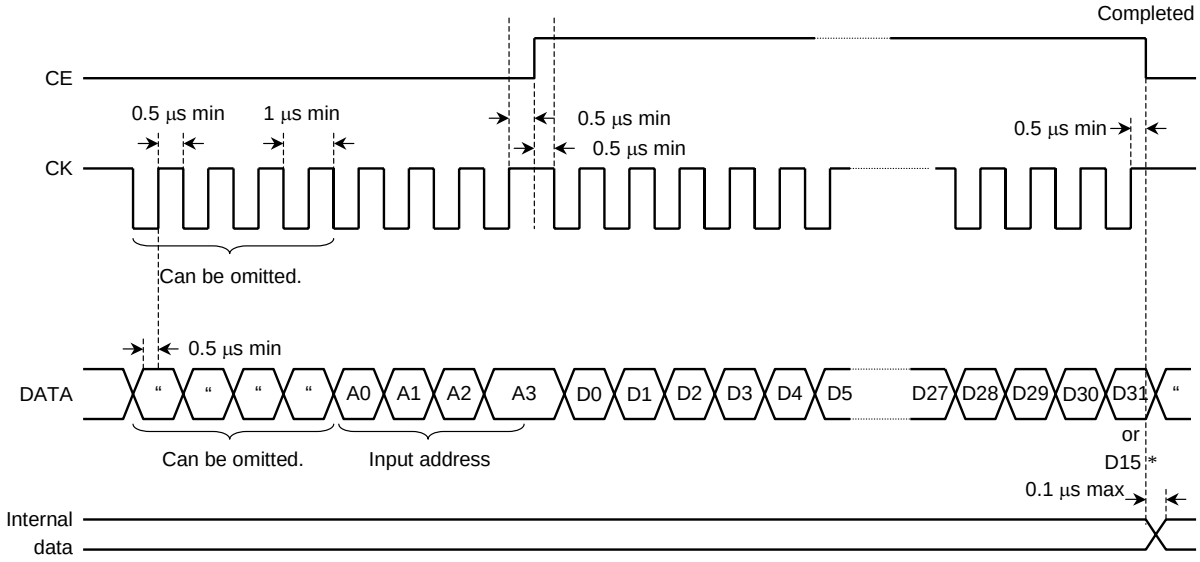
P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

2^{12} — 2^{0} [Irrelevant]

Divisor range n: 16~8191 (10H to 1FFFH)

Serial Transfer Format

Data input mode (D_{OUT} is in high-impedance state at input.)



* In Input Mode 2, set Low at CE pin after D15 is passed.

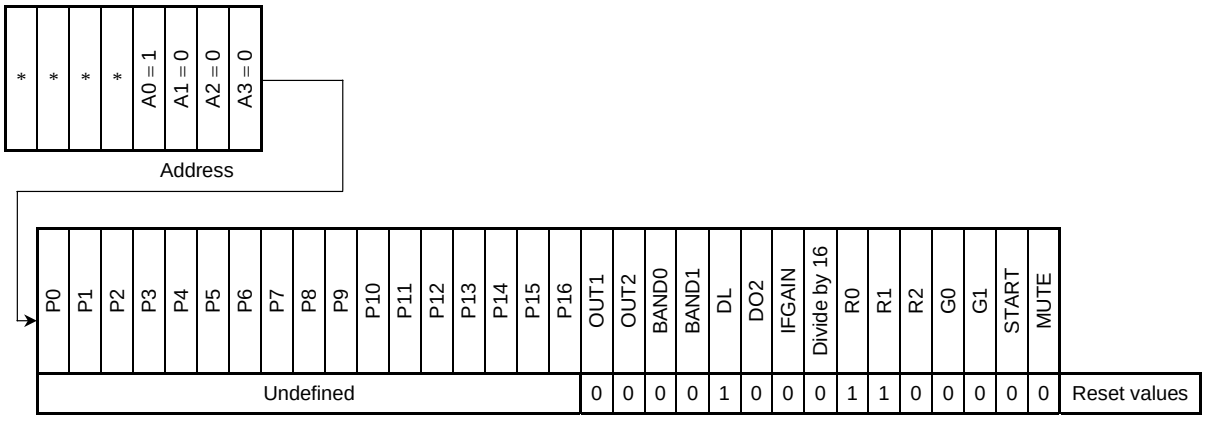
* Do not enter the first data within 100 ms after the power supply is turned on.

* At power on or reset, the reset values are set as shown in the figure below.

Address Format

A0	A1	A2	A3	Mode
1	0	0	0	Input Mode 1
0	1	0	0	Input Mode 2
0	0	0	1	Output Mode (IF count data and data output)

Input Mode 1



Data in Detail

- P0 to 16: N (divisor data P0: LSB, P16: MSB)
- OUT1, 2: When set, a high appears on the OUT pin.
  When cleared, a low appears on the OUT pin.
- BAND 0, 1

	BAND 0	BAND 1
FM	0	0
AM	1	0
TV	0	1
Standby Mode The tuner block, the PLL block and the crystal oscillator: OFF DO: Held at Low	1	1

Note: In standby mode, the X'tal I1 and X'tal I2 bits must be cleared. Otherwise, the oscillator does not run after the TB2132FNG exits from the mode.
The OUT1 and OUT2 bits can be controlled by serial input data, even in standby mode.

- DL: When cleared, DO is in normal state.
  When set, DO is held at low.
- DO2: When cleared, the OUT2 pin is switched to the general-purpose output port.
  When set, the OUT2 pin is switched to the DO output.
- IF GAIN: When cleared, full gain of the FM IF amplifier.
  When set, 2dB more gain than the full gain of the FM IF amplifier.
- Divide by 16: When cleared, FMOSC output: 1/32, TV OSC output: 1/8
  When set, FMOSC output: 1/1, TV OSC output: 1/2

- R0, 1, 2

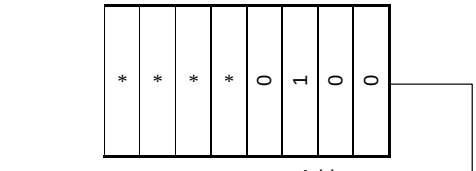
Reference Frequency	R0	R1	R2
1 kHz	0	0	0
1.5625 kHz	1	0	0
3 kHz	0	1	0
3.125 kHz	1	1	0
5 kHz	0	0	1
6.25 kHz	1	0	1
12.5 kHz	0	1	1
25 kHz	1	1	1

- G0, 1

G0	G1	Measuring Time	Waiting Time
0	0	1 ms	3.3 to 4.3 ms
1	0	4 ms	3.3 to 4.3 ms
0	1	16 ms	7.3 to 8.3 ms
1	1	64 ms	7.3 to 8.3 ms

- START: IF count start bit
  When cleared, maintain the count value.
  When set, start measuring and decrease gain by 6dB in the FM/TV IF amplifiers after the count value is reset. MUTE is turned on.
- MUTE: When cleared, MUTE is turned off.
  When set, MUTE is turned on.

Input Mode 2



	MO/ST	LO/DX	OSC0	OSC1	STC	Xtal I1	Xtal I2	PW	TEST1	TEST2	TEST3	TEST4	TEST5	TEST6	TEST7	TEST8
Reset values	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- MO/ST : When cleared, it is in Auto Mode.
  When set, it is in Forced Monaural Mode.
- Lo DX : When cleared, full gain of the FM/TV RF amplifiers
  When set, 40dB less gain than the full gain of FM/TV RF amplifiers.
- OSC level gain : For FM, the oscillation level of the OSC can be reduced from the viewpoint of FCC.
  For AM, to the contrary, the oscillation can be intensified so that the oscillator can run even with a low impedance on the SW band.

OSC0	OSC1	AM OSC	FM OSC
0	0	0dB	0dB
1	0	⊕⊕	⊖⊖
0	1	⊕⊕⊕	⊖⊖⊖
1	1	⊕⊕⊕⊕	⊖⊖⊖⊖

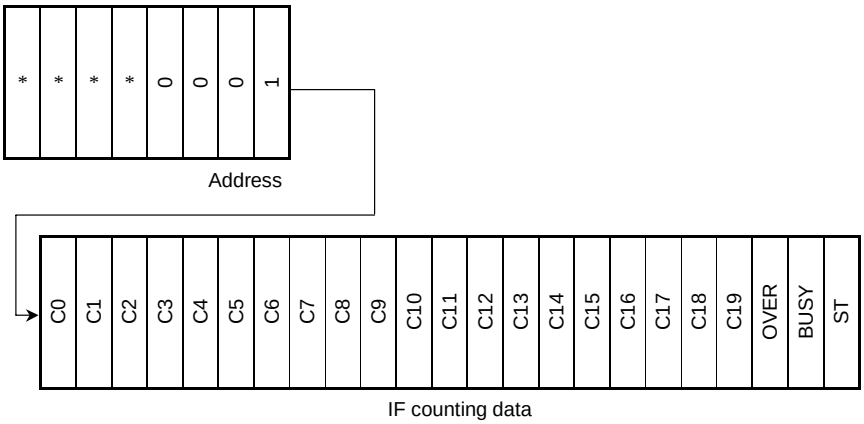
- STC : When cleared, the OUT1 pin is switched to the general-purpose output port.
  When set, the OUT 1 pin is switched to the ST output (stereo output). For stereo reception, the pin is low.
- PW : When the AM, FM 1/32 and TV 1/8 modes are programmed, clear the PW bit.
  When the TV 1/2 and FM are programmed, set the PW bit.
- X'tal I1/X'tal I2 : For FM and TV, set X'tal I1 and X'tal I2 to 0 and 0.
  For AM, the current of the X'tal block can be reduced from the viewpoint of X'tal harmonics interference.

Note: When the standby mode is selected, be sure to reset X'tal I1 and X'tal I2, respectively, to 0 and 0, or the oscillator will fail to run when the standby mode is released.

X'tal I1	X'tal I2	Oscillation Amplitude	Recommended Bandwidth
0	0	Large 1	FM/TV
0	1	Large 2	
1	0	Small 2	
1	1	Small 1	AM

- TEST1 to TEST8: These bits are used for IC testing and must be always 0.

Output Mode



- C0 to 19: General-purpose count data (C0: LSB, C19: MSB)
- OVER: Set 1 when the measured value of general-purpose count data exceeds 20 bits.
- BUSY: When a 0 is read, general-purpose count measurement completes.
  When a 1 is read, general-purpose count measurement is in progress.
- ST: When a 0 is read, it is for monaural reception.
  When a 1 is read, it is for stereo reception.

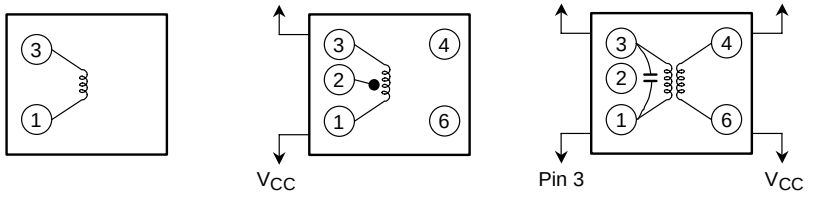
Coil Data

Coil No.	Test Frequency	L (μH)	Co (pF)	Qo	Turns					Wire (mmϕ)	Remarks
					1-2	2-3	1-3	1-4	4-6		
L_1 FM RF	100 MHz	—	—	105	—	—	$3\frac{3}{4}$	—	—	0.12UEW	Toko Co., Ltd. 666SNF-419Z
L_2: TV RF	100 MHz	—	—	55	—	—	1	—	—	0.12UEW	Toko Co., Ltd. 666SNF-413IB
L_3: OSC	100 MHz	—	—	79	—	—	$1\frac{1}{2}$	—	—	0.16UEW	Toko Co., Ltd. P666SNF-421IB
T_1 AM OSC	796 kHz	268	—	65	19	95	—	—	—	0.05UEW	Toko Co., Ltd. 5PNR-4957Y
T_2 AM IFT	455 kHz	—	470	60	—	—	109	—	7	0.05UEW	Toko Co., Ltd. 5PLG-5147X

L_1: FM RF
L_2: TV RF
L_3: OSC

T_1: AM OSC

T_2: AM IFT



Maximum Ratings (Unless otherwise specified, Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}, V_{DD}	−0.3 to 6.0	V
Output with standing voltage (NPN open collector)	V_O	−0.3 to 6.0	
CMOS input voltage	V_{IN}	−0.3 to V_{DD} + 0.3	
Power dissipation (Note)	P_D	500	mW
Operating temperature	T_{opr}	−25 to 75	°C
Storage temperature	T_{stg}	−55 to 150	°C

Note: Power consumption is rated at 25°C. At temperatures higher than 25°C, power consumption is decreased by 4.8 mW per °C.

Electrical Characteristics

1. Tuner Block (Unless otherwise specified,

Ta = 25°C, V_{CC} = 3 V, F/E : f = 98 MHz, f_m = 1 kHz
FM IF: f = 10.7 MHz, Δf = ±75 kHz, f_m = 1 kHz
AM : f = 1 MHz, MOD = 30 %, f_m = 1 kHz
MPX : f_m = 1 kHz, P_{LL} V_{CC} = 3 V)

Characteristics			Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Supply current			$I_{CC\ (TV)}$	—	In TV Mode, V_{in} = 0	1/2 division mode incl. PLL	—	18	—	mA
						1/8 division mode incl. PLL	—	16	23	
			$I_{CC\ (FM)}$	—	In FM Mode, V_{in} = 0	OSC divider bypass mode incl. PLL	—	18	—	
						1/32 division mode incl. PLL	—	16	23	
			$I_{CC\ (AM)}$	—	In AM Mode, V_{in} = 0 (incl. PLL)		—	7.5	11	
F/E	FM input limiting voltage		$V_{in\ (lim)}$	—	V_{in} = 60dBμV EMF, −3dB limiting		—	10	—	dBμV EMF
	TV input limiting voltage			—	V_{in} = 60dBμV EMF, −3dB limiting		—	11	—	dBμV EMF
FM IF	Input limiting voltage		$V_{in\ (lim)\ IF}$	—	V_{in} = 80dBμV EMF, −3dB limiting		38	43	48	dBμV EMF
	Recovered output voltage		V_{OD}	—	V_{in} = 80dBμV EMF		210	260	310	mVrms
	Signal to noise ratio		S/N	—	V_{in} = 80dBμV EMF		—	72	—	dB
	Total harmonic distortion		THD	—	V_{in} = 80dBμV EMF		—	0.3	—	%
	AM rejection ratio		AMR	—	V_{in} = 80dBμV EMF		—	60	—	dB
	IF count sensitivity		IF sens (FM)	—	—		52	57	62	dBμV EMF
AM	Gain		G_V	—	V_{in} = 31dBμV EMF		20	38	70	mVrms
	Recovered output voltage		V_{OD}	—	V_{in} = 60dBμV EMF		65	90	113	mVrms
	Signal to noise ratio		S/N	—	V_{in} = 60dBμV EMF		—	40	—	dB
	Total harmonic distortion		THD	—	V_{in} = 60dBμV EMF		—	1.0	—	%
	IF count sensitivity		IF sens (AM)	—	—		39	44	49	dBμV EMF
MPX	Max. signal input voltage		Vin max (Monaural)	—	fm = 1 kHz, THD = 3%		—	700	—	mVrms
	Input resistance		R_{IN}	—	—		—	55	—	kΩ
	Output resistance		R_{OUT}	—	—		—	5	—	kΩ
	Separation		Sep.	—	L + R = 180 mVrms, P = 20 mVrms SW3: LPF ON	f_m = 100 Hz	—	45	—	dB
						f_m = 1 kHz	35	45	—	
						f_m = 10 kHz	—	45	—	
	Total harmonic distortion	Monaural	THD (Monaural)	—	V_{in} = 200 mVrms		—	0.2	—	%
		Stereo	THD (Stereo)	—	L+R = 180 mVrms, P = 20 mVrms, SW3: LPF ON		—	0.2	—	
	Voltage gain		G_V	—	V_{in} = 200 mVrms		−2.5	−1.0	0.5	dB
	Channel balance		C.B.	—	V_{in} = 200 mVrms		−1.5	0	1.5	dB

Characteristics			Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
MPX	Stereo sensitivity	ON	$V_{L\ (ON)}$	—	Apply pilot signal (19 kHz)	—	10	14	mVrms
		OFF	$V_{L\ (OFF)}$	—		5	8	—	
	Stereo hysteresis		V_H	—	Switched from monaural to stereo operation, and from stereo to monaural operation.	—	2	—	mVrms
	Capture challenge		C.R.	—	P = 20 mVrms	—	±8	—	%
	Signal noise ratio		S/N	—	V_{in} = 200 mVrms	—	78	—	dB
	Muting attenuation		MUTE	—	V_{in} = 200 mVrms	—	78	—	dB

2. PLL Block (Unless otherwise specified, Ta = 25°C, V_{DD} = 3.0 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating supply voltage range	V_{DD}	—		1.8	~	5.5	V
Memory retention voltage range	V_{HD}	—	In Standby Mode	1.55	~	5.5	
Operating supply current	I_{DD1}	—	PLL operation (in pulse swallow mode)	—	3.6	—	mA
	I_{DD2}	—	PLL operation (in direct divide mode)	—	2.2	—	mA
Memory retention current	I_{HD}	—	In Standby Mode	—	0.4	1.0	mA
Crystal oscillation frequency	f_{XT}	—		—	75	—	kHz
Crystal oscillation start time	t_{st}	—	Crystal oscillation frequency = 75 kHz	—	250	—	ms

DATA at Pin 22 and CLOCK at Pin 23, CE at Pin 24

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	Low level	I_{OL1}	—	V_{OL} = 0.3 V	1.0	2.0	—	mA
Input leak current		I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	High level	V_{IH1}	—	—	V_{DD} × 0.8	~	5.5	V
	Low level	V_{IL1}	—	—	0	~	V_{DD} × 0.2	

OUT1 (ST) at Pin 18

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	High level	I_{OH1}	—	$V_{OH} = V_{DD} - 0.3$ V	−0.5	−1.0	—	mA
	Low level	I_{OL1}	—	V_{OL} = 0.3V	1.2	1.7	—	

OUT2 (DO2) at Pin 19

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	High level	I_{OH1}	—	$V_{OH} = V_{DD} - 0.3$ V	−0.3	−0.8	—	mA
	Low level	I_{OL1}	—	V_{OL} = 0.3V	0.5	1.0	—	

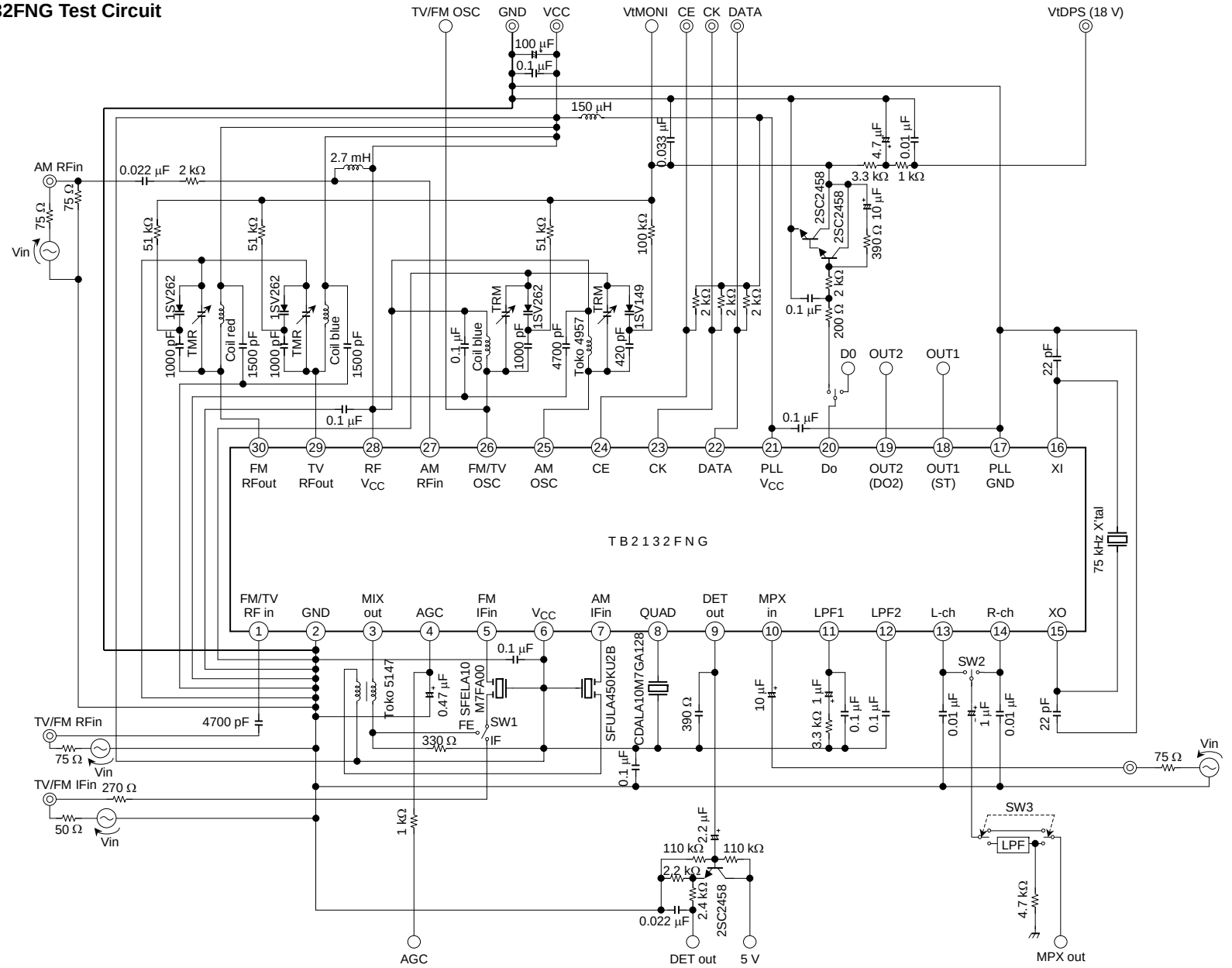
DO at Pin 20

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	High level	I_{OH1}	—	$V_{OH} = \frac{1}{2} V_{DD}$	−1.5	−2.5	—	mA
	Low level	I_{OL1}	—	$V_{OL} = \frac{1}{2} V_{DD}$	2.0	3.0	—	
Output OFF-leak current		I_{TL}	—	$V_O = \frac{1}{2} V_{DD}$	—	—	±100	nA

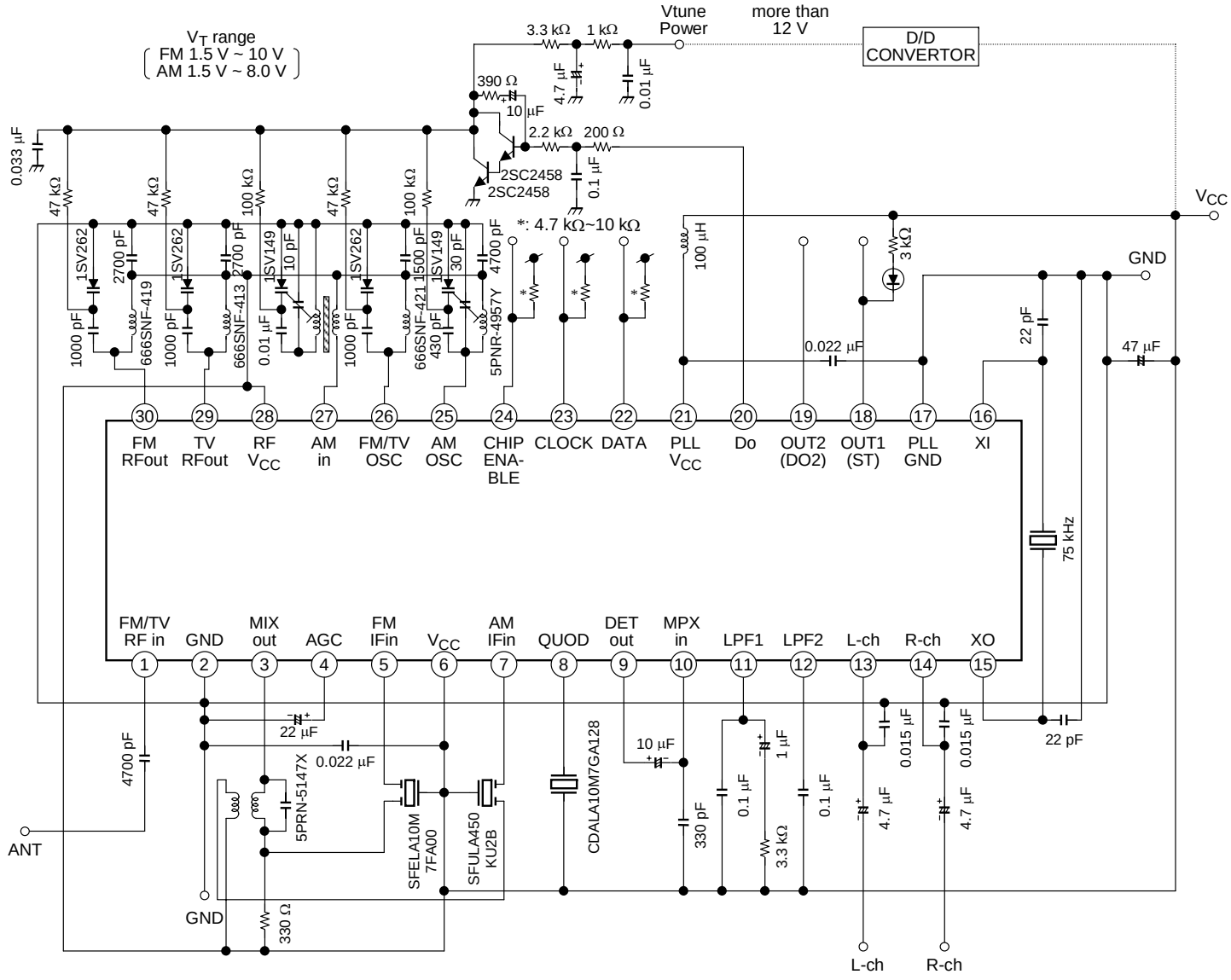
DO2 at Pin 19

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	High level	I_{OH1}	—	$V_{OH} = \frac{1}{2} V_{DD}$	−1.5	−2.5	—	mA
	Low level	I_{OL1}	—	$V_{OL} = \frac{1}{2} V_{DD}$	2.0	3.0	—	
Output OFF-leak current		I_{TL}	—	$V_O = \frac{1}{2} V_{DD}$	—	—	±100	nA

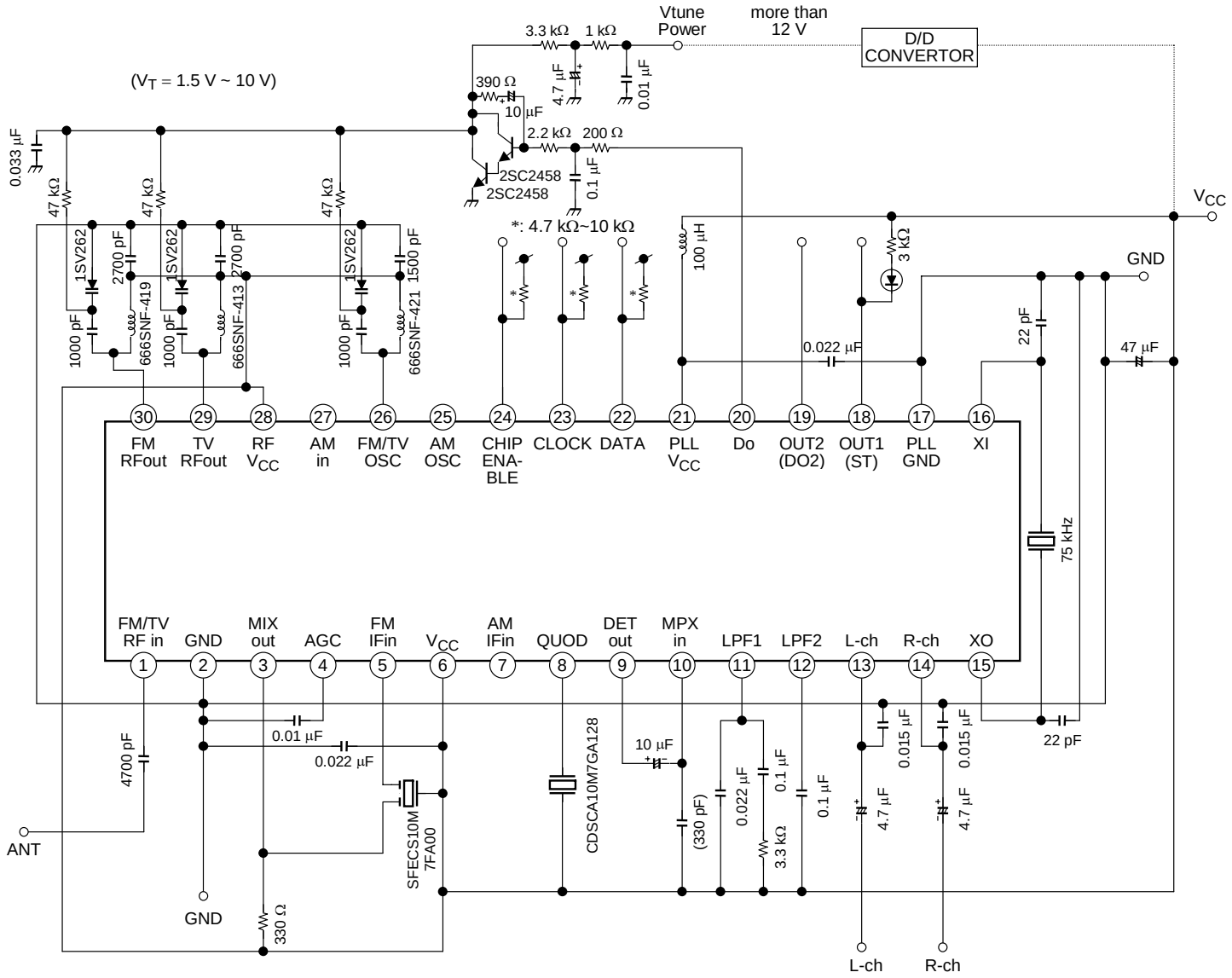
TB2132FNG Test Circuit



Application Circuit

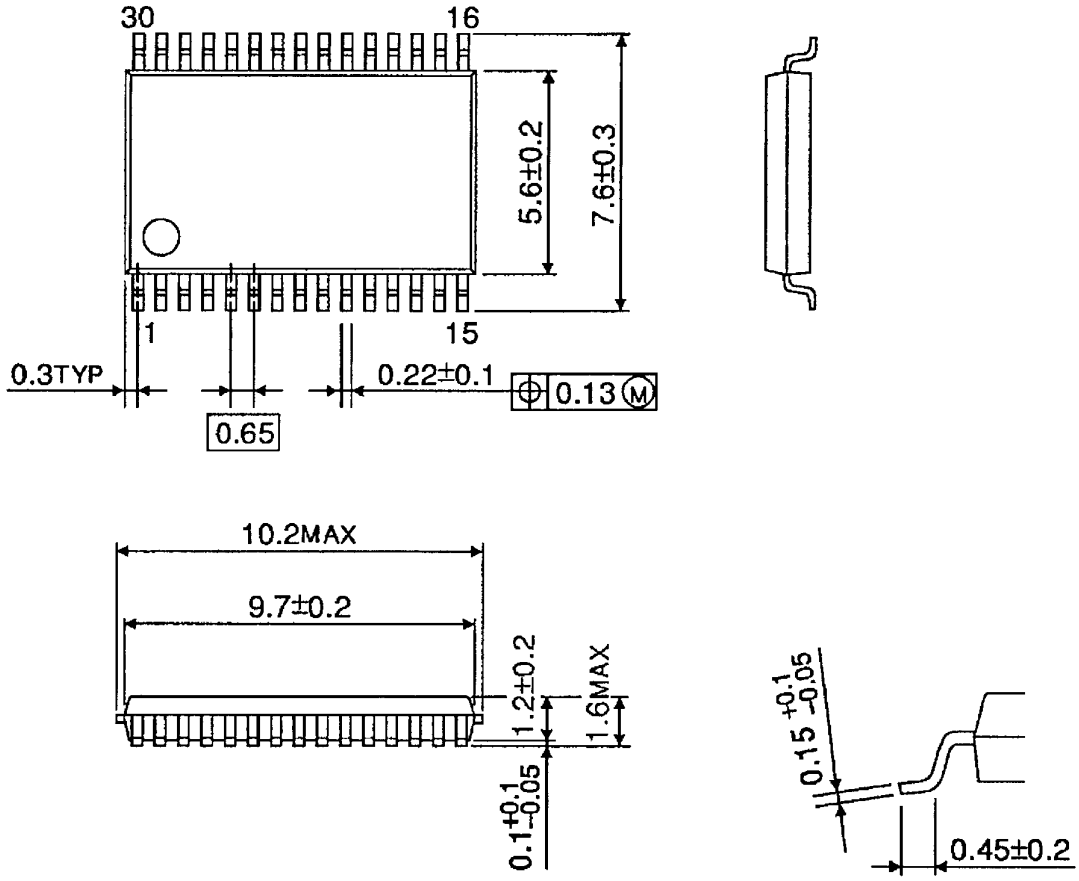


Application Circuit (for FM module) FM/TV



Package Dimensions

SSOP30-P-300-0.65 Unit : mm



Weight: 0.17 g (typ.)

About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-63Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

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