

## TC55257CPL/CFL/CSPL/CFTL/CTRL-70/85/10

PRELIMINARY

### SILICON GATE CMOS

### 32,768 WORD x 8 BIT STATIC RAM

#### Description

The TC55257CPL is a 262,144 bit CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns.

When  $\overline{CE}$  is a logical high, the device is placed in a low power standby mode in which the standby current is 2 $\mu$ A at room temperature. The TC55257CPL has two control inputs. Chip enable ( $\overline{CE}$ ) allows for device selection and data retention control, while an output enable input ( $\overline{OE}$ ) provides fast memory access. The TC55257CPL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required.

The TC55257CPL is offered in a standard dual-in-line 28-pin plastic package (0.6/0.3 inch width), a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

#### Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 100 $\mu$ A (max.)
- Single 5V power supply
- Access time (max.)

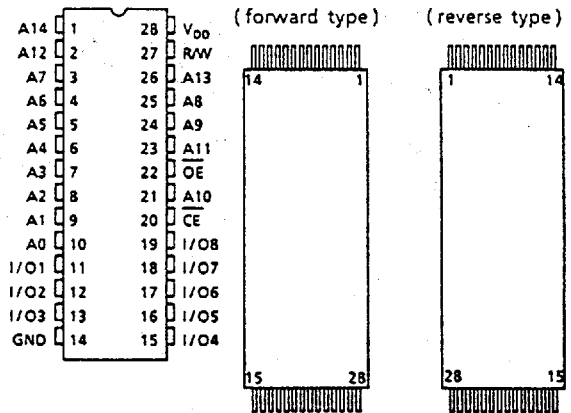
	TC55257CPL/CFL/CSPL/CFTL/CTRL		
	-70	-85	-10
Access Time	70ns	85ns	100ns
$\overline{CE}$ Access Time	70ns	85ns	100ns
$\overline{OE}$ Access Time	35ns	45ns	50ns

- Power down feature:  $\overline{CE}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package
  - TC55257CPL : DIP28-P-600
  - TC55257CFL : SOP28-P-450
  - TC55257CSPL : DIP28-P-300B
  - TC55257CFTL : TSOP28-P
  - TC55257CTRL : TSOP28-P-A

#### Pin Connection (Top View)

○ 28 PIN DIP & SOP

○ 28 PIN TSOP

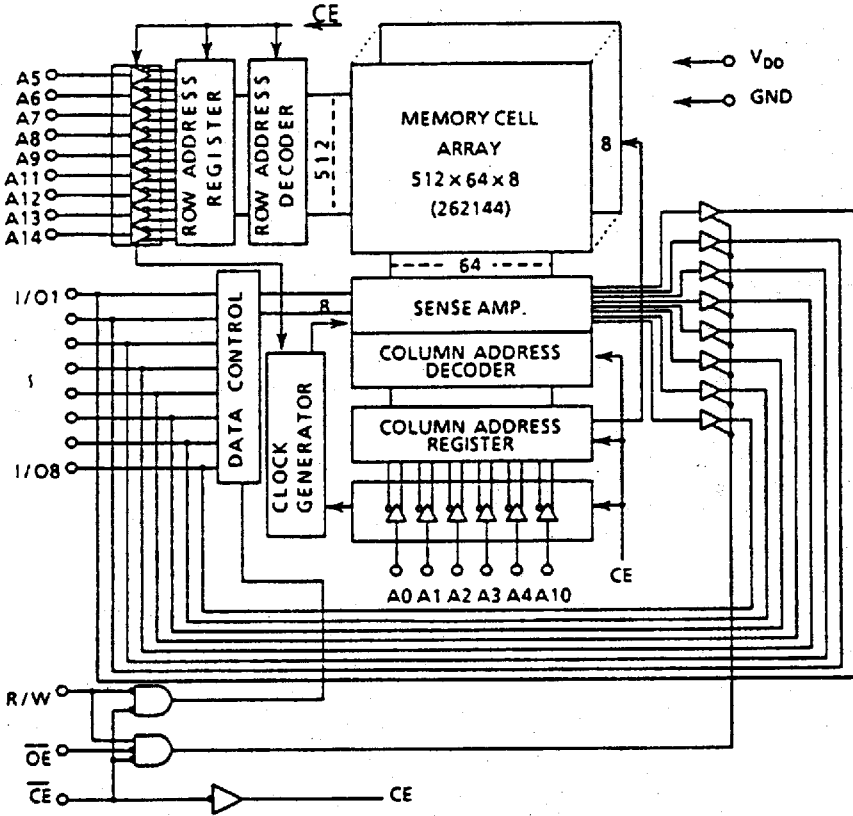


#### Pin Names

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V <sub>DD</sub>	Power (+5V)
GND	Ground

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	$\overline{OE}$	A <sub>11</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>13</sub>	R/W	V <sub>DD</sub>	A <sub>14</sub>	A <sub>12</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A <sub>10</sub>

Block Diagram



Operating Mode

MODE	PIN	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read		L	L	H	D <sub>OUT</sub>	I <sub>DDO</sub>
Write		L	*	L	D <sub>IN</sub>	I <sub>DDO</sub>
Output Deselect		L	H	H	High-Z	I <sub>DDO</sub>
Standby		H	*	*	High-Z	I <sub>DDS</sub>

\* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3 ~ 7.0	V
V <sub>IN</sub>	Input Voltage	-0.3* ~ 7.0	V
V <sub>I/O</sub>	Input and Output Voltage	-0.5* ~ V <sub>DD</sub> + 0.5	V
P <sub>D</sub>	Power Dissipation	1.0/0.8/0.6**	W
T <sub>SOLDER</sub>	Soldering Temperature • Time	260 • 10	°C • sec
T <sub>STRG</sub>	Storage Temperature	-55 ~ 150	°C
T <sub>OPR</sub>	Operating Temperature	0 ~ 70	°C

\* -3.0V with a pulse width of 50ns

\*\* Package dependent: 0.6 inch 1.0W, 0.3 inch 0.8W, 0.45 inch 0.6W

## DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DD}$	Power Supply Voltage	4.5	5.0	5.5	V
$V_{IH}$	Input High Voltage	2.2	—	$V_{DD} + 0.3$	
$V_{IL}$	Input Low Voltage	-0.3*	—	0.8	
$V_{DH}$	Data Retention Supply Voltage	2.0	—	5.5	

\* -3.0V with a pulse width of 50ns

DC Characteristics ( $T_a = 0 \sim 70^\circ\text{C}$ ,  $V_{DD} = 5V \pm 10\%$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
$I_{LI}$	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	$\pm 1.0$	$\mu\text{A}$	
$I_{LO}$	Output Leakage Current	$\overline{CE} = V_{IH}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$	—	—	$\pm 1.0$	$\mu\text{A}$	
$I_{OH}$	Output High Current	$V_{OH} = 2.4\text{V}$	-1.0	—	—	mA	
$I_{OL}$	Output Low Current	$V_{OL} = 0.4\text{V}$	4.0	—	—	mA	
$I_{DDO1}$	Operating Current	$\overline{CE} = V_{IL}$ $R/W = V_{IH}$ Other Input = $V_{IH}/V_{IL}$ $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 1\mu\text{s}$	—	10	—	mA
$I_{DDO2}$		$\overline{CE} = 0.2\text{V}$ $R/W = V_{DD} - 0.2\text{V}$ Other Input = $V_{DD} - 0.2\text{V}/0.2\text{V}$ $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 1\mu\text{s}$	—	5	—	
$I_{DDS1}$	Standby Current	$\overline{CE} = V_{IH}$	—	—	3	mA	
$I_{DDS2}$		$\overline{CE} = V_{DD} - 0.2\text{V}$ $V_{DD} = 2.0\text{V} \sim 5.5\text{V}$	$T_a = 0 \sim 70^\circ\text{C}$	—	—	100	$\mu\text{A}$
		$T_a = 25^\circ\text{C}$	—	2	—		

Capacitance\* ( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ )

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = \text{GND}$	10	

\*This parameter is periodically sampled and is not 100% tested.

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AC Characteristics ( $T_a = 0 \sim 70^\circ\text{C}$ ,  $V_{DD} = 5V \pm 10\%$ )

## Read Cycle

SYMBOL	PARAMETER	TC55257CPL/CFL/CSPL/CFTL/CTRL						UNIT
		-70		-85		-10		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{RC}$	Read Cycle Time	70	—	85	—	100	—	ns
$t_{ACC}$	Address Access Time	—	70	—	85	—	100	
$t_{CO}$	$\overline{CE}$ Access Time	—	70	—	85	—	100	
$t_{OE}$	Output Enable to Output in Valid	—	35	—	45	—	50	
$t_{COE}$	Chip Enable ( $\overline{CE}$ ) to Output in Low-Z	10	—	10	—	10	—	
$t_{OEE}$	Output Enable to Output in Low-Z	5	—	5	—	5	—	
$t_{OD}$	Chip Enable ( $\overline{CE}$ ) to Output in High-Z	—	25	—	30	—	50	
$t_{ODO}$	Output Enable to Output in High-Z	—	25	—	30	—	40	
$t_{OH}$	Output Data Hold Time	10	—	10	—	10	—	

## Write Cycle

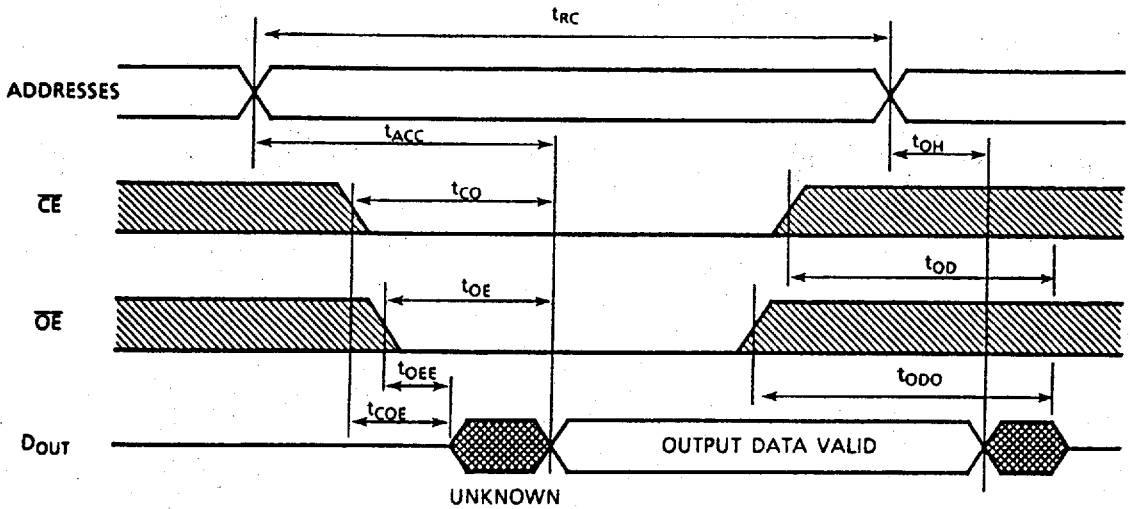
SYMBOL	PARAMETER	TC55257CPL/CFL/CSPL/CFTL/CTRL						UNIT
		-70		-85		-10		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{WC}$	Write Cycle Time	70	—	85	—	100	—	ns
$t_{WP}$	Write Pulse Width	50	—	60	—	70	—	
$t_{CW}$	Chip Selection to End of Write	60	—	65	—	90	—	
$t_{AS}$	Address Setup Time	0	—	0	—	0	—	
$t_{WR}$	Write Recovery Time	0	—	0	—	0	—	
$t_{ODW}$	R/W to Output in High-Z	—	25	—	30	—	50	
$t_{OEW}$	R/W to Output in Low-Z	5	—	5	—	5	—	
$t_{DS}$	Data Setup Time	30	—	40	—	40	—	
$t_{DH}$	Data Hold Time	0	—	0	—	0	—	

## AC Test Conditions

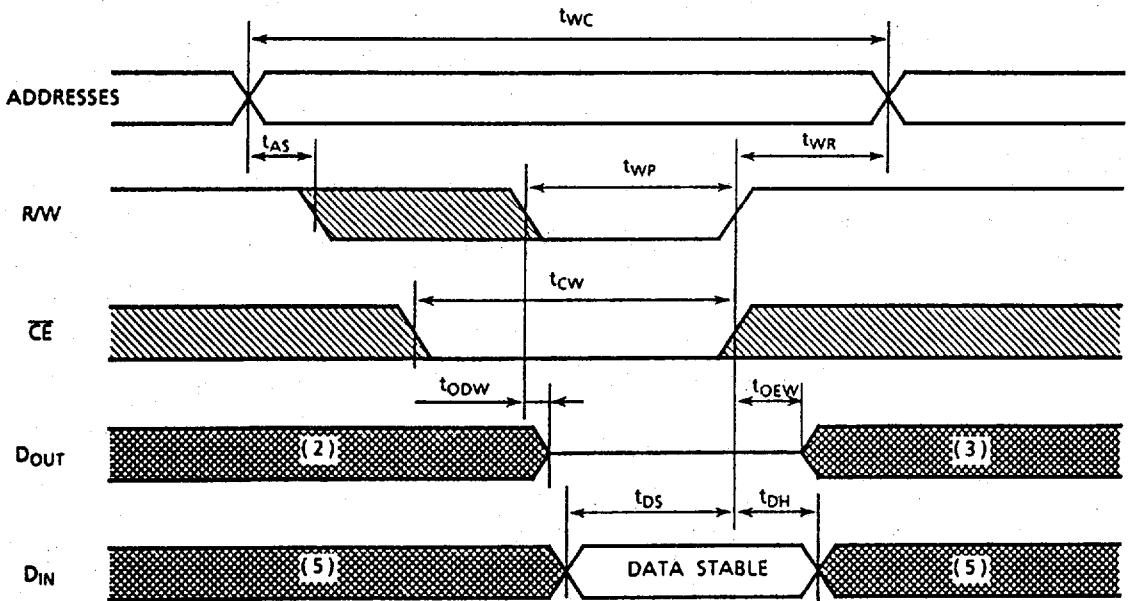
Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and $C_L = 100\text{pF}$

Timing Waveforms

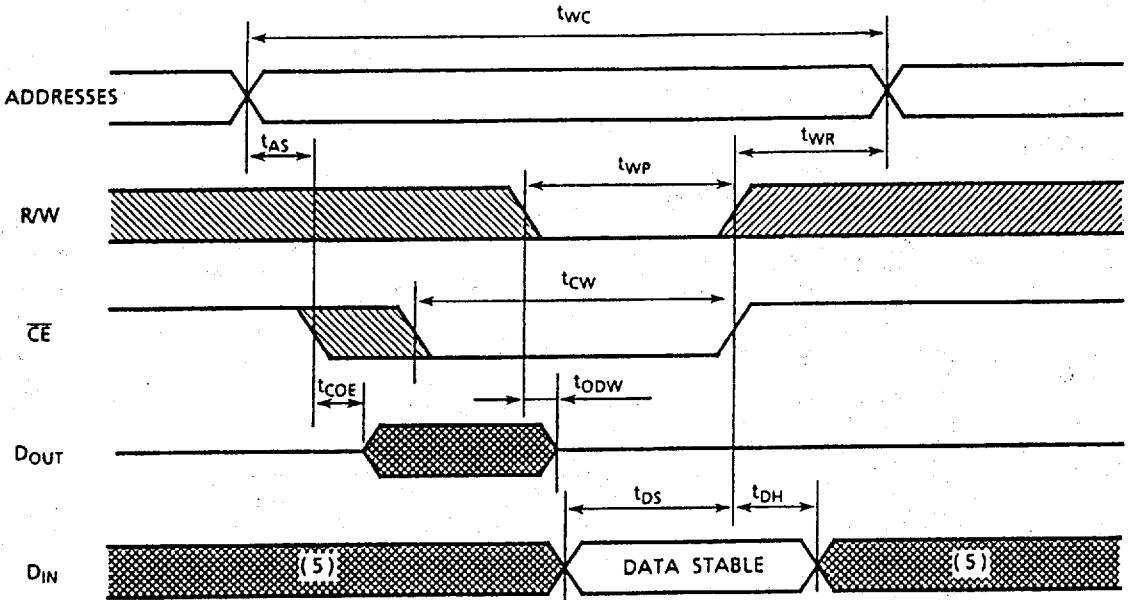
Read Cycle (1)



Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 <sup>(4)</sup> ( $\overline{CE}$  Controlled Write)



Notes:

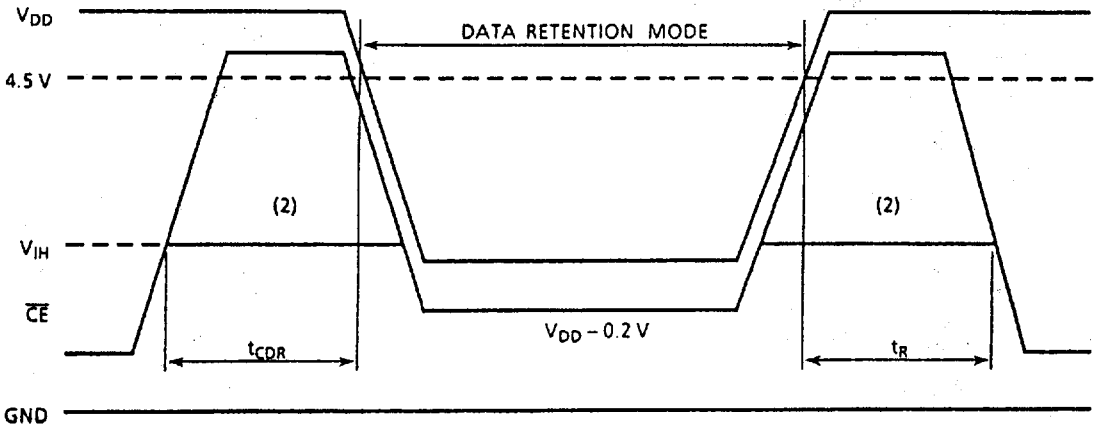
1. R/W is high for read cycles.
2. If the  $\overline{CE}$  low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the  $\overline{CE}$  high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If  $\overline{OE}$  is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.

**Data Retention Characteristics (Ta = 0 ~ 70°C)**

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	—	5.5	V
I <sub>DDS2</sub>	Standby Current	V <sub>DH</sub> = 3.0V	—	50	μA
		V <sub>DH</sub> = 5.5V	—	100	
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode	0	—	—	ns
t <sub>R</sub>	Recovery Time	t <sub>RC(1)</sub>	—	—	

Note (1): Read Cycle Time

**$\overline{CE}$  Controlled Data Retention Mode**



Note (2): If the V<sub>IH</sub> of  $\overline{CE}$  is 2.2V in operation, I<sub>BDS1</sub> current flows during the period that the V<sub>DD</sub> voltage is going down from 4.5V to 2.4V.

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