

GENERAL DESCRIPTION

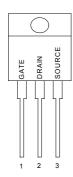
This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced MOSFET is designed to withstand high energy in avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional and safety margin against unexpected voltage transients.

FEATURES

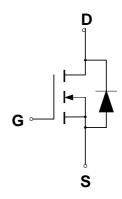
- Robust High Voltage Termination
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- ♦ I_{DSS} and V_{DS}(on) Specified at Elevated Temperature

PIN CONFIGURATION

TO-220 Top View



SYMBOL



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS

Rating		Value	Unit
Drain to Current - Continuous		10	Α
- Pulsed	I _{DM}	40	
Gate-to-Source Voltage - Continue		±20	V
- Non-repetitive	V_{GSM}	±40	V
Total Power Dissipation		125	W
Derate above 25		1.0	W/
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to 150	
Single Pulse Drain-to-Source Avalanche Energy - T _J = 25	E _{AS}	300	mJ
$(V_{DD} = 100V, V_{GS} = 10V, I_{L} = 10A, L = 6mH, R_{G} = 25\Omega)$			
Thermal Resistance - Junction to Case	θ_{JC}	1.7	/W
- Junction to Ambient	θ_{JA}	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	



ORDERING INFORMATION

Part Number	Package
CMT10N40N220	TO-220

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_J = 25$.

			CMT10N40			
Characteristic		Symbol	Min	Тур	Max	Units
Drain-Source Breakdown Voltage		V _{(BR)DSS}	400			V
$(V_{GS} = 0 \text{ V}, I_D = 250 \mu \text{ A})$						
Drain-Source Leakage Current		I _{DSS}				μΑ
$(V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V})$					25	
$(V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125)$					250	
Gate-Source Leakage Current-Forward		I_{GSSF}			100	nA
$(V_{gsf} = 20 \text{ V}, V_{DS} = 0 \text{ V})$						
Gate-Source Leakage Current-Reverse		I_{GSSR}			100	nA
$(V_{gsr} = 20 \text{ V}, V_{DS} = 0 \text{ V})$						
Gate Threshold Voltage		$V_{GS(th)}$	2.0		4.0	V
$(V_{DS} = V_{GS}, I_D = 250 \mu A)$						
Static Drain-Source On-Resistance (V	_{GS} = 10 V, I _D = 5.0A) *	R _{DS(on)}			0.55	Ω
Drain-Source On-Voltage (V _{GS} = 10 V)		$V_{DS(on)}$			6.0	V
$(I_D = 5.0 \text{ A})$						
Forward Transconductance (V _{DS} = 50 '	V, I _D = 5.0A) *	g _{FS}	5.8			mhos
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$	C_{iss}		1570		pF
Output Capacitance	$(v_{DS} = 25 \text{ V}, v_{GS} = 0 \text{ V},$ f = 1.0 MHz)	C _{oss}		230		pF
Reverse Transfer Capacitance	1 – 1.0 MH2)	C_{rss}		55		pF
Turn-On Delay Time	0/ 000 // 1 40 0 4	t _{d(on)}		25		ns
Rise Time	$(V_{DD} = 200 \text{ V}, I_D = 10.0 \text{ A},$	t _r		37		ns
Turn-Off Delay Time	V _{GS} = 10 V,	$t_{d(off)}$		75		ns
Fall Time	$R_G = 10\Omega) *$	t_{f}		31		ns
Total Gate Charge	0/ 0001/ 1 40.04	Q_{g}		46	63	nC
Gate-Source Charge	$(V_{DS} = 320 \text{ V}, I_D = 10.0 \text{ A},$	Q_{gs}		10		nC
Gate-Drain Charge	V _{GS} = 10 V)*	Q_{gd}		23		nC
Internal Drain Inductance		L _D		4.5		nH
(Measured from the drain lead 0.25"	from package to center of die)					
Internal Drain Inductance		Ls		7.5		nH
(Measured from the source lead 0.25" from package to source bond pad)						
SOURCE-DRAIN DIODE CHARACTE	RISTICS	·	•			
Forward On-Voltage(1)	# 40.0 A V 0V	V_{SD}			1.5	V
Forward Turn-On Time	$(I_S = 10.0 \text{ A}, V_{GS} = 0 \text{ V},$	t _{on}		**		ns
Reverse Recovery Time	$d_{IS}/d_t = 100A/\mu s)$	t _{rr}		250		ns

 $^{^{\}star}$ Pulse Test: Pulse Width ~~ 300µs, Duty Cycle ~~ 2%

^{**} Negligible, Dominated by circuit inductance



TYPICAL ELECTRICAL CHARACTERISTICS

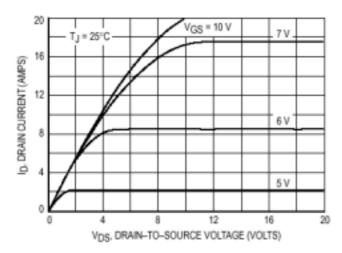


Figure 1. On-Region Characteristics

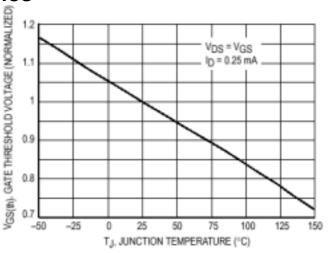


Figure 2. Gate-Threshold Voltage Variation With Temperature

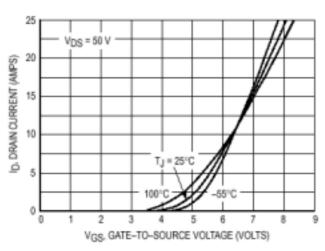


Figure 3. Transfer Characteristics

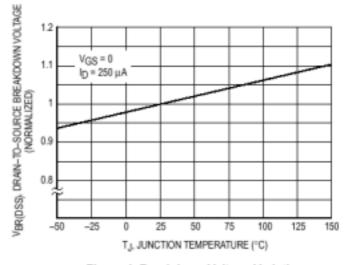


Figure 4. Breakdown Voltage Variation With Temperature

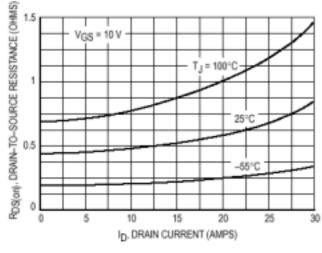


Figure 5. On-Resistance versus Drain Current

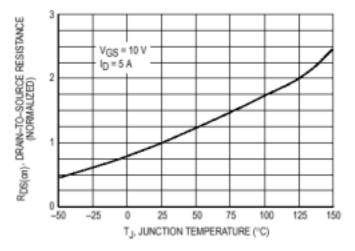
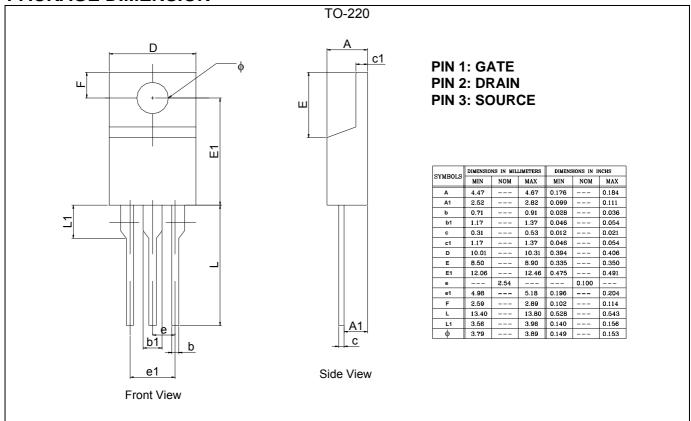


Figure 6. On–Resistance Variation With Temperature



PACKAGE DIMENSION





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