Ordering number : EN *5846

CMOS IC

LC82221L

Motion JPEG Decoder

Preliminary

Overview

The LC82221L is a full-color digital image data expansion IC that accepts data in formats that essentially conform to the JPEG standard. With the provision of frame memory, this IC can input and output image data in standard video formats. In addition, it also supports a wide range of image display functions using that frame memory. As compared to earlier JPEG ICs, this IC features simplified JPEG functionality and a greater emphasis on display functions. Thus it supports the creation of excellent cost-performance ratio systems for applications that require a display system.

Features

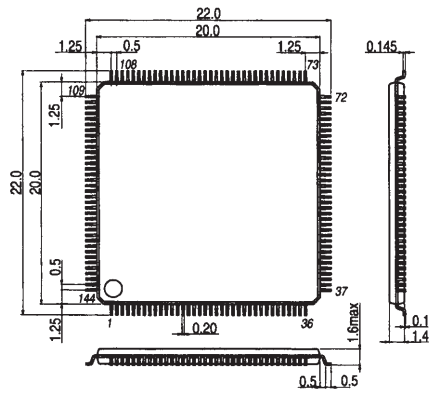
- High image quality image expansion using the JPEG system
- Superlative cost performance achieved by only providing decoding functions.
- Two built-in quantization tables.
- High-speed processing achieved by using fixed Huffman tables. Application do not have to set up these tables.
- Two Huffman tables, one for luminance data and one for chrominance data, are provided.
- Supports scaling factor parameters that allow the quantization factor to be changed.
- DRAM for code data buffering and image data playback can be connected directly.
- Applications can use either 2Mb or 4Mb DRAMs based on the sizes of the image handled and the structure of the system. However, 16-bit data path DRAMs must be used.
- Image data is output in synchronization with an image display synchronizing signal.
- Color structure of the code data is Y:U:V=4:1:1.
- Dedicated code data input bus provided to avoid loading the host bus. DMA transfers are also supported.
- Users can select either RGB or YUV for image data output.
- Built-in YUV to RGB color conversion circuit
- The LC82221L supports image sizes up to 1024 pixels in the horizontal direction. The range of vertical sizes handled can be set up arbitrarily, since it is limited by the size of the DRAM provided.
- 3.3-V single-voltage power supply. Low power.
- The display position and display size can be set.
- SOI and EOI marker support
- Horizontal and vertical scrolling display functions
- Support for overwrite display, in which the next data for expansion is displayed by overwriting the previously expanded image data

Package Dimensions

unit: mm

3214-SQFP144

[LC82221L]

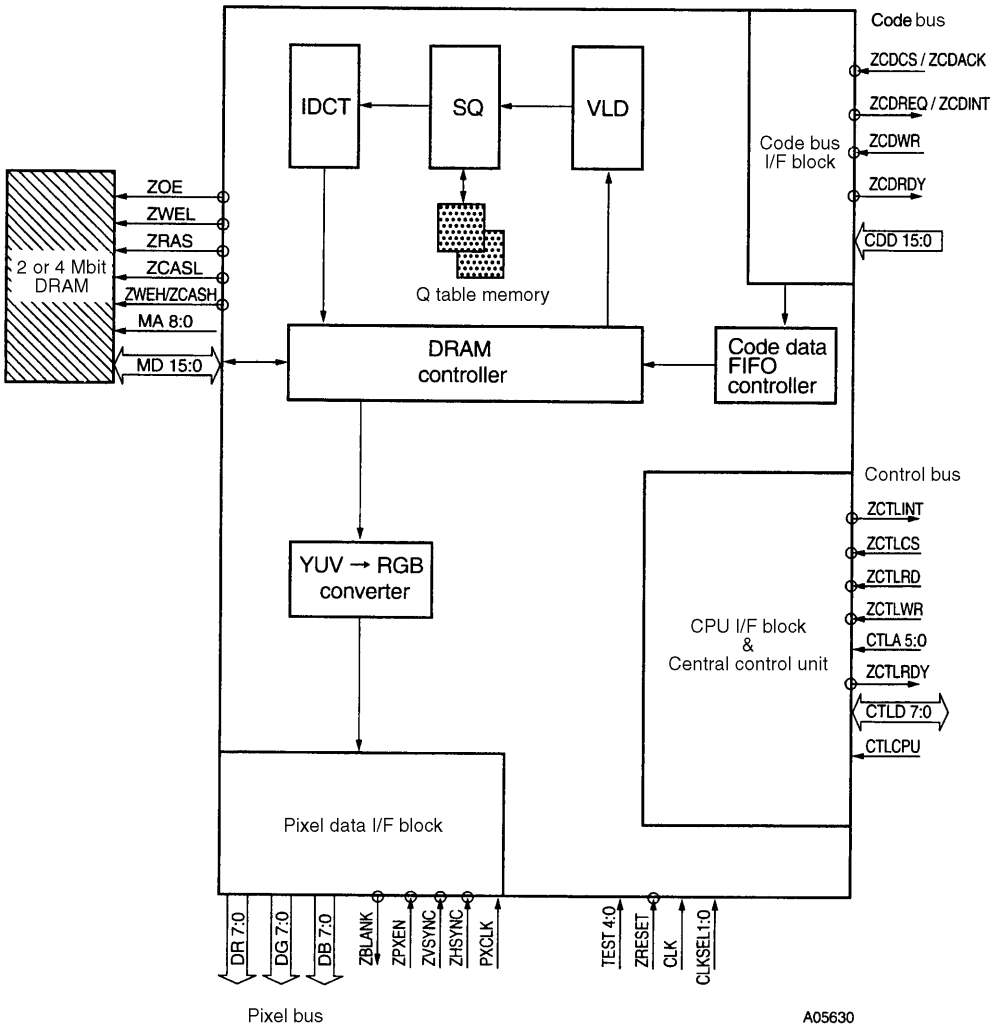


SANYO: SQFP144

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Block Diagram



Specifications

Electrical Characteristics

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD}		–0.3 to +4.6	V
Input and output voltage	V_I, V_O		–0.3 to V_{DD}+0.3	V
Input and output current	I_I, I_O		–20 to +20	mA
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C

Allowable Operating Ranges at Ta = –30 to +70°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		3.0	3.3	3.6	V
Input voltage	V_{IN}		0		V_{DD}	V

DC Characteristics at Ta = –30 to +70°C, V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level voltage	$V_{IH}1$	CMOS level inputs: (1)	0.7 V_{DD}			V
Input low-level voltage	$V_{IL}1$				0.2 V_{DD}	V
Input high-level voltage	$V_{IH}2$	CMOS level Schmitt inputs: (2)	0.75 V_{DD}			V
Input low-level voltage	$V_{IL}2$				0.15 V_{DD}	V
Input high-level current	I_{IH}	V_{IN} = V_{DD}; All input pins (including bus pins)	–10		+10	µA
Input low-level current	$I_{IL}1$	V_{IN} = V_{SS} : (3)	–10		+10	µA
	$I_{IL}2$	V_{IN} = V_{DD}; Pins with pull-up resistors: (4)	–100		–10	µA
Output high-level voltage	V_{OH}	I_{OH} = –6 mA; All output pins (including bus pins)	V_{DD} – 0.8			V
Output low-level voltage	V_{OL}	I_{OL} = 6 mA; All output pins (including bus pins)			0.4	V
Output leakage current	I_{OZ}	When set to high-impedance output: (5)	–10		+10	µA
Pull-up resistance	R_{UP}	(6)	70	140	280	kΩ

Applicable Pins

(1) CTLCPU, CTLA, CTLD, CLKSEL, CLK, CDD, TEST, MD, DG, DB, DR, ZPXEN, ZHSYNC, ZVSYNC, PXCLK

(2) ZCTLCS, ZCTLRD, ZCTLWR, ZRESET, ZCDCS, ZCDWR

(3) CTLCPU, CTLA, CTLD, CLKSEL, CLK, CDD, TEST, DG, DB, DR, ZPXEN, ZHSYNC, ZVSYNC, PXCLK, ZCTLCS, ZCTLRD, ZCTLWR, ZRESET, ZCDCS, ZCDWR

(4) MD

(5) ZCTLRDY, CTLD, ZCDRDY, MD, DG, DB, DR

(6) MD

Pin Functions

Pin Number	Pin Name	Type	Description
1	V_{SS}		Ground
2	ZCTLINT	O	Control bus interrupt request
3	ZCTLCS	I	Control bus select
4	ZCTLRD/RW	I	Control bus read or R/W select
5	ZCTLWR/DS	I	Control bus write/data strobe
6	ZCTLRDY	O	Control bus ready (tri-state output)
7	CTLCPU	I	Control bus CPU type selection
8	V_{DD}		+3.3-V power supply
9	V_{SS}		Ground
10		NC	
11		NC	
12	CTLA5	I	Control bus address
13	CTLA4	I	
14	CTLA3	I	
15	CTLA2	I	
16	CTLA1	I	
17	CTLA0	I	
18	V_{DD}		+3.3-V power supply
19	V_{SS}		Ground
20	CTLD7	I/O	Control bus data
21	CTLD6	I/O	
22	CTLD5	I/O	
23	CTLD4	I/O	
24	CTLD3	I/O	
25	CTLD2	I/O	
26	CTLD1	I/O	
27	CTLD0	I/O	
28	V_{DD}		+3.3-V power supply
29	V_{SS}		Ground
30	CLKSEL0	I	Clock divisor setting
31	CLKSEL1	I	CLKSEL1:0 = 00: No divisor, 01: Divisor = 2, 10: Divisor = 3.
32	CLK	I	System (decode) clock input
33		NC	
34	ZRESET	I	Hardware reset
35		NC	
36	V_{SS}		Ground
37	V_{DD}		+3.3-V power supply
38	ZCDCS/ZCDACK	I	Code bus select/code bus DMA acknowledge
39	ZCDINT/ZCDREQ	O	Code bus interrupt/code bus DMA request
40	ZCDWR	I	Code bus data write signal
41	ZCDRDY	O	Code bus ready (tri-state output)
42	CDD15	I	Code bus data (CDD8 to CDD15 are unused in 8-bit mode.*)
43	CDD14	I	
44	CDD13	I	
45	CDD12	I	

Note: * These pins must be pulled up with a resistance of about 10 kΩ.

Continued on next page.

Continued from preceding page.

Pin Number	Pin Name	Type	Description
46	V_{DD}		+3.3-V power supply
47	V_{SS}		Ground
48	CDD11	I	Code bus data
49	CDD10	I	
50	CDD9	I	
51	CDD8	I	
52	CDD7	I	
53	CDD6	I	
54	V_{DD}		+3.3-V power supply
55	V_{SS}		Ground
56	CDD5	I	Code bus data
57	CDD4	I	
58	CDD3	I	
59	CDD2	I	
60	CDD1	I	
61	CDD0	I	
62	V_{SS}		+3.3-V power supply
63	V_{DD}		Ground
64		NC	
65		NC	
66		NC	
67	TEST0	I	Test pins *
68	TEST1	I	
69	TEST2	I	
70	TEST3	I	
71	TEST4	I	
72	V_{SS}		Ground
73	V_{DD}		+3.3-V power supply
74	ZOE	O	Memory output enable
75	ZWEL	O	Memory write enable (L)
76	ZRAS	O	Row address strobe
77	ZCASL	O	Column address strobe (L)
78	ZWEH/ZCASH	O	Memory write enable (H)/column address strobe (H)
79	V_{SS}		Ground
80	MD15	I/O	Frame memory interface data bus
81	MD14	I/O	
82	MD13	I/O	
83	MD12	I/O	
84	MD11	I/O	
85	MD10	I/O	
86	MD9	I/O	
87	MD8	I/O	
88	MD7	I/O	
89	MD6	I/O	
90	V_{DD}		+3.3-V power supply

Note:* These pins must be tied to ground.

Continued on next page.

Continued from preceding page.

Pin Number	Pin Name	Type	Description
91	V_{SS}		Ground
92	MD5	I/O	Frame memory interface data bus
93	MD4	I/O	
94	MD3	I/O	
95	MD2	I/O	
96	MD1	I/O	
97	MD0	I/O	
98	V_{DD}		+3.3-V power supply
99	MA8	O	Frame memory address signals
100	MA7	O	
101	MA6	O	
102	MA5	O	
103	MA4	O	
104	MA3	O	
105	MA2	O	
106	MA1	O	
107	MA0	O	
108	V_{SS}		Ground
109	V_{DD}		+3.3-V power supply
110	DG7	O	Pixel data bus G (U) *
111	DG6	O	
112	DG5	O	
113	DG4	O	
114	DG3	O	
115	DG2	O	
116	DG1	O	
117	DG0	O	
118	V_{SS}		Ground
119	V_{DD}		+3.3-V power supply
120	DB7	O	Pixel data bus B (V) *
121	DB6	O	
122	DB5	O	
123	DB4	O	
124	DB3	O	
125	DB2	O	
126	V_{DD}		+3.3-V power supply
127	V_{SS}		Ground
128	DB1	O	Pixel data bus B (V) *
129	DB0	O	
130	DR7	O	Pixel data bus R (Y) *
131	DR6	O	
132	DR5	O	
133	DR4	O	
134	V_{SS}		Ground

Note: * These pins must be pulled up with a resistance of about 10 kΩ.

Continued on next page.

Continued from preceding page.

Pin Number	Pin Name	Type	Description
135	DR3	O	Pixel data bus R (Y) *
136	DR2	O	
137	DR1	O	
138	DR0	O	
139	ZPXEN	I	Pixel data enable signal
140	ZBLANK	O	Blanking signal
141	ZHSYNC	I	Horizontal synchronizing signal
142	ZVSYNC	I	Vertical synchronizing signal
143	PXCLK	I	Pixel clock
144	V_{DD}		+3.3-V power supply

Note:* These pins must be pulled up with a resistance of about 10 kΩ.