FEATURES

- ☐ TTL or CMOS compatible
- ☐ RS-170 and RS-343A compatible
- ☐ Low power (100 mW)
- ☐ Up to 75 MHz update rate
- ☐ Single 5 V operation
- ☐ Internal reference

GENERAL DESCRIPTION

The SC11401, SC11402, SC11403 and SC11404 are monolithic CMOS video Digital to Analog Converters (DACs) that provide RS-170 and RS-343A composite video signals. The 24-pin SC11401 and SC11403 are pin and function compatible with the Telmos TLM1840, and TLM1850 (25 MHz device), but Sierra DACs operate at 40 MHz (Telmos TLM1842 and TLM1852).

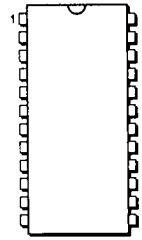
The SC11402 and SC11404 are 20 pin versions in which the Sync Adjust (SADJ), Composite Blank Adjust (CADJ), Bright Adjust (BADJ) and INVERT lines are not brought out. In these devices, INVERT is tied low and data is NOT complemented.

The video DACs take an 8-bit data word, in either true or complement logic, and output a current (Io) with a full scale value set by an external resistor (FS ADJ pin). Normally, the full scale value is adjusted to give 661 millivolts (=255 LSB) across a 75 Ω load. Input data is latched when the CLOCK line is high, and transferred to the output when the CLOCK line goes low. The DACs can be set to zero or full scale with the $\overline{\text{CLEAR}}$ or $\overline{\text{SET}}$ lines, respectively. The $\overline{\text{CLEAR}}$ line requires a clock pulse, just like the data lines, but the $\overline{\text{SET}}$ line is asynchronous and overrides the $\overline{\text{CLEAR}}$ line.

An auxiliary output current (Io') is used when composite video is desired. In this case, Io and Io' are tied together. Their combined values are normally set to 13.33 mA to give a total full scale value (Reference White) of 1,000 mV across a 75 Ω load. Io' is controlled by the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ lines.

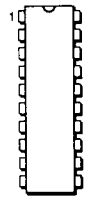
Additionally, Io' can be boosted 28 LSB by pulling the $\overline{\text{BRIGHT}}$ line low. This is useful for intensifying an image.

24-PIN DIP PACKAGE



SC11401CN (40 MHz)
SC11401CN-2 (40 MHz)
SC11403CN (75 MHz)
SC11403CN-2 (75 MHz)

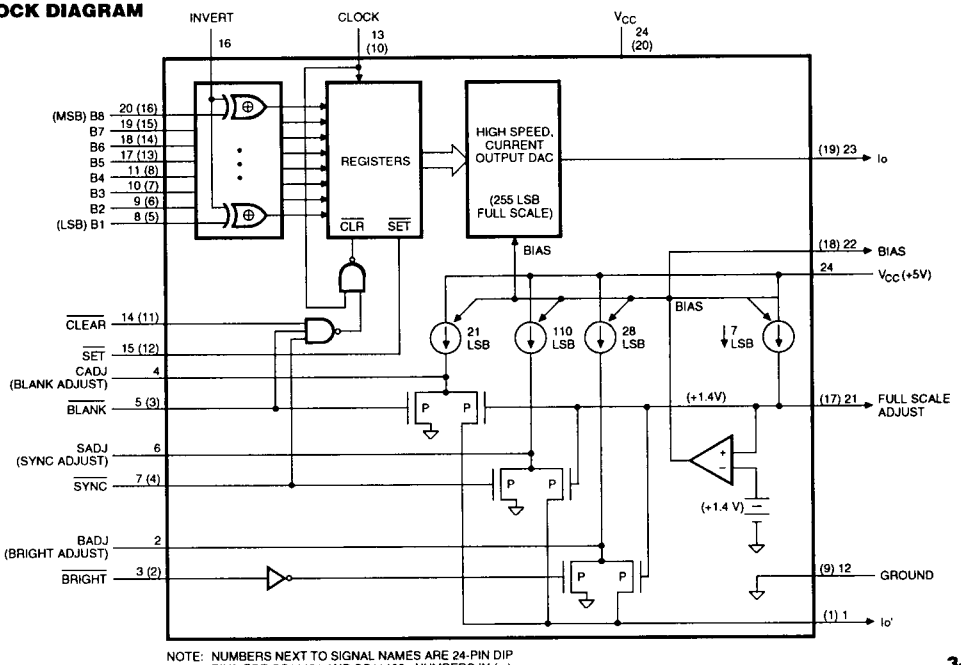
20-PIN DIP PACKAGE



SC11402C (40 MHz)
SC11402CN-2 (40 MHz)
SC11404CN (75 MHz)
SC11404CN-2 (75 MHz)

-2 signifies ± 2 LSB linearity not 1 LSB

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES ARE 24-PIN DIP PINS FOR SC11401 AND SC11403. NUMBERS IN ( ) ARE 20-PIN DIP PINS FOR SC11402 AND SC11404.

PIN DESCRIPTIONS (SC11401 AND SC11403)

PIN	NAME	DESCRIPTION
1, 23	Io', Io	Current source outputs. Io is the output of the 8 bit DAC, Io' is the composite output consisting of Sync, Blank, and Bright components.
2, 4, 6	BADJ, CADJ SADJ	Adjust the values of Bright, Blank, and Sync current sources. See Figure 2 for a typical connection. The current that is fed into these pins will sum with their nominal values.
3, 5, 7	$\overline{\text{BRIGHT}}$,	Control the Bright, Blank, and Sync current sources. Note that $\overline{\text{BLANK}}$, $\overline{\text{BRIGHT}}$ turns on the Bright current source by going LOW. $\overline{\text{BLANK}}$ $\overline{\text{SYNC}}$ and $\overline{\text{SYNC}}$ are the opposite.
8–11, 17–20	B1–B8	The data lines. B1 is the LSB line.
12	GND	GND is digital and analog ground.
24	V_{CC}	V_{CC} is +5 V and should be bypassed directly to GND with at least a 0.1 µF capacitor.
13	CLOCK	Strobes in the data on lines B1–B8. Also used to strobe in $\overline{\text{CLEAR}}$. Data is loaded into the registers while the CLOCK line is high, and transferred to the 8 bit DAC when the CLOCK line goes low.
14	$\overline{\text{CLEAR}}$	Sets the 8 bit DAC to zero (Reference Black) if this line is held low while CLOCK is high. $\overline{\text{CLEAR}}$ is overridden by $\overline{\text{SET}}$.
15	$\overline{\text{SET}}$	Asynchronously sets the registers to full scale (all 1's) if pulled low. This sets the DAC to full scale (Reference White) independent of the CLOCK $\overline{\text{CLEAR}}$, $\overline{\text{SYNC}}$ or $\overline{\text{BLANK}}$ lines.
16	INVERT	Complements the data if pulled high. If left low, the data is unchanged on its way to the registers.
21	FS ADJ	Adjusts the full scale output of the DAC. Since Io' tracks Io, its value is also set by this pin. An internal op amp holds this pin at about +1.4 V. A resistor, Rfs, between this pin and GND sets up the full scale current. The current through the resistor (1.4 V/Rfs) represents 7 LSB. Thus full scale (255 LSB) is (1.4 V/Rfs) • (255/7) = 51/Rfs, where Rfs is expressed in Ω. Normally, for a full scale DAC output of 92.5 IRE (92.5/140 = 0.661 V) and a 75 Ω load, one would use a value of 0.661 V/75 Ω = 51/Rfs. This gives a value of about 5780 W for Rfs. Half this value would produce twice the current — as would be the case if the load was a doubly terminated 75 Ω cable (75 Ω resistors on both ends of the cable).
22	BIAS	Internal line for setting up the current sources. It should be bypassed to V_{CC} (+5 V) with a 0.1 µF capacitor.

FUNCTIONAL DESCRIPTION

The SC11401 family of video DACs differ only in pinout and performance. All have a high speed, current output (Io), 8 bit DAC for the video part of the signal and three separate current sources (Sync, Blank, and Bright) compromising the composite signal (Io').

Figure 1 is a functional block diagram of the SC11401 and SC11403. The SC11402 and SC11404 are similar but the SADJ (Sync Adjust), CADJ (Composite Blank Adjust), BADJ (Bright Adjust) and INVERT lines are not brought out—INVERT is tied low—data is NOT complemented.

Data, B1 through B8, comes into the chip where it is complemented if the INVERT line is high. The data then is latched, and the latches drive an 8 bit DAC. The full scale output of the DAC is determined by a resistor connected from the FS ADJ pin to ground (GND). The current through this resistor represents a value of 7 LSB. Voltage across this resistor is held at about 1.4 V by an op amp that holds the resistor voltage at the same potential as an internal 1.4 V reference. The op amp's output, BIAS, should be bypassed to VCC with a 0.1 µF capacitor.

The three current sources that compromise Io' work independently of the 8 bit DAC. However, both $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$, if pulled low, will clear the registers that drive the DAC. The CLOCK line must be high to accomplish this. The DAC's output then goes low when the CLOCK line goes low—register contents are transferred to the DAC when the CLOCK line falls.

ABSOLUTE MAXIMUM RATINGS (Note 1) Operating beyond these limits may damage the device

Supply Voltage, V_{CC}	+6 V
Supply Current (I_{CC})	6 mA
8 Bit DAC Output Current (Io)	30 mA
Drive Current Into Any Pin	±20 mA
Io Output Voltage (Vo)	–10 V to +2.5 V
Io' Output Voltage (Vo')	–0.3 V to +2.5 V
Logic Input Voltage	GND–0.3 V to V_{CC}+0.3 V

OPERATING CONDITIONS

Ambient Temp. = 25°C, V_{CC} = +5.0 V ±5%, GND = 0.0 V. Io nominally adjusted to give a full scale value of 0.661 V across a 75 Ω load.

Operating Current (Typical)			15 mA
Maximum Output Current (Io + Io') at Vo = +1.2 V			33 mA
Maximum Undistorted Output Voltage, Vo			1.5 V
Resolution			8 Bits
Integral Linearity Error (Max.): SC11401, 1, 3, 4			1 LSB
Differential Nonlinearity Error (Max.): SC11401, 2, 3, 4			1 LSB
Full Scale Adjust Reference Voltage: SC11401, 2, 3, 4	1.26 V Min.	1.4 V Typ.	1.54 V Max.
Offset Current with Current Sources Off — Io + Io' = 10 µA Max.			
Io' Match to Io (Io Nominally 255 LSB at Full Scale):			
Sync			110 LSB ±6 LSB
Blank			21 LSB ±2 LSB
Bright			28 LSB ±3 LSB
Logic Levels:			
Logic 0 Input Voltage			0.8 V Max.
Logic 1 Input Voltage			2.4 V Max.
Input Current			50 µA Max.

Dynamic Characteristics (Clock Amplitude 0.8 V to 3.0 V)

	SC11401, 2	SC11403, 4
Update Rate (Min.)	40 MHz	75 MHz
Data Set-Up Time, Tsu	10 ns Min.	6 ns Min.
Data Hold Time, Th	10 ns Min.	6 ns Min.
Clock to Vo Delay (Typ.), Td	15 ns	15 ns
Output Glitch Voltage	60 mV Max.	60 mV Max.
Output Glitch Energy (Typ.)	100 pV-s	100 pV-s

Notes:
1. DATA is an 8 bit binary value shown here in base 10. "X" means that the code has no effect on the output.
2. LSB = Least Significant Bit of DAC = Full Scale/255, where Full Scale is the DAC output (Io) with a code of 1s.
3. IRE = unit of measurement per RS-170 specification. Full scale is defined to be 140 IRE (=1 V) of which 40 IRE are assigned to Sync, 7.5 IRE to Blank, and 92.5 IRE to the video information (the output of the 8 bit DAC). An additional 10 IRE is supplied by the Bright control line (BRIGHT*).
4. The output represents the sum of the two currents Io and Io' into a 75 Ω load. Io is the current from the 8 bit DAC, and Io' is the current from Sync, Blank, and Bright controls.
5. If either $\overline{\text{BLANK}}$ or $\overline{\text{SYNC}}$ are low, the DAC is set to zero (Io = 0). $\overline{\text{CLEAR}}$ = 0 will also set the DAC to zero. $\overline{\text{SET}}$ = 1 sets the DAC to 255 (full scale). $\overline{\text{SET}}$ overrides $\overline{\text{CLEAR}}$, both override DATA.

3

ELECTRICAL SPECIFICATIONS

DATA (code)	$\overline{\text{BLANK}}$	$\overline{\text{SYNC}}$	$\overline{\text{BRIGHT}}$	Output, Expressed in: LSB	IRE	VOLTS
X	0	0	1	0	0.0	0.000
X	1	0	1	21	7.5	0.054
X	0	0	0	28	10.0	0.073
X	0	1	1	110	40.0	0.285
0	1	1	1	131	47.5	0.339
1	1	1	1	132	47.9	0.342
2	1	1	1	133	255 LSB = 48.2 IRE	92.5 IRE = 0.345
:	:	:	:	:	:	:
:	:	:	:	:	:	:
255	1	1	1	386	140.0	1.000
255	1	1	0	414	150.0	1.073

Table 1. Output Signal vs. Data and Control Lines

Figure 2 shows a typical video application. Notice that Io and Io' are tied together. If the composite signal is not dersired, Io' can be connected to ground. The Sync, Blank, and Bright current sources are adjusted by three individual potentiometers connected between +5 V and ground. Normally, these components aren't used since the composite video signals are pre-set to their nominal values. Full scale adjustment is achieved using a fixed resistor in series with a potentiometer to give a combined sum of about 5780 Ω.

Figure 3 shows a typical composite video signal.

Figure 4 is a timing diagram. Data is clocked into the registers while the CLOCK line is high and transferred to the DAC when the CLOCK line goes low.

Figure 5 shows a non-video application of the SC11401. In this situation, Io' is not used and is left floating. $\overline{\text{BRIGHT}}$ is tied low and $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ are tied high. This shuts off the current sources of Io' and thus reduces power dissipation.

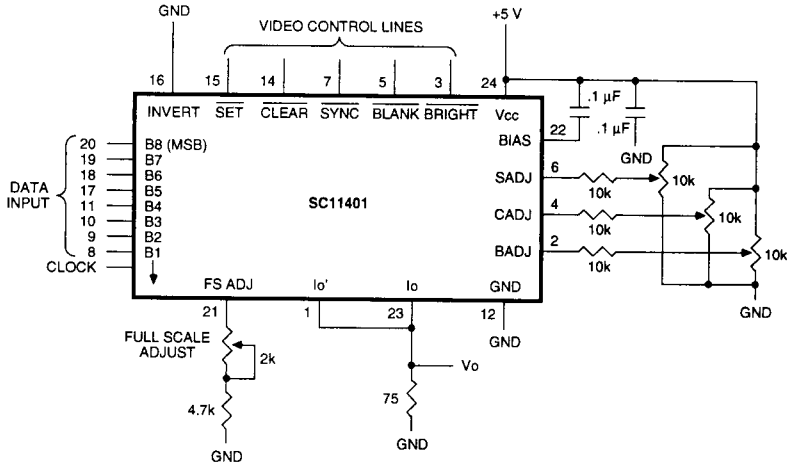


Figure 2. Typical Video Application
The BADJ, CADJ, and SADJ Adjustments are Optional.

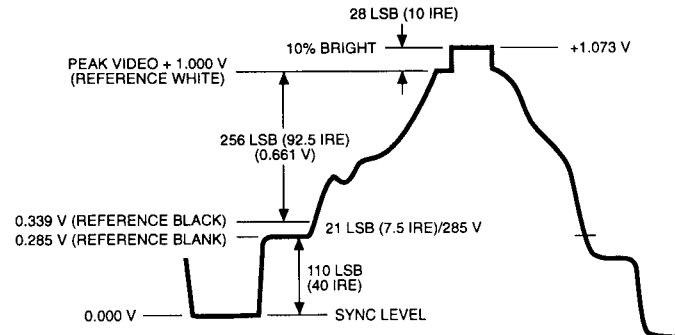


Figure 3. Composite Video Output Signal

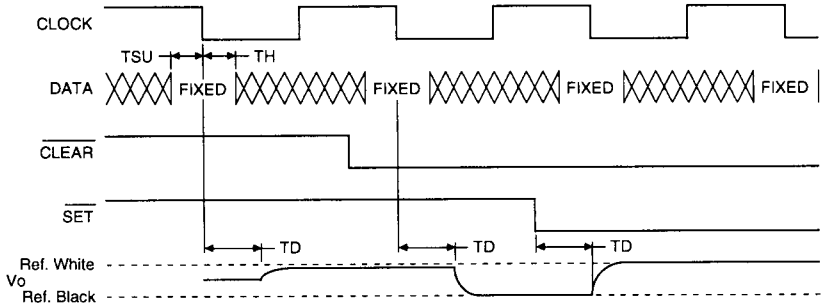


Figure 4. Timing Diagram

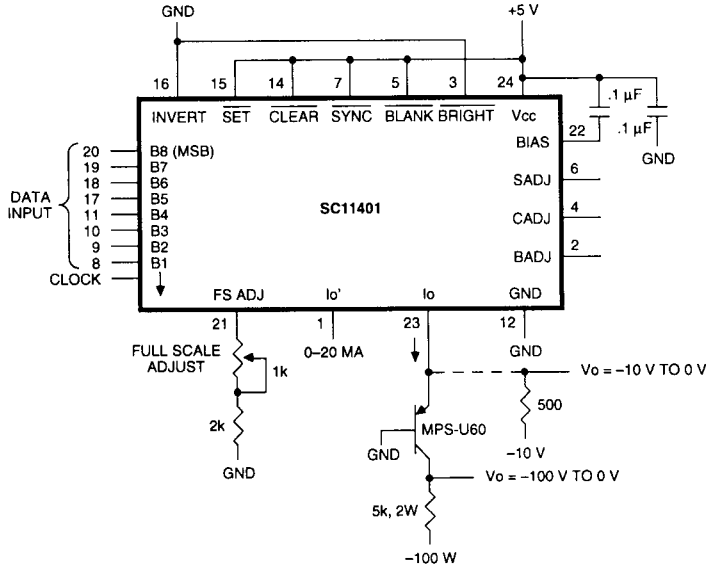


Figure 5. Non-Video Application: High speed DAC with 10 V or 100 V output swing. $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ are pulled high while $\overline{\text{BRIGHT}}$ is low and Io' is left open. This minimizes power consumption by effectively turning off the Io' current sources. The SC11401 can directly drive a 500 Ω load connected to a –10 V supply. For higher voltage swings, a high voltage PNP transistor, such as the MPS-U60 can be used, along with a 5K, 2 Ω resistor.