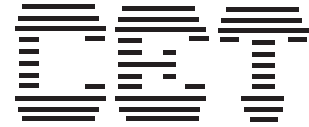


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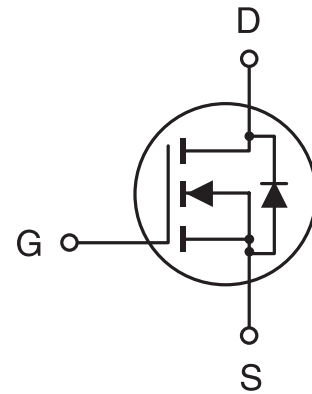
March 1998

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N-Channel Logic Level Enhancement Mode Field Effect

FEATURES

- 60V , 75A , $R_{DS(ON)}=14m\Omega$ @ $V_{GS}=5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- TO-220 & TO-263 package.



ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous -Pulsed	I_D	75	A
	I_{DM}	225	A
Drain-Source Diode Forward Current	I_S	75	A
Maximum Power Dissipation @ $T_c=25^\circ\text{C}$ Derate above 25°C	P_D	150	W
		1	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{STG}	-65 to 175	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

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ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V			25	μA
Gate-Body Leakage	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
ON CHARACTERISTICS^a						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1	1.3	2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =5V, I _D =37.5A		10	14	mΩ
On-State Drain Current	I _{D(ON)}	V _{GS} =5V, V _{DS} =10V	60			A
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =37.5A		60		S
DYNAMIC CHARACTERISTICS^b						
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V f=1.0MHz		2730	3600	pF
Output Capacitance	C _{OSS}			723	1000	pF
Reverse Transfer Capacitance	C _{RSS}			128	170	pF
SWITCHING CHARACTERISTICS^b						
Turn-On Delay Time	t _{D(ON)}	V _{DD} =30V, I _D =75A, V _{GS} =5V, R _{GEN} =10Ω		20	40	ns
Rise Time	t _r			440	600	ns
Turn-Off Delay Time	t _{D(OFF)}			80	150	ns
Fall Time	t _f			250	400	ns
Total Gate Charge	Q _g	V _{DS} =48V, I _D =75A, V _{GS} =5V		104	115	nC
Gate-Source Charge	Q _{gs}			14		nC
Gate-Drain Charge	Q _{gd}			18		nC

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ELECTRICAL CHARACTERISTICS (T_c=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS^a						
Diode Forward Voltage	V _{SD}	V _{GS} = 0V, I _S = 37.5A		0.86	1.3	V

Notes

- a. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

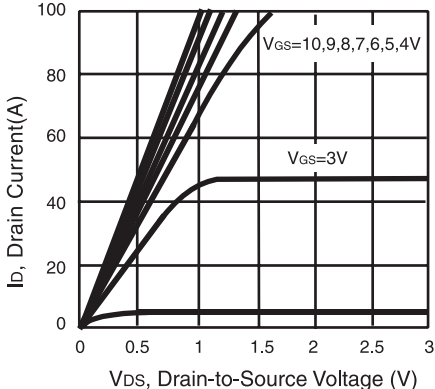


Figure 1. Output Characteristics

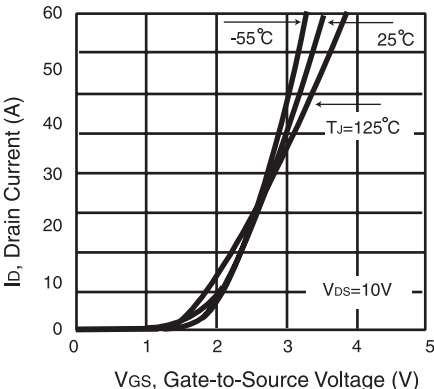


Figure 2. Transfer Characteristics

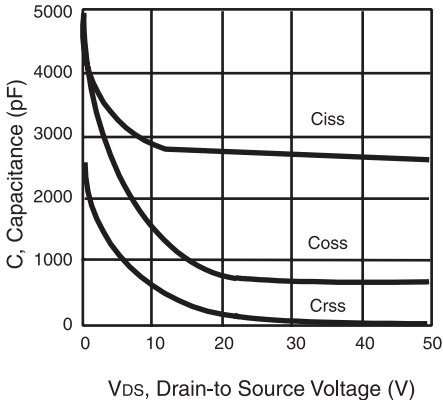


Figure 3. Capacitance

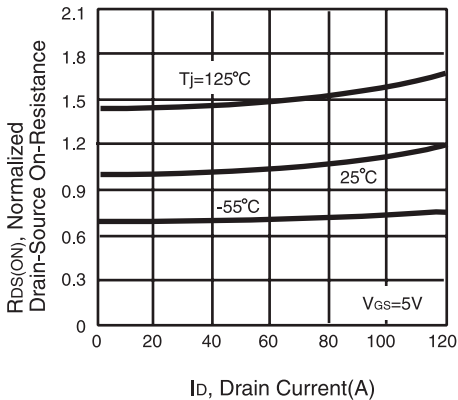


Figure 4. On-Resistance Variation with Drain Current and Temperature

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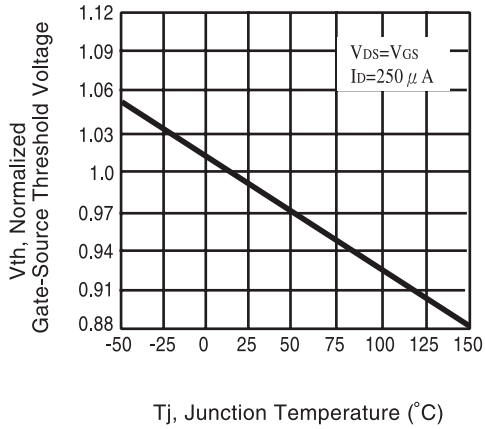


Figure 5. Gate Threshold Variation with Temperature

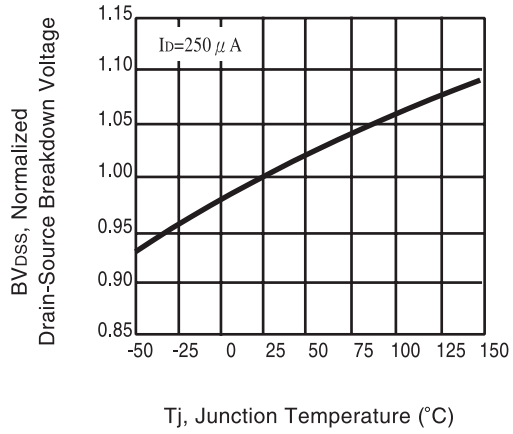


Figure 6. Breakdown Voltage Variation with Temperature

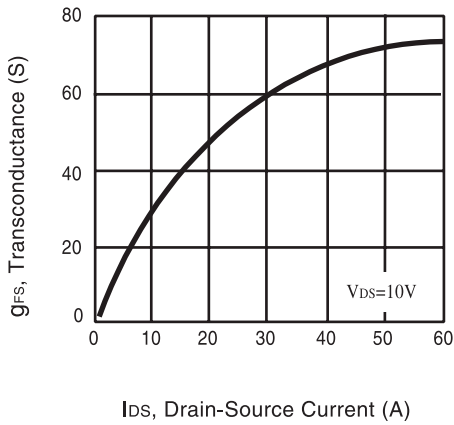


Figure 7. Transconductance Variation with Drain Current

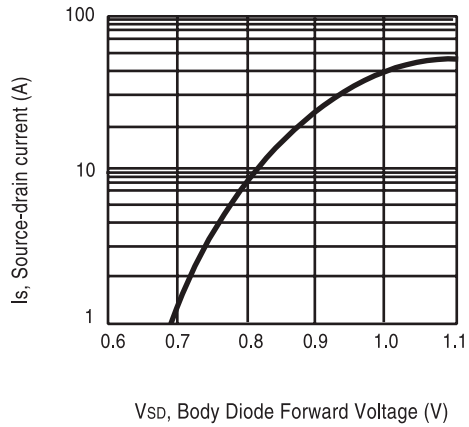


Figure 8. Body Diode Forward Voltage Variation with Source Current

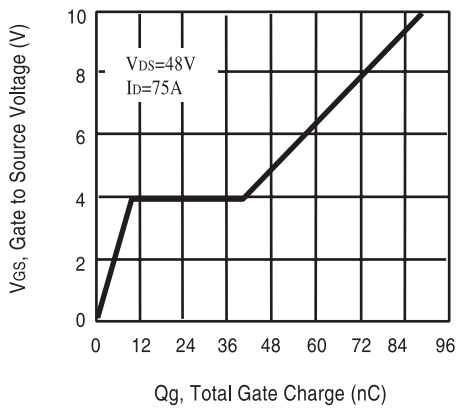


Figure 9. Gate Charge

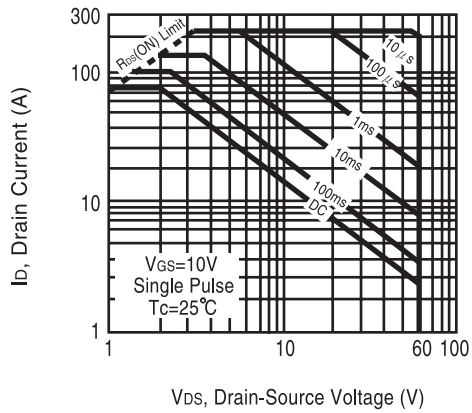


Figure 10. Maximum Safe Operating Area

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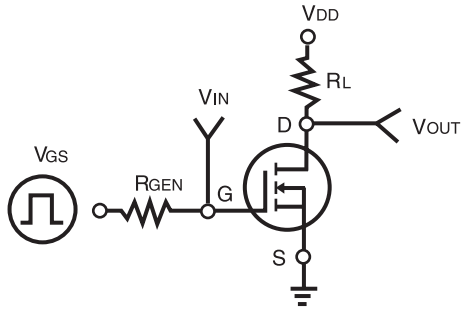


Figure 11. Switching Test Circuit

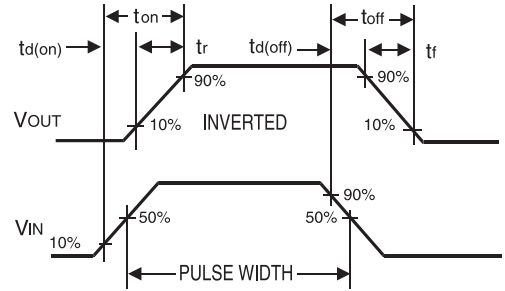


Figure 12. Switching Waveforms

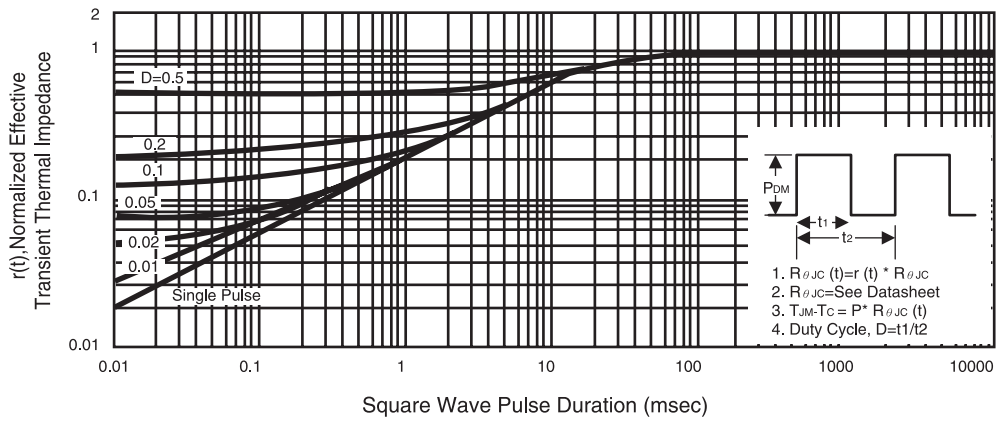


Figure 13. Normalized Thermal Transient Impedance Curve