SONY

PDIC for DVD±R/RW and RAM

Preliminary

CXA2726GA

Description

The CXA2726GA is a PDIC (photodetector IC) developed as a photodetector for the optical pickup of DVD±R/RW and RAM drives.
The photodiode and circuits operate at high speed to allow high-speed read and write. This IC also has a sleep function and small COB (Chip On Board) package.
(Applications: Optical pickups for DVD±R/RW and RAM)

Features

- ◆ Wide band (120MHz)
- ◆ RF differential output (Read Mode: A to D signal addition output)
- ◆ WPP output (WPP1 = A + B, WPP2 = C + D signal addition output)
- ◆ Mode switching function (6-Mode switching + Power save mode: SW1, SW2)
- ◆ 12-division photodiode supporting DPP
- ◆ Small COB package of Land Grid Array type
- ◆ Sleep function (Power save mode)

Package

18-pin LFLGA (Plastic)

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings

(Ta = 25℃)

- Supply voltage — V_{CC} — 5.5 — V
- Operating temperature — Topr — –10 to +80 — ℃
- Storage temperature — Tstg — –40 to +100 — ℃
- Allowable power dissipation — P_D — 550 — mW

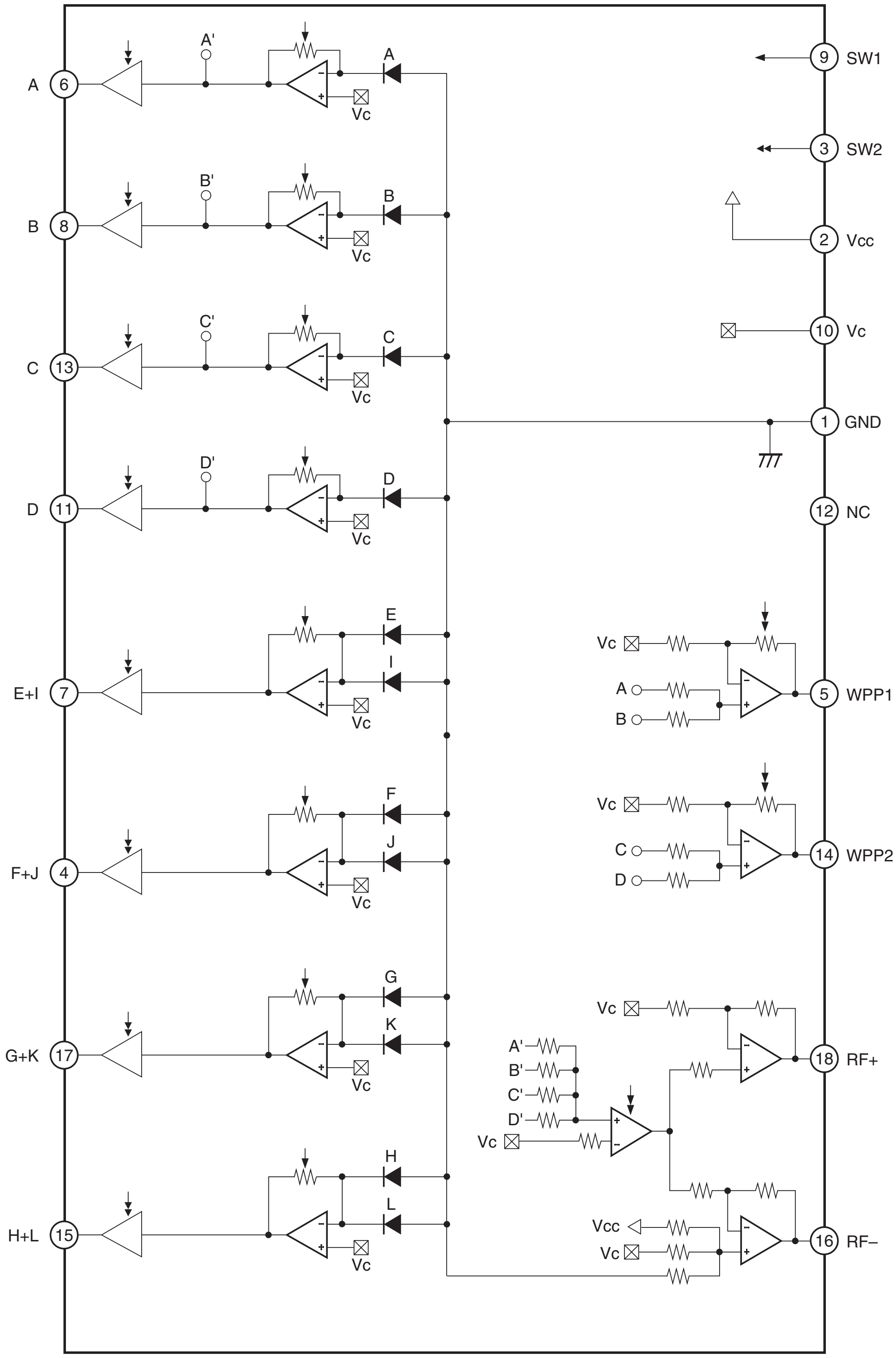
Operating Conditions

- Supply voltage 1 — V_{CC} — 4.5 to 5.5 — V
- Supply voltage 2 — V_C — 1.3 to 2.5 — V
- SW1, SW2: Low — V_{SW} — 0 to 0.4 — V
- SW1, SW2: Middle — V_{SW} — 1.2 to 2.0 — V
- SW1, SW2: High — V_{SW} — 2.9 to V_{CC} — V or OPEN

Output Sensitivity Table

Mode	Name	SW1	SW2	Main	Sub	RF	WPP	Unit
1	Read	Low	Middle	10.00	40.20	8.95	1.67	mV/µW
2		Low	High/Hi-Z	22.40	90.00	20.10	3.73	
3	Write	Middle	Middle	1.30	5.23	—	0.87	
4		Middle	High/Hi-Z	2.91	11.71	—	1.95	
5		High/Hi-Z	Middle	1.00	4.02	—	0.67	
6		High/Hi-Z	High/Hi-Z	2.24	9.01	—	1.50	
SLEEP	Sleep	Don't care	Low	—	—	—	—	

Block Diagram



Arithmetic Formulas

- RF+ = 0.895 × (Ao + Bo + Co + Do)
- RF– = –0.895 × (Ao + Bo + Co + Do)
- WPP1 = (Ao + Bo) × α
- WPP2 = (Co + Do) × α

  * In each mode, α is as follows.

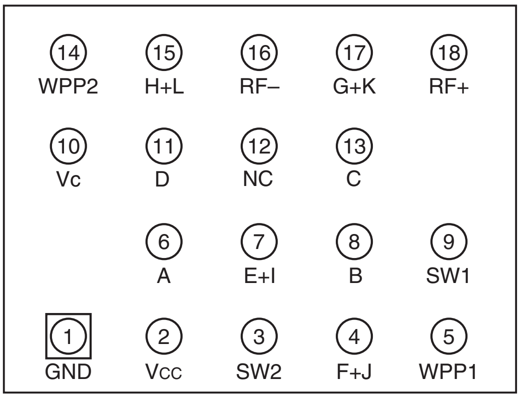
    Mode1 and 2 : 0.167

    Mode3 to 6 : 0.669

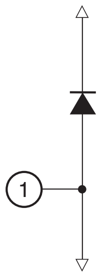
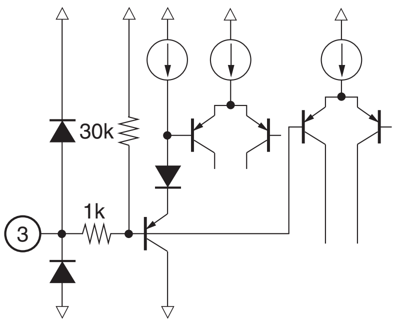
* RF+ and RF– operate only in Mode-1 and Mode-2.

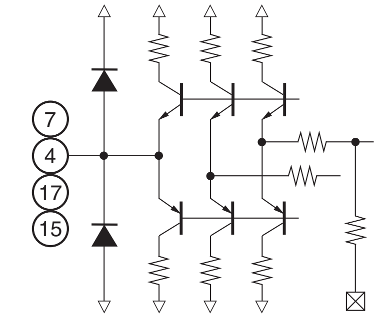
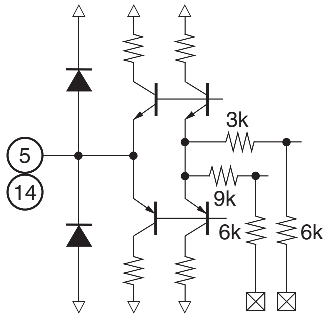
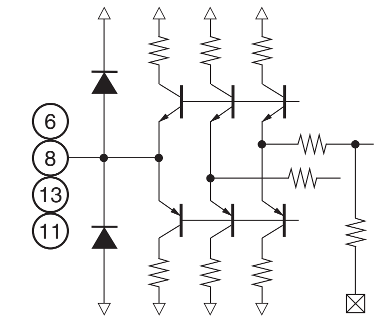
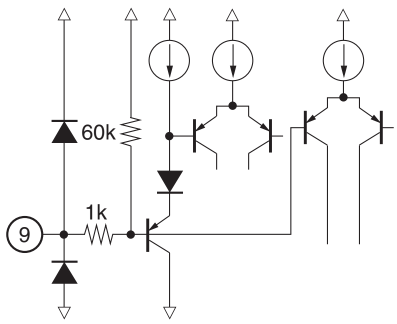
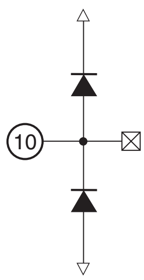
Pin Configuration

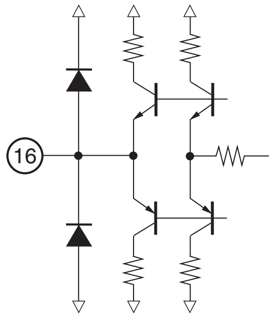
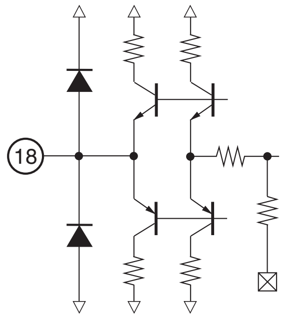
(Top View)



Pin Description

Pin No.	Symbol	I/O	Equivalent circuit	Description
1	GND	I		For a dual power supply: Negative power supply For a single power supply: GND
2	Vcc	I		Positive power supply.
3	SW2	I		Mode switching input. 0 to 0.4V: Low 1.2 to 2.0V: Middle 2.9V to Vcc: High

Pin No.	Symbol	I/O	Equivalent circuit	Description
7 4 17 15	E+I F+J G+K H+L	O		Output of voltage signals converted from optical signals.
5 14	WPP1 WPP2	O		Non-inverted output of added A to D signals. WPP1 = A + B WPP2 = C + D
6 8 13 11	A B C D	O		Output of voltage signals converted from optical signals.
9	SW1	I		Mode switching input. 0 to 0.4V: Low 1.2 to 2.0V: Middle 2.9V to Vcc: High
10	Vc	I		For a dual power supply: GND For a single power supply: Center voltage input

Pin No.	Symbol	I/O	Equivalent circuit	Description
16	RF–	O		Inverted output of added A to D signals.
18	RF+	O		Non-inverted output of added A to D signals.

Electrical and Optical Characteristics 1 (Mode-1: Read Mode/Low Gain)

(V_{CC} = 5.0V, V_C = 1.4V, V_{SW1} = 0V, V_{SW2} = 1.65V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	In the dark	—	44.0	57.5	mA
Output offset voltage (A to D)	Voff	In the dark, V_C reference	–30	0	30	mV
Output offset voltage (E+I to H+L)	Voff	In the dark, V_C reference	–35	0	35	mV
Output offset voltage (WPP1, WPP2)	Voff	In the dark, V_C reference	–30	0	30	mV
Output offset voltage (RF+)	Voff	In the dark, V_C reference	–110	0	110	mV
Output offset voltage (RF–)	Voff	In the dark, V_{CC} – V_C reference	–110	0	110	mV
Output offset matrix	ΔVoff	(A + B) – (C + D), In the dark	–30	0	30	mV
		(A + D) – (B + C), In the dark	–30	0	30	mV
		(A + C) – (B + D), In the dark	–30	0	30	mV
		(G + H + K + L) – (E + F + I + J), In the dark	–30	0	30	mV
		A + B + C + D, In the dark	–50	0	50	mV
		E + F + G + H + I + J + K + L, In the dark	–50	0	50	mV
		(RF+) – (RF–), In the dark	–160	0	160	mV
Offset temperature drift (A to D) *	ΔVoff/T	In the dark	–100	0	100	µV/°C
Offset temperature drift (E+I to H+L) *	ΔVoff/T	In the dark	–150	0	150	µV/°C
Offset temperature drift (WPP1, WPP2) *	ΔVoff/T	In the dark	–100	0	100	µV/°C
Offset temperature drift (RF+, RF–) *	ΔVoff/T	In the dark	–1	0	1	mV/°C
Output voltage (A to D) *	Vo	λ = 650nm, 780nm, Po = 10µW	7.5	10.0	12.5	mV/µW
Output voltage (E+I to H+L) *	Vo	λ = 650nm, 780nm, Po = 10µW	30.15	40.20	50.25	mV/µW
Output voltage (WPP1, WPP2) *	Vo	λ = 650nm, 780nm, Po = 10µW	1.25	1.67	2.09	mV/µW
Output voltage (RF+) *	Vo	λ = 650nm, 780nm, Po = 10µW	6.71	8.95	11.19	mV/µW
Output voltage (RF–) *	Vo	λ = 650nm, 780nm, Po = 10µW	–11.19	–8.95	–6.71	mV/µW
Output voltage ratio (E+I to H+L)/(A to D) *	V_{OR}	λ = 650nm, 780nm, Po = 10µW	3.91	4.12	4.33	—
Output voltage ratio ((RF+) + (RF–))/(A to D) *	V_{OR}	λ = 650nm, 780nm, Po = 10µW	1.77	1.86	1.95	—
Maximum output potential (A to D, E+I to H+L)	Vomax	λ = 650nm, 780nm, Po = 1mW	3.8	4.0	—	V

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Maximum output potential (WPP1, WPP2)	Vomax	λ = 650nm, 780nm, Po = 1mW	2.0	2.2	—	V
Maximum output potential (RF+)	Vomax	λ = 650nm, 780nm, Po = 1mW	3.8	4.0	—	V
Minimum output potential (RF–)	Vomin	λ = 650nm, 780nm, Po = 1mW	—	1.0	1.2	V
Frequency response (A to D) *	fc	λ = 650nm, 780nm Po = 10µW$_{DC}$ + 4µWp-p 100kHz reference, –3dB	90	120	—	MHz
Frequency response (E+I to H+L) *	fc	λ = 650nm, 780nm Po = 10µW$_{DC}$ + 4µWp-p 100kHz reference, –3dB	20	30	—	MHz
Frequency response (WPP1, WPP2) *	fc	λ = 650nm, 780nm Po = 10µW$_{DC}$ + 4µWp-p 100kHz reference, –3dB	90	120	—	MHz
Frequency response ((RF+) – (RF–)) *	fc	λ = 650nm, 780nm Po = 10µW$_{DC}$ + 4µWp-p 100kHz reference, –3dB	90	120	—	MHz
Group delay difference 1 (A to D) *	∆Gd1	100kHz to 70MHz	—	1.0	—	ns
Group delay difference 1 (WPP1, WPP2) *	∆Gd1	100kHz to 70MHz	—	1.1	—	ns
Group delay difference 1 ((RF+) – (RF–)) *	∆Gd1	100kHz to 70MHz	—	0.9	—	ns
Group delay difference 2 (A to D) *	∆Gd2	100kHz to 90MHz	—	1.0	—	ns
Group delay difference 2 (WPP1, WPP2) *	∆Gd2	100kHz to 90MHz	—	1.8	—	ns
Group delay difference 2 ((RF+) – (RF–)) *	∆Gd2	100kHz to 90MHz	—	1.0	—	ns
Slew rate (A to D) *	SR	Calculated at 10% to 90%	—	250	—	V/µs
Slew rate (E+I to H+L) *	SR	Calculated at 10% to 90%	—	170	—	V/µs
Slew rate (RF+, RF–) *	SR	Calculated at 10% to 90%	—	225	—	V/µs
Output noise level (A to D) *	Vn	RBW = 30kHz, f = 1 to 90MHz, In the dark	—	–87	–82	dBm
Output noise level (RF+, RF–)	Vn	RBW = 30kHz, f = 1 to 90MHz, In the dark	—	–81	–75	dBm

Note) 1. Output offset voltage: V_C is the reference.
2. The output voltage represents the potential variation of the output pin between the optical emission and the dark state.
3. Items with an asterisk (*) are design confirmation items.
4. Measurement by optical input: Measurement is made by emitting light to the center of each photodiode.
5. The load conditions (for V_C) are as follows.
A to D: 2kΩ//20pF, E+I to H+L, WPP1, WPP2: 6kΩ//20pF, RF+, RF–: (1µF + (1.3kΩ//10pF))//10pF

Electrical and Optical Characteristics 2 (Mode-2: Read Mode/High Gain)

(Vcc = 5.0V, Vc = 1.4V, Vsw1 = 0V, Vsw2 = 3.3V, Ta = 25℃)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	Icc	In the dark	—	44.0	57.5	mA
Output offset voltage (A to D)	Voff	In the dark, Vc reference	–30	0	30	mV
Output offset voltage (E+I to H+L)	Voff	In the dark, Vc reference	–35	0	35	mV
Output offset voltage (WPP1, WPP2)	Voff	In the dark, Vc reference	–30	0	30	mV
Output offset voltage (RF+)	Voff	In the dark, Vc reference	–110	0	110	mV
Output offset voltage (RF–)	Voff	In the dark, Vcc – Vc reference	–110	0	110	mV
Output offset matrix	ΔVoff	(A + B) – (C + D), In the dark	–30	0	30	mV
		(A + D) – (B + C), In the dark	–30	0	30	mV
		(A + C) – (B + D), In the dark	–30	0	30	mV
		(G + H + K + L) – (E + F + I + J), In the dark	–30	0	30	mV
		A + B + C + D, In the dark	–50	0	50	mV
		E + F + G + H + I + J + K + L, In the dark	–50	0	50	mV
		(RF+) – (RF–), In the dark	–160	0	160	mV
Offset temperature drift (A to D) *	ΔVoff/T	In the dark	–100	0	100	μV/℃
Offset temperature drift (E+I to H+L) *	ΔVoff/T	In the dark	–150	0	150	μV/℃
Offset temperature drift (WPP1, WPP2) *	ΔVoff/T	In the dark	–100	0	100	μV/℃
Offset temperature drift (RF+, RF–) *	ΔVoff/T	In the dark	–1	0	1	mV/℃
Output voltage (A to D) *	Vo	λ = 650nm, 780nm, Po = 10μW	16.8	22.4	28.0	mV/μW
Output voltage (E+I to H+L) *	Vo	λ = 650nm, 780nm, Po = 10μW	67.5	90.0	112.5	mV/μW
Output voltage (WPP1, WPP2) *	Vo	λ = 650nm, 780nm, Po = 10μW	2.79	3.73	4.67	mV/μW
Output voltage (RF+) *	Vo	λ = 650nm, 780nm, Po = 10μW	15.0	20.1	25.1	mV/μW
Output voltage (RF–) *	Vo	λ = 650nm, 780nm, Po = 10μW	–25.1	–20.1	–15.0	mV/μW
Output voltage ratio (E+I to H+L)/(A to D) *	VOR	λ = 650nm, 780nm, Po = 10μW	3.88	4.08	4.28	—
Output voltage ratio ((RF+) + (RF–))/(A to D) *	VOR	λ = 650nm, 780nm, Po = 10μW	1.79	1.88	1.97	—
Maximum output potential (A to D, E+I to H+L)	Vomax	λ = 650nm, 780nm, Po = 1mW	3.8	4.0	—	V

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Maximum output potential (WPP1, WPP2)	Vomax	λ = 650nm, 780nm, Po = 1mW	2.0	2.2	—	V
Maximum output potential (RF+)	Vomax	λ = 650nm, 780nm, Po = 1mW	3.8	4.0	—	V
Minimum output potential (RF–)	Vomin	λ = 650nm, 780nm, Po = 1mW	—	1.0	1.2	V
Frequency response (A to D) *	fc	λ = 650nm, 780nm Po = 10μWDC + 4μWp-p 100kHz reference, –3dB	90	120	—	MHz
Frequency response (E+I to H+L) *	fc	λ = 650nm, 780nm Po = 10μWDC + 4μWp-p 100kHz reference, –3dB	20	30	—	MHz
Frequency response (WPP1, WPP2) *	fc	λ = 650nm, 780nm Po = 10μWDC + 4μWp-p 100kHz reference, –3dB	90	120	—	MHz
Frequency response ((RF+) – (RF–)) *	fc	λ = 650nm, 780nm Po = 10μWDC + 4μWp-p 100kHz reference, –3dB	90	120	—	MHz
Group delay difference 1 (A to D) *	ΔGd1	100kHz to 70MHz	—	1.2	—	ns
Group delay difference 1 (WPP1, WPP2) *	ΔGd1	100kHz to 70MHz	—	1.2	—	ns
Group delay difference 1 ((RF+) – (RF–)) *	ΔGd1	100kHz to 70MHz	—	1.0	—	ns
Group delay difference 2 (A to D) *	ΔGd2	100kHz to 90MHz	—	1.5	—	ns
Group delay difference 2 (WPP1, WPP2) *	ΔGd2	100kHz to 90MHz	—	1.8	—	ns
Group delay difference 2 ((RF+) – (RF–)) *	ΔGd2	100kHz to 90MHz	—	1.0	—	ns
Slew rate (A to D) *	SR	Calculated at 10% to 90%	—	250	—	V/μs
Slew rate (E+I to H+L) *	SR	Calculated at 10% to 90%	—	180	—	V/μs
Slew rate (RF+, RF–) *	SR	Calculated at 10% to 90%	—	225	—	V/μs
Output noise level (A to D) *	Vn	RBW = 30kHz, f = 1 to 90MHz, In the dark	—	–80	–75	dBm
Output noise level (RF+, RF–)	Vn	RBW = 30kHz, f = 1 to 90MHz, In the dark	—	–74	–69	dBm

Note) 1. Output offset voltage: VC is the reference.
2. The output voltage represents the potential variation of the output pin between the optical emission and the dark state.
3. Items with an asterisk (*) are design confirmation items.
4. Measurement by optical input: Measurement is made by emitting light to the center of each photodiode.
5. The load conditions (for VC) are as follows.
A to D: 2kΩ//20pF, E+I to H+L, WPP1, WPP2: 6kΩ//20pF, RF+, RF–: (1μF + (1.3kΩ//10pF))//10pF

Electrical and Optical Characteristics 3 (Mode-3: Write Mode)

(V_{CC} = 5.0V, V_C = 1.4V, V_{SW1} = 1.65V, V_{SW2} = 1.65V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	In the dark	—	39.0	51.0	mA
Output offset voltage (A to D)	Voff	In the dark, V_C reference	–30	0	30	mV
Output offset voltage (E+I to H+L)	Voff	In the dark, V_C reference	–35	0	35	mV
Output offset voltage (WPP1, WPP2)	Voff	In the dark, V_C reference	–30	0	30	mV
Output offset matrix	ΔVoff	(A + B) – (C + D), In the dark	–30	0	30	mV
		(A + D) – (B + C), In the dark	–30	0	30	mV
		(A + C) – (B + D), In the dark	–30	0	30	mV
		(G + H + K + L) – (E + F + I + J), In the dark	–30	0	30	mV
		A + B + C + D, In the dark	–50	0	50	mV
		E + F + G + H + I + J + K + L, In the dark	–50	0	50	mV
Offset temperature drift (A to D) *	ΔVoff/T	In the dark	–100	0	100	µV/°C
Offset temperature drift (E+I to H+L) *	ΔVoff/T	In the dark	–150	0	150	µV/°C
Offset temperature drift (WPP1, WPP2) *	ΔVoff/T	In the dark	–100	0	100	µV/°C
Output voltage (A to D)	Vo	λ = 650nm, 780nm, Po = 350µW	0.98	1.30	1.63	mV/µW
Output voltage (E+I to H+L)	Vo	λ = 650nm, 780nm, Po = 350µW	3.92	5.23	6.54	mV/µW
Output voltage (WPP1, WPP2)	Vo	λ = 650nm, 780nm, Po = 350µW	0.65	0.87	1.09	mV/µW
Output voltage ratio (E+I to H+L)/(A to D)	V_{OR}	λ = 650nm, 780nm, Po = 350µW	3.89	4.09	4.29	—
Maximum output potential (A to D, E+I to H+L, WPP1, WPP2)	Vomax	λ = 650nm, 780nm, Po = 1mW	3.3	3.5	—	V
Frequency response (A to D) *	fc	λ = 650nm, 780nm Po = 10µW_{DC} + 4µWp-p 100kHz reference, –3dB	90	120	—	MHz
Frequency response (E+I to H+L) *	fc	λ = 650nm, 780nm Po = 10µW_{DC} + 4µWp-p 100kHz reference, –3dB	25	60	—	MHz
Frequency response (WPP1, WPP2) *	fc	λ = 650nm, 780nm Po = 10µW_{DC} + 4µWp-p 100kHz reference, –3dB	100	130	—	MHz

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Group delay difference 1 (A to D, WPP1, WPP2) *	ΔGd1	100kHz to 70MHz	—	1.0	—	ns
Group delay difference 2 (A to D, WPP1, WPP2) *	ΔGd2	100kHz to 90MHz	—	1.9	—	ns
Settling time (A to D) *	Tset	Output 299mV → 15 ± 3mV	—	18.0	—	ns
Settling time (E+I to H+L) *	Tset	Output 323mV → 6.5 ± 1.3mV	—	27.0	—	ns
Settling time (WPP1, WPP2) *	Tset	Output 20mV → 399 ± 4mV	—	15.0	—	ns
Settling time (WPP1, WPP2) *	Tset	Output 399mV → 20 ± 4mV	—	15.0	—	ns
Slew rate (A to D) *	SR	Calculated at 10% to 90%	—	210	—	V/μs
Slew rate (E+I to H+L) *	SR	Calculated at 10% to 90%	—	200	—	V/μs
Slew rate (WPP1, WPP2) *	SR	Calculated at 10% to 90%	—	260	—	V/μs
Output noise level (A to D) *	Vn	RBW = 30kHz, f = 1 to 90MHz, In the dark	—	–93	–88	dBm
Output noise level (WPP1, WPP2) *	Vn	RBW = 30kHz, f = 1 to 90MHz, In the dark	—	–89	–84	dBm

Note) 1. Output offset voltage: V_C is the reference.
2. The output voltage represents the potential variation of the output pin between the optical emission and the dark state.
3. Items with an asterisk (*) are design confirmation items.
4. Measurement by optical input: Measurement is made by emitting light to the center of each photodiode.
5. The load conditions (for V_C) are as follows.
A to D: 2kΩ//20pF, E+I to H+L, WPP1, WPP2: 6kΩ//20pF

Electrical and Optical Characteristics 4 (Mode-4: Write Mode)

(V_{CC} = 5.0V, V_C = 1.4V, V_{SW1} = 1.65V, V_{SW2} = 3.3V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	In the dark	—	39.0	51.0	mA
Output offset voltage (A to D)	Voff	In the dark, V_C reference	–30	0	30	mV
Output offset voltage (E+I to H+L)	Voff	In the dark, V_C reference	–35	0	35	mV
Output offset voltage (WPP1, WPP2)	Voff	In the dark, V_C reference	–30	0	30	mV
Output offset matrix	ΔVoff	(A + B) – (C + D), In the dark	–30	0	30	mV
		(A + D) – (B + C), In the dark	–30	0	30	mV
		(A + C) – (B + D), In the dark	–30	0	30	mV
		(G + H + K + L) – (E + F + I + J), In the dark	–30	0	30	mV
		A + B + C + D, In the dark	–50	0	50	mV
		E + F + G + H + I + J + K + L, In the dark	–50	0	50	mV
Offset temperature drift (A to D) *	ΔVoff/T	In the dark	–100	0	100	µV/°C
Offset temperature drift (E+I to H+L) *	ΔVoff/T	In the dark	–150	0	150	µV/°C
Offset temperature drift (WPP1, WPP2) *	ΔVoff/T	In the dark	–100	0	100	µV/°C
Output voltage (A to D)	Vo	λ = 650nm, 780nm, Po = 175µW	2.73	2.91	3.41	mV/µW
Output voltage (E+I to H+L)	Vo	λ = 650nm, 780nm, Po = 175µW	8.78	11.71	14.63	mV/µW
Output voltage (WPP1, WPP2)	Vo	λ = 650nm, 780nm, Po = 175µW	1.46	1.95	2.44	mV/µW
Output voltage ratio (E+I to H+L)/(A to D)	V_{OR}	λ = 650nm, 780nm, Po = 175µW	3.78	3.98	4.18	—
Maximum output potential (A to D, E+I to H+L, WPP1, WPP2)	Vomax	λ = 650nm, 780nm, Po = 1mW	3.5	3.7	—	V
Frequency response (A to D) *	fc	λ = 650nm, 780nm Po = 10µW_{DC} + 4µWp-p 100kHz reference, –3dB	90	120	—	MHz
Frequency response (E+I to H+L) *	fc	λ = 650nm, 780nm Po = 10µW_{DC} + 4µWp-p 100kHz reference, –3dB	30	50	—	MHz
Frequency response (WPP1, WPP2) *	fc	λ = 650nm, 780nm Po = 10µW_{DC} + 4µWp-p 100kHz reference, –3dB	100	130	—	MHz

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Group delay difference 1 (A to D, WPP1, WPP2) *	ΔGd1	100kHz to 70MHz	—	1.4	—	ns
Group delay difference 2 (A to D, WPP1, WPP2) *	ΔGd2	100kHz to 90MHz	—	2.4	—	ns
Settling time (A to D) *	Tset	Output 690mV → 34.5 ± 6.9mV	—	18.0	—	ns
Settling time (E+I to H+L) *	Tset	Output 745mV → 14.9 ± 3mV	—	27.0	—	ns
Settling time (WPP1, WPP2) *	Tset	Output 920mV → 46 ± 9.2mV	—	15.0	—	ns
Settling time (WPP1, WPP2) *	Tset	Output 46mV → 920 ± 9.2mV	—	15.0	—	ns
Slew rate (A to D) *	SR	Calculated at 10% to 90%	—	250	—	V/µs
Slew rate (E+I to H+L) *	SR	Calculated at 10% to 90%	—	200	—	V/µs
Slew rate (WPP1, WPP2) *	SR	Calculated at 10% to 90%	—	260	—	V/µs
Output noise level (A to D) *	Vn	RBW = 30kHz, f = 1 to 90MHz, In the dark	—	–87	–82	dBm
Output noise level (WPP1, WPP2) *	Vn	RBW = 30kHz, f = 1 to 90MHz, In the dark	—	–85	–80	dBm

Note)
1. Output offset voltage: V_C is the reference.
2. The output voltage represents the potential variation of the output pin between the optical emission and the dark state.
3. Items with an asterisk (*) are design confirmation items.
4. Measurement by optical input: Measurement is made by emitting light to the center of each photodiode.
5. The load conditions (for V_C) are as follows.
   A to D: 2kΩ//20pF, E+I to H+L, WPP1, WPP2: 6kΩ//20pF

Electrical and Optical Characteristics 5 (Mode-5: Write Mode)

(V_{CC} = 5.0V, V_C = 1.4V, V_{SW1} = 3.3V, V_{SW2} = 1.65V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	In the dark	—	39.0	51.0	mA
Output offset voltage (A to D)	Voff	In the dark, V_C reference	–30	0	30	mV
Output offset voltage (E+I to H+L)	Voff	In the dark, V_C reference	–35	0	35	mV
Output offset voltage (WPP1, WPP2)	Voff	In the dark, V_C reference	–30	0	30	mV
Output offset matrix	ΔVoff	(A + B) – (C + D), In the dark	–30	0	30	mV
		(A + D) – (B + C), In the dark	–30	0	30	mV
		(A + C) – (B + D), In the dark	–30	0	30	mV
		(G + H + K + L) – (E + F + I + J), In the dark	–30	0	30	mV
		A + B + C + D, In the dark	–50	0	50	mV
		E + F + G + H + I + J + K + L, In the dark	–50	0	50	mV
Offset temperature drift (A to D) *	ΔVoff/T	In the dark	–100	0	100	µV/°C
Offset temperature drift (E+I to H+L) *	ΔVoff/T	In the dark	–150	0	150	µV/°C
Offset temperature drift (WPP1, WPP2) *	ΔVoff/T	In the dark	–1	0	1	mV/°C
Output voltage (A to D)	Vo	λ = 650nm, 780nm, Po = 350µW	0.75	1.00	1.25	mV/µW
Output voltage (E+I to H+L)	Vo	λ = 650nm, 780nm, Po = 350µW	3.01	4.02	5.03	mV/µW
Output voltage (WPP1, WPP2)	Vo	λ = 650nm, 780nm, Po = 350µW	0.50	0.67	0.84	mV/µW
Output voltage ratio (E+I to H+L)/(A to D)	V_{OR}	λ = 650nm, 780nm, Po = 350µW	3.95	4.16	4.37	—
Maximum output potential (A to D, E+I to H+L, WPP1, WPP2)	Vomax	λ = 650nm, 780nm, Po = 1mW	3.3	3.5	—	V
Frequency response (A to D) *	fc	λ = 650nm, 780nm Po = 10µW_{DC} + 4µWp-p 100kHz reference, –3dB	90	120	—	MHz
Frequency response (E+I to H+L) *	fc	λ = 650nm, 780nm Po = 10µW_{DC} + 4µWp-p 100kHz reference, –3dB	50	75	—	MHz
Frequency response (WPP1, WPP2) *	fc	λ = 650nm, 780nm Po = 10µW_{DC} + 4µWp-p 100kHz reference, –3dB	95	150	—	MHz

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Group delay difference 1 (A to D, WPP1, WPP2) *	ΔGd1	100kHz to 70MHz	—	1.4	—	ns
Group delay difference 2 (A to D, WPP1, WPP2) *	ΔGd2	100kHz to 90MHz	—	2.4	—	ns
Settling time (A to D) *	Tset	Output 230mV $\rightarrow$ 11.5 $\pm$ 2.3mV	—	15.0	—	ns
Settling time (E+I to H+L) *	Tset	Output 248mV $\rightarrow$ 5 $\pm$ 1mV	—	24.0	—	ns
Settling time (WPP1, WPP2) *	Tset	Output 306.7mV $\rightarrow$ 15.3 $\pm$ 3.1mV	—	15.0	—	ns
Settling time (WPP1, WPP2) *	Tset	Output 15.3mV $\rightarrow$ 306.7 $\pm$ 3.1mV	—	15.0	—	ns
Slew rate (A to D) *	SR	Calculated at 10% to 90%	—	210	—	V/µs
Slew rate (E+I to H+L) *	SR	Calculated at 10% to 90%	—	200	—	V/µs
Slew rate (WPP1, WPP2) *	SR	Calculated at 10% to 90%	—	260	—	V/µs
Output noise level (A to D) *	Vn	RBW = 30kHz, f = 1 to 90MHz, In the dark	—	–93	–88	dBm
Output noise level (WPP1, WPP2) *	Vn	RBW = 30kHz, f = 1 to 90MHz, In the dark	—	–89	–84	dBm

Note)
1. Output offset voltage: V_C is the reference.
2. The output voltage represents the potential variation of the output pin between the optical emission and the dark state.
3. Items with an asterisk (*) are design confirmation items.
4. Measurement by optical input: Measurement is made by emitting light to the center of each photodiode.
5. The load conditions (for V_C) are as follows.
   A to D: 2kΩ//20pF, E+I to H+L, WPP1, WPP2: 6kΩ//20pF

Electrical and Optical Characteristics 6 (Mode-6: Write Mode)

(V_{CC} = 5.0V, V_C = 1.4V, V_{SW1} = 3.3V, V_{SW2} = 3.3V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	ICC	In the dark	—	39.0	51.0	mA
Output offset voltage (A to D)	Voff	In the dark, VC reference	–30	0	30	mV
Output offset voltage (E+I to H+L)	Voff	In the dark, VC reference	–35	0	35	mV
Output offset voltage (WPP1, WPP2)	Voff	In the dark, VC reference	–30	0	30	mV
Output offset matrix	ΔVoff	(A + B) – (C + D), In the dark	–30	0	30	mV
		(A + D) – (B + C), In the dark	–30	0	30	mV
		(A + C) – (B + D), In the dark	–30	0	30	mV
		(G + H + K + L) – (E + F + I + J), In the dark	–30	0	30	mV
		A + B + C + D, In the dark	–50	0	50	mV
		E + F + G + H + I + J + K + L, In the dark	–50	0	50	mV
Offset temperature drift (A to D) *	ΔVoff/T	In the dark	–100	0	100	µV/°C
Offset temperature drift (E+I to H+L) *	ΔVoff/T	In the dark	–150	0	150	µV/°C
Offset temperature drift (WPP1, WPP2) *	ΔVoff/T	In the dark	–100	0	100	µV/°C
Output voltage (A to D)	Vo	λ = 650nm, 780nm, Po = 175µW	1.68	2.24	2.80	mV/µW
Output voltage (E+I to H+L)	Vo	λ = 650nm, 780nm, Po = 175µW	6.75	9.01	11.26	mV/µW
Output voltage (WPP1, WPP2)	Vo	λ = 650nm, 780nm, Po = 175µW	1.12	1.50	1.88	mV/µW
Output voltage ratio (E+I to H+L)/(A to D)	VOR	λ = 650nm, 780nm, Po = 175µW	3.83	4.03	4.23	—
Maximum output potential (A to D, E+I to H+L, WPP1, WPP2)	Vomax	λ = 650nm, 780nm, Po = 1mW	3.5	3.7	—	V
Frequency response (A to D) *	fc	λ = 650nm, 780nm Po = 10µWDC + 4µWp-p 100kHz reference, –3dB	90	120	—	MHz
Frequency response (E+I to H+L) *	fc	λ = 650nm, 780nm Po = 10µWDC + 4µWp-p 100kHz reference, –3dB	35	60	—	MHz
Frequency response (WPP1, WPP2) *	fc	λ = 650nm, 780nm Po = 10µWDC + 4µWp-p 100kHz reference, –3dB	95	150	—	MHz

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Group delay difference 1 (A to D, WPP1, WPP2) *	ΔGd1	100kHz to 70MHz	—	1.2	—	ns
Group delay difference 2 (A to D, WPP1, WPP2) *	ΔGd2	100kHz to 90MHz	—	2.3	—	ns
Settling time (A to D) *	Tset	Output 515mV → 25.8 ± 5.2mV	—	15.0	—	ns
Settling time (E+I to H+L) *	Tset	Output 556.6mV → 11.1 ± 2.2mV	—	24.0	—	ns
Settling time (WPP1, WPP2) *	Tset	Output 687mV → 34.4 ± 6.9mV	—	15.0	—	ns
Settling time (WPP1, WPP2) *	Tset	Output 34.4mV → 687 ± 6.9mV	—	15.0	—	ns
Slew rate (A to D) *	SR	Calculated at 10% to 90%	—	250	—	V/µs
Slew rate (E+I to H+L) *	SR	Calculated at 10% to 90%	—	200	—	V/µs
Slew rate (WPP1, WPP2) *	SR	Calculated at 10% to 90%	—	260	—	V/µs
Output noise level (A to D) *	Vn	RBW = 30kHz, f = 1 to 90MHz, In the dark	—	–87	–82	dBm
Output noise level (WPP1, WPP2) *	Vn	RBW = 30kHz, f = 1 to 90MHz, In the dark	—	–85	–80	dBm

Note) 1. Output offset voltage: V_C is the reference.
2. The output voltage represents the potential variation of the output pin between the optical emission and the dark state.
3. Items with an asterisk (*) are design confirmation items.
4. Measurement by optical input: Measurement is made by emitting light to the center of each photodiode.
5. The load conditions (for V_C) are as follows.
   A to D: 2kΩ//20pF, E+I to H+L, WPP1, WPP2: 6kΩ//20pF

Electrical and Optical Characteristics 7 (Read to Write Mode Switching Characteristics)

(V_{CC} = 5.0V, V_C = 1.4V, Ta = 25°C)

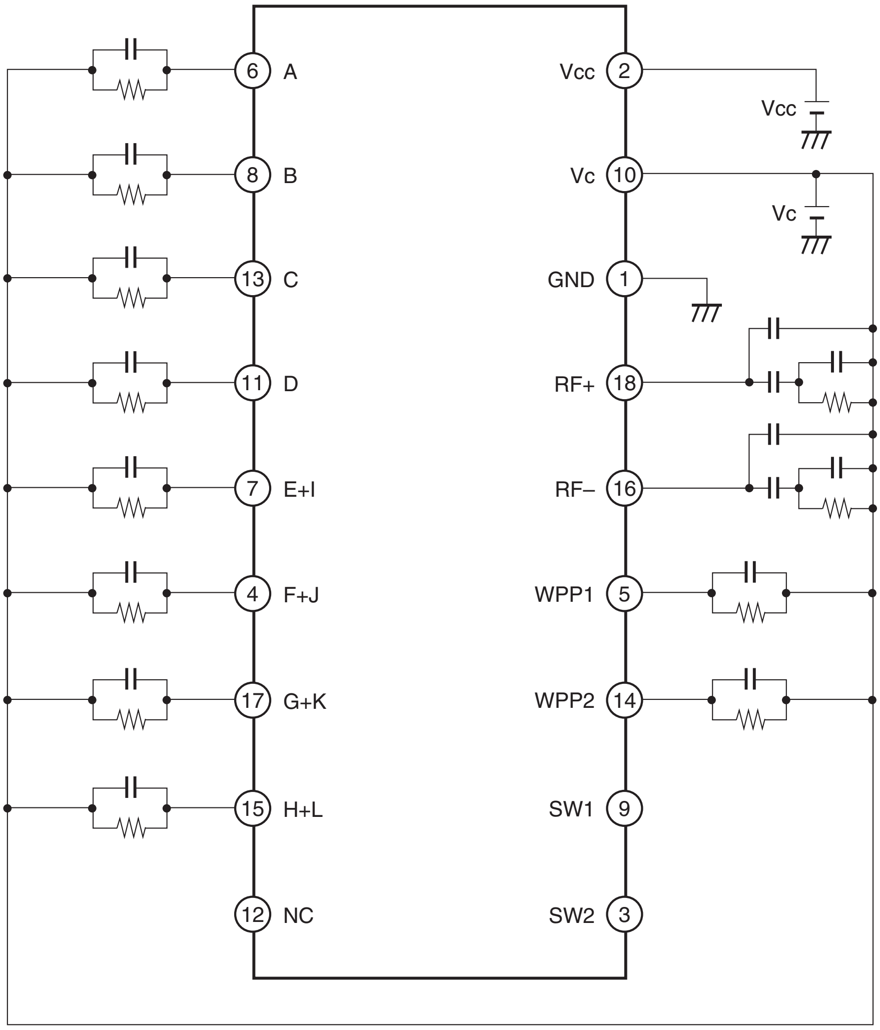
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Mode switching time (A to D, RF+, RF–)	Tset	λ = 650nm, 780nm, Po = 5µW Output level ±2% (Read mode ⇒ Write mode)	—	180	—	ns

Electrical and Optical Characteristics 8 (Sleep Mode)

(V_{CC} = 5.0V, V_C = 1.4V, V_{SW2} = 0V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	In the dark	—	0.7	1.0	mA

Measurement Circuit



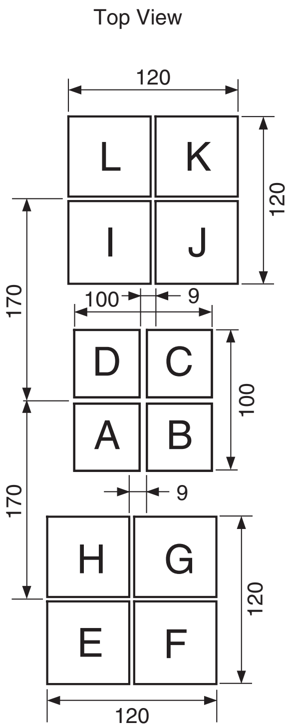
* The load conditions are as follows.

A to D	: 2kΩ//20pF
E+I to H+L, WPP1, WPP2	: 6kΩ//20pF
RF+, RF–	: (1µF + (1.3kΩ//10pF))//10pF

Photodetector Pattern Dimensions

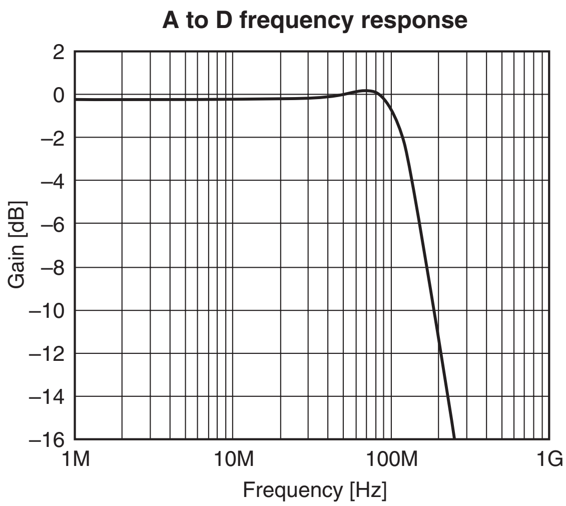
(Unit: µm)

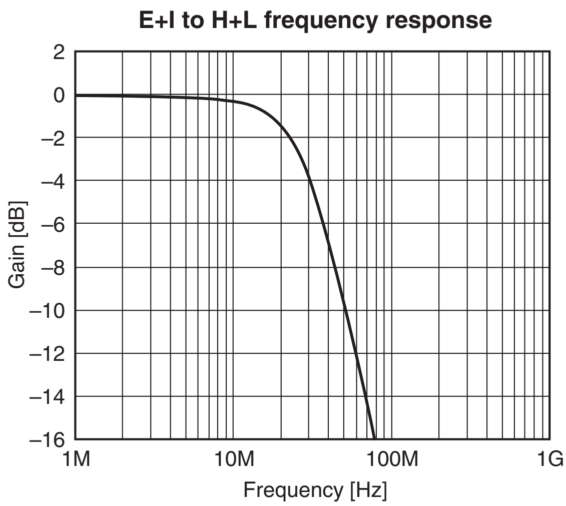
* Division line width: 4µm

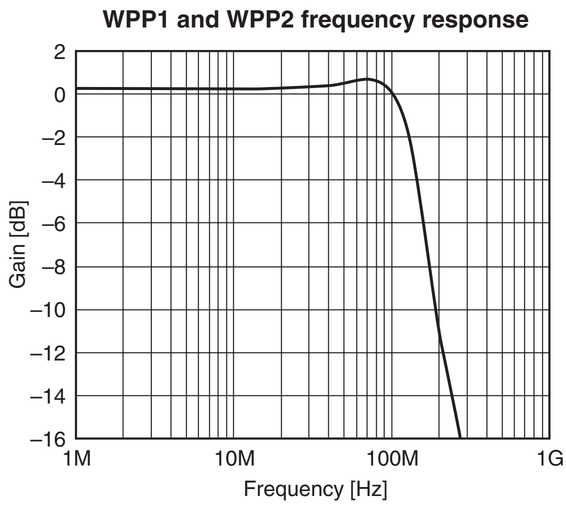


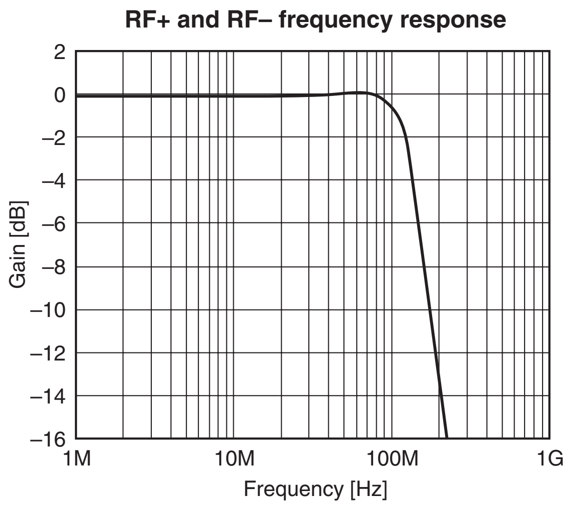
Example of Representative Characteristics (Frequency Response)

Mode-1

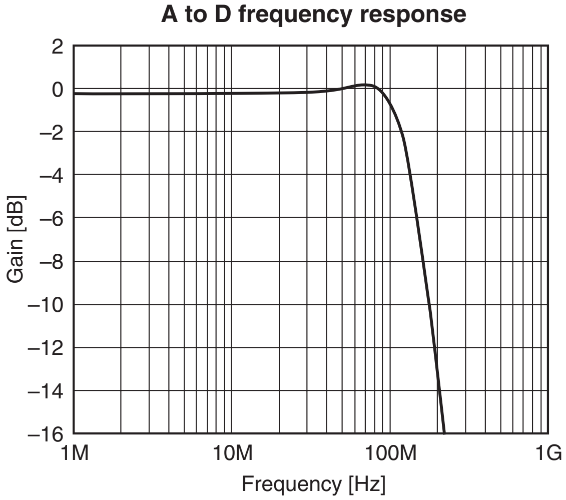


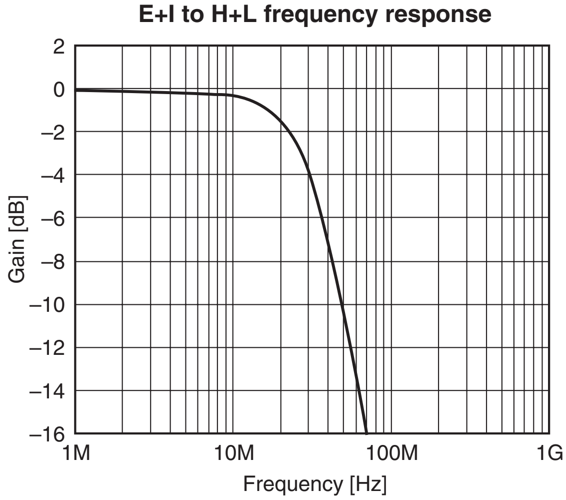


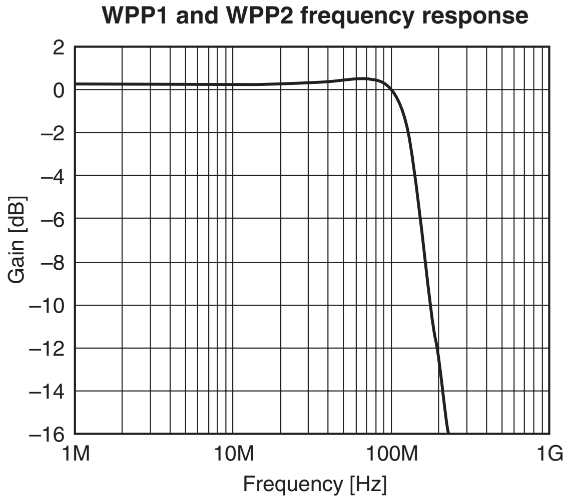


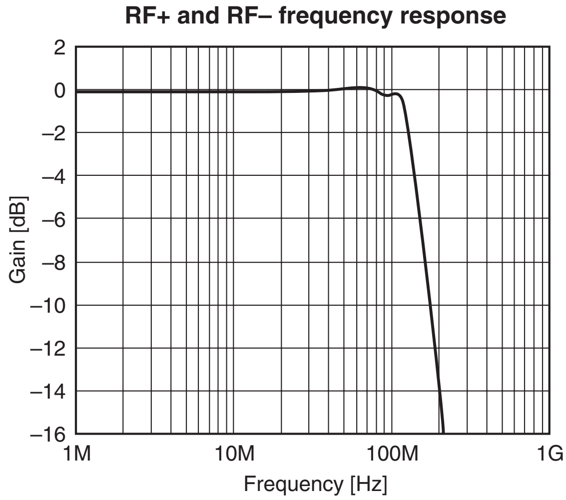


Mode-2

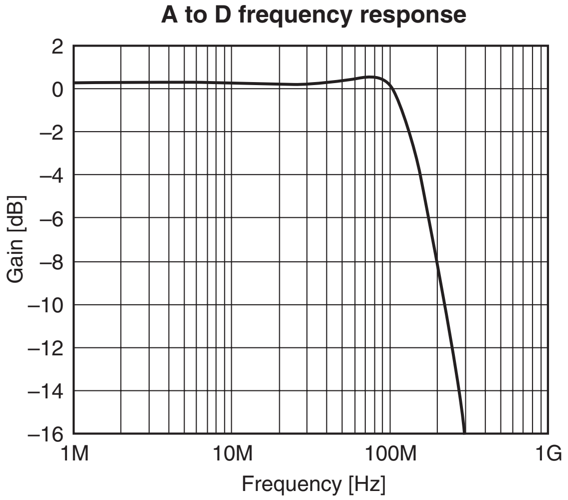

A to D frequency response
Gain [dB]
2
0
–2
–4
–6
–8
–10
–12
–14
–16
1M
10M
100M
1G
Frequency [Hz]

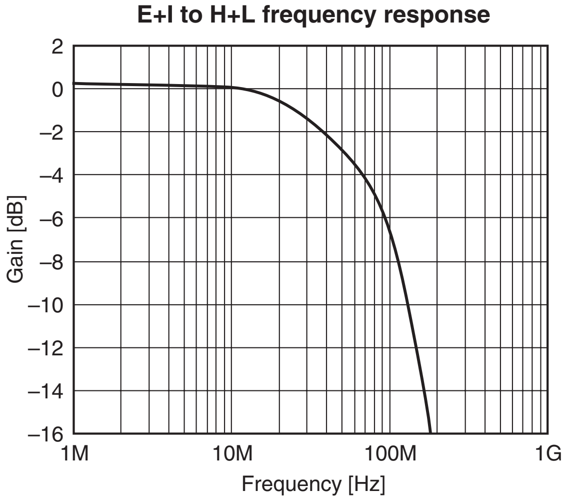

E+I to H+L frequency response
Gain [dB]
2
0
–2
–4
–6
–8
–10
–12
–14
–16
1M
10M
100M
1G
Frequency [Hz]

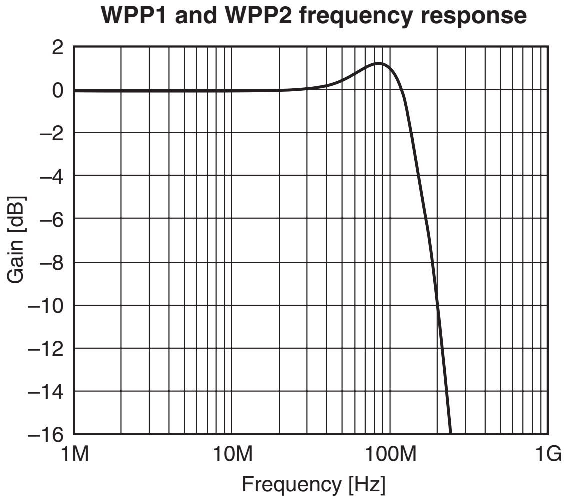

WPP1 and WPP2 frequency response
Gain [dB]
2
0
–2
–4
–6
–8
–10
–12
–14
–16
1M
10M
100M
1G
Frequency [Hz]


RF+ and RF– frequency response
Gain [dB]
2
0
–2
–4
–6
–8
–10
–12
–14
–16
1M
10M
100M
1G
Frequency [Hz]

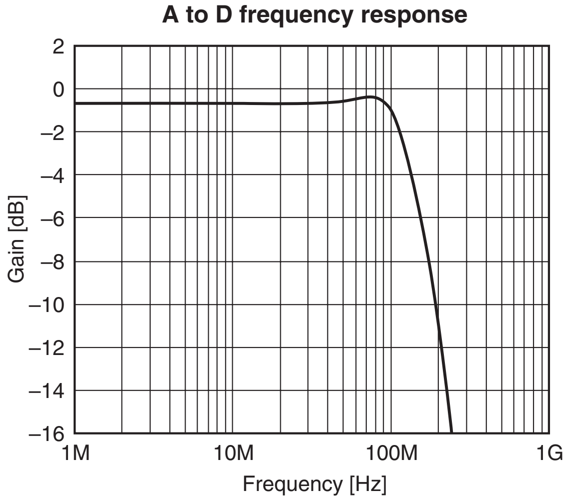
Mode-3

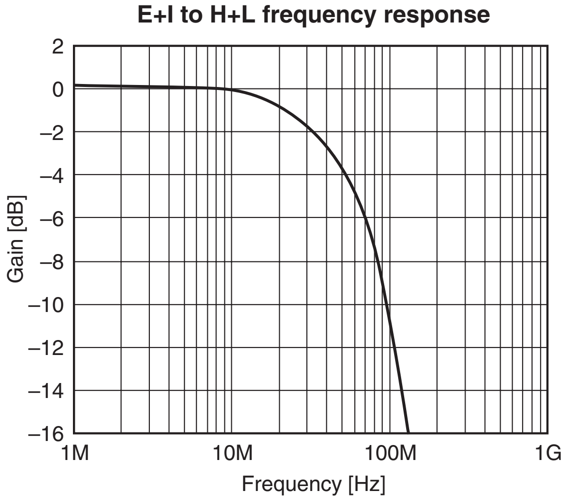

A to D frequency response
Gain [dB]
2
0
–2
–4
–6
–8
–10
–12
–14
–16
1M
10M
100M
1G
Frequency [Hz]

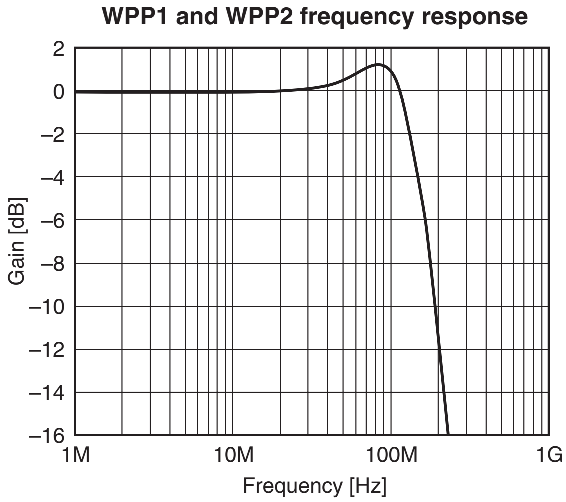

E+I to H+L frequency response
Gain [dB]
2
0
–2
–4
–6
–8
–10
–12
–14
–16
1M
10M
100M
1G
Frequency [Hz]


WPP1 and WPP2 frequency response
Gain [dB]
2
0
–2
–4
–6
–8
–10
–12
–14
–16
1M
10M
100M
1G
Frequency [Hz]

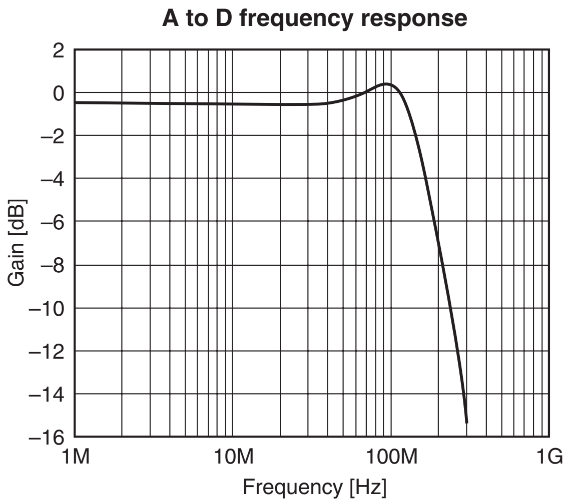
Mode-4

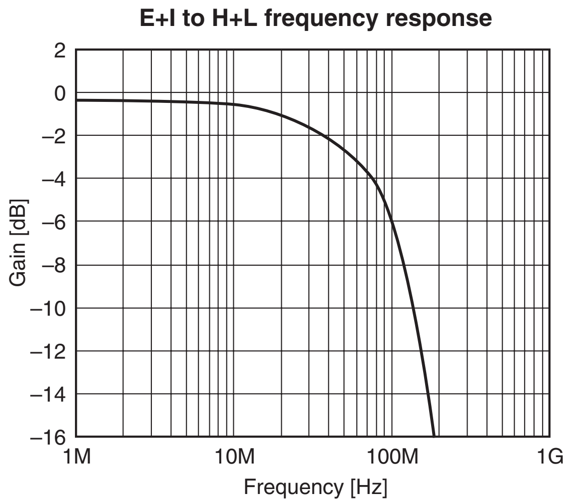

A to D frequency response
Gain [dB]
2
0
–2
–4
–6
–8
–10
–12
–14
–16
1M
10M
100M
1G
Frequency [Hz]

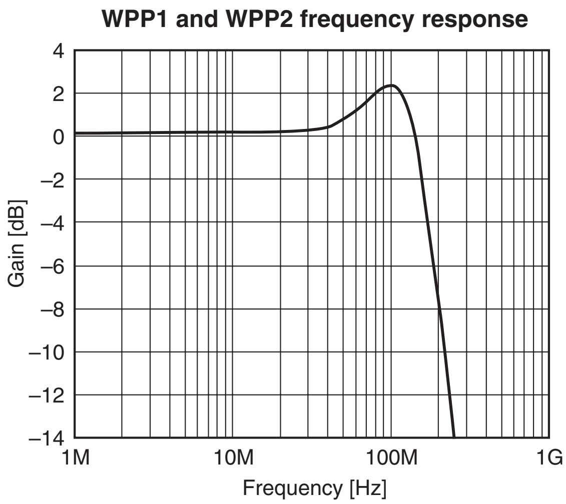

E+I to H+L frequency response
Gain [dB]
2
0
–2
–4
–6
–8
–10
–12
–14
–16
1M
10M
100M
1G
Frequency [Hz]


WPP1 and WPP2 frequency response
Gain [dB]
2
0
–2
–4
–6
–8
–10
–12
–14
–16
1M
10M
100M
1G
Frequency [Hz]

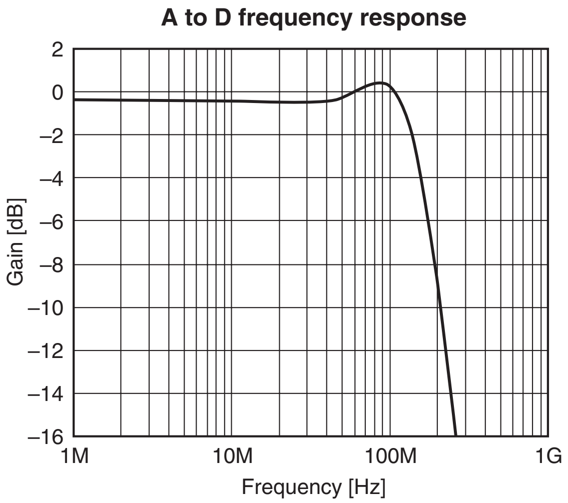
Mode-5

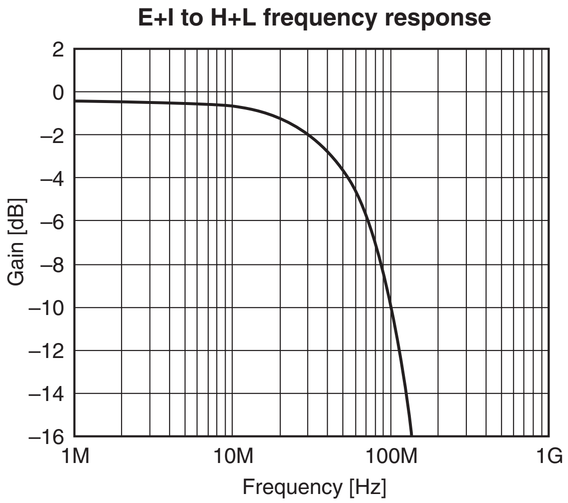

A to D frequency response
2
0
–2
–4
–6
–8
–10
–12
–14
–16
Gain [dB]
1M
10M
100M
1G
Frequency [Hz]

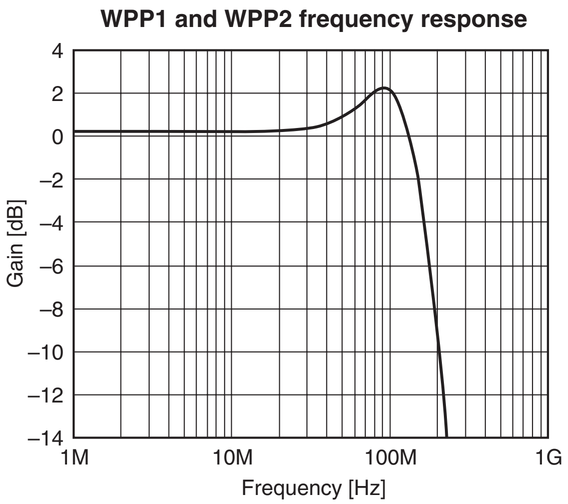

E+I to H+L frequency response
2
0
–2
–4
–6
–8
–10
–12
–14
–16
Gain [dB]
1M
10M
100M
1G
Frequency [Hz]


WPP1 and WPP2 frequency response
4
2
0
–2
–4
–6
–8
–10
–12
–14
Gain [dB]
1M
10M
100M
1G
Frequency [Hz]

Mode-6

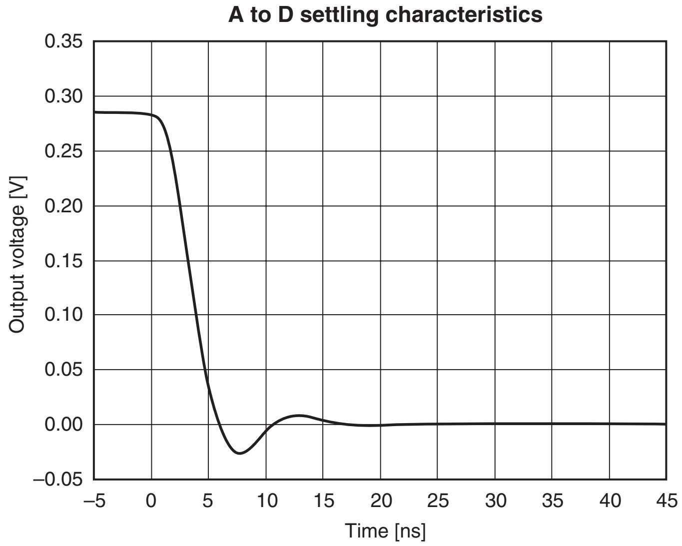

A to D frequency response
Gain [dB]
2
0
–2
–4
–6
–8
–10
–12
–14
–16
1M
10M
100M
1G
Frequency [Hz]

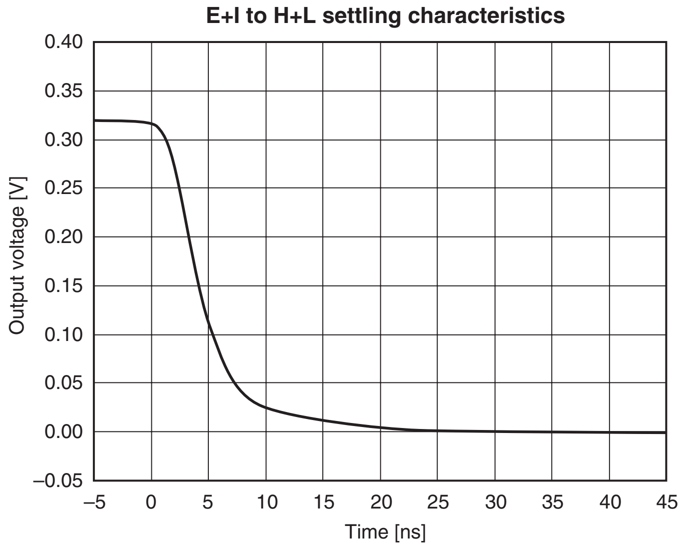

E+I to H+L frequency response
Gain [dB]
2
0
–2
–4
–6
–8
–10
–12
–14
–16
1M
10M
100M
1G
Frequency [Hz]

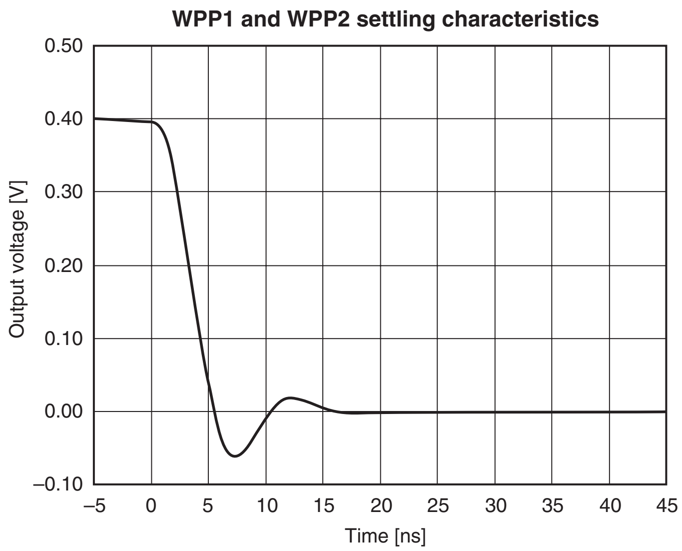

WPP1 and WPP2 frequency response
Gain [dB]
4
2
0
–2
–4
–6
–8
–10
–12
–14
1M
10M
100M
1G
Frequency [Hz]

Example of Representative Characteristics (Settling Characteristics)

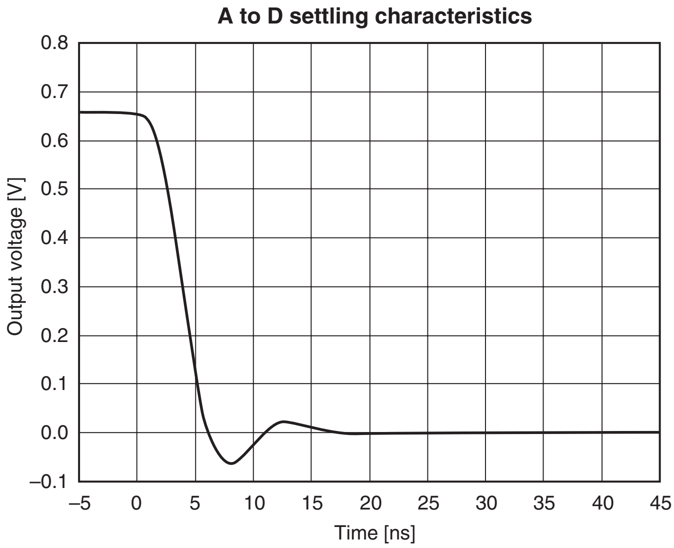
Mode-3

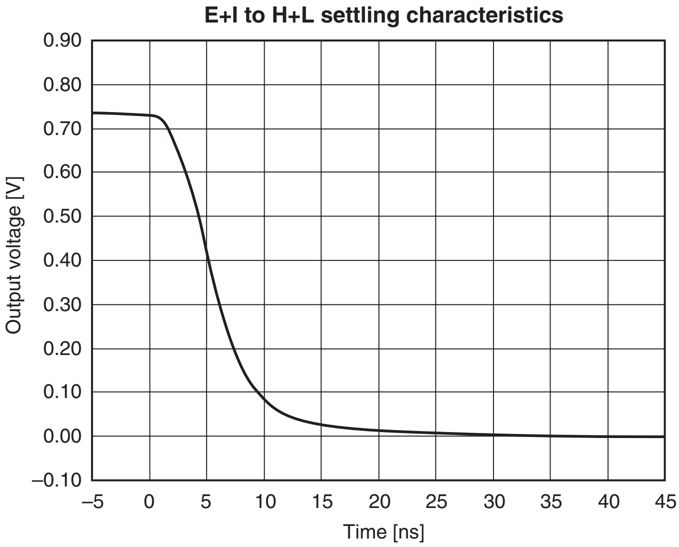


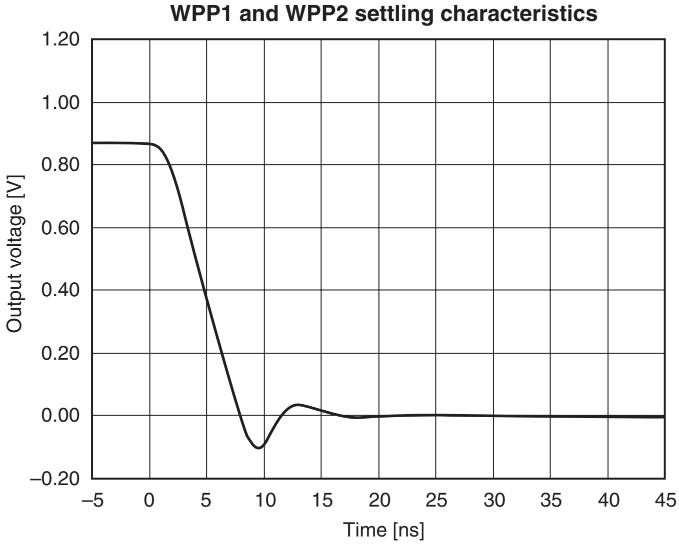




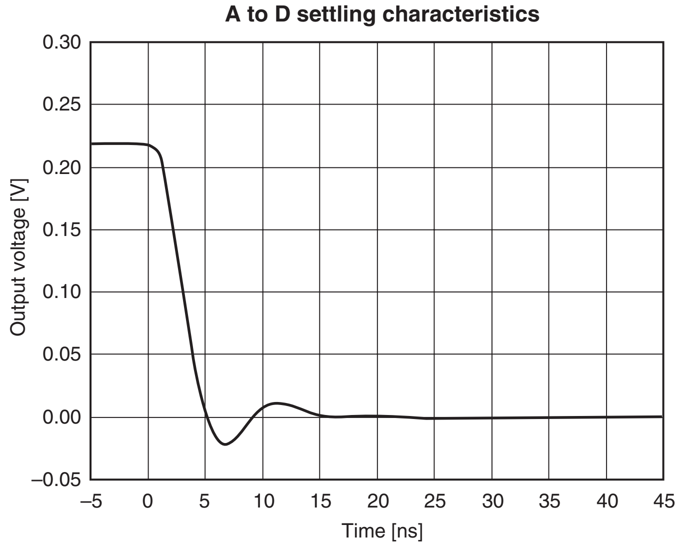
Mode-4

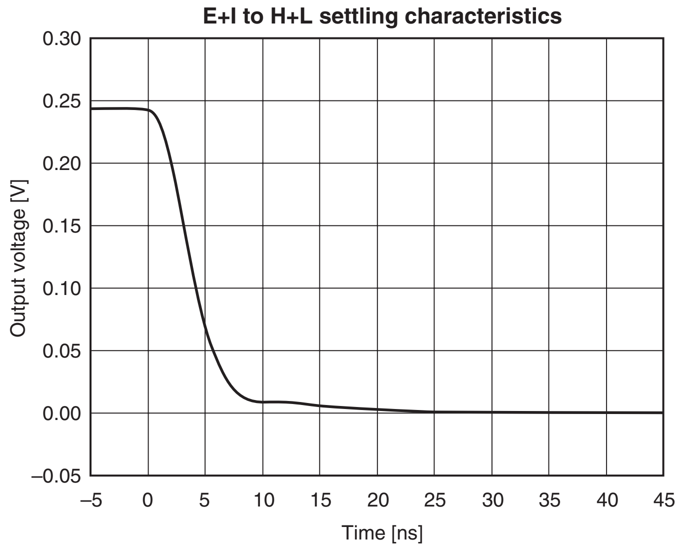

A to D settling characteristics
Output voltage [V]
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
–0.1
–5
0
5
10
15
20
25
30
35
40
45
Time [ns]

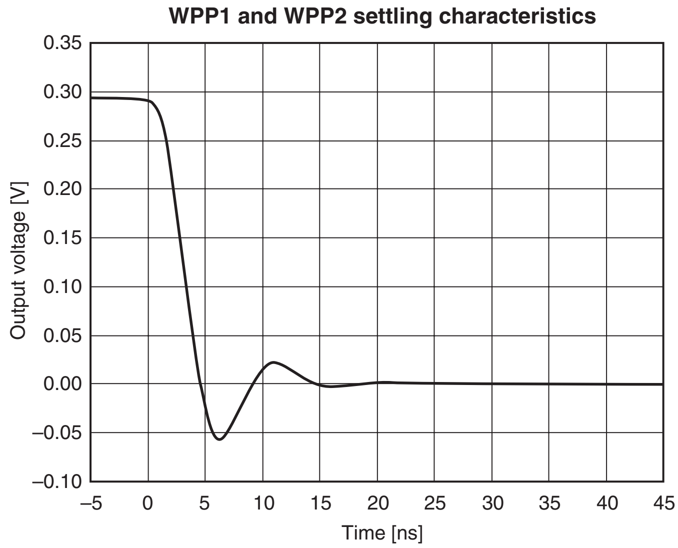

E+I to H+L settling characteristics
Output voltage [V]
0.90
0.80
0.70
0.60
0.50
0.40
0.30
0.20
0.10
0.00
–0.10
–5
0
5
10
15
20
25
30
35
40
45
Time [ns]


WPP1 and WPP2 settling characteristics
Output voltage [V]
1.20
1.00
0.80
0.60
0.40
0.20
0.00
–0.20
–5
0
5
10
15
20
25
30
35
40
45
Time [ns]

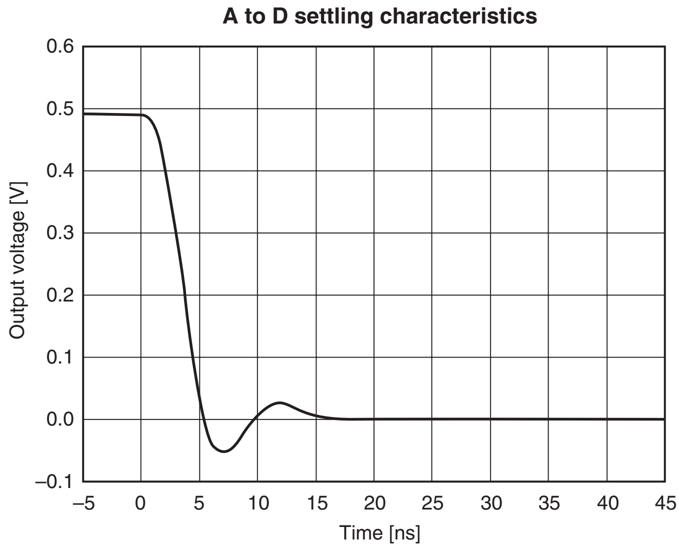
Mode-5

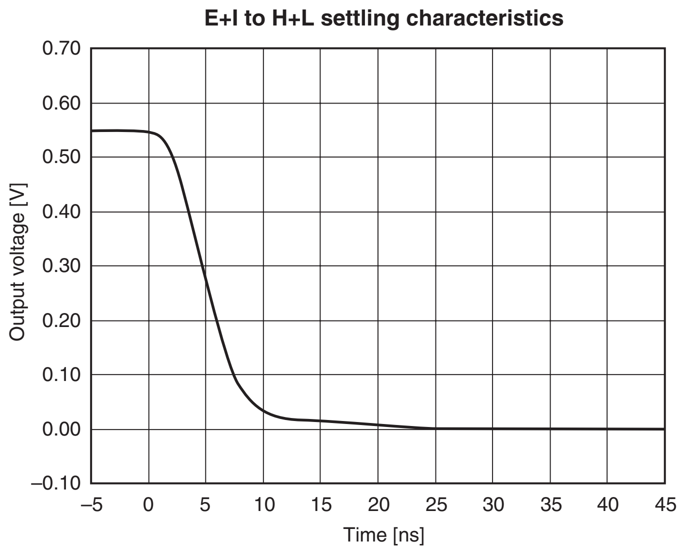

A to D settling characteristics
Output voltage [V]
0.30
0.25
0.20
0.15
0.10
0.05
0.00
–0.05
–5
0
5
10
15
20
25
30
35
40
45
Time [ns]

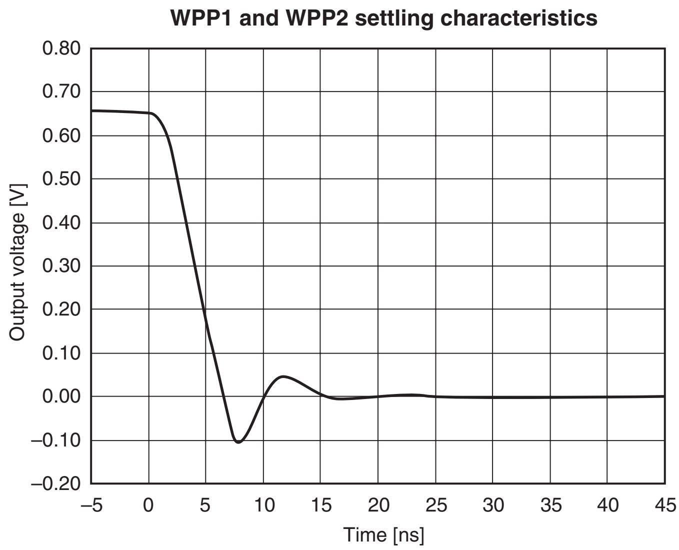

E+I to H+L settling characteristics
Output voltage [V]
0.30
0.25
0.20
0.15
0.10
0.05
0.00
–0.05
–5
0
5
10
15
20
25
30
35
40
45
Time [ns]


WPP1 and WPP2 settling characteristics
Output voltage [V]
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0.00
–0.05
–0.10
–5
0
5
10
15
20
25
30
35
40
45
Time [ns]

Mode-6


A to D settling characteristics
Output voltage [V]
0.6
0.5
0.4
0.3
0.2
0.1
0.0
–0.1
–5
0
5
10
15
20
25
30
35
40
45
Time [ns]


E+I to H+L settling characteristics
Output voltage [V]
0.70
0.60
0.50
0.40
0.30
0.20
0.10
0.00
–0.10
–5
0
5
10
15
20
25
30
35
40
45
Time [ns]


WPP1 and WPP2 settling characteristics
Output voltage [V]
0.80
0.70
0.60
0.50
0.40
0.30
0.20
0.10
0.00
–0.10
–0.20
–5
0
5
10
15
20
25
30
35
40
45
Time [ns]

Notes on Operation

1. Power supply

The CXA2726GA can be used with a single power supply or a dual power supply. However, this IC is not provided with a center voltage generating circuit, and so when used with a single power supply the center voltage must be supplied from the RF amplifier or other device.
The power supply connections for each case are shown in the table below.

	V_{CC} (Pin 2)	V_C (Pin 10)	GND (Pin 1)
Dual power supply	Positive power supply	GND	Negative power supply
Single power supply	Positive power supply	Center voltage	GND

The potential difference between the V_{CC} pin and the GND pin should be in the range of 4.5 to 5.5V for both a single power supply and a dual power supply.

2. Mechanical strength of package

The mechanical strength of the package is not guaranteed for the CXA2726GA.
Do not employ a mounting method which applies a heavy load to the package.

3. Visual inspection standard

The visual inspection standards over the photodetector are as follows.

(1) Foreign object limit
A to L: Equivalent area ϕ10μm or less

(2) Inspection method
Using a metallurgical microscope (×50, coaxial illumination, bright field image), focus on the photodetector and measure the sharp shadow size.

(3) Inspection range
Entire photodetector area (entire area of A to L on page 21).

4. Bypass capacitors

Connect 0.1µF capacitors "between the V_{CC} and V_C pins and between the V_C and GND pins" or "between the V_{CC} and GND pins and between the V_C and GND pins" to lower the power supply line impedance.
Use a flexible printed circuit (FPC) pattern or take other measures so that the bypass capacitors can be located near the PDIC.

5. Electrostatic strength

The CXA2726GA has a electrostatic strength of 300V*1, and should be used in an environment where countermeasures against electrostatic discharge have been implemented.

*1 Testing method: EIAJ ED-4701-1 C-111A Testing method A

6. Soldering

Reflow soldering: Finish reflow soldering under the recommended conditions described on the next page.
Also, take care not to apply stress to the package during preheating and in the heated condition including immediately after soldering because the resin is softened in these cases.

Reflow Soldering Recommended Conditions 1

1. Perform infrared or hot air reflow, or use an oven that combines these methods.

2. Finish reflow soldering within the following range after unsealing the moisture-proof packing.

   30°C/70%RH/8h → Reflow → 30°C/70%RH/8h → Reflow

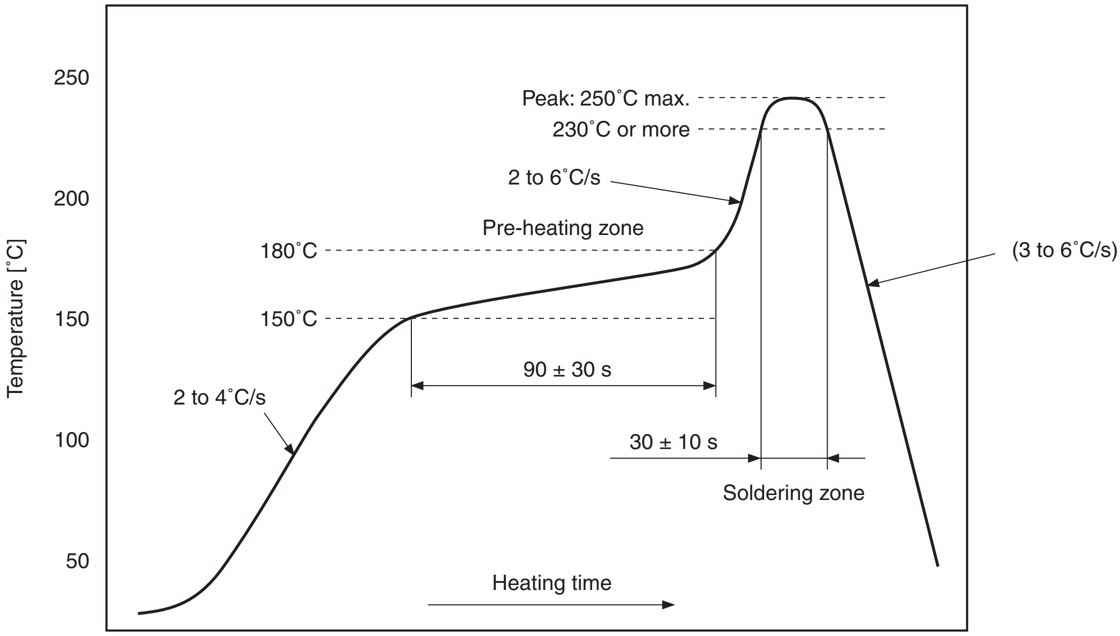
   Note) Perform reflow soldering a maximum of two times.

   When reflow soldering cannot be performed within these specifications, baking should first be performed under either of the following conditions.

   [Baking conditions]

   - 125°C, 10 to 48h
   - Baking can be performed in the taped condition.
   - Baking should be performed only one time.

3. Reflow conditions: Perform reflow soldering within the range shown in the figure below.



Be sure to consult your Sony representative when performing reflow soldering outside of the ranges described above.

Reflow Soldering Recommended Conditions 2

1. Perform infrared or hot air reflow, or use an oven that combines these methods.

2. Finish reflow soldering within the following range after unsealing the moisture-proof packing.

   30°C/80%RH/12h → Reflow

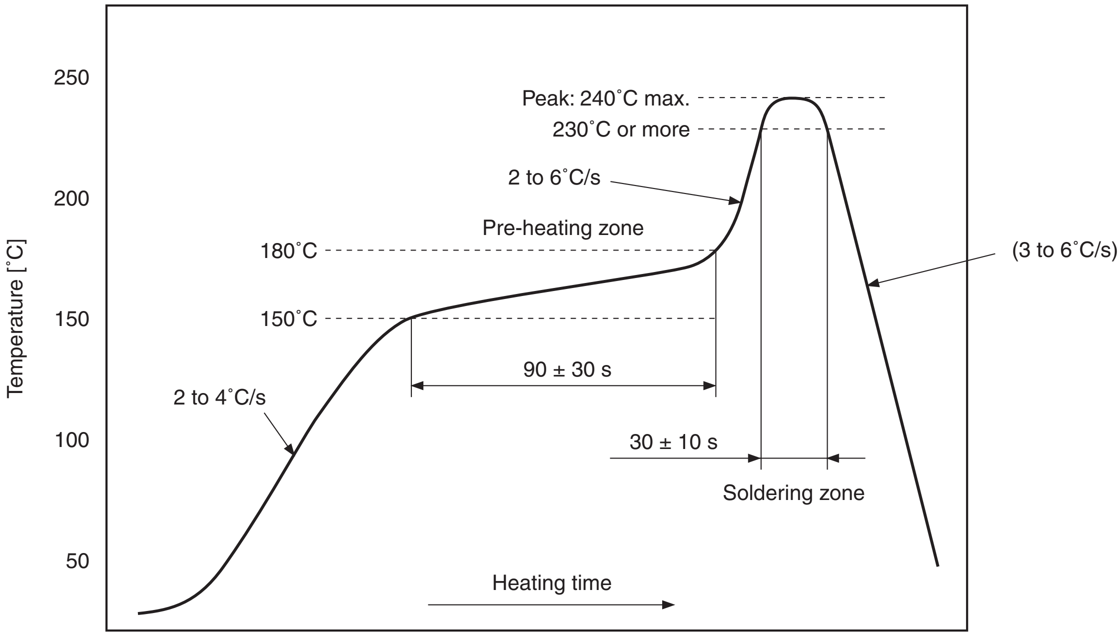
   Note) Perform reflow soldering only one time.

   When reflow soldering cannot be performed within these specifications, baking should first be performed under either of the following conditions.

   [Baking conditions]

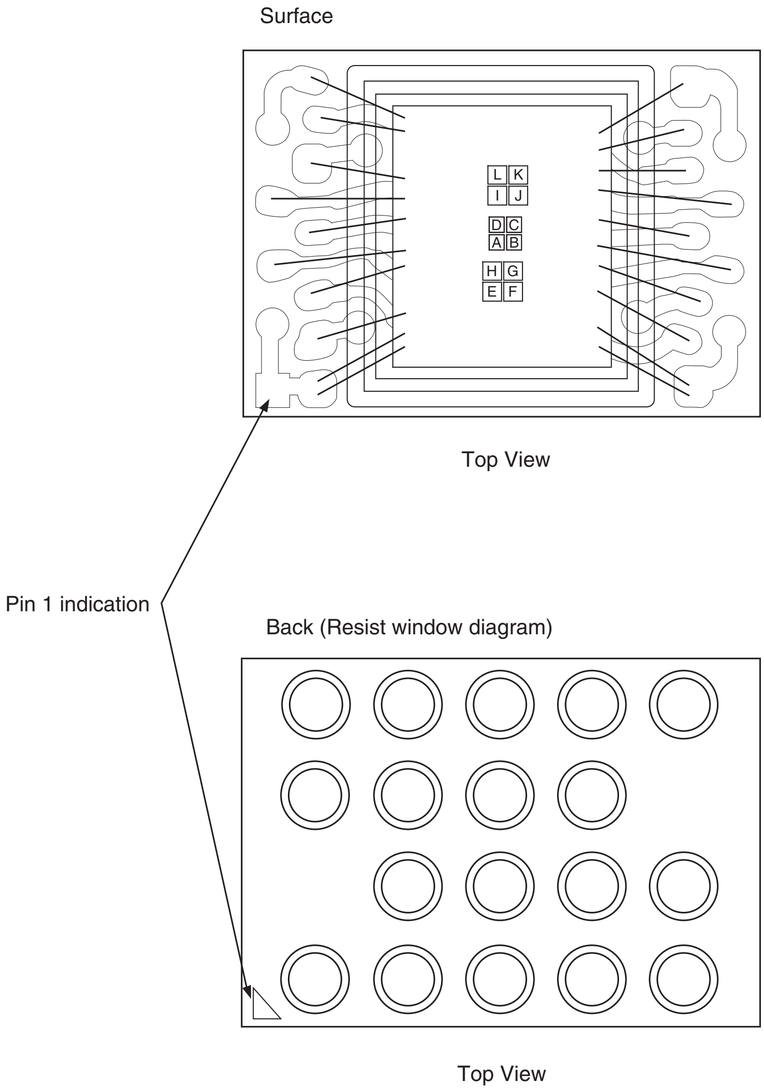
   - 125°C, 10 to 48h
   - Baking can be performed in the taped condition.
   - Baking should be performed only one time.

3. Reflow conditions: Perform reflow soldering within the range shown in the figure below.



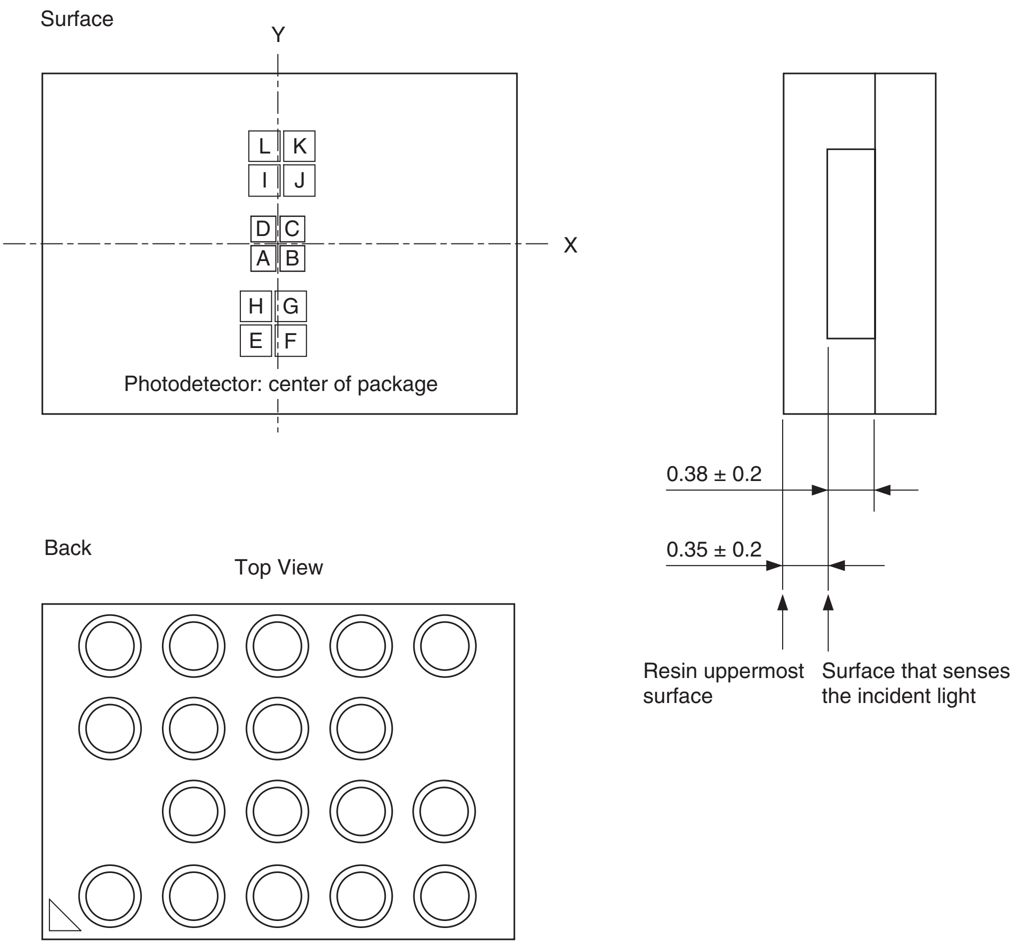
Be sure to consult your Sony representative when performing reflow soldering outside of the ranges described above.

Pin 1 Indication Explanation Figure



Photodetector Position

(Unit: mm)

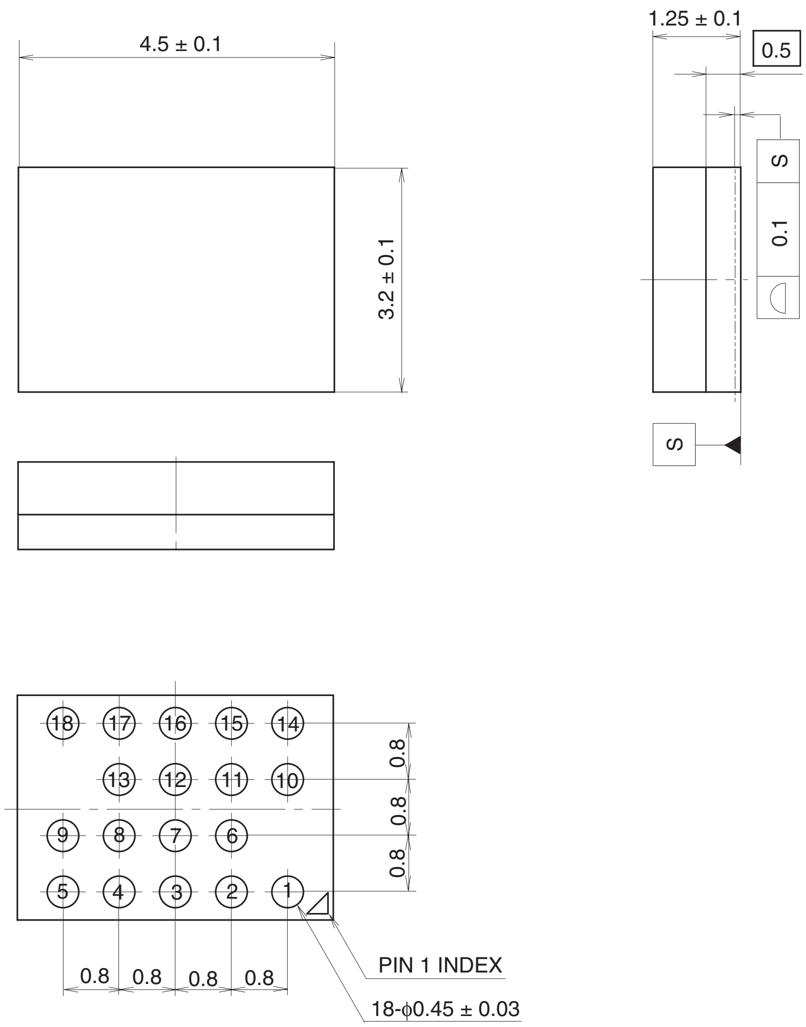


- The resin thickness (mechanical dimension) over the photodetector is 0.35 ± 0.2mm.
  The resin refractive index is as follows.
  650nm: n = 1.55, 780nm: n = 1.54
- The photodetector center position accuracy is as follows.
  X, Y: 0 ± 0.16mm, angular θ: 0 ± 2° (with the X axis as θ = 0°)

Package Outline

(Unit: mm)

18PIN LFLGA



SONY CODE	LFLGA-18P-391
JEITA CODE	————
JEDEC CODE	————

PACKAGE MATERIAL	GLASS EPOXY
TERMINAL TREATMENT	NICKEL & GOLD PLATING
TERMINAL MATERIAL	COPPER
PACKAGE MASS	0.03g