Integrated Circuit Systems, Inc.

ICS87946I-147

LOW SKEW, ÷1, ÷2 LVCMOS/LVTTL CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS87946I-147 is a low skew, ÷1, ÷2 LVCMOS/LVTTL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS87946I-147 has two selectable single ended clock inputs. The single ended clock inputs accept LVCMOS or LVTTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 10 to 20 by utilizing the ability of the outputs to drive two series terminated lines.

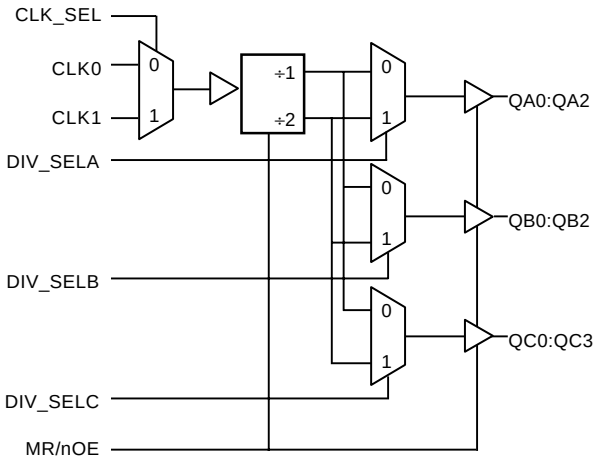
The divide select inputs, DIV_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The master reset input, MR/nOE, resets the internal frequency dividers and also controls the active and high impedance states of all outputs.

The ICS87946I-147 is characterized at full 3.3V for input V_{DD}, and mixed 3.3V and 2.5V for output operating supply mode. Guaranteed bank, output and part-to-part skew characteristics make the ICS87946I-147 ideal for those clock distribution applications demanding well defined performance and repeatability.

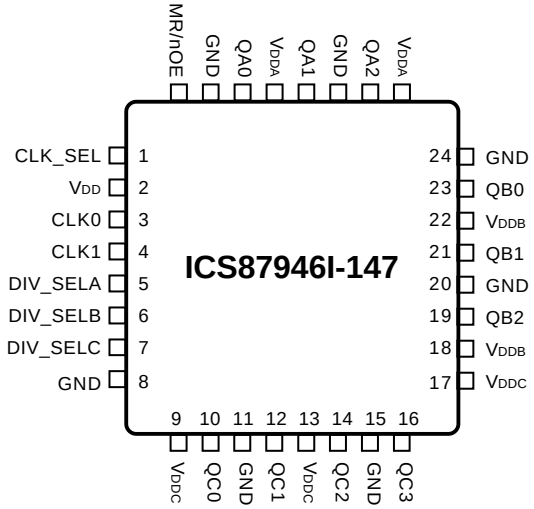
FEATURES

- 10 single ended LVCMOS/LVTTL outputs, 7Ω typical output impedance
- Selectable CLK0 and CLK1 LVCMOS/LVTTL clock inputs
- CLK0 and CLK1 can accept the following input levels: LVCMOS and LVTTL
- Maximum output frequency: 250MHz
- Bank skew: 30ps (maximum)
- Output skew: 175ps (maximum)
- Part-to-part skew: 850ps (maximum)
- Multiple frequency skew: 200ps (maximum)
- 3.3V input, outputs may be either 3.3V or 2.5V supply
- -40°C to 85°C ambient operating temperature
- Pin compatible to the MPC9446 and MPC946

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm body package
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1. When LOW, selects CLK0. LVCMOS / LVTTL interface levels.
2	V_{DD}	Power		Positive supply pin.
3, 4	CLK0, CLK1	Input	Pullup	LVCMOS / LVTTL clock inputs.
5	DIV_SELA	Input	Pulldown	Controls frequency division for Bank A outputs. LVCMOS / LVTTL interface levels.
6	DIV_SELB	Input	Pulldown	Controls frequency division for Bank B outputs. LVCMOS / LVTTL interface levels.
7	DIV_SELC	Input	Pulldown	Controls frequency division for Bank C outputs. LVCMOS / LVTTL interface levels.
8, 11, 15, 20, 24, 27, 31	GND	Power		Power supply ground.
9, 13, 17	V_{DDC}	Power		Positive supply pins for Bank C outputs.
10, 12, 14, 16	QC0, QC1, QC2, QC3	Output		Bank C outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
18, 22	V_{DDB}	Power		Positive supply pins for Bank B outputs.
19, 21, 23	QB2, QB1, QB0	Output		Bank B outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
25, 29	V_{DDA}	Power		Positive supply pins for Bank A outputs.
26, 28, 30	QA2, QA1, QA0	Output		Bank A outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
32	MR/nOE	Input	Pulldown	Active HIGH Master Reset. Active LOW output enable. When logic HIGH, the internal dividers are reset and the outputs are tri-stated (HiZ). When logic LOW the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, *V_{DDx} = 3.6V		25		pF
R_{OUT}	Output Impedance			7		Ω

*NOTE: V_{DDx} denotes V_{DDA}, V_{DDB}, V_{DDC}.

TABLE 3. FUNCTION TABLE

Inputs				Outputs		
MR/nOE	DIV_SELA	DIV_SELB	DIV_SELC	QA0:QA2	QB0:QB2	QC0:QC3
1	X	X	X	Hi Z	Hi Z	Hi Z
0	0	X	X	fIN/1	Active	Active
0	1	X	X	fIN/2	Active	Active
0	X	0	X	Active	fIN/1	Active
0	X	1	X	Active	fIN/2	Active
0	X	X	0	Active	Active	fIN/1
0	X	X	1	Active	Active	fIN/2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDx} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDx}$ = 3.3V ± 0.3V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.0	3.3	3.6	V
V_{DDx}	Output Supply Voltage; NOTE 1		3.0	3.3	3.6	V
I_{DD}	Power Supply Current				55	mA
I_{DDx}	Output Supply Current				23	mA

NOTE 1: V_{DDx} denotes V_{DDA}, V_{DDB}, V_{DDC}.

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDx}$ = 3.3V ± 0.3V, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL, MR/nOE		2		V_{DD} + 0.3	V
		CLK0, CLK1		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL, MR/nOE		-0.3		0.8	V
		CLK0, CLK1		-0.3		1.3	V
I_{IH}	Input High Current	DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL, MR/nOE	$V_{DD} = V_{IN}$ = 3.6V			150	µA
		CLK0, CLK1	$V_{DD} = V_{IN}$ = 3.6V			5	µA
I_{IL}	Input Low Current	DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL, MR/nOE	V_{DD} = 3.6V, V_{IN} = 0V	-5			µA
		CLK0, CLK1	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V
I_{OZL}	Output Tristate Current Low			-5			µA
I_{OZH}	Output Tristate Current High					5	µA

NOTE 1: Outputs terminated with 50Ω to V_{DDx}/2. See Parameter Measurement Section, 3.3V Output Load Test Circuit.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDx} = 3.3V \pm 0.3V$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1	f ≤ 250MHz	2		5	ns
*t*sk(b)	Bank Skew; NOTE 2, 7	Measured on rising edge at $V_{DDx}/2$			30	ps
*t*sk(o)	Output Skew; NOTE 3, 7	Measured on rising edge at $V_{DDx}/2$			175	ps
*t*sk(w)	Multiple Frequency Skew; NOTE 4, 7	Measured on rising edge at $V_{DDx}/2$			275	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 5, 7	Measured on rising edge at $V_{DDx}/2$			850	ps
t_R / t_F	Output Rise/Fall Time; NOTE 6	20% to 80%	400		950	ps
t_{PW}	Output Pulse Width		$t_{PERIOD}/2 - 1$	$t_{PERIOD}/2$	$t_{PERIOD}/2 + 1$	ns
t_{EN}	Output Enable Time; NOTE 6	f = 10MHz			3	ns
t_{DIS}	Output Disable Time; NOTE 6	f = 10MHz			3	ns

NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDx}/2$ of the output.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDx}/2$.
NOTE 4: Defined as skew across banks of outputs operating at different frequencies with the same supply voltages and equal load conditions.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDx}/2$.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4C. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDx} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDx}	Output Supply Voltage; NOTE 1		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				55	mA
I_{DDx}	Output Supply Current				22	mA

NOTE 1: V_{DDx} denotes V_{DDA}, V_{DDB}, V_{DDC}.

TABLE 4D. LVCMOS/LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDx} = 2.5V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL, nMR/OE		2		V_{DD} + 0.3	V
		CLK0, CLK1		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL, nMR/OE		-0.3		0.8	V
		CLK0, CLK1		-0.3		1.3	V
I_{IH}	Input High Current	DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL, nMR/OE	V_{DD} = V_{IN} = 3.465V			150	µA
		CLK0, CLK1	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL, nMR/OE	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		CLK0, CLK1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1			1.8			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V
I_{OZL}	Output Tristate Current Low			-5			µA
I_{OZH}	Output Tristate Current High					5	µA

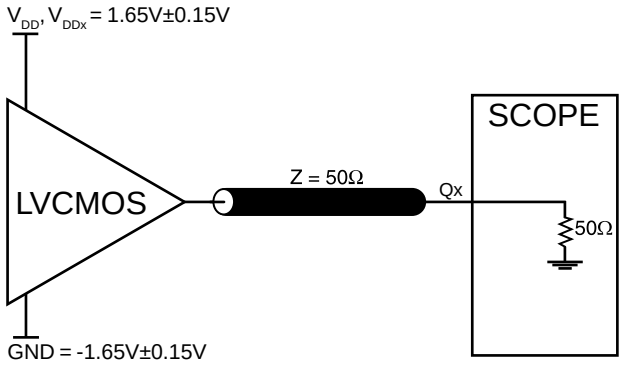
NOTE 1: Outputs terminated with 50Ω to V_{DDx}/2. See Parameter Measurement Section, 3.3V/2.5V Output Load Test Circuit.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDx} = 2.5V ± 5%, T_A = -40°C TO 85°C

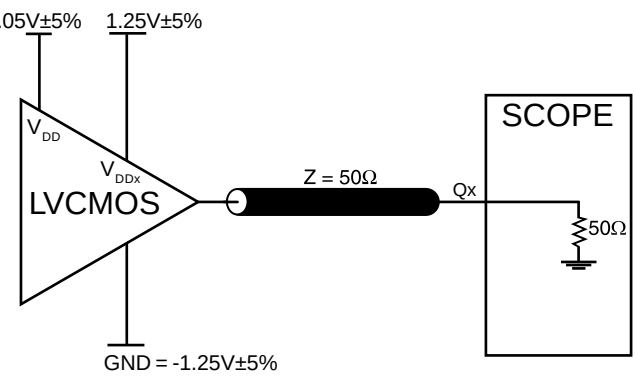
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1	f ≤ 250MHz	2		5	ns
*t*sk(b)	Bank Skew; NOTE 2, 7	Measured on rising edge at V_{DDx}/2			35	ps
*t*sk(o)	Output Skew; NOTE 3, 7	Measured on rising edge at V_{DDx}/2			175	ps
*t*sk(w)	Multiple Frequency Skew; NOTE 4, 7	Measured on rising edge at V_{DDx}/2			200	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 5, 7	Measured on rising edge at V_{DDx}/2			875	ps
t_R / t_F	Output Rise/Fall Time; NOTE 6	20% to 80%	400		950	ps
t_{PW}	Output Pulse Width		t_{PERIOD}/2 - 1	t_{PERIOD}/2	t_{PERIOD}/2 + 1	ns
t_{EN}	Output Enable Time; NOTE 6	f = 10MHz			3	ns
t_{DIS}	Output Disable Time; NOTE 6	f = 10MHz			3	ns

NOTE 1: Measured from the V_{DD}/2 of the input to V_{DDx}/2 of the output.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions. Measured at V_{DDx}/2.
NOTE 4: Defined as skew across banks of outputs operating at different frequencies with the same supply voltages and equal load conditions.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDx}/2.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

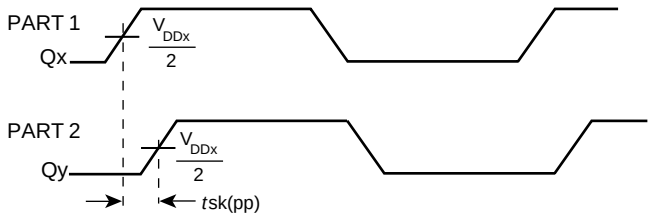
PARAMETER MEASUREMENT INFORMATION



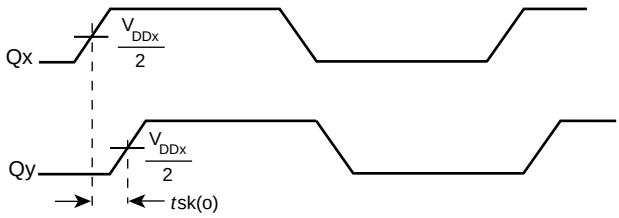
3.3V OUTPUT LOAD AC TEST CIRCUIT



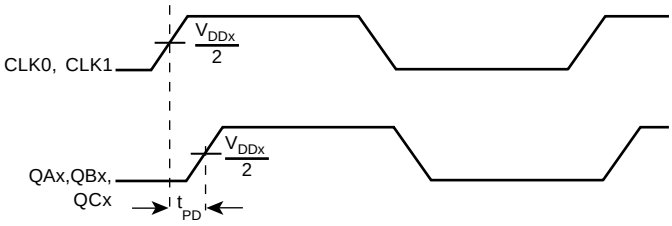
3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT



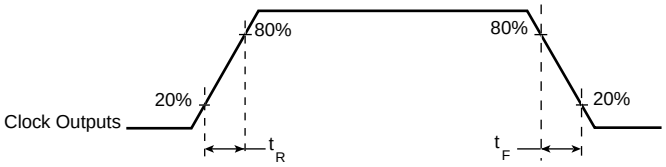
PART-TO-PART SKEW



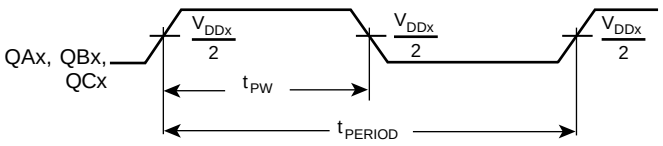
OUTPUT SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

t_{PW} & t_{PERIOD}

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87946I-147 is: 1204

PACKAGE OUTLINE - Y SUFFIX

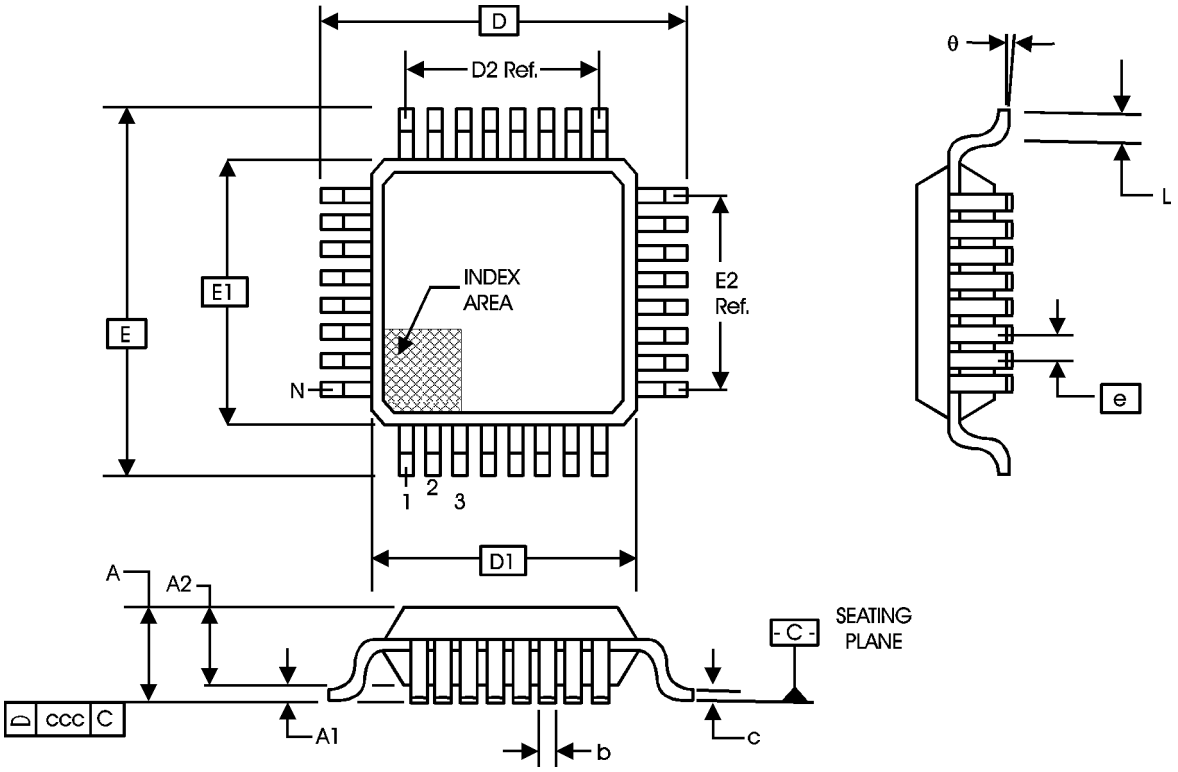


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS87946AYI-147	87946AI147	32 Lead LQFP	250 per tray	-40°C to 85°C
ICS87946AYI-147T	87946AI147	32 Lead LQFP on Tape and Reel	1000	-40°C to 85°C

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