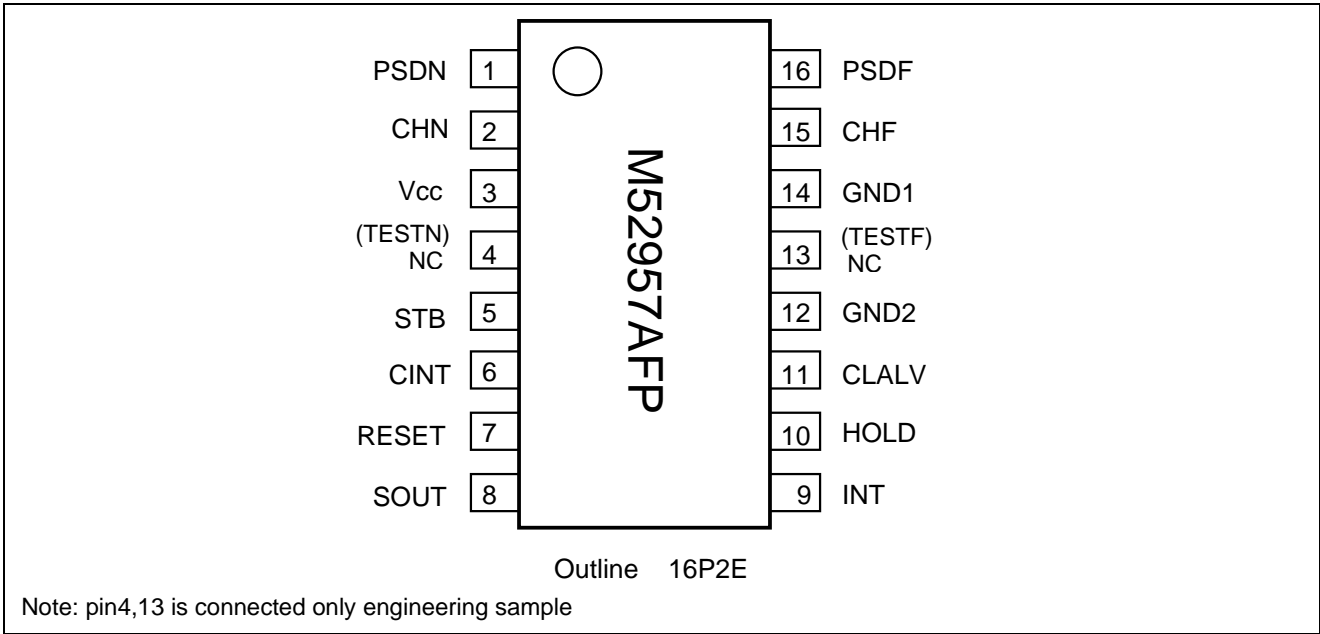
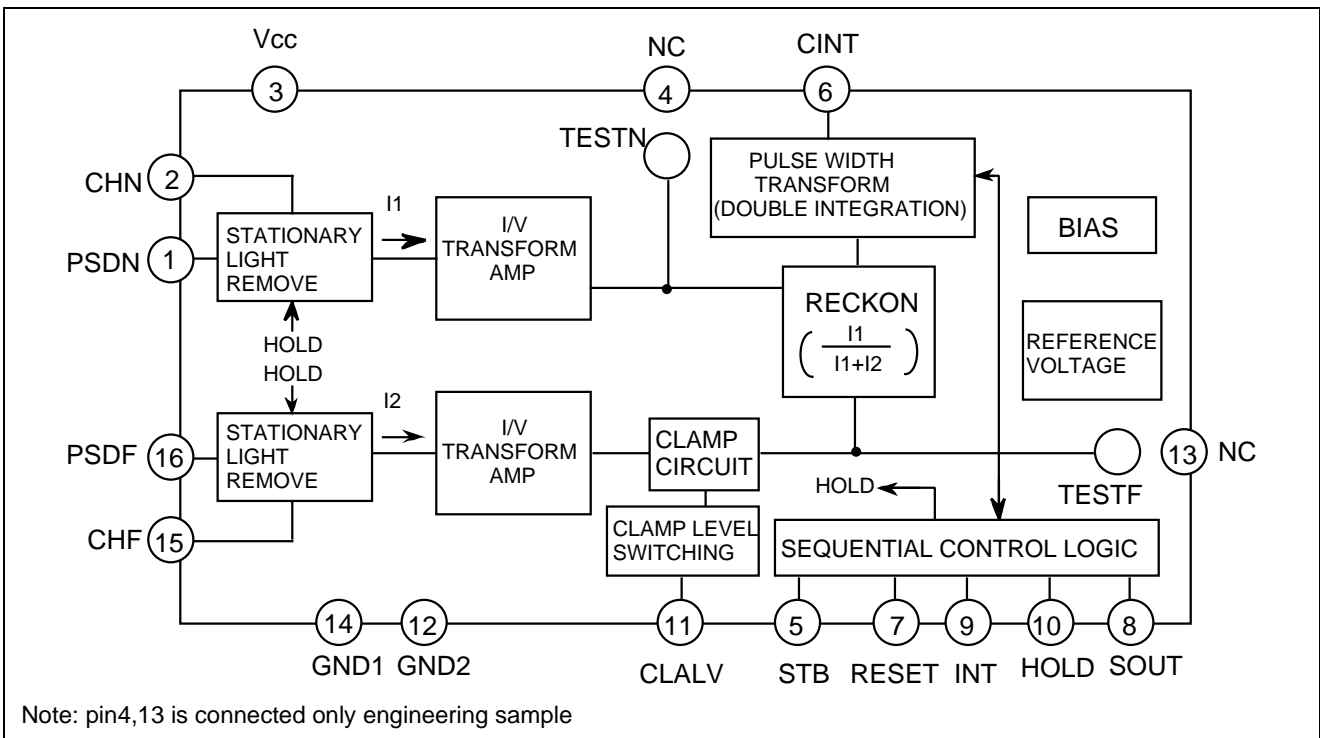




Pin Configuration



Block Diagram



**Absolute Maximum Ratings**

(Ta = 25°C, unless otherwise noted.)

<b>Parameter</b>	<b>Symbol</b>	<b>Ratings</b>	<b>Unit</b>	<b>Remark</b>
Supply voltage	VCC	7.0	V	note 1
Power dissipation	Pd	320	mW	Ta=25°C
Thermal derating	Kθ	-3.2	mW/°C	Ta≥25°C
Pin supply voltage	VIF	7.0	V	Pin5, 7, 8, 9, 10, 11
Another pin supply voltage	VI/O	-0.3 to VCC + 0.3	V	note 2
Output pin inflow current	Isout	0.5	mA	NPN open collector
Operating temperature	Topr	-10 to 50	°C	
Storage temperature	Tstg	-40 to 125	°C	

Notes : 1. As a principle, do not provide a supply voltage reversely.

2. As a principle, do not provide the terminals with the voltage over supply voltage or under ground voltage.

## Electrical characteristics

(Ta = 25°C, VCC = 5.0V, unless otherwise noted.)

Classification	Parameter	Symbol	Limits			Unit	Test conditions	Note
			Min.	Typ.	Max.			
	Operating supply voltage range	VCC	2.2	3.0	5.5	V		
Consuming current	Usual consuming current	ICC1	—	5.9	7.7	mA		
	While Rapid charge consuming current 1	ICC2	—	17.7	23.0	mA	While CH rapid charge consuming current	*1
	While Rapid charge consuming current 2	ICC3	—	19.0	24.7	mA	While CH and CINT rapid charge consuming current	*1
	While STAND BY consuming current	ICC4	—	—	1.0	μA		*1
HOLD pin	HOLD "H" input voltage	VHOH	1.1	—	7.0	V		
	HOLD "L" input current	VHOL	0	—	0.3	V		
	HOLD "H" input current	IHOH	—	—	1.0	μA	VIH=5.5V	
	HOLD "L" input voltage	IHOL	-100	-75	-50	μA	VIL=0V	
INT pin	INT "H" input voltage	VINH	1.1	—	7.0	V		
	INT "L" input voltage	VINL	0	—	0.3	V		
	INT "H" input current	IINH	—	—	1.0	μA	VIH=5.5V	
	INT "L" input current	IINL	-100	-75	-50	μA	VIL=0V	
CLALV pin	CLALV "H" input voltage	VCLH	1.1	—	7.0	V		
	CLALV "L" input voltage	VCLL	0	—	0.3	V		
	CLALV "H" input current	ICLH	—	—	1.0	μA	VIH=5.5V	
	CLALV "L" input current	ICLL	-100	-75	-50	μA	VIL=0V	
RESET pin	RESET "H" input voltage	VREH	1.1	—	7.0	V		
	RESET "L" input voltage	VREL	0	—	0.3	V		
	RESET "H" input current	IREH	—	—	1.0	μA	VIH=5.5V	
	RESET "L" input current	IREL	-100	-75	-50	μA	VIL=0V	
STB pin	STB "H" input voltage	VSTH	VCC-0.3	—	7.0	V		
	STB "L" input voltage	VSTL	0	—	0.3	V		
	STB "H" input current	ISTH	—	—	3.0	μA	VIH=5.5V	
	STB "L" input current	ISTL	-150	-100	-50	μA	VIL=0V	
HOLD C	CH rapid charge current	ICHQC	-2000	-1000	-500	μA	IPSD=5μA , VCH=0V	*1
	CH stationary charge current	ICHC	-30	-20	-10	μA	VCH=0V	*1
	CH stationary discharge current	ICHHD	10	20	30	μA	VCH=1.5V	*1

## Electrical characteristics (cont.)

(Ta = 25°C, VCC = 3.0V, unless otherwise noted.)

Classification	Parameter	Symbol	Limits			Unit	Test conditions	Note
			Min.	Typ.	Max.			
Double integration	CINT rapid charge current	ICINTC	84	120	156	μA	VCI=1V (CINT stable period)	*1
	CINT reference voltage	VCINT	1.6	1.8	2.0	V	GND criterion	*1
	The first integration current	ICI1	4.06	5.80	7.54	μA	VCINT=1.5V	*1
	The second integration current	ICI2	-3.20	-2.46	-1.27	μA	VCHF=2V , VCHN=0V	*1
	The first integration current stability percentage	ΔICI1	—	—	10	%		*2
	The second integration current stability percentage	ΔICI2	—	—	10	%		*2
	The first and second integration current ratio	ICI12	2.12	2.36	2.60		ICI1   /   ICI2	
AF input condition 1	AF output time(9:1)-1	D(9:1) - 1	11.78	13.40	15.02	msec	Near side9 : Far side1	*3
	AF output time(6:4)-1	D(6:4) - 1	7.77	8.95	10.13	msec	Near side6 : Far side4	*3
	AF output time(3:7)-1	D(3:7) - 1	3.77	4.51	5.25	msec	Near side3 : Far side7	*3
	AF slope -1	ΔAF - 1	6.57	8.89	11.21	msec		*3
	AF linearity-1	LAF - 1	0.9	1.0	1.1			*3
AF input condition 2	AF output time(9:1)-2	D(9:1) - 2	11.78	13.40	15.02	msec	Near side9 : Far side1	*3
	AF output time(6:4)-2	D(6:4) - 2	7.77	8.95	10.13	msec	Near side6 : Far side4	*3
	AF output time(3:7)-2	D(3:7) - 2	3.77	4.51	5.25	msec	Near side3 : Far side7	*3
	AF slope -2	ΔAF - 2	6.57	8.89	11.21	msec		*3
	AF linearity-2	LAF - 2	0.9	1.0	1.1			*3
AF input condition 3	AF output time(9:1)-3	D(9:1) - 3	11.78	13.40	15.02	msec	Near side9 : Far side1	*3
	AF output time(6:4)-3	D(6:4) - 3	7.77	8.95	10.13	msec	Near side6 : Far side4	*3
	AF output time(3:7)-3	D(3:7) - 3	3.77	4.51	5.25	msec	Near side3 : Far side7	*3
	AF slope -3	ΔAF - 3	6.57	8.89	11.21	msec		*3
	AF linearity-3	LAF - 3	0.9	1.0	1.1			*3
AF input condition 1 minus 2	ΔAF output time(9:1)	ΔD(9:1)	—	—	280	μsec	Near side9 : Far side1 (Condition 1-2)	
	ΔAF output time(6:4)	ΔD(6:4)	—	—	280	μsec	Near side6 : Far side4 (Condition 1-2)	
	ΔAF output time(3:7)	ΔD(3:7)	—	—	280	μsec	Near side3 : Far side7 (Condition 1-2)	
Data	SOUT leak current	ISOUTL	—	—	1.0	μA	VIN = 5.5V	
	SOUT saturation voltage	VSOUTS	—	—	0.3	V	IOUT=500μA	
Sensor	Signal light saturation current	ΔINF	3.0	—	—	μA		*4
	Stationary light remove current	IPSD	—	—	30	μA		*4
	Clamp level	ICLAM	-30	—	30	%	Change quantity for Typ. current	

- \*1 : Set up the logic control terminal, correspond to the parameter.
- \*2 : Change ratio between the first integration current and the second integration current at a voltage of CINT that is {CINT reference voltage(VCINT)-0.1V} and 1V.

$$\Delta I_{C1} = \left( 1 - \frac{\text{The first integration current (CINT=1V)}}{\text{The first integration current (CINT=VCINT-0.1V)}} \right) \times 100\%$$

$$\Delta I_{C2} = \left( 1 - \frac{\text{The second integration current (CINT=1V)}}{\text{The second integration current (CINT=VCINT-0.1V)}} \right) \times 100\%$$

- \*3 : Connect the resistance of 120K $\Omega$  instead of PSD and establish current output from PHOTO COUPLER correspond to the parameter. And input the varied resistance ratio. And measure the pulse width of SOUT output at that time, obtain AFslope and AF linearity from the equations below.

Input condition1: I<sub>PSD</sub> (Stationary light current)=0 I<sub>1</sub>+I<sub>2</sub>=100nA

Input condition2: I<sub>PSD</sub> (Stationary light current)=0 I<sub>1</sub>+I<sub>2</sub>=50nA

Input condition3: I<sub>PSD</sub> (Stationary light current)=10 $\mu$ A I<sub>1</sub>+I<sub>2</sub>=100nA

D(9 : 1) ••• The pulse width of SOUT output at input with I<sub>1</sub>:I<sub>2</sub>=9:1

D(6 : 4) ••• The pulse width of SOUT output at input with I<sub>1</sub>:I<sub>2</sub>=6:4

D(3 : 7) ••• The pulse width of SOUT output at input with I<sub>1</sub>:I<sub>2</sub>=3:7

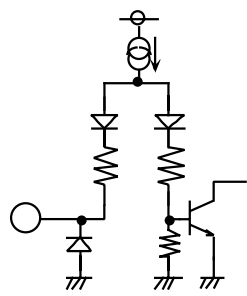
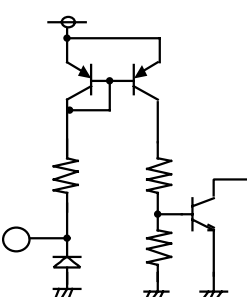
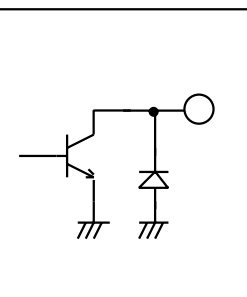
AF slope : DAF = D(9 : 1) - D(7 : 3)

AF linearity : L(AF) = (D(9 : 1) - D(6 : 4)) / (D(6 : 4) - D(7 : 3))

PSD quite resistance : 120K $\Omega$

- \*4 : The input current of one side channel when stationary light remove circuit and I/V transform AMP is not saturated.

## Description of Pin

Pin name	Circuit diagram	Parameter	Limits			Unit	Test conditions and note	
			Min.	Typ.	Max.			
HOLD INT CLALV RESET		"H"input voltage	1.1	—	7.0	V		
		"L"input voltage	0	—	0.3			
		"H"input current	—	—	1.0	μA		VIH=5.5V
		"L"input current	-100	-75	-50			VIL=0V
STB		"H"input voltage	VCC-0.3	—	7.0	V		
		"L"input voltage	0	—	0.3			
		"H"input current	—	—	3.0	μA		VIH=5.5V
		"L"input current	-150	-100	-50			VIL=0V
SOUT		"L"output voltage	—	—	0.3	V	IOL=500μA	
		"H"leak current	—	—	1.0	μA	VIN=5.5V	





(3)CLALV

This terminal sets up clamp level.

As including D/A of 4bit, 16way clamp level setting is possible by inputting clock after reset is canceled(include none clamp).

Set up current value of each bit is on the right table.  
The number of input clock and set up clamp level is as follows.

bit	Set up current (Typ.)
1	0.125 nA
2	0.25 nA
3	0.5 nA
4	1.0 nA

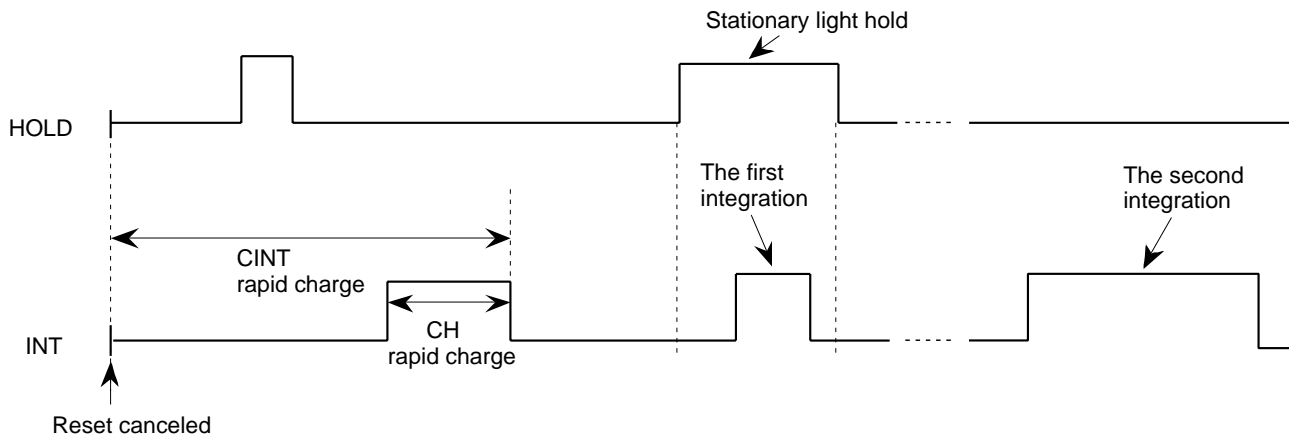
Clock value	Clamp level(Typ.)	Clock value	Clamp level(Typ.)
0	None clamp	12	1.500 nA
1	0.125 nA	13	1.625 nA
2	0.250 nA	14	1.750 nA
3	0.375 nA	15	1.875 nA
4	0.500 nA	16	None clamp
5	0.625 nA	17	0.125 nA
6	0.750 nA	18	0.250 nA
7	0.875 nA	19	0.375 nA
8	1.000 nA	20	0.500 nA
9	1.125 nA	:	:
10	1.250 nA	:	:
11	1.375 nA	:	:

Clamp level is established with fall edge of input clock.  
It repeats the same value after 16 clock.

(4) HOLD INT

These terminals implement the following controls by inputting HIGH/LOW.

- a. CINT rapid charge ON , OFF
- b. CHrapid charge ON , OFF
- c. Stationary light hold ON , OFF
- d. The first integration ON , OFF
- e. The second integration ON , OFF



- a. CINT rapid charge  
After reset is canceled, the capacity of CINT is charged rapidly until INT terminal first falls.
- b. CH rapid charge  
After reset is canceled, the capacity of CH is charged rapidly until INT terminal first rises and falls.
- c. Stationary light hold  
After reset is canceled, holds the stationary light while HOLD terminal is HIGH.
- d. The first integration  
After reset is canceled, as HOLD terminal is HIGH and INT terminal is HIGH, the first integration is implemented while INT terminal is HIGH. Therefore, the first integration must be finished (INT terminal from HIGH to LOW) until stationary light hold will be completed (HOLD terminal from HIGH to LOW)
- e. The second integration  
After reset is canceled, the second integration is implemented as HOLD terminal is LOW and INT terminal is HIGH. And, the second integration is completed by exceeding judgment level of CINT terminal although INT terminal is HIGH.

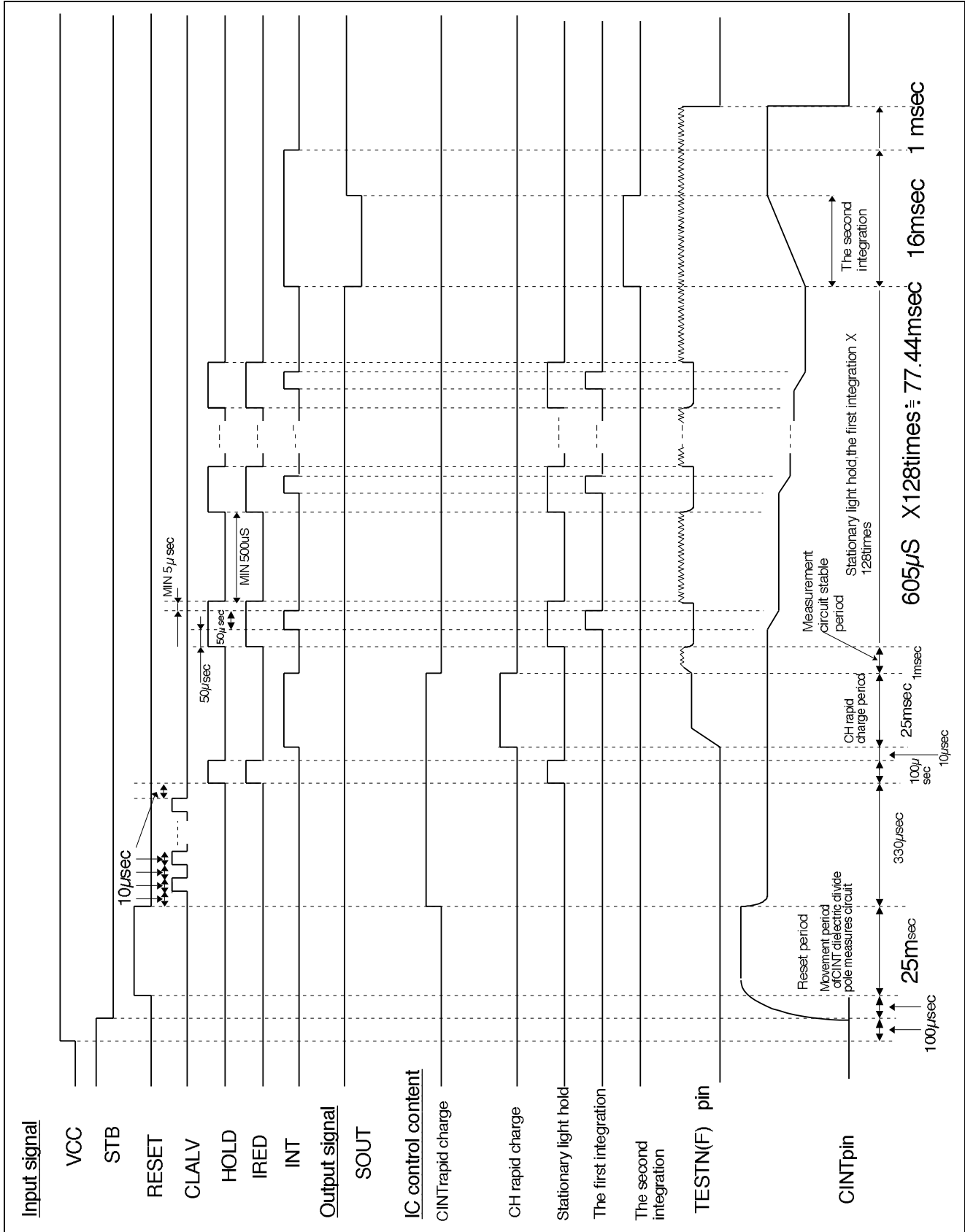
(5)SOUT

When the second integration starts, This terminal becomes from HIGH to LOW.

If CINT terminal exceeds judge level or INT terminal becomes from HIGH to LOW, this terminal becomes from LOW to HIGH.

(notice)As the signal from microcomputer, the signal that controls IRED ON/OFF is required except for above mentioned control signals. But applying the timing of HOLD is available.

Sequential Time Chart Example

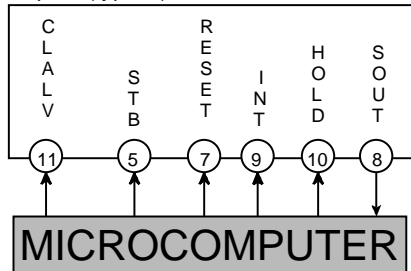


## Mask Option

(1) The second integration current value can be doubled. (2.5μ → 5.0μA)

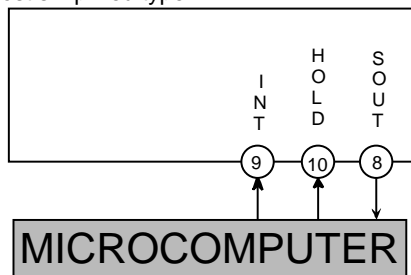
(2) Control terminal variation

① Full spec (typical)



This type uses CLALV,STB,RESET,INT,HOLD,SOUT terminal as I/F terminal to the microcomputer. This is the typical type at M52957AFP.

② Most simplified type



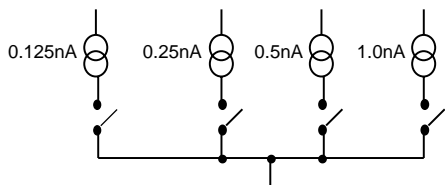
This type does not connect CLALV,STB,RESET terminals to the microcomputer. When above mentioned terminals are not connected to the microcomputer without changing mask,connect each terminal to the ground. In this case,clamp level becomes 0 and standby function is lost. Power on reset in IC is used as reset.

③ Explanation of the terminal that can be simplified.

(a)CLALV ••••• In the typical type,16way clamp levels can be set by the external control,but also the terminal can be simplified by mask option as follows.

(I) Clamp level fixation ••••• Selects 1 point from 16 steps of clamp level and fixes it.

(II) Clamp level 2 step changeover •••••Selects 2 points from clamp level and switches it by changing CLALV terminal HIGH/LOW. However,as selecting 2 points,there is a following constraint.



Fixes 3 parts of 4 switches correspond to each bit in figure to ON or OFF,controls another part by CLALV terminal .

(b)STB ••••• When no standby function required such as VCC is switched ON/OFF, STB terminal can be eliminated.

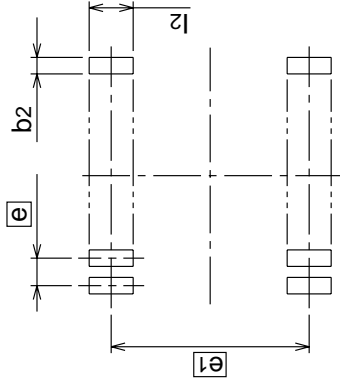
(c)RESET ••••• Since IC include power on reset circuit, RESET terminal can be eliminated, As merit of controlling RESET terminal from outside, distance detection time can be shortened because there is no need to switch VCC to STB terminal ON/OFF at consecutive distance detection.

Package Dimensions

**16P2E-A**

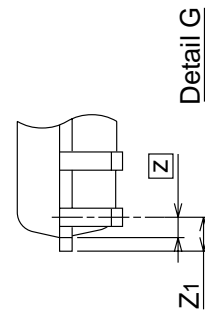
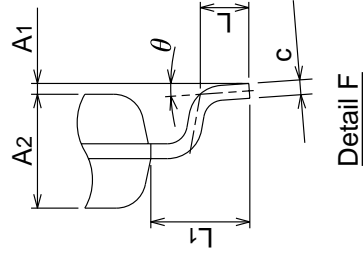
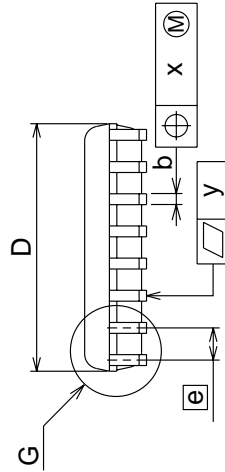
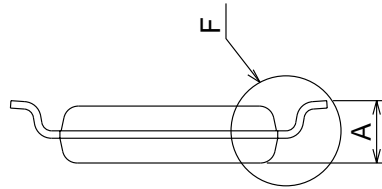
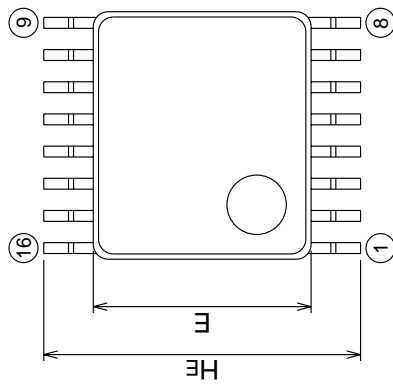
EIAJ Package Code SSOP16-P-225-0.65	JEDEC Code —	Weight(g) 0.06	Lead Material Alloy 42
--	-----------------	-------------------	---------------------------

**Plastic 16pin 225mil SSOP**



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.45
A1	0	0.1	0.2
A2	—	1.15	—
b	0.17	0.22	0.32
c	0.13	0.15	0.2
D	4.9	5.0	5.1
E	4.3	4.4	4.5
e	—	0.65	—
HE	6.2	6.4	6.6
L	0.3	0.5	0.7
L1	—	1.0	—
Z	—	0.225	—
Z1	—	—	0.375
x	—	—	0.13
y	—	—	0.1
$\theta$	0°	—	10°
b2	—	0.35	—
e1	—	5.8	—
l2	1.0	—	—



## RENESAS Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

---

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.  
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
  2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
  3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.  
The information described here may contain technical inaccuracies or typographical errors.  
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.  
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
  4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
  5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
  6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
  7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.  
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
  8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.
- 



### RENESAS SALES OFFICES

<http://www.renesas.com>

**Renesas Technology America, Inc.**  
450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited.**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom  
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

**Renesas Technology Europe GmbH**  
Dornacher Str. 3, D-85622 Feldkirchen, Germany  
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

**Renesas Technology Hong Kong Ltd.**  
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2375-6836

**Renesas Technology Taiwan Co., Ltd.**  
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

**Renesas Technology (Shanghai) Co., Ltd.**  
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China  
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

**Renesas Technology Singapore Pte. Ltd.**  
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001