ZARLINK
SEMICONDUCTOR

MA2901

RADIATION HARD 4-BIT MICROPROCESSOR SLICE

The MA2901 is an industry standard 4-bit microprocessor slice It provides a set of ALU functions selected by microcode data applied to the inputs. The device is cascadable to handle any word length. It can be used as a building block in the construction of microcomputers and controllers tailored to meet specialised applications.

Dual Address Architecture
Machine cycles are saved by simultaneous, independent access to two working registers.

ALU has Eight Functions
Operations performed are addition, two subtractions and five logic functions on two source operands.

Four State Flags
Zero, negative, carry and overflow.

Left / Right Shift is Independent of ALU
Only one cycle taken for add and shift operations.

Expandable
Any number of MA2901 units can be connected together to achieve longer word lengths.

Micro Programmable
Three groups, each of three bits, for ALU function, source operand and destination control.

FEATURES

■ Fully Compatible with Industry Standard 2901

■ CMOS SOS Technology

■ High SEU Immunity and Latch-up Free

■ High Speed

■ Low Power

OPERATION

A detailed block diagram of the microprogrammable microprocessor structure is shown in figure 1. The circuit is a four-bit slice, cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the figure 1 are the 16-word by 4-bit 2-port RAM and the high speed ALU.

Data from any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A-address field input. Likewise, data from any of the 16 words of the RAM as defined by the B-address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A-select field and B-select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B-address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

The ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.
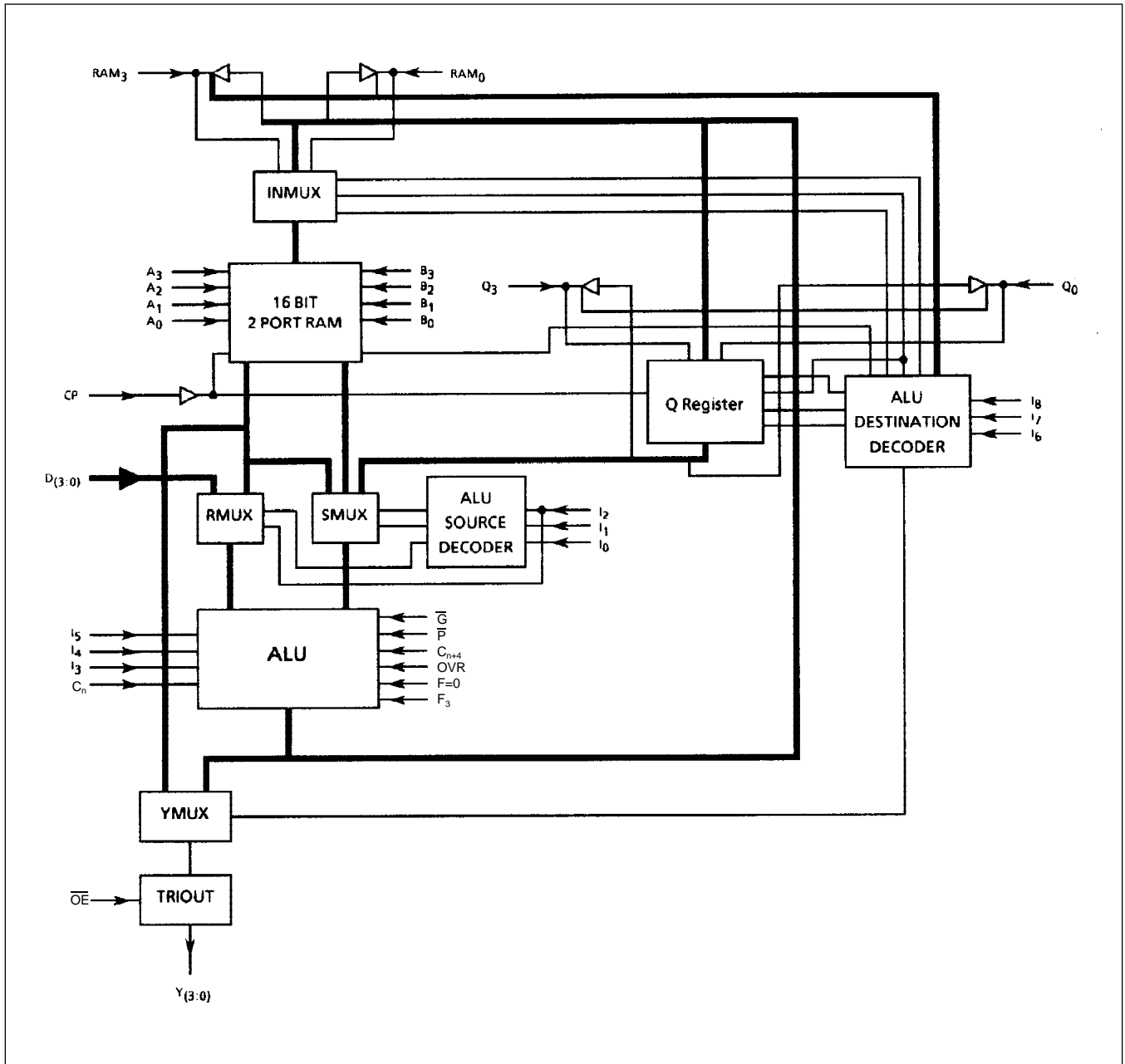
Figure 1: Block Diagram

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent the AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant sourced operand pairs for the ALU. The MA2901 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the eight source operand combinations are as shown in figure 2. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Figure 3. The octal code is also shown for reference. The normal technique for cascading ALU of several devices is in a look-ahead carry mode. Carry generate, GN, and carry propagate, PN, are outputs of the device for use with a carry-look-ahead-generator. A carry-out $Cn + 4$, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (Cn) and carry-out (Cn+4) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3, F=0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is when $Cn + 3$ and $Cn + 4$ are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstruction inputs. These combinations are shown in figure 4.

The four-bit data output field (Y) features three-state outputs and can be directly bus organised. An output control (OEN) is used to enable the three-state outputs. When OEN is HIGH, the Y outputs are in the high impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (x 2) or shifted down one position (÷ 2). The shifter has two ports; labeled RAM_0 and RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer.

Microcode				ALU Source Operands	
I_2	I_1	I_0	Octal Code	R	S
L	L	L	0	A	C
L	L	H	1	A	B
L	H	L	2	0	Q
L	H	H	3	0	B
H	L	L	4	0	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	0

Figure 2: ALU Source Operand Control

Microcode				ALU Function	Symbol
I_5	I_4	I_3	Octal Code		
L	L	L	0	R plus S	R + S
L	L	H	1	S minus R	S - R
L	H	L	2	R minus S	R - S
L	H	H	3	R OR S	R S
H	L	L	4	RN AND S	RN S
H	L	H	5	R AND S	R S
H	H	L	6	R EX-OR S	R S
H	H	H	7	R EX-NOR S	RN SN

+ = plus; - = minus; $\lor$ = OR;   = AND;   = EX-OR

Figure 2: ALU Function Control

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In the shift up mode, the RAM$_3$ buffer is enabled and the RAM$_0$ multiplexer input is enabled. Likewise, in the shift down mode, the RAM$_0$ buffer and RAM$_3$ input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. The shifter is controlled from the I$_6$, I$_7$ and I$_8$ microinstruction inputs as defined in Figure 4.

Similarly, the Q register is driven from a 3-input multiplexer. In the non-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q$_0$ and the other is Q$_3$. The operation of these two ports is similar to the RAM shifter and is also controlled from I$_6$, I$_7$ and I$_8$ as shown in Figure 4.

The clock input shown in Figure 1 controls the RAM, the Q resister and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled new data will be written into the RAM file (word) defined by the B address field when the clock input is LOW.

SOURCE OPERANDS & ALU FUNCTION

Any one of eight source operand pairs can be selected by instruction inputs Io, I$_1$ and I$_2$ for use by the ALU; instruction inputs I$_3$, I$_4$, and I$_5$ then control function selection for the ALU - five logic and three arithmetic functions. In the arithmetic mode, the carry input (Cn) also affects the ALU functions; the carry input has no effect on the 'F' result in the logic mode. These control parameters (I$_6$ - I$_0$ and Cn) are summarised in Figure 5 to completely define the ALU/source operand functions.

The ALU functions can also be examined on a task basis: that is, add, subtract, AND, OR, and so on. Again, in the arithmetic mode, the carry input still affects the result, whereas in the logic mode it will not. Figures 6 and 7, respectively, define the various logic and arithmetic functions of the ALU; both carry states (Cn = 0 / Cn = 1) are defined in the function matrices.

Microcode				RAM Function		Q-Reg Function		Y Output	RAM Shifter		Q Shifter	
I$_8$	I$_7$	I$_6$	Octal Code	Shift	Load	Shift	Load		RAM$_0$	RAM$_3$	Q$_0$	Q$_3$
L	L	L	0	X	None	None	F Q	F	X	X	X	X
L	L	H	1	X	None	X	None	F	X	X	X	X
L	H	L	2	None	F B	X	None	A	X	X	X	X
L	H	H	3	None	F B	X	None	F	X	X	X	X
H	L	L	4	Down	F/2 B	Q/2 Q	F	-	F0	IN$_3$	Q$_0$	IN$_3$
H	L	H	5	Down	F/2 B	X	None	F	F$_0$	IN$_3$	Q$_0$	X
H	H	L	6	Up	2F B	Up	2Q Q	F	IN$_0$	F$_3$	IN$_3$	Q$_3$
H	H	H	7	Up	2F B	X	None	F	IN$_0$	F$_3$	X	Q$_3$

X = Don't Care. Electrically, the shift pin is a TTL input internally connected to a TRI-STATE output which is in the high-impedance state.
B = Register addressed by 8 inputs. Up is towards MSB, Down is towards LSB.

Figure 4: ALU Destination Control

	I$_{2,1,0}$Octal	0	1	2	3	4	5	6	7
Octal I$_{5,4,3}$	ALU Source /ALU Function	A,Q	A,B	0,Q	0,B	0,A	D,A	D,Q	D,0
0	C$_n$=L R plus S	A+Q	A+B	Q	B	A	D + A	D + Q	D
	C$_n$=H	A+Q+1	A+B+1	Q +1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	C$_n$=L S minus R	Q-A-1	B-A-1	Q -1	B - 1	A - 1	A - D1	Q - D - 1	-D - 1
	C$_n$=H	Q-A	B-A	Q	B	A	A - D	Q - D	- D
2	C$_n$=L R minus S	A-Q-1	A-B-1	-Q-1	- B - 1	- A - 1	D - A -1	D - Q - 1	D - 1
	C$_n$=H	A-Q	A-B	- Q	- B	- A	D - A	D - Q	D
3	R or S	A $\vee$ Q	A $\vee$ B	Q	B	A	D $\vee$ A	D $\vee$ Q	D
4	R and S	A Q	A B	0	0	0	D A	D Q	0
5	RN and S	AN Q	AN B	Q	B	A	DN A	DN Q	0
6	R EX-OR S	A Q	A B	Q	B	A	D A	D Q	D
7	R EX NOR S	AN QN	AN BN	Q	B	A	DN AN	DN QN	DN

+ = plus; - = minus; $\vee$ = OR; = AND; = EX-OR

Figure 5: Source Operand and ALU Function Matrix

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Octal $I_{5,4,3}/I_{2,1,0}$	Group	Function
40		A Q
41	AND	A B
45		D A
46		D Q
30		A $\lor$ Q
31	OR	A $\lor$ B
35		D $\lor$ A
36		D $\lor$ Q
60		A Q
61	EX-OR	A B
65		D A
66		D Q
70		AN QN
71	EX-NOR	AN BN
75		DN AN
76		DN QN
72		$\underline{Q}$
73	INVERT	$\underline{B}$
74		$\underline{A}$
77		$\underline{D}$
62		Q
63	PASS	B
64		A
67		D
32		Q
33	PASS	B
34		A
37		D
40		0
43	'ZERO'	0
44		0
47		0
50		AN Q
51	AND	AN B
55		DN A
56		DN Q

+ = plus; - = minus; $\lor$ = OR;   = AND;   = EX-OR

Figure 6: ALU Logic Mode Functions (C_n Irrelevant)

Octal $I_{5,4,3}/I_{2,1,0}$	Cn=0(Low)		Cn = 1 (High)	
	Group	Function	Group	Function
00		A + Q		A + Q +1
01	ADD	A + B	ADD	A + B +1
05		D + A	plus one	D + A +1
06		D + Q		D + Q + 1
02		Q		Q +1
03	PASS	B	Increment	B + 1
04		A		A + 1
07		D		D + 1
12		Q - 1		Q
13	Decrement	B - 1	PASS	B
14		A - 1		A
27		D - 1		D
22		- Q - 1		- Q
23	1s comp	- B - 1	2s comp	- B
24		- A - 1	(negate)	- A
17		- D - 1		- D
10		Q - A -1		Q - A
11		B - A-1		B - A
15	SUBTRACT	A - D-1		A - D
16	(1s comp)	Q - D-1	SUBTRACT	Q - D
20		A - Q-1	(2s comp)	A - Q
21		A - B-1		A - B
25		D - A-1		D - A
26		D - Q-1		D - Q

Figure 7: ALU Arithmetic Mode Functions

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PIN DESCRIPTION

Name	I/O	Description
A_{0-3}	I	The four address inputs to the register stack used to select one register whose contents are displayed through the A port
B_{0-3}	I	The four address inputs to the register stack used to select one register whose contents are displayed through the B port and into which new data can be written when the clock goes LOW
I_{0-8}	I	The nine instruction control lines. Used to determine what data sources will be applied to the ALU($I_{0,1,2}$), what function the ALU will perform ($I_{3,4,5}$), and what data is to be deposited in the Q-register or the register stack ($I_{6,7,8}$)
Q_3 RAM_3	I/O	The shift line at the MSB of the Q-register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the device. When the destination code on $I_{6,7,8}$ indicates an up shift (Octal 6 or 7) the three state outputs are enabled and the MSB of the Q-register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three state outputs are electrically OFF (high impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q-register (Octal 4) and RAM (Octal 4 or 5)
Q_0 RAM_0	I/O	Shift lines like Q_3 and RAM_3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q-register and ALU data.
D_{0-3}	I	Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the device D_0 is the LSB
Y_{0-3}	O	The four data outputs. These are three-state output lines. When they are enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code $I_{6,7,8}$.
OEN	I	Output enable. When OEN is HIGH, the Y outputs are OFF; when OEN is LOW, the Y outputs are active (HIGH or LOW)
GN,PN	O	The carry generate and propagate outputs of the internal ALU. These signals are used with the MA2901 for carry lookahead.
OVR	O	Overflow. This pin is logically the Exclusive OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit
F = 0	O	This is an open collector output which goes HIGH(OFF) if the data on the four ALU outputs F_{0-3} are all LOW. In positive logic, it indicates that the result of the ALU operation is zero
F_3	O	The most significant ALU output bit.
C_n	I	The carry-in to the internal ALU.
$C_n + 4$	O	The carry-out of the ALU internal ALU.
CP	I	The clock input. The Q-register and register stack outputs change on the clock LOW - to HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

Figure 8: Pin Description

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DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Figure 9: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Subgroup	Definition
1	Static characteristics specified in Figure 11 at +25°C
2	Static characteristics specified in Figure 11 at +125°C
3	Static characteristics specified in Figure 11 at -55°C
7	Functional characteristics at +25°C
8A	Functional characteristics at +125°C
8B	Functional characteristics at -55°C
9	Switching characteristics specified in Figures 12, 13 and 14 at +25°C
10	Switching characteristics specified in Figures 12, 13 and 14 at +125°C
11	Switching characteristics specified in Figures 12, 13 and 14 at -55°C

Figure 10: Definition of Subgroups

Symbol	Parameter	Conditions	Total dose radiation not exceeding 3×10^5 Rad(Si)			Units
			Min	Typ	Max	
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	-	2.4	-	-	V
V_{IL}	Input Low Voltage	-	-	-	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -6mA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 10mA	-	-	0.4	V
I_{IN}	Input Leakage Current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	±10	µA
I_{OZ}	Output Leakage Current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	±50	µA
I_{DD}	Power Supply Current	Static, V_{DD} = 5.5V	-	0.1	10	mA

V_{DD} = 5V±10%, over full operating temperature range.
Mil-Std-883, method 5005, subgroups 1, 2, 3
Notes: 1. Guaranteed but not measured at -55°C

Figure 11: Operating Electrical Characteristics

MA2901

AC ELECTRICAL CHARACTERISTICS

Read-Modify-Write Cycle (from selection of A,B registers to end of a cycle	40ns
Maximum Clock Frequency to shift Q(50% duty cycle, I = 432 or 632)	25MHz
Minimum Clock LOW time	20ns
Minimum Clock HIGH time	20ns
Minimum Clock Period	40ns

Note: 1. These timings are applied during functional tests and are not routinely measured.

Figure 12: Cycle Time and Clock Characteristics

From Input	To Output							
	Y	F_3	$C_n + 4$	G,P	F = 0	OVR	RAM_0 RAM_3	Q_0 Q_3
A,B Address	65	55	60	55	70	65	65	-
D	55	40	50	50	65	55	55	-
C_n	60	40	35	-	55	35	50	-
$I_{0,1,2}$	70	50	55	55	70	55	65	-
$I_{3,4,5}$	60	45	50	45	65	50	65	-
$I_{6,7,8}$	45	-	-	-	-	-	30	30
A Bypass ALU(I=2xx)	45	-	-	-	-	-	-	-
Clock	55	50	55	50	50	55	55	35

Note: All timings in ns

Figure 13: Combinational Propagation Delays

Input	CP: Set-up Time Before H L	Hold Time After H L	Set-up Time Before L H	Hold Time After L H
A,B Source Address	25	5	30	-
B Destination Address	25	No change	No change	5
D	-	-	40	0
C_n	-	-	40	0
$I_{0,1,2}$	-	-	45	0
$I_{3,4,5}$	-	-	45	0
$I_{6,7,8}$	10	No change	No change	10
$RAM_{0,3}, Q_{0,3}$	-	-	15	10

MIL-STD-883, method 5005, subgroups 9, 10, 11

Note: 1. V_{DD} = 5V ±10%, over full operational temperature range

2. CL = 50 pF

Figure 14: Set-up and Hold Times Relative to Clock (CP) Input

OUTLINES AND PIN ASSIGNMENTS

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	51.31	-	-	2.020
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG405

Pin	Signal		Pin	Signal
1	A3		40	OE
2	A2		39	Y3
3	A1		38	Y2
4	A0		37	Y1
5	I6		36	Y0
6	I8		35	P
7	I7		34	OVR
8	RAM3		33	Cn+4
9	RAM0		32	G
10	VDD		31	F3
11	F = 0		30	VSS
12	I0		29	Cn
13	I1		28	I4
14	I2		27	I5
15	CP		26	I3
16	Q3		25	D0
17	B0		24	D1
18	B1		23	D2
19	B2		22	D3
20	B3		21	Q0

Top View
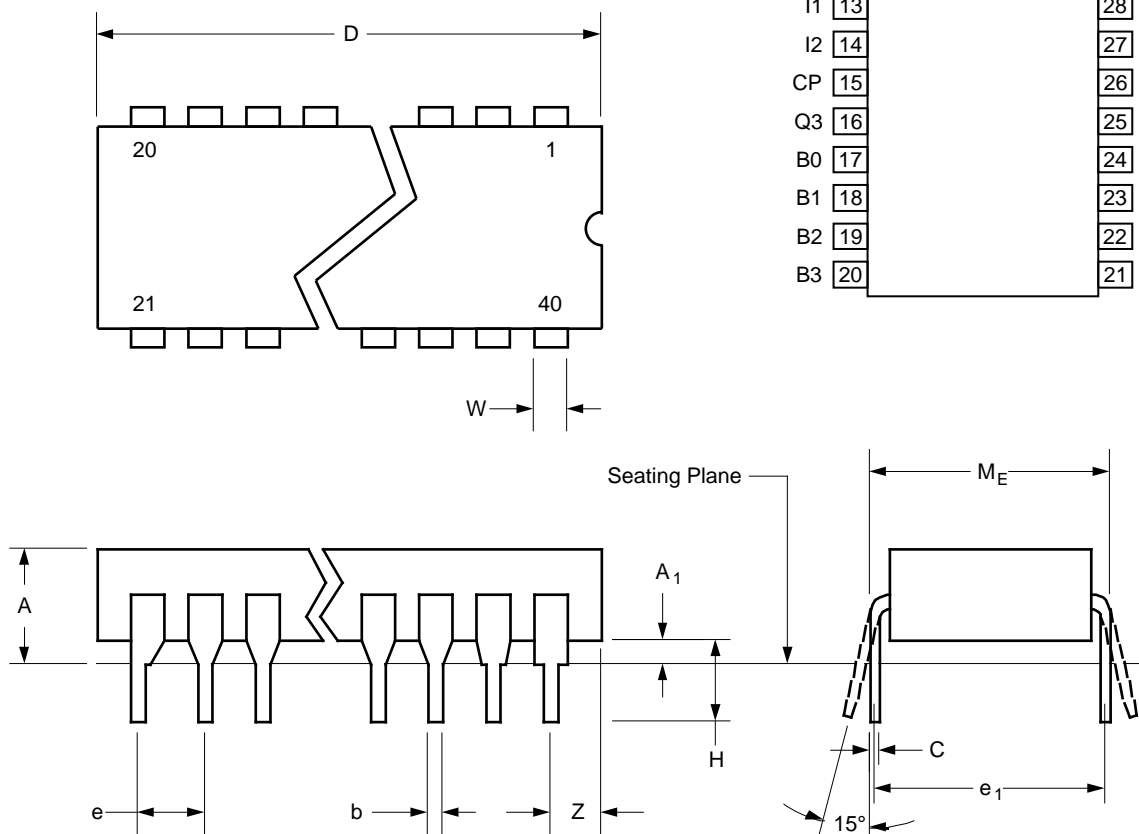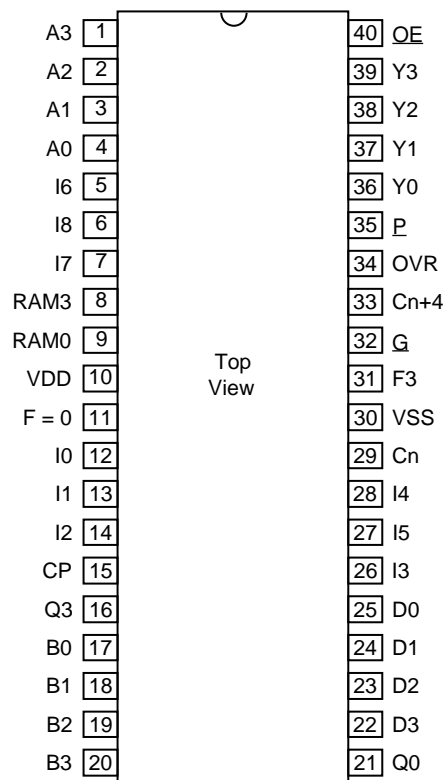
Figure 15: 40-Lead Ceramic DIL (Solder Seal) - Package Style C

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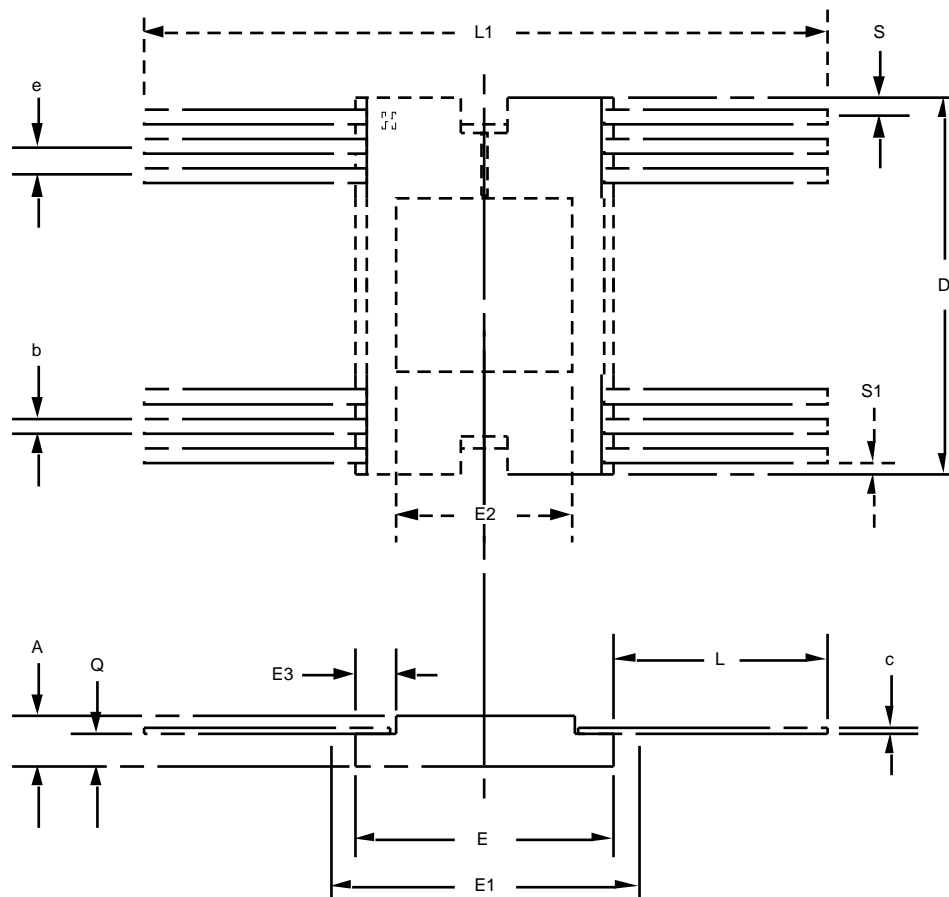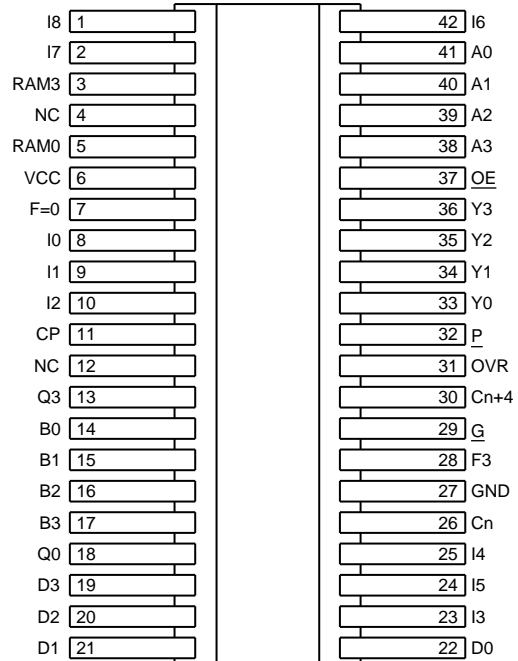| Ref	Millimetres		Inches	
	Min.	Max.	Min.	Max.
A	1.75	2.49	0.070	0.098
b	0.43	0.53	0.017	0.023
c	0.15	0.25	0.006	0.010
D	26.67	27.69	1.050	1.080
E	15.75	16.76	0.620	0.660
E1	-	17.27	-	0.630
E2	13.21	-	0.520	-
E3	0.76	-	0.030	-
e	1.14	1.40	0.045	0.055
L	7.87	9.40	0.310	0.370
L1	32.51	34.54	1.250	1.360
Q	0.76	1.52	0.030	0.060
S	-	1.14	-	0.045
S1	0.13	-	0.005	-

XG136

Figure 16: 42-Lead Flatpack (Solder Seal)

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 method 1019 Ionizing Radiation (total dose) test.
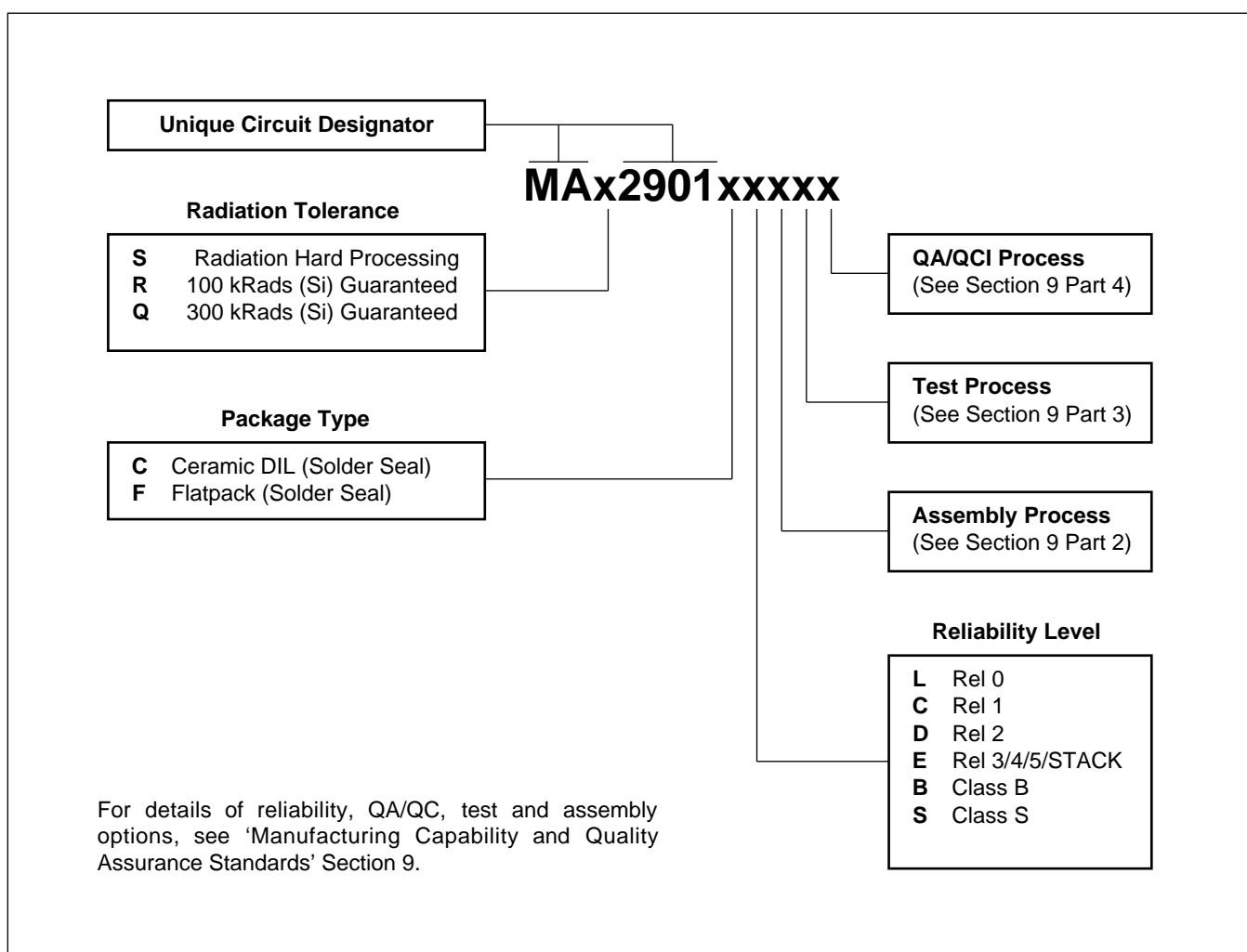
Total Dose (Function to specification)*	3×10^5 Rad(Si)
Transient Upset (Stored data loss)	5×10^{10} Rad(Si)/sec
Transient Upset (Survivability)	$>1 \times 10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1 \times 10^{15}$ n/cm^2
Single Event Upset**	1×10^{-10} Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 17: Radiation Hardness Parameters

ORDERING INFORMATION

Unique Circuit Designator

MAx2901xxxxx

Radiation Tolerance

S	Radiation Hard Processing
R	100 kRads (Si) Guaranteed
Q	300 kRads (Si) Guaranteed

Package Type

C	Ceramic DIL (Solder Seal)
F	Flatpack (Solder Seal)

QA/QCI Process
(See Section 9 Part 4)

Test Process
(See Section 9 Part 3)

Assembly Process
(See Section 9 Part 2)

Reliability Level

L	Rel 0
C	Rel 1
D	Rel 2
E	Rel 3/4/5/STACK
B	Class B
S	Class S

For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

MA2901

GEC PLESSEY
SEMICONDUCTORS

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