silicon systems®
A TDK Group Company

SSI 78P7220
DS-3 Line Receiver

Preliminary Data

November 1991

DESCRIPTION

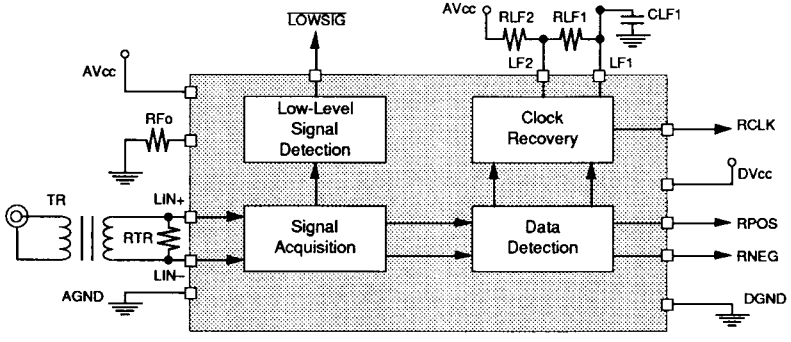
The SSI 78P7220 is a clock and data recovery device intended for DS-3 (44.736 Mbit/s) applications. The receiver has a very wide dynamic range and is designed to accept B3ZS-encoded Alternate-Mark Inversion (AMI) inputs; it provides clock, positive data, negative data, and low-level signal detector logical outputs. The 78P7220 includes a fixed line equalizer to overcome intersymbol interference caused by long line lengths. The SSI 78P7220 requires a 5-volt supply and is available in 16-pin DIP and surface mount packages.

FEATURES

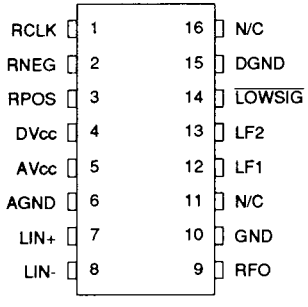
- **Receive interface for DS-3 (44.736 Mbit/s) applications**
- **Unique clock recovery circuit, requires no crystals, inductors or external clocks**
- **Standard unipolar CMOS level logic outputs**
- **Compliant with Bellcore TR-TSY-000499, ANSI T1.102-1987, CCITT G.703**
- **Low-level input signal indication**
- **Available in DIP or surface mount packages**
- **Industrial temperature range -40 to + 85°C**

5

BLOCK DIAGRAM



PIN DIAGRAM



16-Pin DIP, SON

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 78P7220 is intended to be used as a DS-3 Line Receiver to perform the functions of receiving Pulse Code Modulated signals in an alternate mark inversion format. It accepts encoded line data and provides separated and synchronized data and clock outputs.

The receiver input is normally transformer-coupled to the source of encoded alternate polarity pulses. The signal first enters a line equalizer which is designed to overcome the intersymbol interference caused by long line length. The variable gain amplifier is used to adjust the signals applied to the voltage comparators to a relatively constant peak amplitude over the range of expected input levels. This is accomplished by means of the peak detector and AGC amplifier wherein the amplified signal peaks are compared with a fixed reference voltage, and the filtered difference applied to the variable gain stage which cause the signal peaks to nearly equal the reference value.

The amplified positive and negative input data pulses are detected by high speed voltage comparators. The detection threshold is a fixed percentage of the peak value which is applied as the comparator reference. In this way, even though the input signal amplitude may fall below the minimum value which can be regulated by the variable gain circuits, the proper detection threshold is maintained.

Should the input signal falls below the minimum value, this condition is detected and indicated at the $\overline{\text{LOWSIG}}$ output. A time delay is provided before this output is active so that transient interruptions do not needlessly cause the indication.

Outputs of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase locked loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator.

This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high-precision and/or adjustable oscillators or tuned circuits. A single external resistor is used to establish the oscillator center frequency. The response characteristics for the phase locked loop is established by external filter components.

The phase locked reference oscillator is employed to strobe the detected data into output latches and is also available as an output for externally synchronizing the data.

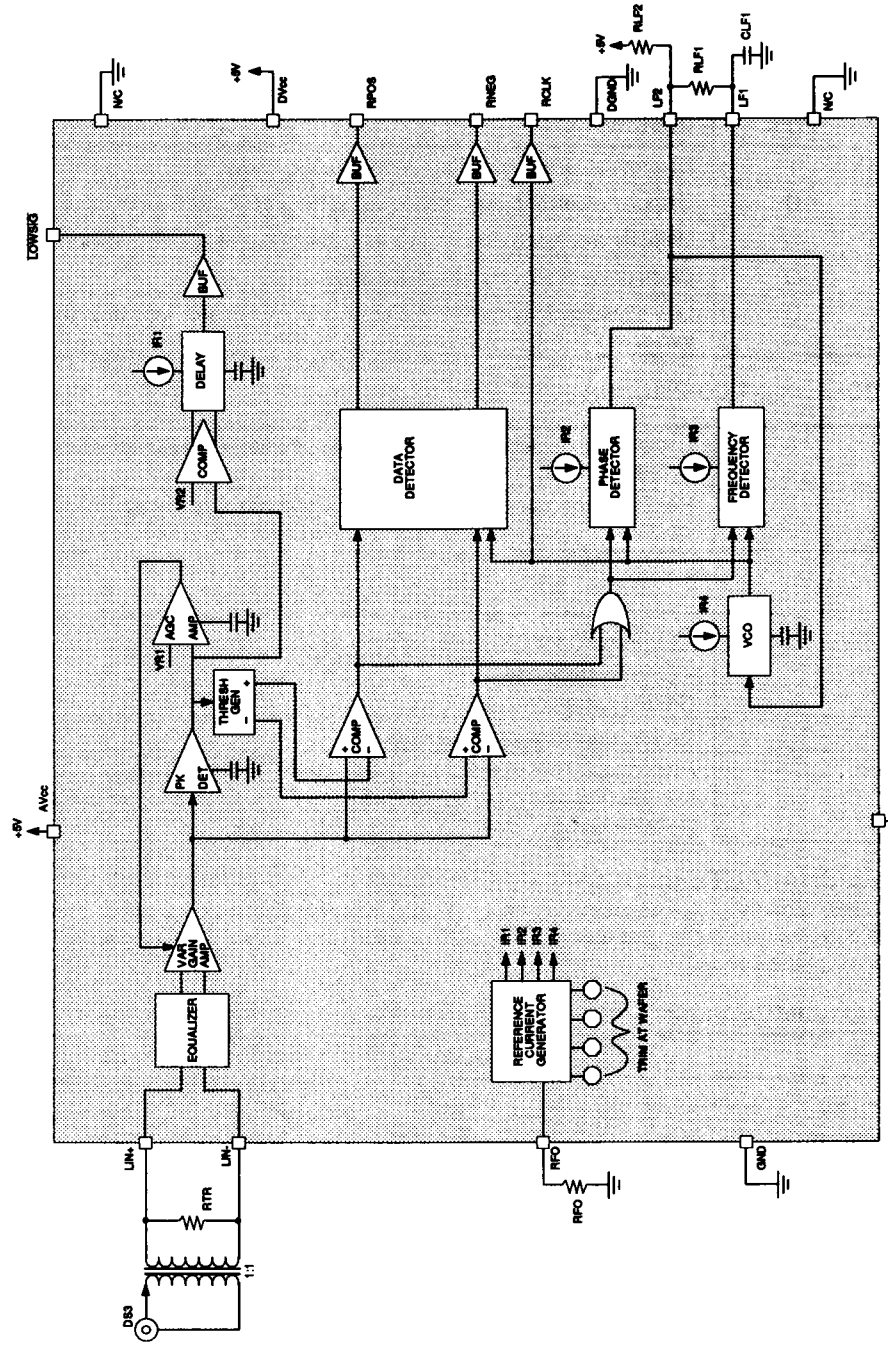


FIGURE 1: Functional Diagram

5

PIN DESCRIPTION

RECEIVER

NAME	TYPE	DESCRIPTION
LIN+, LIN-	I	Differential inputs, transformer-coupled from line.
RPOS	O	Unipolar receiver output, active as result of positive pulse at inputs.
RNEG	O	Unipolar receiver output, active as result of negative pulse at inputs.
RCLK	O	Clock pulses recovered from line data.
$\overline{\text{LOWSIG}}$	O	Low signal logic output indicating that input signal is less than threshold value.

EXTERNAL COMPONENT CONNECTION

RFO	I	Resistor connected to AGND to provide center frequency of voltage controlled oscillator.
LF1, LF2	-	Resistor-capacitor loop filter network to establish bandwidth of phase locked loop.

POWER

AVcc	-	5V power supply for analog circuits.
DVcc	-	5V power supply for logic outputs.
AGND	-	Ground return for analog circuits.
DGND	-	Ground return for logic outputs.
NC	-	No connect. These pins are not connected to the chip. They should be tied to the appropriate ground pin (see Figure 1) to minimize pin-to-pin coupling capacitance.

ELECTRICAL CHARACTERISTICS

(T_A = -40°C to 85°C, Vcc = 5V ±5%, unless otherwise noted.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value. Operation above absolute maximum ratings may permanently damage the device.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive 5.0V supply: AVcc, DVcc	6.0	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Ambient Operating Temperature, T_A	-40 to +85	°C
Pin Ratings: LIN+, LIN-, RFO, LF2, LF1	-0.3 to Vcc +0.3	V
Pin Ratings: RPOS, RNEG, RCLK, $\overline{\text{LOWSIG}}$	-0.3 to Vcc +0.3	V
	or +12	mA

SUPPLY CURRENTS AND POWER

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	Supply Current	Outputs load of 15 pF, normal operation	46	75	89	mA
P	Power Dissipation	Output load of 15 pF, TA = 85°C			0.47	W

EXTERNAL COMPONENTS (Refer to Figure 1 for location of components.)

RFO	Loop center freq. resistor	1% tolerance		5.25		kΩ
RLF1	Loop filter resistor	1% tolerance		6.04		kΩ
RLF2	Loop filter resistor	5% tolerance		100		kΩ
CLF1	Loop filter capacitor	5% tolerance		0.22		µF
TR	Receive line transformer			TBD		
RTR	Receive termination resistor	1% tolerance		75		Ω

DIGITAL OUTPUTS

(CMOS-compatible pins: $\overline{\text{LOWSIG}}$, RPOS, RNEG, RCLK.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value.

VOL	Output low voltage	IOL = 0.1 mA		.2	1.0	V
VOH	Output high voltage	IOH = -0.1 mA	4.0	4.7		V

RECEIVER

All of the measurements for the receiver are made with the following conditions unless otherwise stated:

1. The input signal is transformer coupled.
2. RFO = 5.25 kΩ
3. The circuit is connected as in Figure 1.
4. The maximum cable length (type 728A, RG59B, or equivalent) is 450 feet from DSX3.

VIN	Input signal voltage	Input AC-Coupled	±0.045		±1.20	Vpk
RIN	Input Resistance	Input at chip's common mode voltage (4.4V)	15	20	30	kΩ
VDTH	Receive data detection threshold	Relative to peak amplitude for 22.37 MHz sinusoidal input		50		%
VLOW	Receive data low signal threshold	Relative to peak amplitude for 22.37 MHz sinusoidal input	±60		±85	mV

5

RECEIVER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VLOWT	Receive data low signal delay	Sinusoidal input at 1V and 22.37 MHz after signal removal		900		ns
TRCF	Receive clock period			22.35		ns
TRC	Receive clock pulse width			12.75		ns
TRCPT	Receive clock positive transition time	C_L = 15 pF		4.5	6	ns
TRCNT	Receive clock negative transition time	C_L = 15 pF		4.5	6	ns
TRDP TRDN	Positive or negative receive data pulse width			25.48		ns
TRDPS TRDNS	Receive data set-up time		5.0	11.18	13.7	ns
TRDPH TRDNH	Receive data hold time		5.0	11.18	13.7	ns
	Receive input jitter tolerance	sine, 22.3 kHz	±3.35			ns
	high frequency	to 300 kHz	0.3			UIpp
	Receive input jitter tolerance	sine, 10 Hz to 2.3 kHz	±55.88			ns
	low frequency		5.0			UIpp
KD	Clock Recovery Phase Detector Gain	All 1's data pattern KD = .418/RFO	72	80	88	µA/Rad
KO	Clock Recovery Phase Locked Oscillator Gain		12	14.5	17	Mrad/ sec. -Volt

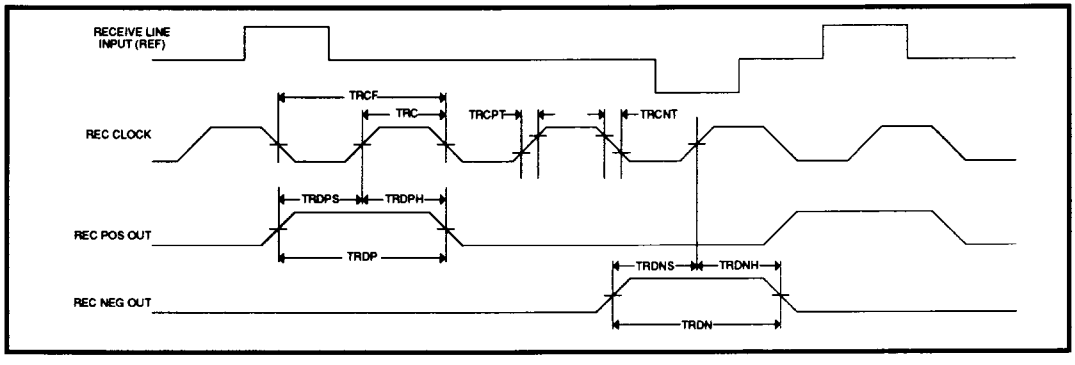
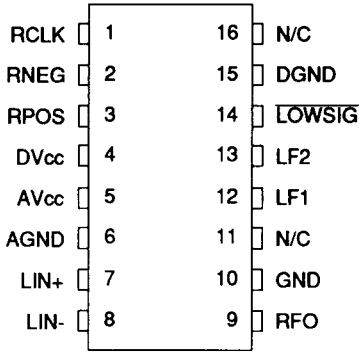


FIGURE 2: Receive Waveforms

PACKAGE PIN DESIGNATIONS

(Top View)



16-Pin DIP, SON

5

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 78P7220, DS-3 Line Receiver		
Standard width 16-pin Plastic DIP	78P7220-IP	78P7220-IP
Narrow width (150-mil) small outline	78P7220-IN	78P7220-IN

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX (714) 573-6914

