DATA SHEET

NEC ELECTRON DEVICE

MOS INTEGRATED CIRCUIT

μPD3571

5 000 BIT CCD LINEAR IMAGE SENSOR

The μPD3571 is a 5 000 bit linear image sensor that converts light to voltage. It consists of a 5 000-bit photosensor array, two 2 518-bit CCD charge transfer registers, and an output amplifier.

The photosensor has a pitch of 7 μm pitch.

FEATURES

- Built-in output signal amplifier circuit
- High response to the fluorescent lamp source, which is five times as sensitive as the previous NEC μPD791D model
- Peak response: 550 nm green
- Data rate: 24 MHz high speed driving
- High resolution reading of A3-width at 16 dot/nm
- Single 12 V power drive

ORDERING INFORMATION

Part Number	Package
μPD3571D	22-pin ceramic DIP (CERDIP) (400 mil)

BLOCK DIAGRAM

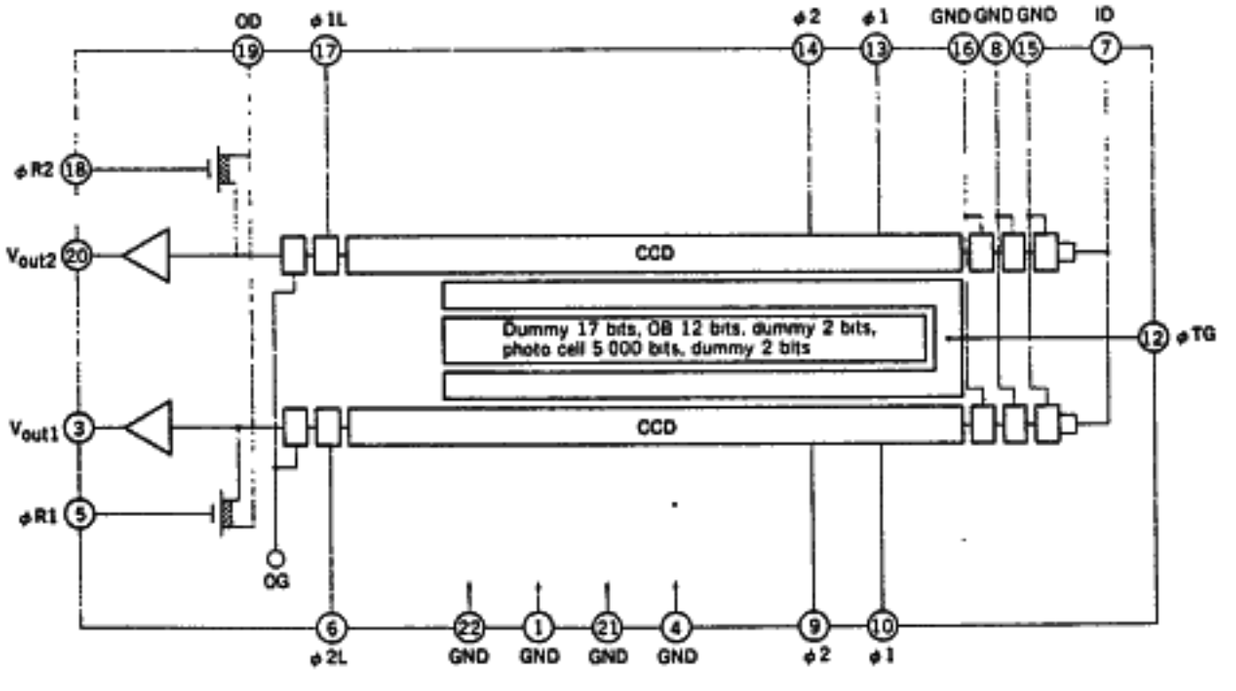
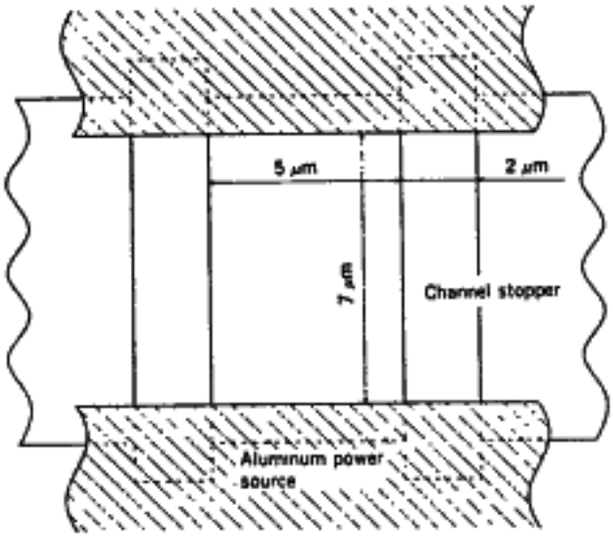
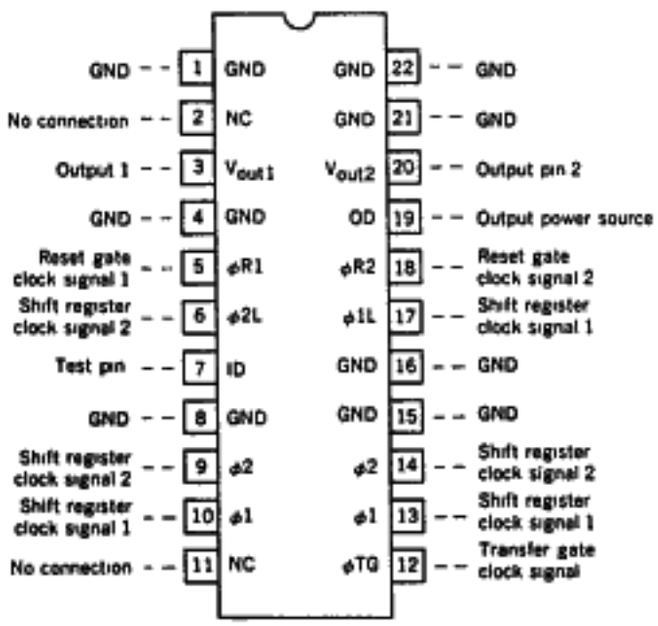


PHOTO ELEMENT CONFIGURATION DIAGRAM



PIN CONFIGURATION DIAGRAM (Top View)



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ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Output drain voltage	V_{OD}	−0.3 to +15	V
Test pin ID voltage	V_{ID}	−0.3 to +15	V
Shift register clock signal voltage	$V_{1,2}$	−0.3 to +15	V
Reset signal voltage	VR	−0.3 to +15	V
Transfer gate signal voltage	VTG	−0.3 to +15	V
Operating ambient temperature	T_{opt}	−25 to +60	°C
Storage temperature	T_{stg}	−40 to +100	°C

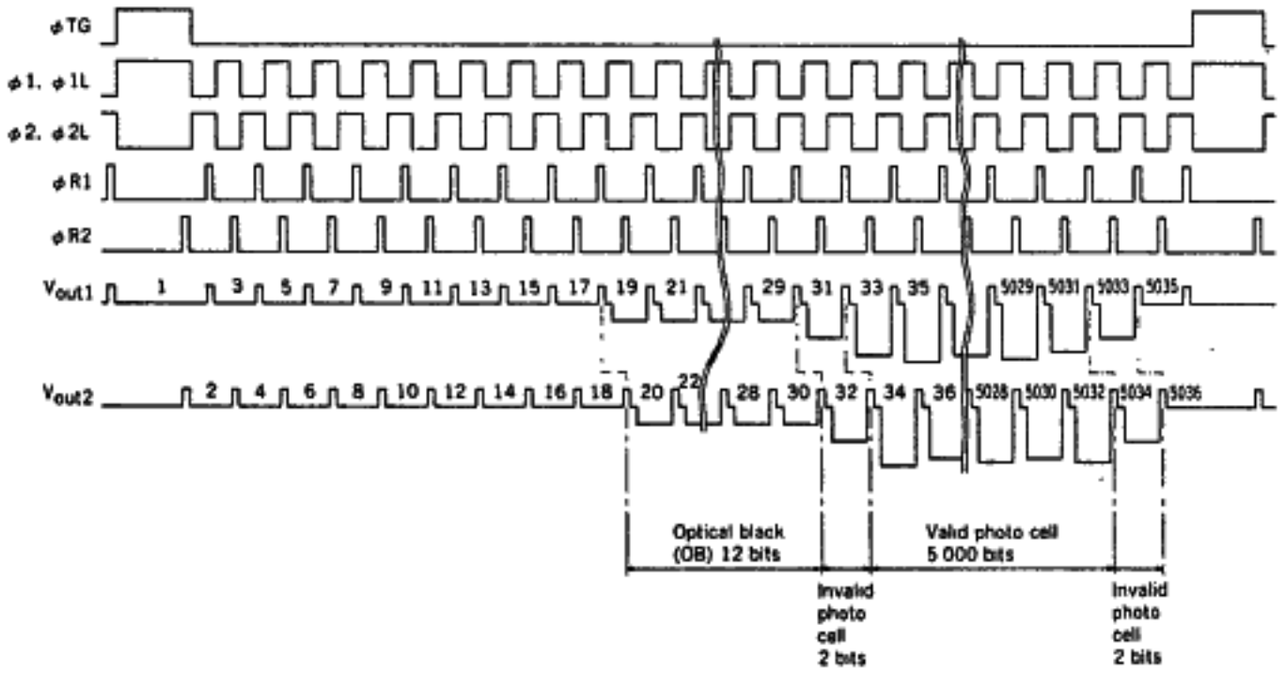
RECOMMENDED OPERATING CONDITIONS (T_a = −25 to +60 °C)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Output drain voltage	V_{OD}	11.4	12.0	12.6	V
Test pin G_1 voltage	V_{G1}		0		V
Test pin G_2 voltage	V_{G2}		0		V
Test pin ID voltage	V_{ID}		12.0		V
Test pin φIR voltage	$V_{\phi IR}$		0		V
Shift register clock φ1 signal high level	$V_{\phi 1H}$	8.0	12.0	12.6	V
Shift register clock φ1 signal low level	$V_{\phi 1L}$	−0.3	0	0.5	V
Shift register clock φ2 signal high level	$V_{\phi 2H}$	8.0	12.0	12.6	V
Shift register clock φ2 signal low level	$V_{\phi 2L}$	−0.3	0	0.5	V
Reset signal φR1H high level	$V_{\phi R1H}$	8.0	12.0	13.0	V
Reset signal φR1L low level	$V_{\phi R1L}$	−0.3	0	0.5	V
Reset signal φR2H high level	$V_{\phi R2H}$	8.0	12.0	13.0	V
Reset signal φR2L low level	$V_{\phi R2L}$	−0.3	0	0.5	V
Transfer gate signal high level	$V_{\phi TGH}$	8.0	12.0	12.6	V
Transfer gate signal low level	$V_{\phi TGL}$	−0.3	0	0.5	V
Data rate	$f_{\phi R}$		2	24	MHz

ELECTRIC CHARACTERISTICS (T_a = 25 °C, V_{OD} = 12.0 V, $f_{\phi 1}$ = 1 MHz, data rate = 2 MHz, storage time = 10 ms, light source: 2 856 K tungsten bulb)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Saturation voltage	V_{sat}	1.0	1.5		V	
Saturation exposure	SE		1.0		Lxs	White fluorescent lamp
Photo response non-uniformity	PRNU		±5	±10	%	V_{out}: 500 mV, White fluorescent lamp
Average dark signal	ADS		1	5	mV	Light input interruption
Dark signal non-uniformity	DSNU		2	10	mV	Light input interruption, peak value
Power consumption	P_W		100		mW	
Output impedance	Z_O		0.5	1	kΩ	
Sensitivity	R	3.85	5.5	7.15	V/Lxs	W lamp
	R	1.05	1.5	1.95	V/Lxs	White fluorescent lamp
Response peak wavelength			550		nm	
Offset level	V_{os}	4.0	7.0	9.0	V	
Shift register clock pin input capacity	$C_{\phi 1}$		450	600	pF	
Reset pin input capacity	$C_{\phi R}$		10	15	pF	
Transfer gate signal pin input capacity	$C_{\phi TG}$		150	200	pF	
Output setup delay time	t_d		20	50	ns	

TIMING CHART



* φ1, φ1L, φ2, φ2L, φR1, V_{out1}, V_{out2} timing charts

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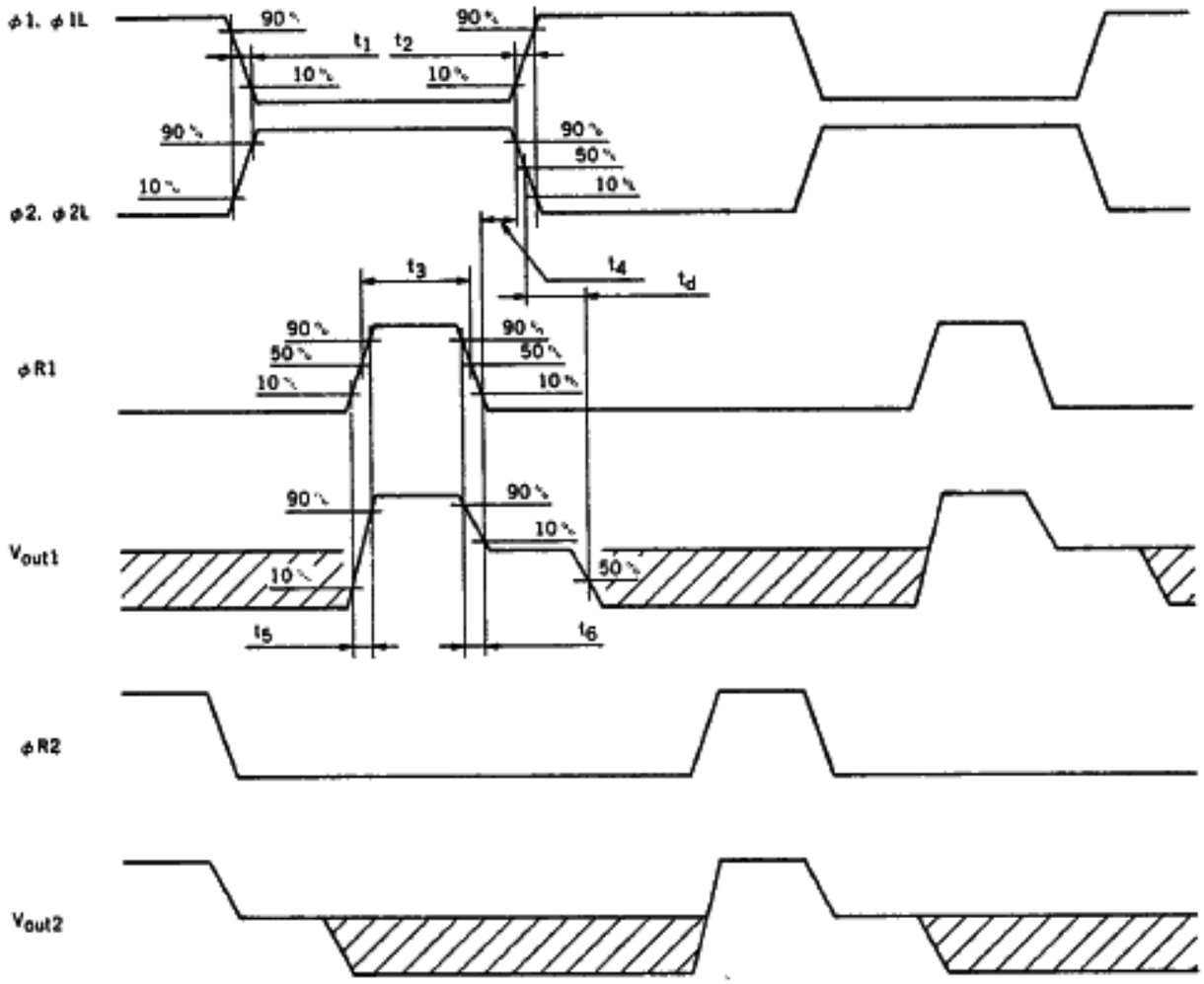
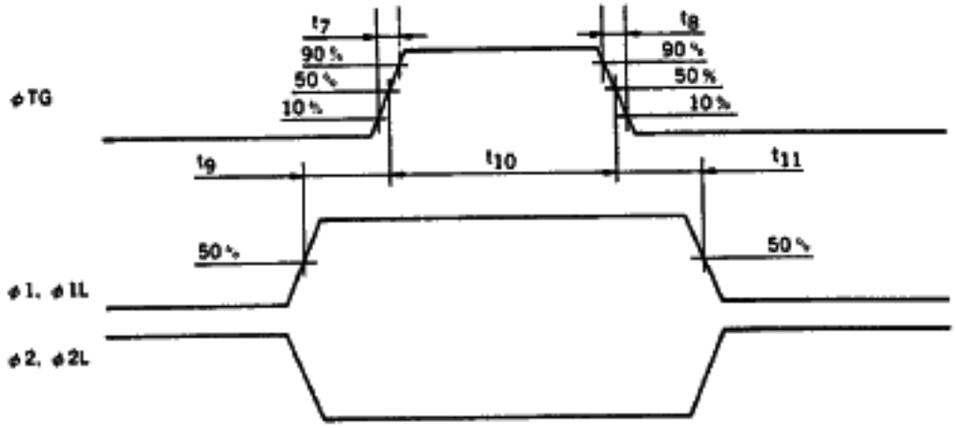
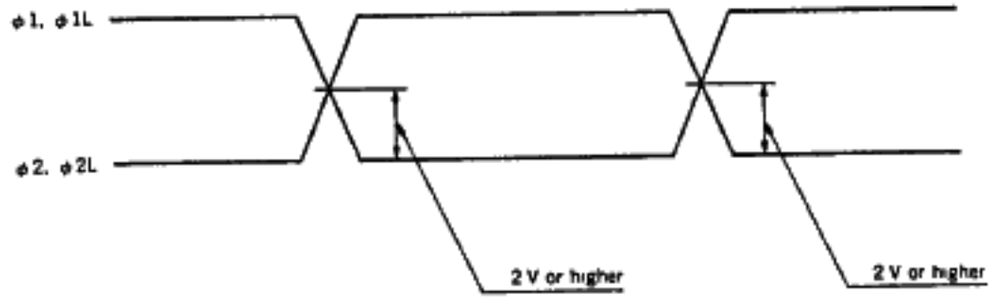


* φTG, φ1, φ1L, φ2, φ2L timing charts



* φ1, φ1L, φ2, φ2L cross points



Name	MIN.	TYP.	MAX.
t_1, t_2	0	100	200
t_3	20	100	-
t_4	0	20	
t_5, t_6	0	20	50
t_7, t_8	0	50	100
t_9, t_{11}	10	100	--
t_{10}	300	1000	-

(ns)

DEFINITIONS OF SPECIAL TERMS

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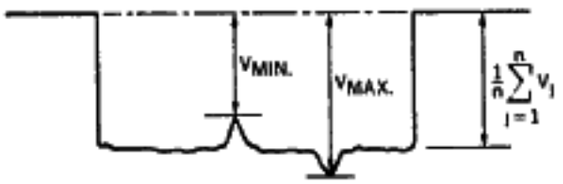
1. Saturation Voltage (V_{sat})
   The point at which the response linearity is lost.

2. Saturation Exposure (SE)
   The multiple of storage time (s) and illumination (lx) at which saturation voltage is reached.

3. Photo Response Non-Uniformity (PRUN)
   The ratio of the peak bottom to the average output voltage of all valid bits. Obtained from the following formula.

$$PRNU(\%) = \left(\frac{V_{MAX.} \text{ or } V_{MIN.}}{\frac{1}{n}\sum_{j=1}^{n} V_j} - 1 \right) \times 100$$

n : Number of valid bits
V_j : Output voltage of each bit



4. Average Dark Signal (ADS)
   Average output voltage during light interruption.

$$ADS(mV) = \frac{1}{n}\sum_{j=1}^{n} V_j$$

5. Dark Signal Non-uniformity (DSUN)
   The peak output voltage against the idle level during light interruption.

6. Output Impedance (Z_o)
   Output impedance observed externally.

7. Response (R)
   The quotient of output voltage divided by exposure (lx·s).
   Response may vary with the use of light sources not designated in the electric characteristics section.

STANDARD CHARACTERISTIC CURVES (T_a = 25 °C)

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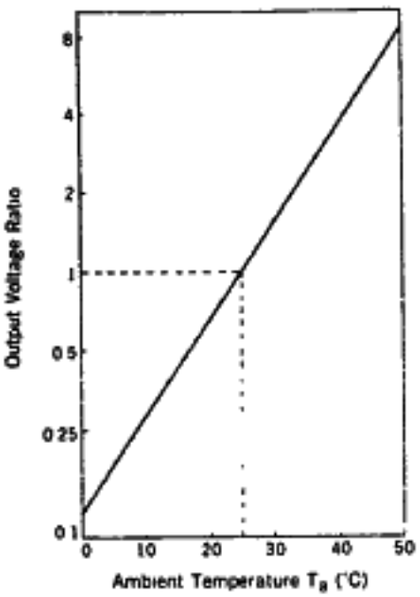
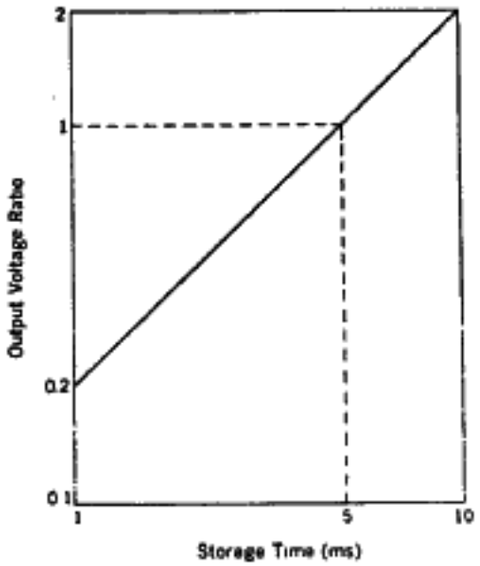
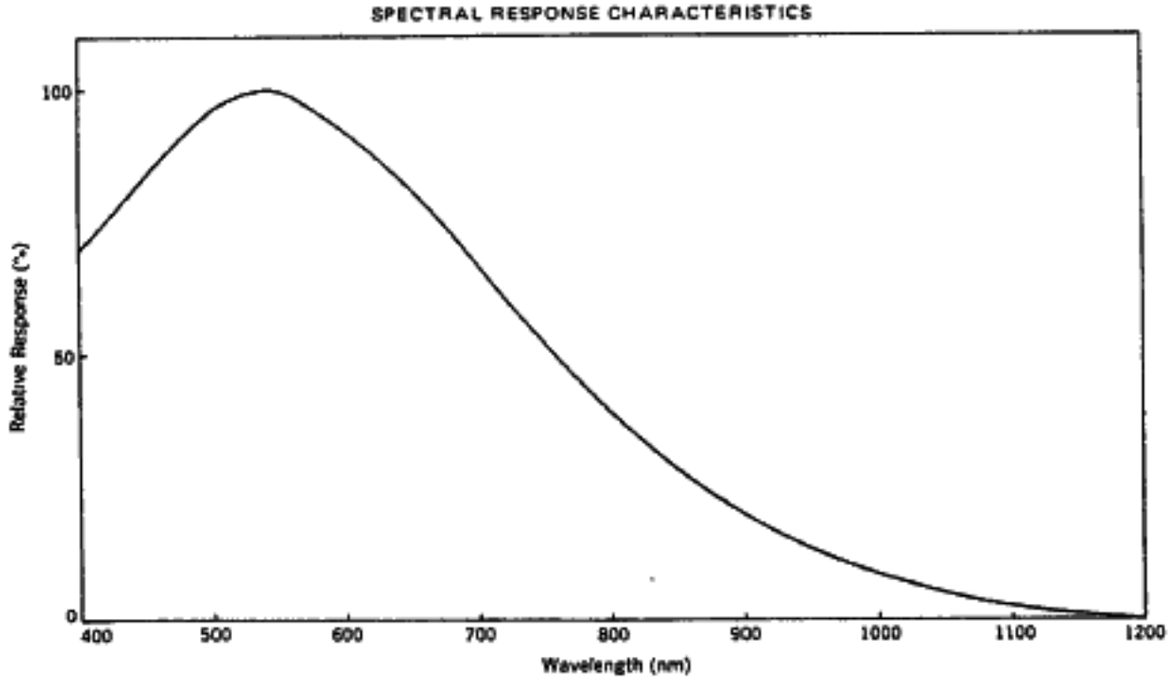
DARK SIGNAL TEMPERATURE CHARACTERISTICS

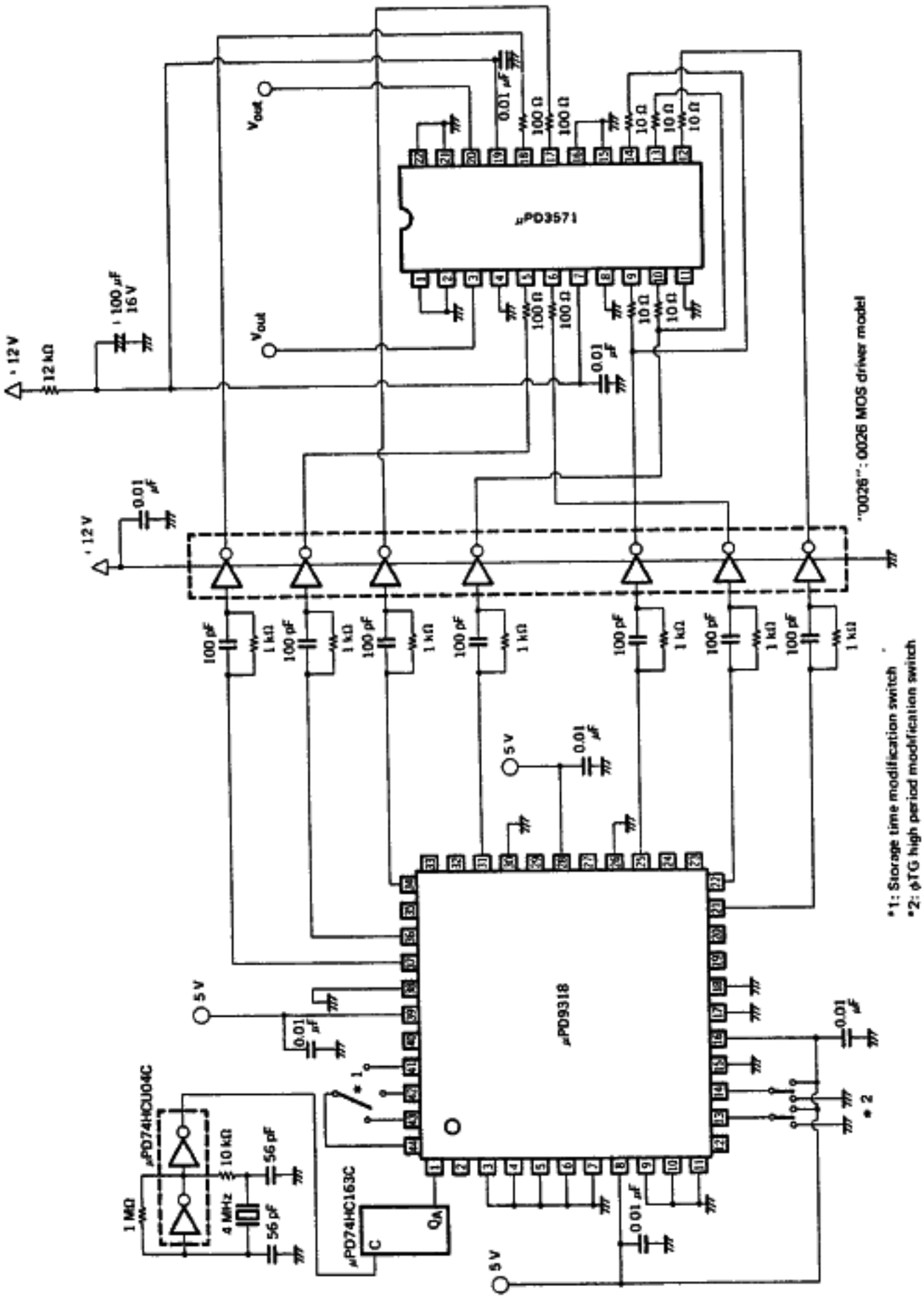


STORAGE TIME OUTPUT VOLTAGE CHARACTERISTICS



SPECTRAL RESPONSE CHARACTERISTICS




μPD3571
μPD9318
μPD74HCU04C
μPD74HC163C
"0026": 0026 MOS driver model
*1: Storage time modification switch
*2: φTG high period modification switch

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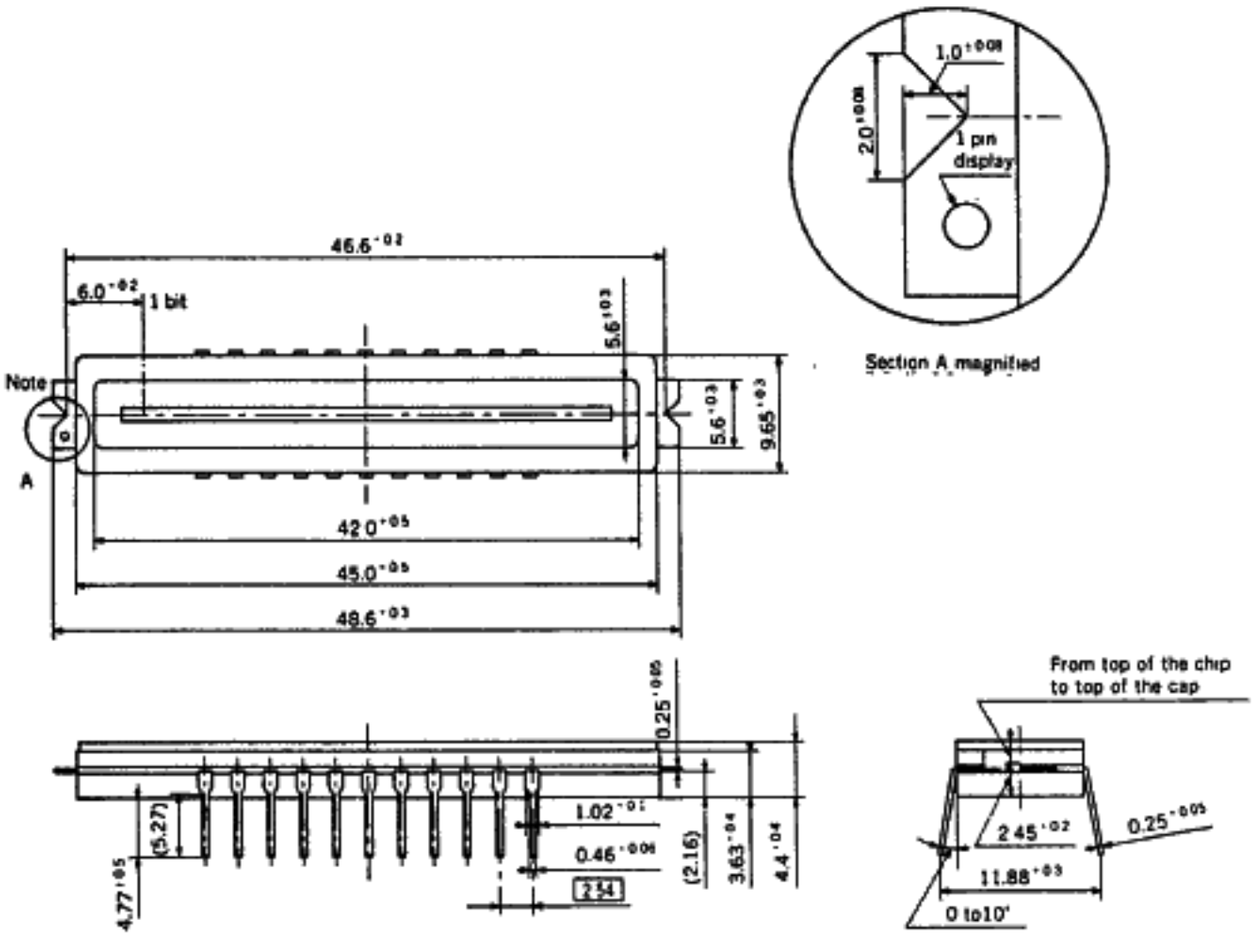
PACKAGE DIMENSIONS (Unit: mm)



Name	Dimensions	Refraction
Glass cap	44.6 × 9.25 × 0.7	1.5

* Note: Use the standard board in open state, without applying potential.

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