To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK1315(L)(S), 2SK1316(L)(S)

Silicon N-Channel MOS FET

ADE-208-1267 (Z)
1st. Edition
Mar. 2001

Application

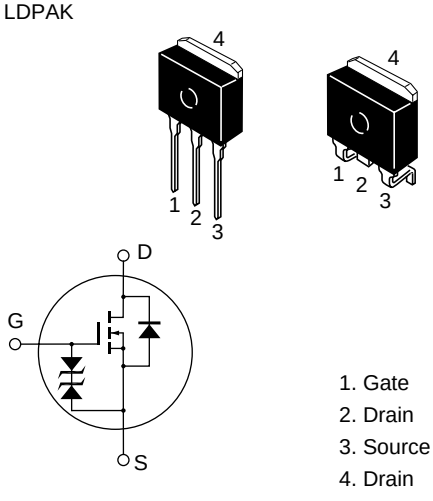
High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator, DC-DC converter and motor driver

Outline

LDPAK



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1315	V_{DSS}	450	V
	2SK1316		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	8	A
Drain peak current		$I_{D(pulse)}$*[1]	32	A
Body to drain diode reverse drain current		I_{DR}	8	A
Channel dissipation		Pch*[2]	60	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

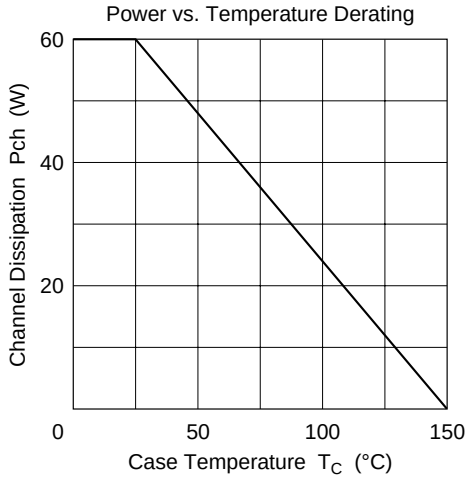
Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at T_C = 25°C

Electrical Characteristics (Ta = 25°C)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK1315	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1316		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1315	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1316						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1315	$R_{DS(on)}$	—	0.55	0.7	Ω	I_D = 4 A, V_{GS} = 10 V *[1]
	2SK1316		—	0.60	0.8		
Forward transfer admittance		|yfs|	4.5	7.5	—	S	I_D = 4 A, V_{DS} = 10 V *[1]
Input capacitance		Ciss	—	1150	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Output capacitance		Coss	—	340	—	pF	
Reverse transfer capacitance		Crss	—	55	—	pF	
Turn-on delay time		$t_{d(on)}$	—	17	—	ns	I_D = 4 A, V_{GS} = 10 V, R_L = 7.5 Ω
Rise time		t_r	—	55	—	ns	
Turn-off delay time		$t_{d(off)}$	—	100	—	ns	
Fall time		t_f	—	45	—	ns	
Body to drain diode forward voltage		V_{DF}	—	0.9	—	V	I_F = 8 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	350	—	ns	I_F = 8 A, V_{GS} = 0, di_F/dt = 100 A/µs

Note: 1. Pulse test

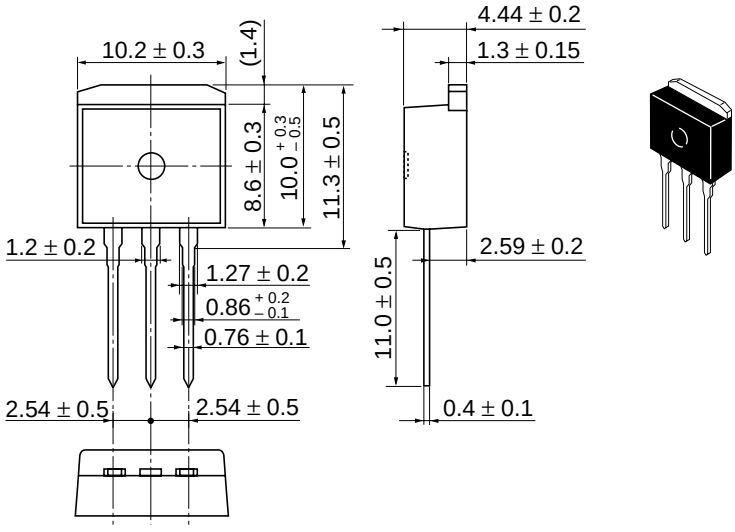
See characteristic curves of 2SK1159, 2SK1160.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)

Package Dimensions

As of January, 2001

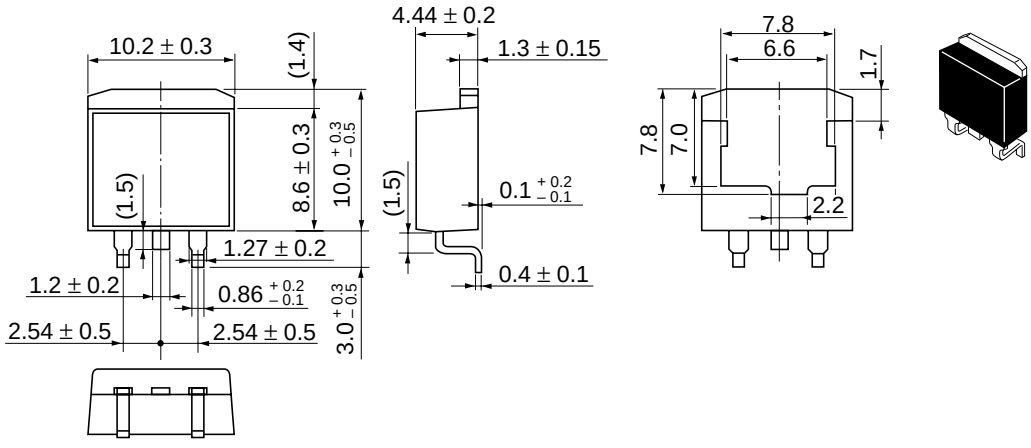
Unit: mm



Hitachi Code	LDPAK (L)
JEDEC	—
EIAJ	—
Mass (reference value)	1.4 g

As of January, 2001

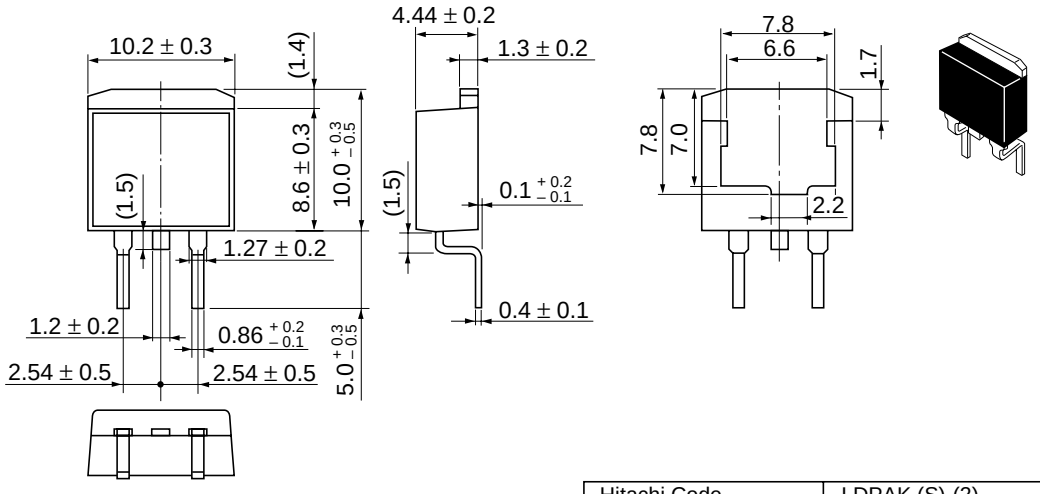
Unit: mm



Hitachi Code	LDPAK (S)-(1)
JEDEC	—
EIAJ	—
Mass (reference value)	1.3 g

As of January, 2001

Unit: mm



Hitachi Code	LDPAK (S)-(2)
JEDEC	—
EIAJ	—
Mass (reference value)	1.35 g

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