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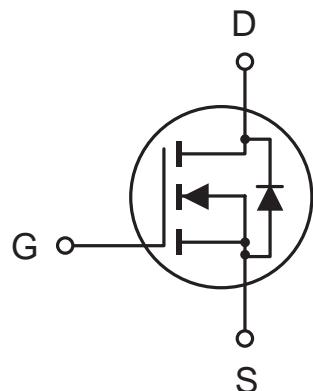
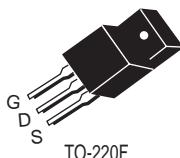
CEF02N6

Sep. 2002

## N-Channel Logic Level Enhancement Mode Field Effect Transistor

### FEATURES

- 600V , 1.5A ,  $R_{DS(ON)}=5\Omega$  @ $V_{GS}=10V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- TO-220F full-pak for through hole



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### ABSOLUTE MAXIMUM RATINGS ( $T_c=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V
Drain Current-Continuous -Pulsed	$I_D$	1.5	A
	$I_{DM}$	4.5	A
Drain-Source Diode Forward Current	$I_S$	4.5	A
Maximum Power Dissipation @ $T_c=25^\circ C$ Derate above 25°C	$P_D$	29	W
		0.23	W/°C
Operating and Storage Temperature Range	$T_J, T_{STG}$	-65 to 150	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	4.3	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	65	°C/W

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## ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE AVALANCHE RATING<sup>a</sup></b>						
Single Pulse Drain-Source Avalanche Energy	E <sub>AS</sub>	V <sub>DD</sub> = 50V, L = 60mH R <sub>G</sub> = 9.1Ω		125		mJ
Maximum Drain-Source Avalanche Current	I <sub>AS</sub>			2		A
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	600			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 600V, V <sub>GS</sub> = 0V			25	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±30V, V <sub>DS</sub> = 0V			±100	nA
<b>ON CHARACTERISTICS<sup>a</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2		4	V
Drain-Source On-State Resistance	R <sub>D(S)ON</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 1A		3.8	5.0	Ω
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 10V	2			A
Forward Transconductance	g <sub>F</sub>	V <sub>DS</sub> = 50V, I <sub>D</sub> = 1A		1.2		S
<b>SWITCHING CHARACTERISTICS<sup>b</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> = 300V, I <sub>D</sub> = 2A, V <sub>GS</sub> = 10V R <sub>GEN</sub> = 18Ω		18	35	ns
Rise Time	t <sub>r</sub>			18	35	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			50	90	ns
Fall Time	t <sub>f</sub>			16	40	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 480V, I <sub>D</sub> = 2A, V <sub>GS</sub> = 10V		20	25	nC
Gate-Source Charge	Q <sub>gs</sub>			2		nC
Gate-Drain Charge	Q <sub>gd</sub>			12		nC

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## ELECTRICAL CHARACTERISTICS ( $T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DYNAMIC CHARACTERISTICS<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS}=25\text{V}, V_{GS}=0\text{V}$ $f=1.0\text{MHz}$	250			pF
Output Capacitance	$C_{oss}$		50			pF
Reverse Transfer Capacitance	$C_{rss}$		30			pF
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>a</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS}=0\text{V}, I_S=1.5\text{A}$			1.5	V

### Notes

- a.Pulse Test:Pulse Width $\leq 300\ \mu\text{s}$ , Duty Cycle $\leq 2\%$ .
- b.Guaranteed by design, not subject to production testing.

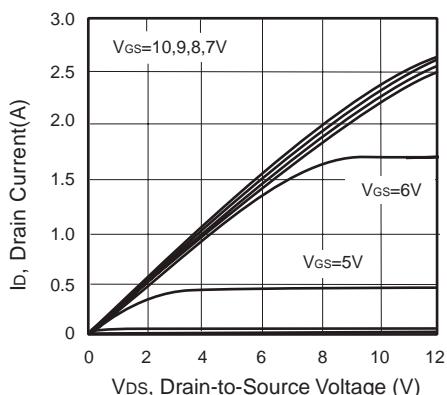


Figure 1. Output Characteristics

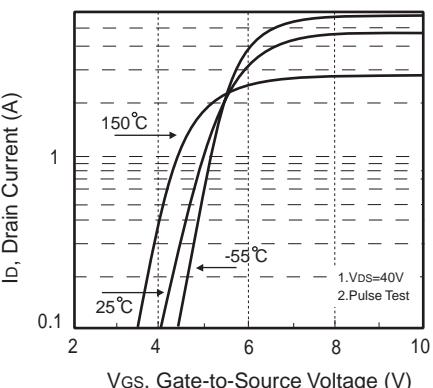
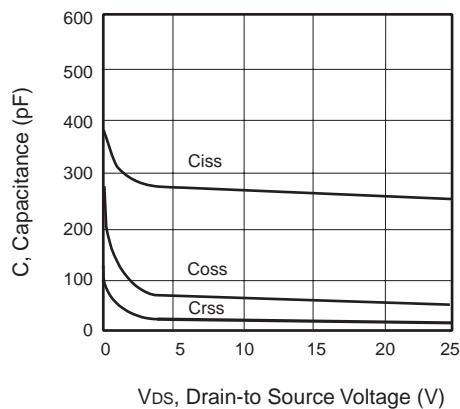


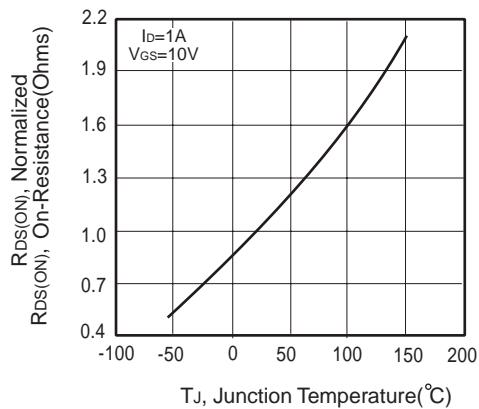
Figure 2. Transfer Characteristics

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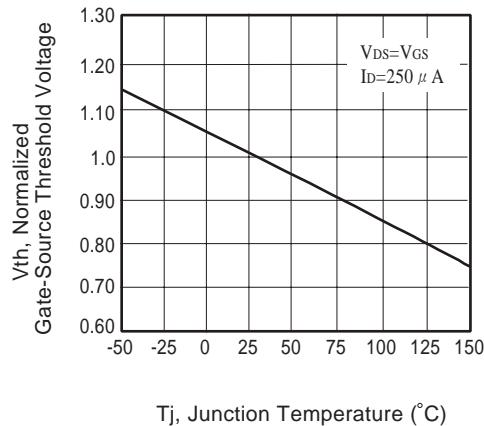
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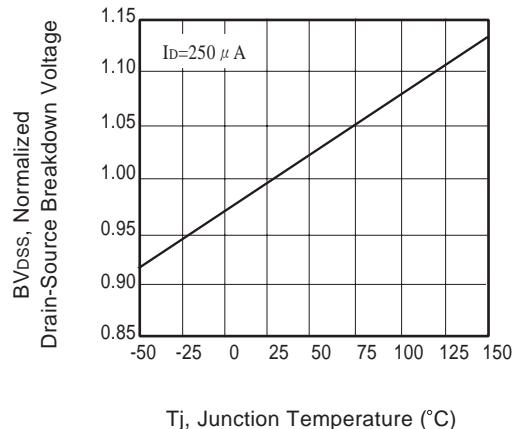
**Figure 3. Capacitance**



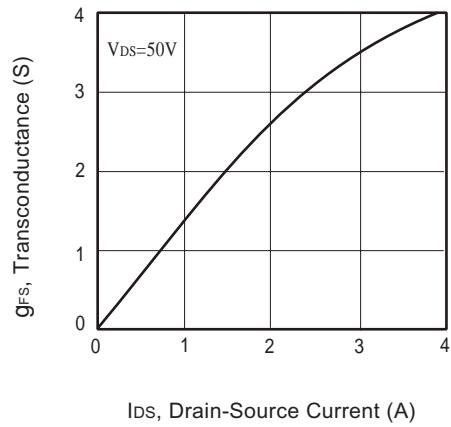
**Figure 4. On-Resistance Variation with Temperature**



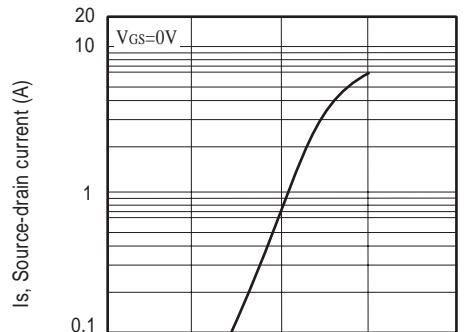
**Figure 5. Gate Threshold Variation with Temperature**



**Figure 6. Breakdown Voltage Variation with Temperature**



**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**

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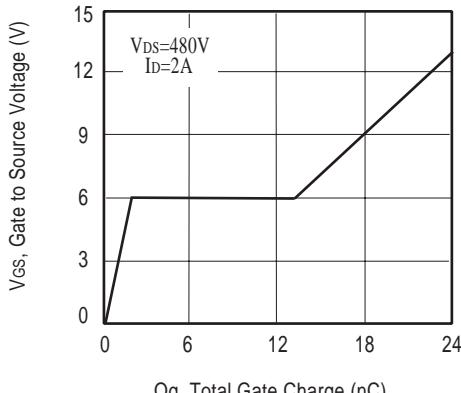
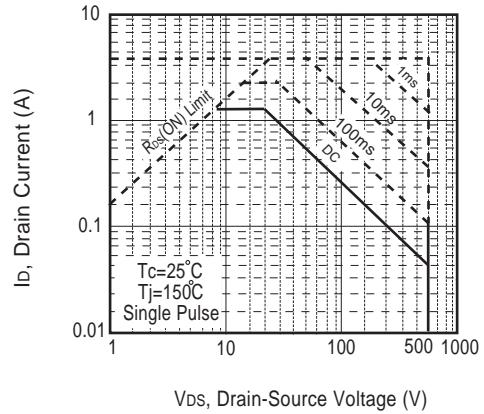


Figure 9. Gate Charge



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Figure 10. Maximum Safe Operating Area

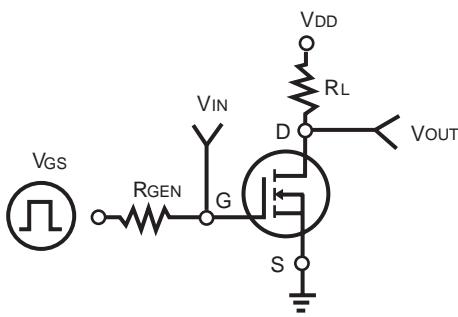


Figure 11. Switching Test Circuit

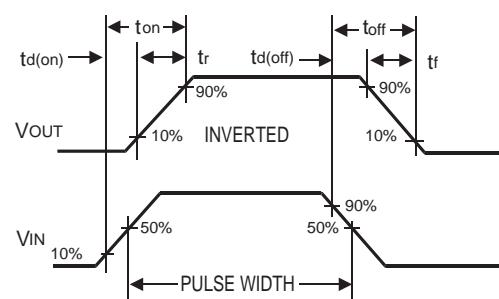


Figure 12. Switching Waveforms

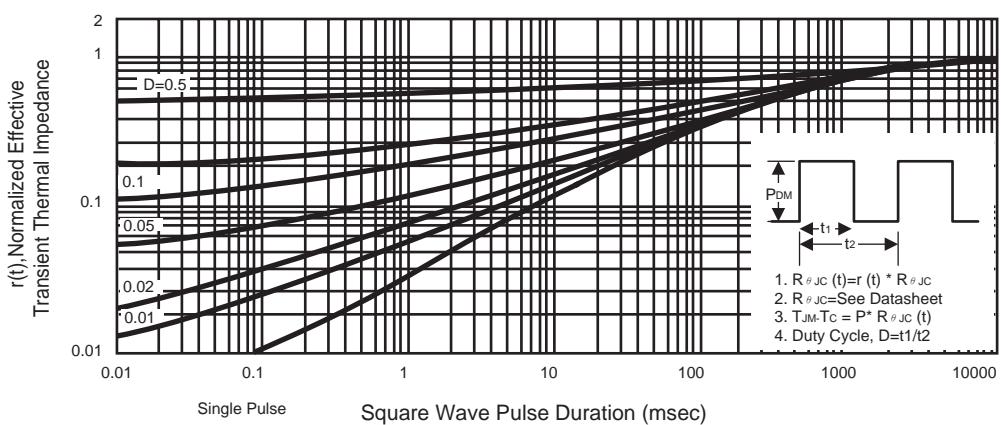


Figure 13. Normalized Thermal Transient Impedance Curve