IN74AC112

Dual J-K Flip-Flop with Set and Reset

High-Speed Silicon-Gate CMOS

N SUFFIX
PLASTIC

D SUFFIX
SOIC

ORDERING INFORMATION
IN74AC112N Plastic
IN74AC112D SOIC
T_A = -40° to 85° C for all packages

The IN74AC112 is identical in pinout to the LS/ALS112, HC/HCT112. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALS outputs.

Each flip-flop is negative-edge clocked and has active-low asynchronous Set and Reset inputs.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 µA; 0.1 µA @ 25°C
- High Noise Immunity Characteristic of CMOS Devices
- Outputs Source/Sink 24 mA
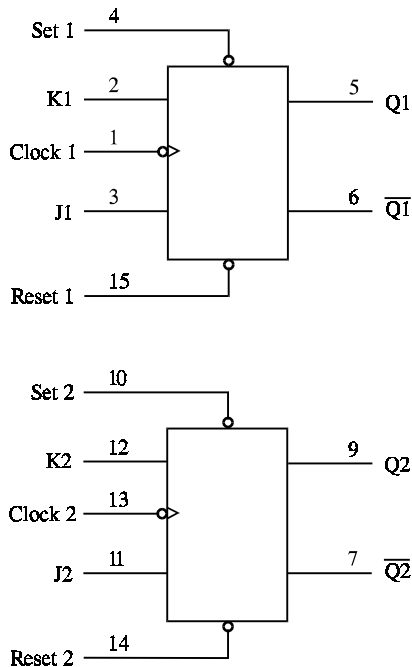
PIN ASSIGNMENT

CLOCK 1	1 ●	16	V_{CC}
K1	2	15	RESET 1
J1	3	14	RESET 2
SET 1	4	13	CLOCK 2
Q1	5	12	K2
$\overline{Q1}$	6	11	J2
$\overline{Q2}$	7	10	SET 2
GND	8	9	Q2

LOGIC DIAGRAM

PIN 16=V_{CC}
PIN 8 = GND

FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	⌐_	L	L	No Change	
H	H	⌐_	L	H	L	H
H	H	⌐_	H	L	H	L
H	H	⌐_	H	H	Toggle	
H	H	L	X	X	No Change	
H	H	H	X	X	No Change	
H	H	_/	X	X	No Change	

* Both outputs will remain low as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously
X = Don't Care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
          SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Temperature, All Package Types		-40	+85	°C
I_{OH}	Output Current - High			-24	mA
I_{OL}	Output Current - Low			24	mA
t_r, t_f	Input Rise and Fall Time * (except Schmitt Inputs)	V_{CC} =3.0 V V_{CC} =4.5 V V_{CC} =5.5 V	0 0 0	150 40 25	ns/V

* V_{IN} from 30% to 70% V_{CC}

        This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.
        Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

INTEGRAL

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limits 25 °C	Guaranteed Limits -40°C to 85°C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V	3.0 4.5 5.5	2.1 3.15 3.85	2.1 3.15 3.85	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V	3.0 4.5 5.5	0.9 1.35 1.65	0.9 1.35 1.65	V
V_{OH}	Minimum High-Level Output Voltage	$I_{OUT} \leq$ -50 µA	3.0 4.5 5.5	2.9 4.4 5.4	2.9 4.4 5.4	V
		*V_{IN}=V_{IH} or V_{IL} I_{OH}=-12 mA I_{OH}=-24 mA I_{OH}=-24 mA	3.0 4.5 5.5	2.56 3.86 4.86	2.46 3.76 4.76	
V_{OL}	Maximum Low-Level Output Voltage	$I_{OUT} \leq$ 50 µA	3.0 4.5 5.5	0.1 0.1 0.1	0.1 0.1 0.1	V
		*V_{IN}=V_{IH} or V_{IL} I_{OL}=12 mA I_{OL}=24 mA I_{OL}=24 mA	3.0 4.5 5.5	0.36 0.36 0.36	0.44 0.44 0.44	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	5.5	±0.1	±1.0	µA
I_{OLD}	+Minimum Dynamic Output Current	V_{OLD}=1.65 V Max	5.5		75	mA
I_{OHD}	+Minimum Dynamic Output Current	V_{OHD}=3.85 V Min	5.5		-75	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND	5.5	4.0	40	µA

* All outputs loaded; thresholds on input associated with output under test.
+Maximum test duration 2.0 ms, one output loaded at a time.
Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}

INTEGRAL

AC ELECTRICAL CHARACTERISTICS(C_L=50pF,Input t_r=t_f=3.0 ns)

Symbol	Parameter	V_{CC}* V	Guaranteed Limits				Unit
			25 °C		-40°C to 85°C		
			Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency (Figure 1)	3.3 5.0	145 145		125 125		MHz
t_{PLH}	Propagation Delay, Clock to Q or $\overline{Q}$ (Figure 1)	3.3 5.0	1.0 1.0	16.0 13.0	1.0 1.0	17.0 13.5	ns
t_{PHL}	Propagation Delay, Clock to Q or $\overline{Q}$ (Figure 1)	3.3 5.0	1.0 1.0	16.0 13.0	1.0 1.0	16.5 13.5	ns
t_{PLH}	Propagation Delay, Set or Reset to Q or $\overline{Q}$ (Figure 2)	3.3 5.0	1.0 1.0	11.0 9.5	1.0 1.0	11.5 10.0	ns
t_{PHL}	Propagation Delay, Set or Reset to Q or $\overline{Q}$ (Figure 2)	3.3 5.0	1.0 1.0	11.0 9.5	1.0 1.0	11.5 10.0	ns
C_{IN}	Maximum Input Capacitance	5.0	4.5		4.5		pF

		Typical @25°C,V_{CC}=5.0 V	
C_{PD}	Power Dissipation Capacitance	35	pF

*Voltage Range 3.3 V is 3.3 V ±0.3 V
 Voltage Range 5.0 V is 5.0 V ±0.5 V

TIMING REQUIREMENTS(C_L=50pF,Input t_r=t_f=3.0 ns)

Symbol	Parameter	V_{CC}* V	Guaranteed Limits		Unit
			25 °C	-40°C to 85°C	
t_{su}	Minimum Setup Time, J or K to Clock (Figure 3)	3.3 5.0	6.5 4.5	7.5 5.0	ns
t_h	Minimum Hold Time, Clock to J or K (Figure 3)	3.3 5.0	0 0	0 0	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	3.3 5.0	6.0 5.0	6.5 5.5	ns
t_w	Minimum Pulse Width,Set or Reset (Figure 2)	3.3 5.0	6.5 5.0	7.5 5.5	ns
t_{rec}	Minimum Recovery Time, Set or Reset to Clock (Figure 2)	3.3 5.0	0 0	0 0	ns

*Voltage Range 3.3 V is 3.3 V ±0.3 V
 Voltage Range 5.0 V is 5.0 V ±0.5 V
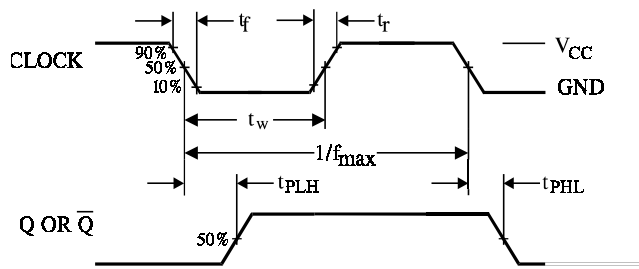
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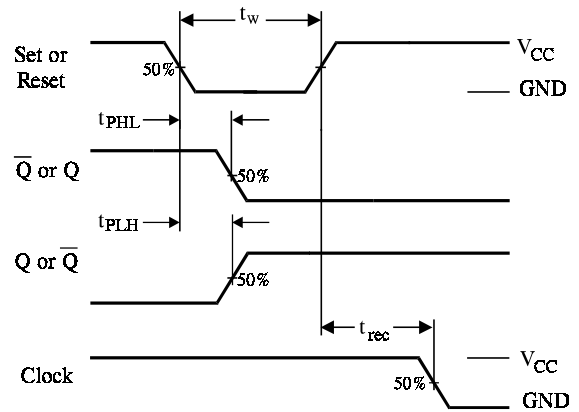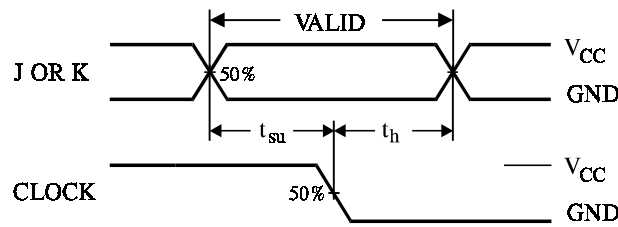Figure 1. Switching Waveform

Figure 2. Switching Waveform

Figure 3. Switching Waveform

EXPANDED LOGIC DIAGRAM