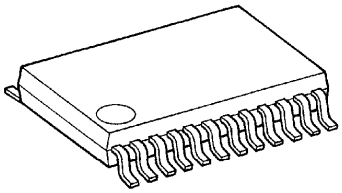
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9464FN

Σ-Δ MODULATION DA CONVERTER WITH BUILT-IN 8 TIMES OVERSAMPLING DIGITAL / ANALOG FILTER

The TC9464FN is a second-order Σ-Δ modulation 1-bit DA converter incorporating an 8 times oversampling digital / analog filter developed for digital audio equipment.

Because the IC includes an analog filter it can output a direct analog waveform, thus reducing the size and cost of the DA converter.



SSOP24-P-300-0.65A

Weight : 0.14g (Typ.)

FEATURES

- Built-in 8 times oversampling digital filter
- Built-in digital de-emphasis filter
- In serial operating mode, output amplitude can be set in 128 steps of resolution using microcontroller commands
- In parallel control mode, soft mute output can be set in 64 steps in 20ms
- Built-in LR common zero detection output function
- DAC oversampling ratio (OSR) : 192fs
- Double-speed operation capable
- Sampling frequencies : 44.1kHz, 32kHz, 48kHz
- Built-in third-order analog filter
- The digital filter and DA converter characteristics are as shown next page

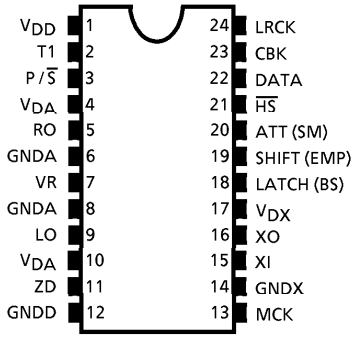
DIGITAL FILTER (at fs = 44.1kHz)

	DIGITAL FILTER	PASSBAND RIPPLE	TRANSIENT BANDWIDTH	ATTENUATION
Standard Operation	8fs	±0.11dB	20k~24.1kHz	−26dB or less
Double-speed Operation	8fs	±0.11dB	20k~24.1kHz	−26dB or less

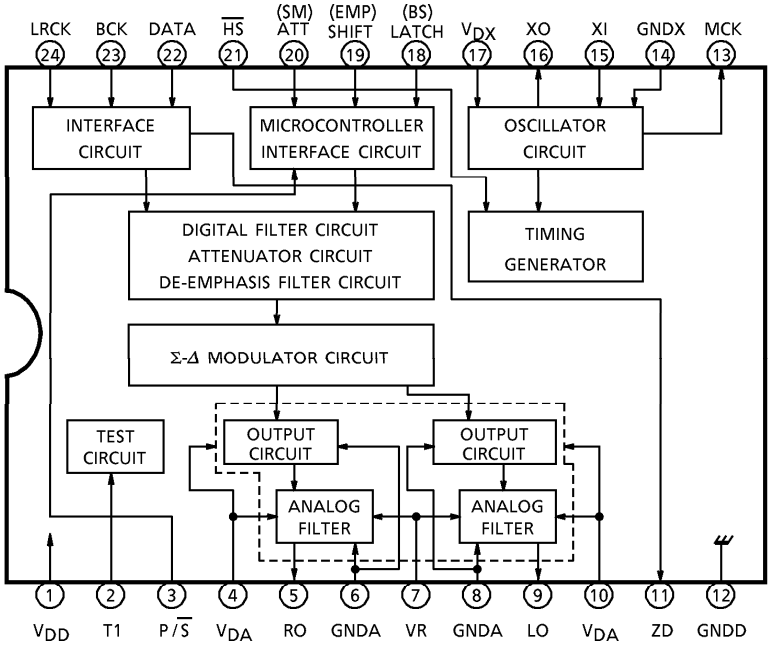
DA CONVERTER (V_{DD} = 5V)

	OSR	NOISE DISTORTION	S / N RATIO
Standard Operation	192fs	−85dB (Typ.)	96dB (Typ.)
Double-speed Operation	96fs	−85dB (Typ.)	86dB (Typ.)

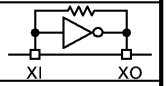
PIN ASSIGNMENT



BLOCK DIAGRAM



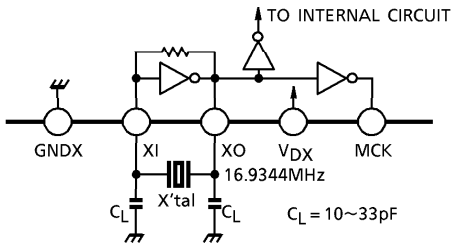
PIN DESCRIPTION

PIN No.	SYMBOL	I / O	FUNCTION	REMARKS
1	V_{DD}	—	Digital block power pin	
2	T1	I	Test pin Always set to low.	
3	P / $\overline{S}$	I	Parallel / serial mode select pin	
4	V_{DA}	—	Analog power pin	
5	RO	O	Right channel analog data output pin	
6	GNDA	—	Analog GND pin	
7	VR	I	Reference voltage input pin	
8	GNDA	—	Analog GND pin	
9	LO	O	Left channel analog data output pin	
10	V_{DA}	—	Analog power pin	
11	ZD	O	Zero data detection output pin common to left and right channels	
12	GNDD	—	Digital GND pin	
13	MCK	O	System clock output pin	
14	GNDX	—	Crystal oscillator GND pin	
15	XI	I	Crystal oscillator connecting pins Generate the clock required by the system.	
16	XO	O		
17	V_{DX}	—	Crystal oscillator power pin	
18	LATCH (BS)	I	In serial mode, data latch signal input pin In parallel mode, de-emphasis filter mode select pin	Schmitt input
19	SHIFT (EMP)	I	In serial mode, shift clock input pin In parallel mode, de-emphasis filter control pin	Schmitt input
20	ATT (SM)	I	In serial mode, data input pin In parallel mode, soft mute control pin	Schmitt input
21	$\overline{HS}$	I	Standard / double-speed operation control pin When H : standard operation, when L : double-speed mode	
22	DATA	I	Data input pin	
23	BCK	I	Bit clock input pin	
24	LRCK	I	LR clock input pin	

DESCRIPTION OF BLOCK OPERATION

1. Crystal Oscillator Circuit and Timing Generator

The clock required for the IC's internal operation can be generated by connecting a crystal and capacitors as in the diagram below. The IC will also operate when a system clock is input from an external source through XI (pin 15). However in this case, due consideration should be taken of the fact that waveform characteristics such as jitter and rising / falling characteristics of the system clock significantly affect the DA converter noise distortion and the S / N.



Use a crystal with a low IC value and good startup characteristics.

Fig.1 Crystal Oscillator Circuit

The timing generator generates the clocks or process timing signals required for such functions as digital filtering and de-emphasis filtering.

2. Data Input Circuit

DATA and the LRCK are loaded to the LSI internal shift registers on the BCK signal rising edge. Accordingly, as shown in the Fig.2 timing example, the DATA and LRCK signals must be input on the BCK signal falling edge. In addition, DATA is designed so that the 16 bits before the change point of LRCK are regarded as valid data. Therefore, when BCK is 48fs or 64fs, for example, effective data must be input before the change point of LRCK.

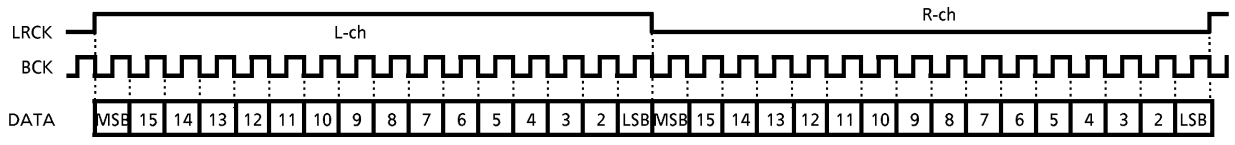


Fig.2a Example of Input Timing Chart

When BCK is 48fs or 64fs, input valid data before the change point of LRCK as in the figure below.

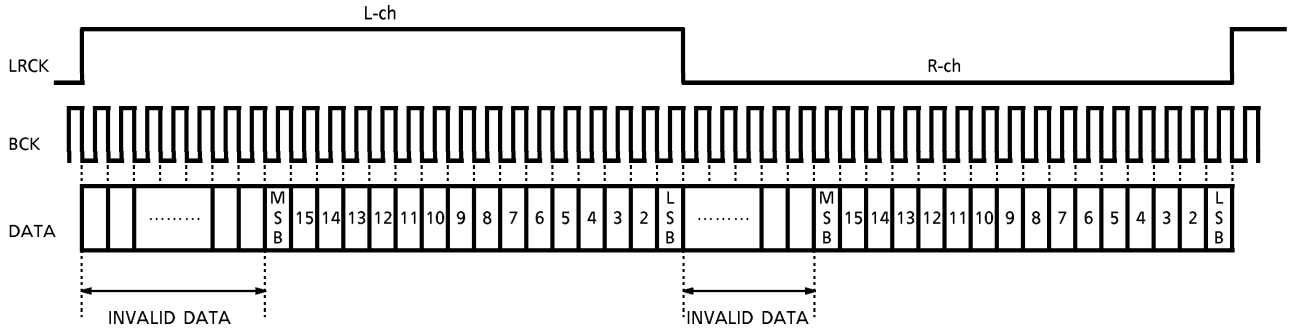


Fig.2b Example of Input Timing Chart

3. Digital Filter

In both standard and double-speed operation, an 8 times oversampling IIR digital filter eliminates aliasing noise component outside the bandwidth.

Table 1 Basic Characteristics of Digital Filter (fs = 44.1kHz)

SET MODE	PASS BAND RIPPLE	TRANSIENT BANDWIDTH	ATTENUATION
Standard Operation	±0.11dB	20.0k~24.1kHz	−26dB or less
Double-speed Operation	±0.11dB	20.0k~24.1kHz	−26dB or less

Fig.3 shows the digital filter frequency characteristics. (Same as for double-speed operation.)

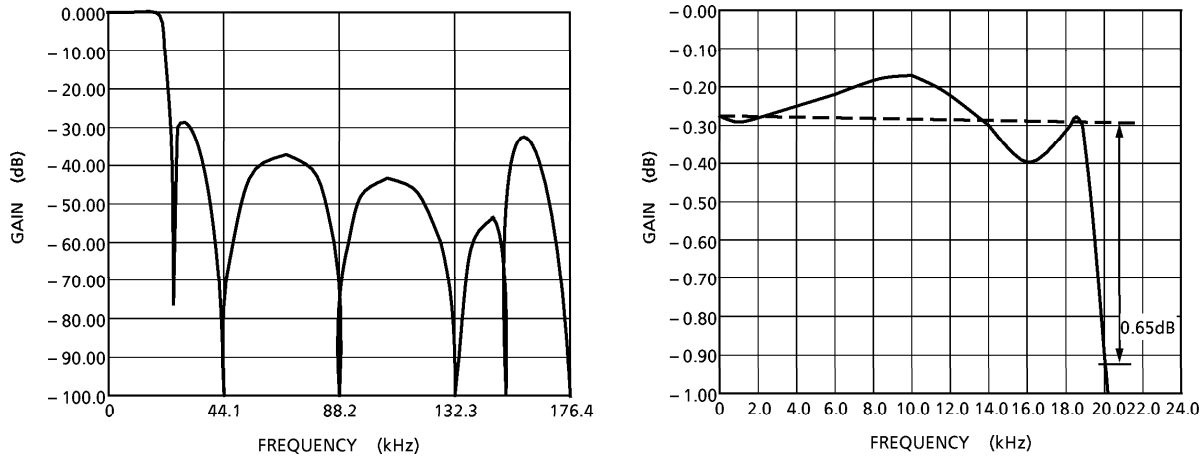


Fig.3 Frequency Characteristics of Digital Filter (fs = 44.1kHz)

4. De-emphasis Filter

By switching the mode, the digital de-emphasis circuit can be set to three frequencies : 32kHz, 44.1kHz, and 48kHz.

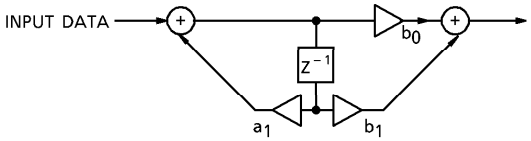
In parallel mode ($P/\overline{S} = H$), these frequencies are set by the LATCH (BS) (pin 18) and SHIFT (EMP) (pin 19) pins. In serial mode ($P/\overline{S} = L$), the frequencies are set using microcontroller commands. (For details for setting in serial mode, see the section on the microcontroller interface function.)

Table 2 Digital De-emphasis Filter Frequency Coefficient Setting (In Parallel Mode)

LATCH (BS)	H	H	L	L	
SHIFT (EMP)	H	L	H	L	
Mode (fs selection)	32	48	44.1	Off	(kHz)

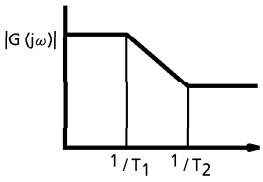
The digitalization of the de-emphasis filter eliminates the need for such external components as resistors, capacitors, and analog switches. In addition, the coefficients are adjusted to reduce error in the de-emphasis filter characteristics.

The following diagrams show the filter structure and characteristics.



Transfer function : $H(Z) = \dfrac{(b_0 + b_1 Z^{-1})}{(1 - a_1 Z^{-1})}$

Fig.4 IIR Digital De-Emphaiss Filter

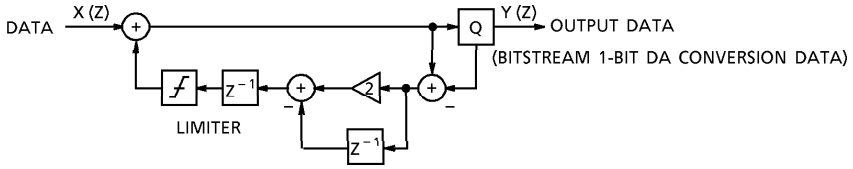


$T_1 = 50\mu s$, $T_2 = 15\mu s$

Fig.5 Filter Characteristics

5. DA Conversion Circuit

The TC9464FN incorporates a second-order Σ-Δ modulation DA converter for two channels (simultaneous output type). Fig.6 shows the converter's internal structure.



Second-order Σ-Δ converter : $Y(Z) = X(Z) + (1 - Z^{-1})^2 Q(Z)$

Fig.6 Σ-Δ Modulation DA Converter

The clock of the Σ-Δ modulation unit is designed to operate at 192fs. Fig.7 shows the noise shaping characteristics.

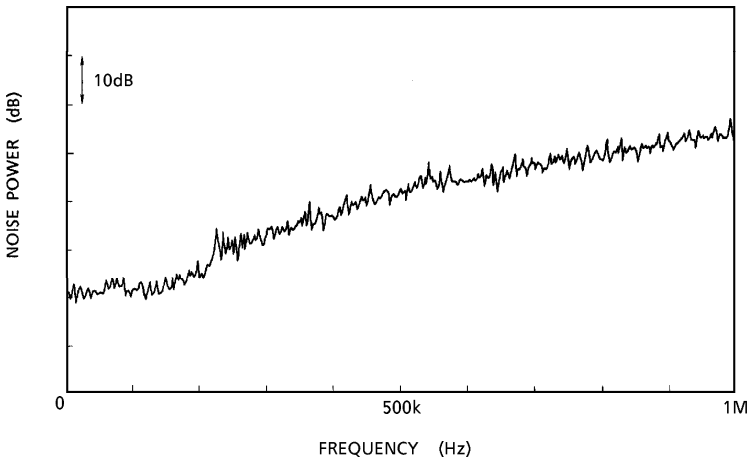


Fig.7 Noise Shaping Characteristics

6. Data Output Circuit

The output circuit incorporates a third-order analog low-pass filter.

This allows the IC to directly obtain analog signals from the IC output pins RO (pin 5) and LO (pin 9).

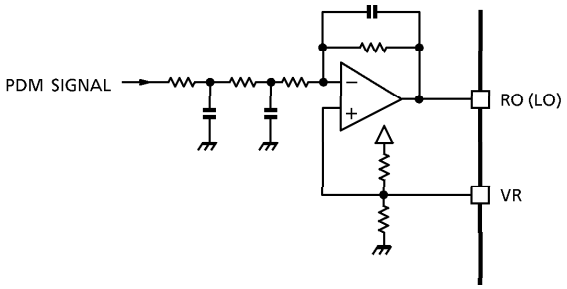


Fig.8 Analog Filter Circuit

7. Soft Mute Circuit

The TC9464FN incorporates a soft mute function. In parallel mode (P / $\overline{S}$ = H), switching the SM pin from low to high performs soft mute on the DA converter output. Fig.9 shows the soft mute on / off settings and the DA converter output.

Soft mute on / off control is disabled during output level transition.

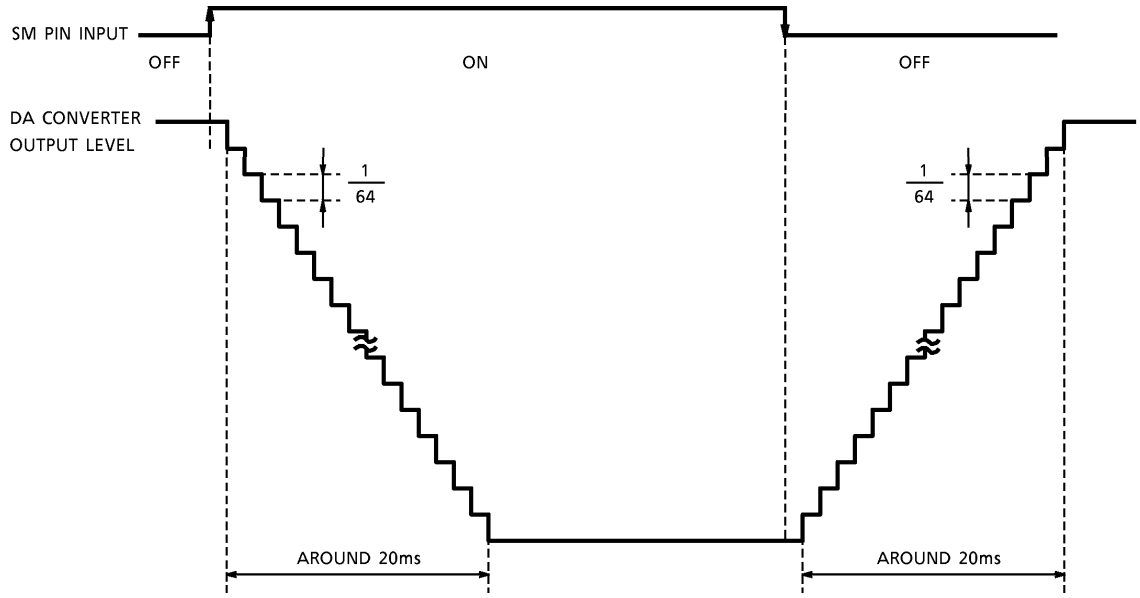


Fig.9 Changes in Soft Mute DA Converter Output Level

8. Zero Data Detection Output Circuit

The TC9464FN incorporates a zero data detection output circuit. If data in both the left and right channels are zero data for 350ms or longer, the ZD pin (pin 11) changes from low to high.

If the data in both the L and R channels is other than zero data, ZD is fixed to L.

9. Description of Internal Control Signals

The P/$\overline{S}$ pin can be used to switch between parallel control mode (P/$\overline{S}$ pin = high in DC setting mode) and serial control mode (P/$\overline{S}$ pin = low in microcontroller setting mode). The following describes the control functions.

9-1 Parallel Control Mode (P/$\overline{S}$ pin = high)

In parallel control mode, pins 18, 19, and 20 are used as the mode setting pins shown in the table below.

Table 3 Parallel Control Mode

PIN No.	PIN NAME	PIN DESCRIPTION
18	BS	De-emphasis filter mode switching pin
19	EMP	De-emphasis control pin
20	SM	Soft mute control pin

9-2 Serial Control Mode (P/$\overline{S}$ pin = low : Microcontroller interface function)

In serial control mode, a microcontroller can perform the IC settings. In serial control mode, pins 18, 19, and 20 are used as the attenuator input pins as shown in the table below.

Table 4 Pins in Serial Control Mode

PIN No.	PIN NAME	PIN DESCRIPTION
18	LATCH	Data latch signal input pin
19	SHIFT	Shift clock signal input pin
20	ATT	Data input pin

The LATCH and ATT signals are loaded to the LSI internal shift register on the SHIFT signal rising edge. Accordingly, as shown in the Fig.10 timing example, the data input from the ATT pin on the shift signal rising edge must be valid. The LATCH pulse must rise at least 1.5μs after the final clock rising edge input from the SHIFT pin. Operating the shift clock with LATCH low destabilizes the internal states, possibly causing malfunction.

Therefore, set the LATCH signal to low level after loading D7 to the register.

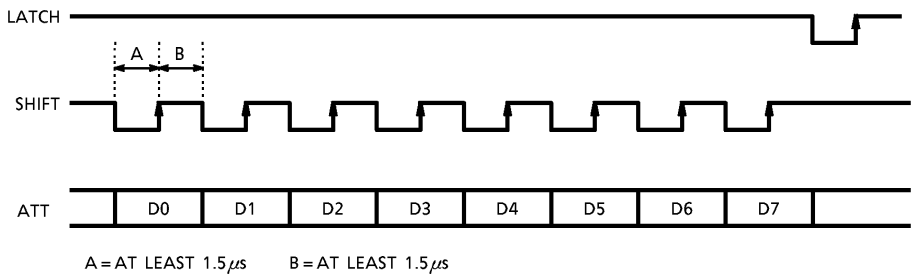


Fig.10 Example of Serial Control Mode Data Setting Timing

In serial control mode, control is as follows.

Set all the control bits when the IC power is switched on.

Table 5 Serial Mode Control

SERIAL INPUT DATA	CONTROL SIGNAL	
D7	0	1
D6	AT6	μBS
D5	AT5	μEMP
D4	AT4	—
D3	AT3	—
D2	AT2	—
D1	AT1	—
D0	AT0	—

AT0 to 6 : Attenuation level setting
μBS : De-emphasis switching
μEMP : De-emphasis on / off switching

(1) Digital attenuator

D7 = low sets digital attenuator control mode. The attenuator can be set in 128 steps. The following table shows the relationship between the commands and the output.

Table 6 Attenuator Data vs Audio Output

ATTENUATION DATA D6 VS D0	AUDIO OUTPUT
7F (HEX)	0dB
7E (HEX)	– 0.069dB
⋮	⋮
01 (HEX)	– 42.076dB
00 (HEX)	– ∞

The 01 (HEX) to 7E (HEX) attenuation value is calculated by the following formula.

ATT = 20ℓog (input data / 127) dB

Example : With attenuation data 7A :

ATT = 20ℓog (122 / 127) dB = – 0.349dB

D7 = high sets de-emphasis switching mode.

(2) Digital de-emphasis filter

The digital de-emphasis filter is controlled by the μEMP and μBS signals.

Table 7 Digital De-emphasis Filter Setting

μBS	H	H	L	L
μEMP	H	L	H	L
Mode (fs selection)	32	48	44.1	Off

(kHz)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~6.0	V
	V_{DA}	−0.3~6.0	
	V_{DX}	−0.3~6.0	
Input Voltage	V_{in}	−0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	200	mW
Operating Temperature	T_{opr}	−35~85	°C
Storage Temperature	T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, $V_{DD} = V_{DX} = V_{DA} = 5V$)

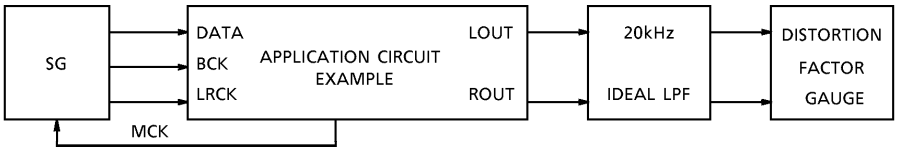
DC Characteristics

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	MAX.	MAX.	UNIT
Operating Supply Voltage		V_{DD}	—	Ta = −35~85°C	4.5	5.0	5.5	V
		V_{DX}			4.5	5.0	5.5	
		V_{DA}			4.5	5.0	5.5	
Supply Current		I_{DD}	—	XI = 16.9MHz	—	12	20	mA
Input Voltage	High Level	V_{IH}	—	—	V_{DD} × 0.7	—	V_{DD}	V
	Low Level	V_{IL}			0	—	V_{DD} × 0.3	
Input Current	High Level	I_{IH}	—	—	−10	—	10	μA
	Low Level	I_{IL}						

AC CHARACTERISTICS (Oversampling ratio = 192fs)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Noise Distortion	THD + N1	1	Total harmonic distortion + noise 1kHz sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 5V$	—	− 85	− 80	dB
Signal-to-noise Ration	S / N	1		88	96	—	dB
Dynamic Range	DR	1	1kHz sine wave, − 60dB input conversion	90	95	—	dB
Crosstalk	CT	1	1kHz sine wave, full-scale input	—	− 95	− 90	dB
Analog Output Level	Aout1	1	1kHz sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 5V$	—	1175	—	mVrms
Operating Frequency	f_{opr}	—	$V_{DD} = V_{DA} = V_{DX} \geqq 4.5V$	10	16.9344	19.2	MHz
Input Frequency	f_{LR}	—	LRCK duty cycle = 50%	30	44.1	100	kHz
	f_{BCK}		BCK duty cycle = 50%	0.96	2.1168	4.3	MHz
Rise Time	t_r	—	LRCK, BCK pin (10 to 90%)	—	—	15	ns
Fall Time	t_f			—	—	15	
Delay Time	t_d	—	BCK Edge → LRCK, DATA	—	—	40	ns

- Test circuit 1 : Using application circuit

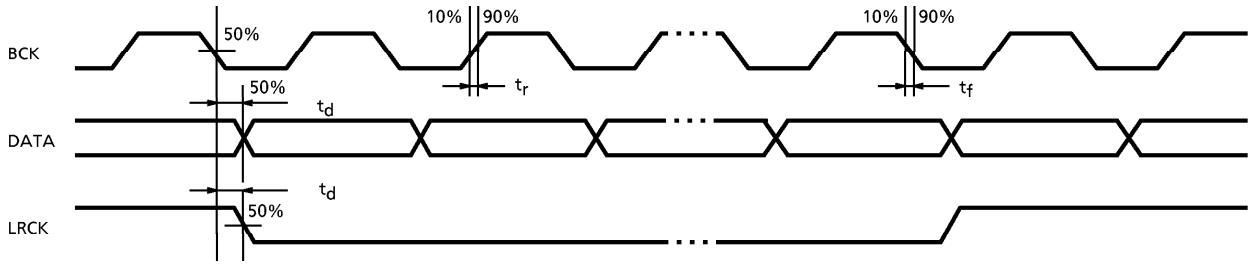


SG : Anritsu MG-22A or equivalent
LPF : Shibasoku 725C built-in filter
Distortion factor gauge : Shibasoku 725C or equivalent

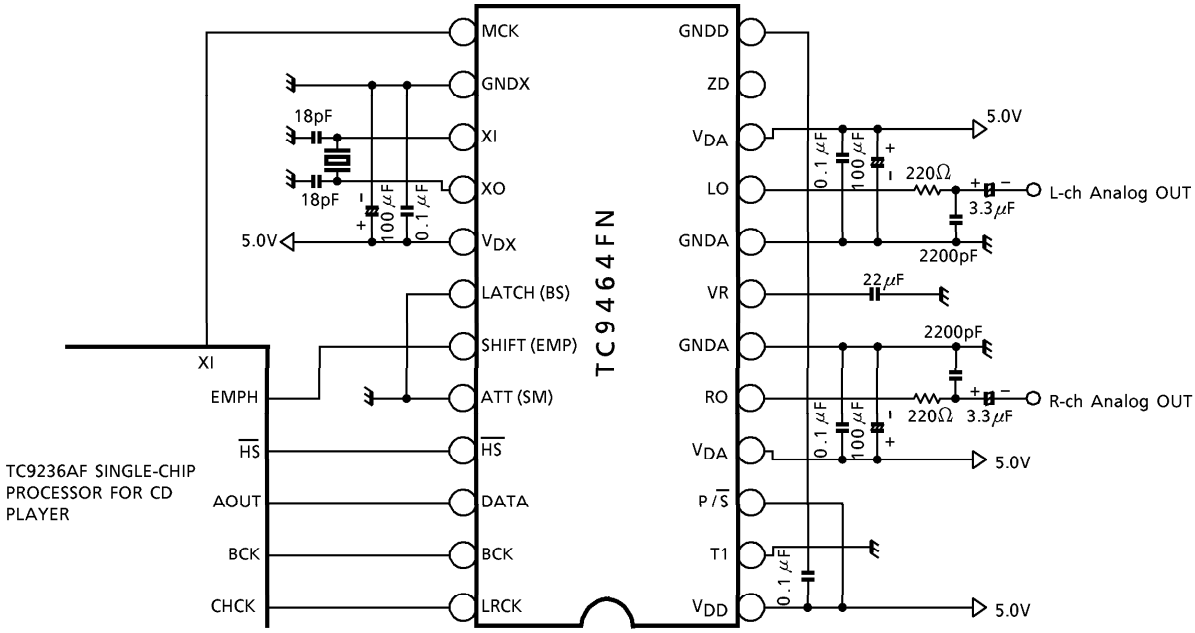
PARAMETER MEASURED	DISTORTION FACTOR GAUGE FILTER SETTING A WEIGHT
THD + N, CT	Off
S / N, DR	On

A weight
: IEC-A or equivalent

- AC characteristic point (Input signal setting : LRCK, BCK, DATA)



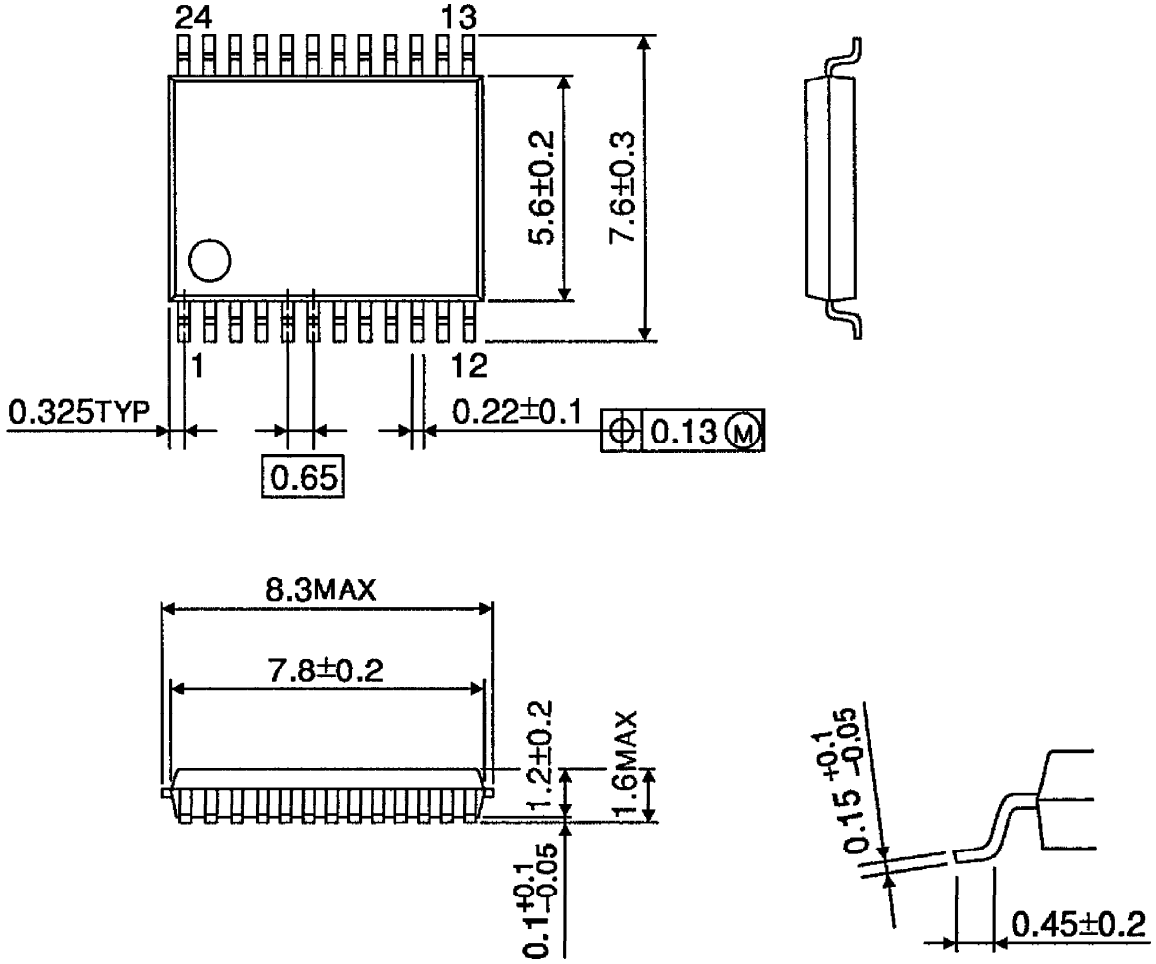
APPLICATION CIRCUIT



PACKAGE DIMENSIONS

SSOP24-P-300-6.65A

Unit : mm



Weight : 0.14g (Typ.)

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