TDK SEMICONDUCTOR CORP.

AVPro® 5003
Triple SCART A/V Switch

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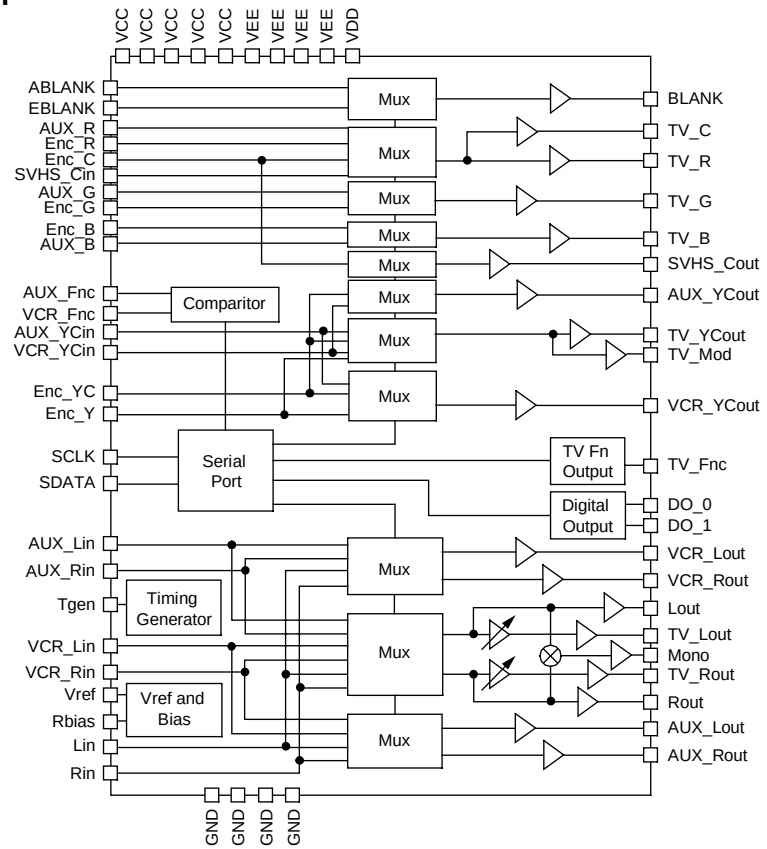
DESCRIPTION

The AVPro® 5003 is a low cost IC that performs switching of analog audio and video signals. The device accepts analog audio and video inputs from three external sources, typically a video encoder IC/stereo DAC, an auxiliary SCART connector, and a VCR SCART connector. The input signals from these sources are presented to a set of internal multiplexers that perform the SCART switching function. Outputs are provided to the VCR and auxiliary SCART connectors, as well as a TV SCART connector and an RF modulator. Video outputs are buffered to drive 150 Ω loads. Audio outputs are buffered to provide 2 Vrms output into 600 ohms. Typical applications for the 5003 include digital video recorders (DVRs) and digital receivers for satellite, cable, and terrestrial television.

FEATURES

- **SCART connections for TV, VCR, AUX**
- **Integrated video drivers**
- **Integrated audio drivers**
  - **Negative supply eliminates AC coupling caps**
- **5-bit audio attenuation for TV output**
  - **Attenuation from 0 to 31 dB, 1 dB steps**
  - **Mute of TV outputs**
- **Serial port control of SCART switching**
- **64-lead MQFP packaging (JEDEC MO-108)**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

SCART Video Switching
The device is designed to accept video signals from several SCART video resources. The device includes an analog multiplexer that receives the external video signals and allows routing of the signals to the various video outputs on the device. Writing bits to serial port Register 1 controls switching.

RGB Outputs: The device accepts RGB video signals from two sources. The *AUX_R*, *AUX_G*, *AUX_B* input pins are typically connected to the auxiliary SCART connector. The *Enc_R*, *Enc_G*, *Enc_B* input pins are connected to the RGB outputs of an external video encoder device. The lower two bits of serial port Register 1 determine which RGB input port will be used as the source for the *TV_R*, *TV_G*, *TV_B* output pins. When these bits are set to xxxxxx00, the auxiliary SCART is used as the input. When these bits are set to xxxxxx01, the video encoder is used as the input.

The RGB sync can be selected from either the RGB signals or the output on *TV_YCout,* as set by the MSB of serial port Register 0. Setting this bit selects the timing signal for the DC restore circuit. The DC restore circuit acts to position the blank level to 0.6 V at the output video load. When the bit is high, the timing signal is from the output on *TV_YCout* from either the *AUX_YCin* or *Enc_YC.* When the bit is low, the timing signal will detect sync on either of the RGB signals. The associated blanking signal from respective video sources is also switched accordingly with a delay matched to that of the RGB signals.

When the SVHS mode is active, the *TV_R* pin receives a chroma signal from either *Enc_C* or *SVHS_Cin*. The DC restore averages to approximately 1.8 VDC at the output pin. The *TV_G*, *TV_B* outputs are also disabled (~0 V) in this mode.

TV Composite Output: The device accepts up to three composite (YC) video sources. The *AUX_YCin* input pin is typically connected to the Video In pin on the auxiliary SCART connector. The *VCR_YCin* input pin is typically connected to the Video In pin from the VCR SCART connector. The *Enc_YC* input pin is typically connected to the YC output from the external video encoder device. Two bits in the serial port register determine which of the composite input signals will be switched to the *TV_YCout* output pin. When bits of Register 1 are set to xxxx00xx, the signal on *AUX_YCin* is used as the input. When the bits are set to xxxx01xx, the signal on *Enc_YC* is used as the input. When the bits are set to xxxx10xx, the signal on *VCR_YCin* is used as the input. The *TV_YCout* pin can be active with a composite video signal when RGB inputs are active. When the TV SVHS mode is selected the composite video mode is not available and the *TV_YCout* pin provides luminance information to the TV SCART connector. The DC restore circuit acts to position the blank level to 0.6 V at the output 75 ohm load.

RF Modulator Outputs: The device has a *TV_Mod* output that follows the *TV_YCout* signal. When the TV SCART has composite video, *TV_Mod* can be fed directly to the RF modulator. When the TV is in SVHS mode, the *TV_Mod* output (luminance) can be summed with the *TV_C* output (chroma) to provide a composite signal for the RF modulator. When the TV SCART has composite available, the *TV_C* output can be disabled via the MSB of serial port Register 1.

Auxiliary Composite Output: The VCR and video encoder composite video sources are available to switch to the *AUX_YCout* output pin. This pin is typically connected to the Video Out pin on the auxiliary SCART connector. A bit in serial port Register 1 determines the signal source for the *AUX_YCout* output pin. Setting the register to x0xxxxxx selects the signal on *VCR_YCin*, while setting the register to x1xxxxxx selects the signal on *ENC_YC*. The DC restore circuit acts to position the blank level to 0.5 V at the output pin.

VCR Composite Output: The auxiliary SCART and video encoder composite video sources are available to switch to the *VCR_YCout* output pin. This pin is typically connected to the Video Out pin on the VCR SCART connector. Two bits in serial port Register 1 determine the source for the *AUX_YCout* output pin. Setting the register to xx01xxxx selects the signal on *AUX_YCin*, while setting the register to xx10xxxx selects the signal on *ENC_YC*.

SVHS Switching: The device supports the SVHS mode from the VCR SCART connector. The *SVHS_Cin* pin provides chroma information from the VCR SCART connector to the TV SCART connector. The *SVHS_Cout* pin provides chroma information

from the encoder IC to the VCR SCART connector. The encoder chroma output can also be routed to the *TV_R* pin to support SVHS applications. When Register 1 is set to xxxx1011, the SVHS mode is selected with *SVHS_Cin* and *VCR_YCin* providing the chroma and luma inputs, respectively. In this mode, the load for the VCR chroma source (SCART pin 15) is provided by the series resistor for the SVHS_Cout pin and the low output impedance of the amplifier. The *SVHS_Cin* is ac coupled, and its dc bias set to approximately 0.9V. When the bits are set to xxxx1110, the *ENC_C* and *ENC_Y* inputs provide the chroma and luma inputs, respectively.

The VCR SCART can also receive SVHS information from the video encoder by setting the register bits to xx00xxxx. Note that when the VCR is receiving information it cannot be used as a signal source for other devices.

Function Switch: The device monitors the function switch pin (pin 8) of the auxiliary SCART and VCR SCART connectors, *AUX_Fnc* and *VCR_Fnc* pins, respectively. It is also known as slow blanking. Each of these inputs can detect three distinct levels and set two bits in serial port read Register 0. When the SCART input level is 0 to 2 V, the register bits are set to 00. When the input level is 4.5 to 7.0 V, the register bits are set to 01. When the input level is 9.5 to 12 V, the register bits are set to 10.

The device also provides a function switching output (*TV_Fnc*) to the TV SCART connector (pin 8). The output level is determined by the state of two LSBs in serial port write Register 0. The table below defines the state of the *TV_Fnc* pin based on the register bit values.

Bits	Output voltage	Function
xxxxxx00	~0 V	Normal TV
xxxxxx01	~6 V	16:9 aspect
xxxxxx10	~ 11 V	Peritelevision
xxxxxx11	~ 11 V	Peritelevision

SCART Audio switching

The device is designed to accept stereo audio inputs from an external audio DAC and from auxiliary SCART and VCR SCART connectors. The device provides audio outputs to the TV SCART, auxiliary SCART, and VCR SCART connectors. It also provides fixed gain, stereo line outputs of the audio output on the TV SCART. The line outputs are intended for use by an external stereo receiver/amplifier. These outputs are also combined for a Mono output to a RF modulator.

The audio inputs are considered to be associated with the respective composite video input. As a result, the video selection determines which audio signals will be switched to a given SCART output. Refer to the SCART Video Switching section of this document for more information.

Volume Control: The device provides control of the output level on the TV audio outputs (*TV_Lout/Rout*). The output level is controlled through serial port write Register 2. The lower 6-bits of this register set an attenuation level from 0 to -63 dB in 1 dB steps, where xx000000 is 0 dB and xx111111 is -63 dB. However, the attenuation is only specified to 5-bits of accuracy (-31 dB).The mute function is controlled by the fifth bit of write Register 0, which allows these outputs to be muted to -75 dB. When this bit is set to 0, the attenuator is active. When it is set to 1, the outputs are muted to -75 dB. This bit can be set independent of the attenuation register such that the output can be muted before any change in volume, or any switching of audio sources. The audio control circuits have a zero crossing detector that allows volume control changes to be completed only when the audio signal is near a zero crossing. This prevents audible popping and clicking during a volume change.

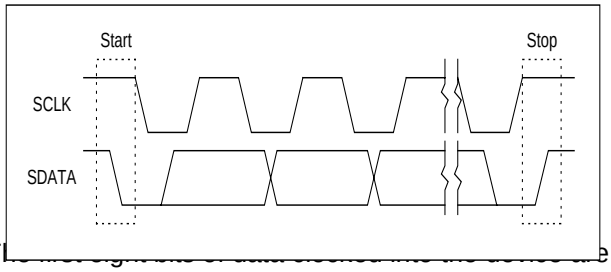
Hot-plug of SCART connectors. The 5003 devices are sensitive to discharge caused by floating chassis grounds between audio/video equipment. This is observed when the SCART cables are repeatedly connected and disconnected while the 5003 is powered on inside the IRD. When the SCART cable is unplugged, an AC potential can exist between equipments. When the SCART cable is plugged back into the IRD, the AC potential discharges through the SCART connector. If the discharge occurs through the shield of the SCART connector or the ground pins, there is no problem. If the discharge occurs through the signal pins, the 5003 devices can experience a latch-up condition and a high current situation will exist. The latch-up will occur if the pulse created by the discharge has a fast rising edge, typically a few hundred pico-seconds. This is an order of magnitude faster than a standard ESD pulse so the internal ESD diodes of the 5003 will not respond fast enough to protect the device. This problem can be resolved by placing a

small shunt capacitor on each SCART I/O pin. The capacitor slows the rising edge of the discharge pulse and allows the internal ESD diodes to react to the discharge. Good results are achieved using a 470 pF value, but an exact value should be calculated for each signal line depending upon the signal type so as to avoid roll-off of the intended signal. As an alternate approach, external diodes can be used to shunt this discharge.

Digital Outputs
The device includes programmable digital outputs (*DO_0,* and *DO_1)*. These pins are general purpose outputs programmed by bits in serial port Register 0. Bit 3 of this register controls *DO_0* while bit 4 controls *DO_1*. Setting the register bits to 0 puts these outputs in the LOW state. Setting the register bits to 1 puts the outputs in the HIGH state. Internal pull-ups are incorporated.

Serial Port Definition
Internal functions of the device are monitored and controlled by a simple two-wire serial port that is compatible with the inter-IC (I2C) bus. The serial port operates in a slave mode only and can be written to or read from. The default address of the device is 1001000x. The serial port uses a clock input (*SCLK*) that is driven by the bus master and a bi-directional data input (*SDATA*) to perform all data transfers.

Data Transfers: The device is enabled for a data transfer when the *SDATA* pin is driven from HIGH to LOW by the bus master while the *SCLK* pin is HIGH. The data transfer is complete when the bus master drives the *SDATA* pin from LOW to HIGH while the *SCLK* pin is HIGH.



The first eight bits of data clocked into the device are decoded to determine if a valid address has been received. The first seven bits of information are the address with the eighth bit indicating whether the cycle is a read (bit is HIGH) or a write (bit is LOW). If the address is valid for this device, on the falling *SCLK* edge of the eighth bit of data, the device will drive the *SDATA* pin low and hold it LOW until the next falling edge of the *SCLK* pin to acknowledge the address transfer. Once a valid address is detected the device will continue to transmit or receive data until the process is complete, or the bus master issues a stop.

Reset: At power-up the serial port defaults to the states indicated in boldface type. At device power-up, the device also generates an acknowledge. The device also responds to the system level reset that is transmitted through the serial port. When the master sends the address 00000000 followed by the data 00000110, the device resets to the default condition, and generates and acknowledge.

I2C Latch-up. The 5003 may latch-up if the I2C bus is active and there is no power to the 5003 device. In a typical application, this will not occur as the I2C bus and the 5003 device are powered from the same power supply. This condition typically occurs when evaluating the 5003 devices on a demo board. When the I2C is powered on and the 5003 device is powered off, the I/O lines of the I2C bus are active and therefore will be at +5V. The *SDATA* pin internal ESD diodes will begin to conduct current through the *SDATA* pin and attempt to power-on internal circuits of the device. When power is applied to the 5003 device, circuits can be in an unknown state and therefore latch-up occurs. This is prevented by disconnecting the I2C interface when the device is powered down.

Power Supply Sequence: The 5003 require three power supplies (12V, 5V and –5V) for proper operation. Similar to other CMOS devices that are powered from multiple supplies, the 5003 family device requires proper power ramp-up sequence to avoid forwardly biasing the substrate diodes which can cause destructive latch-up. In order to insure that the chip substrate diodes are always reverse biased, the –5V supply should always be applied before the other two supplies. The preferred power ramp-up sequences is "–5V, +12V and then +5V." If this sequence can not be achieved, placing schottky diodes from –5V to ground and / or +12V to +5V supply, depending upon sequence and timing, can prevent latchup.

Serial Port Register Table (Write registers); Device Address = 10010000 (Bold indicates default setting)

REGISTER	FUNCTION	BITS	DESCRIPTION
0	TV Function Control	**xxxxxx00**	**Level 0; normal TV output (TV_Fnc = 0V)**
		xxxxxx01	Level 1A; 16:9 aspect ratio (TV_Fnc = 6V)
		xxxxxx10	Level 1B; Peritelevision output mode (TV_Fnc =11V)
		xxxxxx11	Level 1B; not valid mode (TV_Fnc =11V)
0	Digital Outputs (independent)	**xxxx00xx**	**DO_0, DO_1 are set LOW**
		xxxx11xx	DO_0, DO_1 are set HIGH
0	TV Mute Control*	**xxx0xxxx**	**TV audio (TV_Lout/TV_Rout, Lout/Rout/Mono) output = ON**
		xxx1xxxx	TV audio (TV_Lout/TV_Rout, Lout/Rout/Mono) output = Mute
0	n/a	**x00xxxxx**	**Reserved: Set these bits to "0" for normal operation**
0	RGB Sync Source	**0xxxxxxx**	**RGB sync /DC restore source = RGB**
		1xxxxxxx	RGB sync /DC restore source = TV_YC
1	TV RGB/ S video chroma Source (S Video has chroma on TV_R. TV_G & TV_B outputs are disabled.)	xxxxxx00	TV RGB signal source = Auxiliary SCART input (RGB)
		xxxxxx01	**TV RGB signal source = Video encoder IC,**
		xxxxxx10	TV RGB signal source = Video encoder IC, chroma on TV red
		xxxxxx11	TV RGB signal source = VCR SCART (red) chroma on TV red
1	TV composite video / Audio Source	xxxx00xx	TV composite & audio signal source = Auxiliary SCART input
		xxxx01xx	**TV composite & audio signal source = Video encoder IC audio DAC IC**
		xxxx10xx	TV composite & audio signal source = VCR SCART input
		xxxx11xx	TV composite (S video luma) & audio signal source = Video encoder IC (Enc_Y), audio DAC IC
1	VCR Signal Source	xx00xxxx	SVHS mode, source = Video encoder IC (Y & C), audio DAC IC
		xx01xxxx	VCR signal source = Auxiliary SCART composite input
		xx10xxxx	**VCR signal source = Video encoder IC (YC), audio DAC IC**
		xx11xxxx	VCR signal source = Video encoder IC (YC), audio DAC IC
1	Auxiliary Output Select	x0xxxxxx	Auxiliary signal source = VCR SCART input
		x1xxxxxx	**Auxiliary signal source = Video encoder IC, audio DAC IC**
1	TV Chroma RF output	**0xxxxxxx**	**TV_C (chroma RF) output: output disabled**
		1xxxxxxx	TV_C (chroma) output: = TV_R (for RF mod to sum Y & C)
2	TV Volume Control*	**xx000000**	**TV audio volume = normal (0 dB)**
		xx011111	TV audio volume = minimum (31 dB atten.)
2	n/a	**00xxxxxx**	

Serial Port Register Table (Read register); Device Address = 10010001 (Bold indicates default setting)

0	AUX Function Control Input	**xxxxxx00**	**Level 0; normal TV output (TV_Fnc = 0 volts)**
		xxxxxx01	Level 1A; 16:9 aspect ratio (TV_Fnc = 6 volts)
		xxxxxx10	Level 1B; Peritelevision output mode (TV_Fnc = 11 volts)
0	VCR Function Control Input	**xxxx00xx**	**Level 0; normal TV output (TV_Fnc = 0 volts)**
		xxxx01xx	Level 1A; 16:9 aspect ratio (TV_Fnc= 6 volts)
		xxxx10xx	Level 1B; Peritelevision output mode (TV_Fnc = 11 volts)
0	n/a	**0000xxxx**	**Reserved: These bits set to "0" in normal operation**

SCART Switching Table

INPUT PIN	OUTPUT PIN
AUX_R: Red input from AUX SCART Enc_R: Red input from video encoder IC Enc_C: Chroma input from video encoder IC SVHS_Cin: Chroma input from VCR SCART	TV_R: Red video output to TV or SVHS chroma output to TV
AUX_R: Red input from AUX SCART Enc_R: Red input from video encoder IC Enc_C: Chroma input from video encoder IC SVHS_Cin: Chroma input from VCR SCART	TV_C: Follows TV_R output. Chroma output to sum Y & C for RF modulator when TV in S video mode, On/off selectable
AUX_G: Green input from AUX SCART Enc_G: Green input from video encoder IC	TV_G: Green video output to TV
AUX_B: Blue input from AUX SCART Enc_B: Blue input from video encoder IC	TV_B: Blue video output to TV
ABLANK: Blanking input from AUX SCART EBLANK: Blanking input from video encoder IC	BLANK: TV blanking output for RGB
AUX_YCin: Composite input from AUX SCART Enc_YC: Composite input from video encoder IC Enc_Y: Luma input from video encoder IC VCR_YCin: Composite (YC or Y) input from VCR	TV_YCout: Composite video, RGB sync, or Luma output to TV
AUX_YCin: Composite input from AUX SCART Enc_YC: Composite input from video encoder IC Enc_Y: Luma input from video encoder IC VCR_YCin: Composite (YC or Y) input from VCR	TV_Mod: Follows TV_YCout output. Composite (or luma sum with chroma) output to RF modulator
AUX_YCin: Composite input from AUX SCART Enc_YC: Composite input from video encoder IC Enc_Y: Luma input from video encoder IC	VCR_YCout: Composite or Luma output to VCR
Enc_C: Chroma input from video encoder IC	SVHS_Cout: Chroma output to VCR
Enc_YC: Composite input from video encoder IC VCR_YCin: Composite input from VCR SCART	AUX_YCout: Composite video output to auxiliary SCART
AUX_Lin: Left audio input from AUX SCART Lin: Left audio input from audio DAC VCR_Lin: Left audio input from VCR SCART	Lout: Left audio output to RCA jack
AUX_Lin: Left audio input from AUX SCART Lin: Left audio input from audio DAC VCR_Lin: Left audio input from VCR SCART	TV_Lout: Left audio output to TV SCART
Lin: Left audio input from audio DAC VCR_Lin: Left audio input from VCR SCART	AUX_Lout: Left audio output to auxiliary SCART
AUX_Lin: Left audio input from AUX SCART Lin: Left audio input from audio DAC	VCR_Lout: Left audio output to VCR SCART
AUX_Rin: Right audio input from AUX SCART Rin: Right audio input from audio DAC VCR_Rin: Right audio input from VCR SCART	Rout: Right audio output to RCA jack
AUX_Rin: Right audio input from AUX SCART Rin: Right audio input from audio DAC VCR_Rin: Right audio input from VCR SCART	TV_Rout: Right audio output to TV SCART
Rin: Right audio input from audio DAC VCR_Rin: Right audio input from VCR SCART	AUX_Rout: Right audio output to auxiliary SCART
AUX_Rin: Right audio input from AUX SCART Rin: Right audio input from audio DAC	VCR_Rout: Right audio output to VCR SCART

PIN DESCRIPTIONS

NAME	TYPE	DESCRIPTION
Analog Pins:		
ABLANK	I	Auxiliary Blanking Input: In a typical system, this pin is connected to the RGB status pin (pin 16, fast blanking) from the auxiliary SCART connector.
AUX_R	I	Auxiliary Red Input: In a typical system, this pin is connected to the RED input pin (pin 15) of the auxiliary SCART connector. This input can be selected as the signal source for the TV_R output pin.
AUX_G	I	Auxiliary Green Input: In a typical system, this pin is connected to the GREEN input pin (pin 11) of the auxiliary SCART connector. This input can be selected as the signal source for the TV_G output pin.
AUX_B	I	Auxiliary Blue Input: In a typical system, this pin is connected to the BLUE input pin (pin 7) of the auxiliary SCART connector. This input can be selected as the signal source for the TV_B output pin.
AUX_Fnc	I	Function Switching Input, AUX: In a typical system, this pin is connected to pin 8 of the auxiliary SCART connector to monitor the function select input from that device. This input can identify three different levels and record the level in the serial port register.
AUX_YCin	I	Auxiliary Video Input: In a typical system, this pin is connected to the composite video input pin (pin 20) of the auxiliary SCART connector. This input can be selected as the signal source for the TV_YCout and/or VCR_YCout pins.
AUX_Lin	I	Auxiliary Left Audio Input: In a typical system, this pin is connected to the L Audio Output pin (pin 3) of the auxiliary SCART connector. This input can be selected as the signal source for the TV_Lout and/or VCR_Lout pins.
AUX_Rin	I	Auxiliary Right Audio Input: In a typical system, this pin is connected to the R Audio Output pin (pin 1) of the auxiliary SCART connector. This input can be selected as the signal source for the TV_Rout and/or VCR_Rout pins.
EBLANK	I	Encoder Blanking Input: In a typical system, this pin is connected to the fast blanking signal from the external video encoder device.
Enc_R	I	Encoder Red Input: In a typical system, this pin is connected to the RED output pin from the external video encoder device. This input can be selected as the signal source for the TV_R output pin.
Enc_G	I	Encoder Green Input: In a typical system, this pin is connected to the GREEN output pin from the external video encoder device. This input can be selected as the signal source for the TV_G output pin.
Enc_B	I	Encoder Blue Input: In a typical system, this pin is connected to the BLUE output pin from the external video encoder device. This input can be selected as the signal source for the TV_B output pin.
Enc_YC	I	Encoder Video Input: In a typical system, this pin is connected to the composite video output pin from the external video encoder device. This input can be selected as the signal source for the AUX_YCout, TV_YCout and/or VCR_YCout pins.
Enc_Y	I	Encoder Luminance Input: In a typical system, this pin is connected to the composite video output pin from the external video encoder device when operating S video. This input can be selected as the signal source for the TV_YCout and/or VCR_YCout pins.

PIN DESCRIPTIONS (continued)

NAME	TYPE	DESCRIPTION
Enc_C	I	Encoder Chrominance Input: In a typical system, this pin is connected to the TV_R output pin from the external video encoder device when operating S video. This input can be selected as the signal source for the TV_R and/or VCR's SVHS_Cout output pin.
Lin	I	Left Audio Input: In a typical system, this pin is connected to the left audio output pin of the external audio DAC. This input can be selected as the signal source for the TV_Lout, VCR_Lout and/or AUX_Lout pins.
Rin	I	Right Audio Input: In a typical system, this pin is connected to the right audio output pin of the external audio DAC. This input can be selected as the signal source for the TV_Rout, VCR_Rout and/or AUX_Rout pins.
SVHS_Cin	I	SVHS Chroma Input: In a typical system, this pin is connected to the SVHS Chroma pin (pin 15) on the VCR SCART connector. It provides chroma input from the VCR when the SVHS mode is selected for the TV connector.
VCR_YCin	I	VCR Video Input: In a typical system, this pin is connected to the composite video input pin (pin 20) of the VCR SCART connector. This input can be selected as the signal source for the TV_YCout and/or AUX_YCout pins.
VCR_Lin	I	VCR Left Audio Input: In a typical system, this pin is connected to the L Audio Output pin (pin 3) of the VCR SCART connector. This input can be selected as the signal source for the TV_Lout and/or AUX_Lout pins.
VCR_Rin	I	VCR Right Audio Input: In a typical system, this pin is connected to the R Audio Output pin (pin 1) of the VCR SCART connector. This input can be selected as the signal source for the TV_Rout and/or AUX_Rout pins.
VCR_Fnc	I	Function Switching Input, VCR: In a typical system, this pin is connected to pin 8 of the VCR SCART connector to monitor the function select input from that device. This input can identify three different levels and records the level in the serial port register.
AUXYCout	O	Auxiliary Video Output: This pin is the composite video output to the auxiliary SCART connector (pin 19).
AUX_Lout	O	Auxiliary Left Audio Output: This pin is the output to the left channel audio (pin 3) of the auxiliary SCART connector.
AUX_Rout	O	Auxiliary Right Audio Output: This pin is the output to the right channel audio (pin1) of the auxiliary SCART connector.
BLANK	O	Blanking output: This output provides the blanking signal to the TV SCART connector (pin 16). This signal is either the blanking signal from the auxiliary SCART connector (ABLANK) or the signal from the external video encoder (EBLANK).
Lout	O	Left Audio Output: This pin is the output to the left channel audio RCA jack.
Rout	O	Right Audio Output: This pin is the output to the right channel audio RCA jack.
Mono	O	Mono Audio Output: This pin is sum of Lout & Rout to the RF modulator input.
SVHS_Cout	O	SVHS Chroma Output: This pin is typically AC coupled to pin 15 of the VCR SCART connector. When the S-video mode is selected for the VCR connector, video from the video encoder input pin (Enc_C) is output to this pin
TV_YCout	O	TV Video Output: This pin is the composite video output to the TV SCART connector (pin 19). In the SVHS mode, this pin provides luminance information.

PIN DESCRIPTIONS (continued)

NAME	TYPE	DESCRIPTION
TV_Mod	O	TV Modulator Video Output: This pin follows the composite video output to the *TV_YCout* signal to the TV SCART connector. It provides composite video for an external RF modulator. In S video mode, it provides luminance information only
TV_R	O	TV Red Output: This pin provides Red video output to the TV SCART connector (pin 15). In S video mode, this pin provides the chroma information.
TV_C	O	TV Chroma Output: This pin provides chroma signal to sum with TV_Mod's luminance when operating in S video mode for composite video signal for RF modulator. It is on/off selectable.
TV_G	O	TV Green Output: This pin provides Green video output to the TV SCART connector (pin 11).
TV_B	O	TV Blue Output: This pin provides Blue video output to the TV SCART connector (pin 7).
TV_Lout	O	TV Left Audio Output: This pin is the output to the left channel audio (pin 3) of the TV SCART connector.
TV_Rout	O	TV Right Audio Output: This pin is the output to the right channel audio (pin1) of the TV SCART connector.
TV_Fnc	O	Function Output TV: This pin is the function switching output to the TV SCART connector pin 8. The output level is determined by the serial port write register.
VCR_YCout	O	VCR Video Output: This pin is the composite video output to the VCR SCART connector (pin 20). In the SVHS mode, this pin provides luminance information from the video encoder IC (pin Enc_Y).
VCR_Lout	O	VCR Left Audio Output: This pin is the output to the left channel audio (pin 3) of the VCR SCART connector.
VCR_Rout	O	VCR Right Audio Output: This pin is the output to the right channel audio (pin1) of the VCR SCART connector.
Digital Pins:		
DO_0	O	Digital Output 0: This pin is a general purpose output that is controlled by serial port register.
DO_1	O	Digital Output 1: This pin is a general purpose output that is controlled by serial port register.
SCLK	I	Serial Clock Input: This pin accepts a serial port clock input signal.
SDATA	I	Serial Data Input: This is a tri-state pin that receives or transmits serial data.
Power/Ground Pins:		
VCC	-	+5 VDC power inputs.
VEE	-	-5 VDC power inputs.
VDD	-	+12 VDC power input for function switching
Vref	-	Internal voltage reference, bypass pin. Add capacitor 4.7 uF to ground.
GND	-	Ground for all blocks.
Rbias	-	Bias point of internal current generator. Add resistor 10k to ground.
Tgen	-	Reference point for internal timing circuit. Add capacitor 470 pF to ground.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device

PARAMETER	RATING	UNIT
Storage temperature	-55 to 150	°C
Junction operating temperature	+150	°C
Positive supply voltages	-0.3 < VCC < 6V; VCC-0.3 < VDD < 13	V
Negative supply voltages	-6 < VEE < +0.3	V
Voltage applied to Digital Inputs	-0.3V to VCC+0.3	V
audio/video input pins	VEE -0.3V to VCC+0.3	V
function input pins (300 Ω source)	-0.3V to +15	V

TARGET SPECIFICATIONS

Unless otherwise specified: 0° < Ta < 70 °C; power supplies VCC = +5.0 V ±5%, VEE = -5.0 V ±5% VDD = 12.0 V ±5%.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Operating Characteristics					
Power supply currents	All outputs loaded				mA
	VCC (+5 VDC)		130	150	
	VEE (-5 VDC)	-65	-45		
	VDD (+12 VDC)		18	28	
PSRR	f_{in} = 100 Hz, 0.1 Vpp on VCC/ VEE	40			dB
Switch time	From serial data acknowledge		2.0		µsec
Serial Port Timing (reference timing diagram on page 15)					
SCLK Input Frequency				400	kHz
SCLK LOW time (t_{CL})		1.3			µsec
SCLK HIGH time (t_{CH})		0.6			µsec
Rise time (t_{RT})	*SCLK* and *SDATA*			300	nsec
Fall time (t_{FT})	*SCLK* and *SDATA*			300	nsec
Data set-up time* (t_{DSU})	*SDATA* change to *SCLK* HIGH	100			nsec
Data hold time* (t_{DH})	*SCLK* LOW to *SDATA* change	0			nsec
Start set-up time (t_{SSU})		0.6			µsec
Start hold time (t_{SH})		0.6			µsec
Glitch rejection	maximum pulse on *SCLK* and/or *SDATA*			50	nsec
* These specifications also apply to an acknowledge generated by the device.					

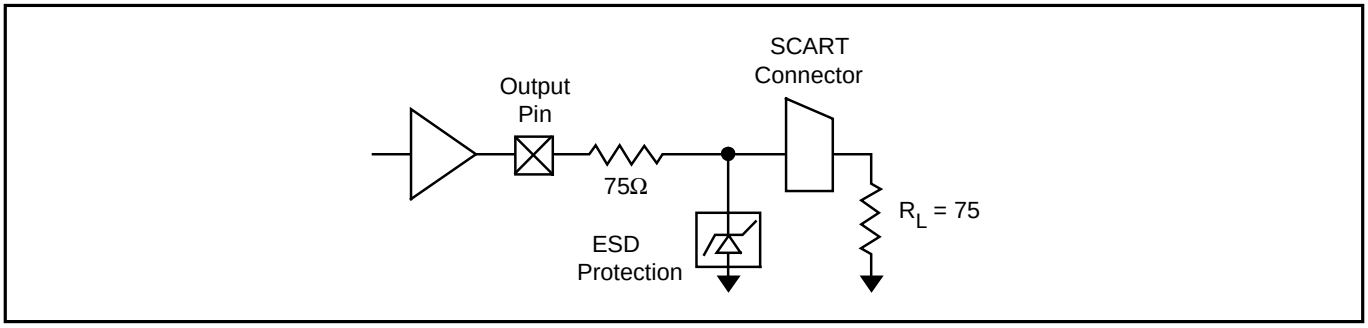
PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Digital I/O Characteristics (SCLK, SDATA)					
High level input voltage		0.7* VCC		VCC+0.3	V
Low level input voltage		GND-0.3		0.3* VCC	V
High level input current	Vin = Vcc - 1.0V	-10		10	µA
Low level input current	Vin = 1.0V	-10		-10	µA
Low level output voltage (SDATA)	I_{OL} = 3 mA		0.4	0.6	V
Fall time (t_{FT})(SDATA) acknowledge or read	V_{IH} MIN to V_{IL} Max with CL = 400 pF			250	nS
Digital I/O Characteristics (DO_0, DO_1, TV_Fnc, AUX_Fnc, VCR_Fnc)					
Digital output low level output voltage	DO_0, DO_1, Register bits read 0 4.7 k pullup		0.4		V
TV_Fnc output level 10 k load	Register 0 = xxxxxx00 Register 0 = xxxxxx01 Register 0 = xxxxxx10 or 11	0.0 5.0 10.0	1.0 6.0 10.5	1.2 6.5 VDD	V V V
AUX_Fnc/VCR_Fnc input levels	Register bits read 00 Register bits read 01 Register bits read 10	0.0 4.5 9.5		2.0 7.0 VDD	V V V

Video Characteristics - Unless otherwise noted, typical output loading on all video outputs is 150 Ω. All video outputs are capable of withstanding a sustained 75 ohm load to ground without damage.

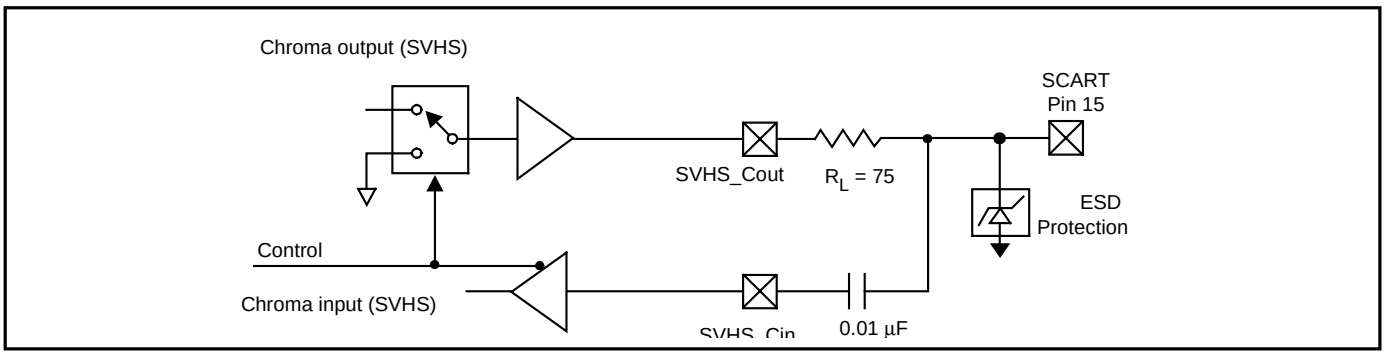
Input impedance	All video inputs	100			kΩ
Input dynamic range	f_{in} = 100 kHz, THD < 1.0%		1.25		Vpp
Gain	1.0 Vpp input, f_{in} = 100 kHz	1.9	2.0	2.1	V/V
Output gain inequality	RGB or SVHS output channel to channel	-2.5		2.5	%
Output DC level at IC pin					V
Blank level clamp voltage	RGB, CVBS or luma		1.3		V
Average level	chroma		1.9		V
Signal to noise ratio	1 Vpp input	58	65		dB
Cross talk	f_{in} = 4.43 MHz, 1 Vpp			-45	dB
Output to output differential delay	RGB signals, f_{in} = 100 kHz	-20		20	nsec
Blanking level	Input or output, logical “0”	0.0		0.4	V
	Input or output, logical “1”	1.0		3.0	V
Blanking delay	BLANK to RGB signals	-50		50	nsec
Differential phase	TV_YCout	-3.0		2.5	Deg.
Differential gain	TV_YCout	-5		5	%

Audio Characteristics - Unless otherwise noted, all audio outputs shall drive a load of 10 kΩ. All audio outputs will withstand a sustained short to ground without damage.

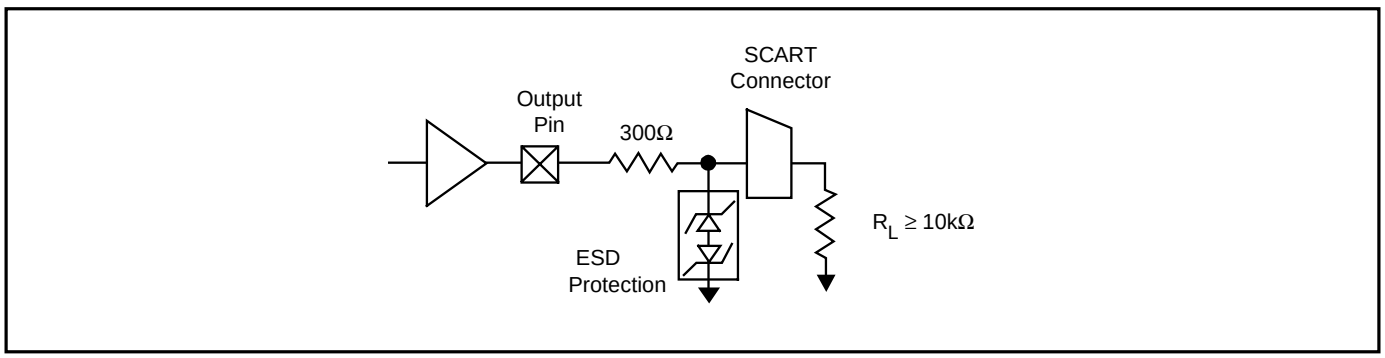
PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input impedance		20	50		kΩ
Gain	f_{in} = 1.0 kHz, 1 Vpp	0.95	1.0	1.05	V/V
Frequency response	1 Vpp input				
	Flat within ± 0.3 dB	20			kHz
	Measured -3 dB point	100			kHz
Signal to Noise ratio A weighting filter	f_{in} = 1.0 kHz, 2 Vrms, 0 dB attenuation	90			dB
Distortion (THD)	f_{in} = 1.0 kHz, 1 Vrms, 0 dB attenuation		.02	0.05	%
	f_{in} = 1.0 kHz, 2 Vrms, 0 dB attenuation			0.10	%
Output impedance			TBD		Ω
Output DC Offset	Input to Output, Stereo	-40		40	mV
Output DC Offset	Input to Output, Mod_Mono	-45		45	mV
Output phase matching	f_{in} = 1.0 kHz, 1 Vrms; any stereo pair		0.5		Deg.
Channel separation Left - Right	f_{in} = 1.0 kHz, 1 Vrms, 0 dB attenuation	80			dB
Channel separation channel - channel					
Output attenuation (volume control)	TV_Lout/TV_Rout				
	Register 2 = xx000000, Mute = OFF		0		dB
	Register 2 = xx011111, Mute = OFF		-31		dB
	Mute ON (Register 0 = xxx1xxxx)		-75		dB
Attenuation accuracy	5 bit (0 – 31 dB)	-5		5	%
Audio to video path delay	Video input = 1.0 Vpp @ 100 kHz		1.5		µsec
	Audio input = 1.0 kHz, 1 Vrms				



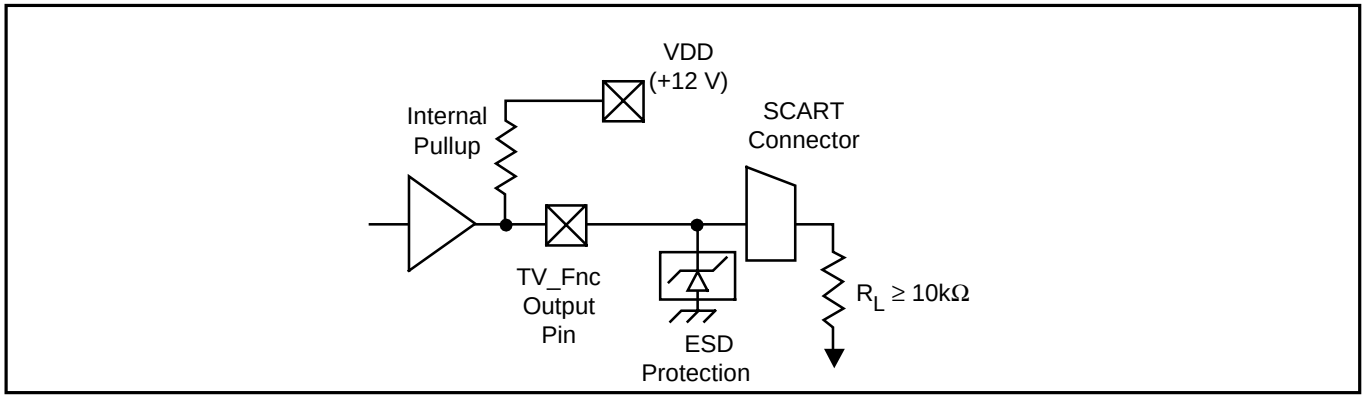
Video Output Load (Typical)



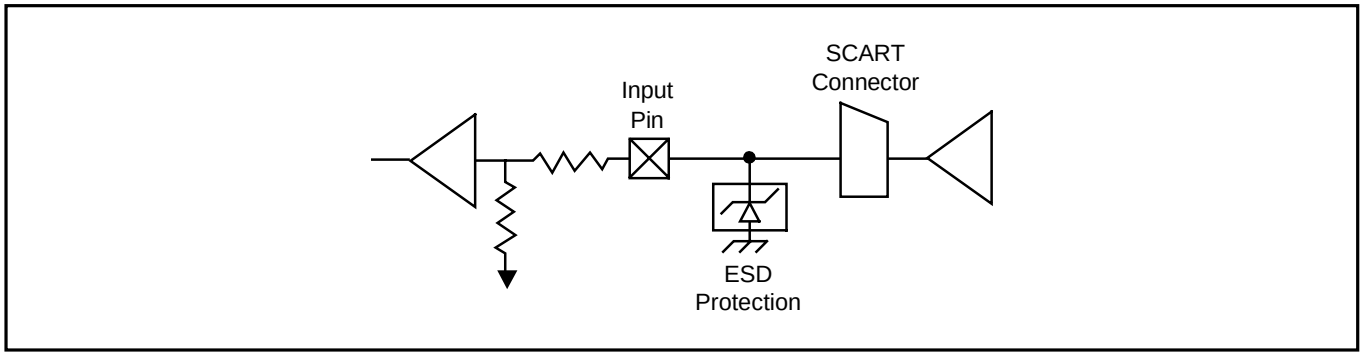
VCR SCART pin 15 Load (Typical)



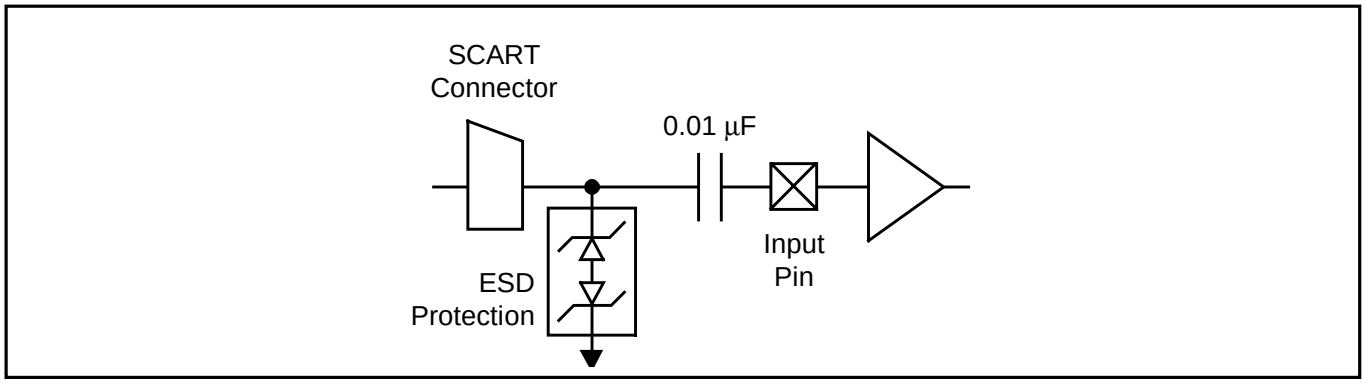
Audio Output Load (Typical)



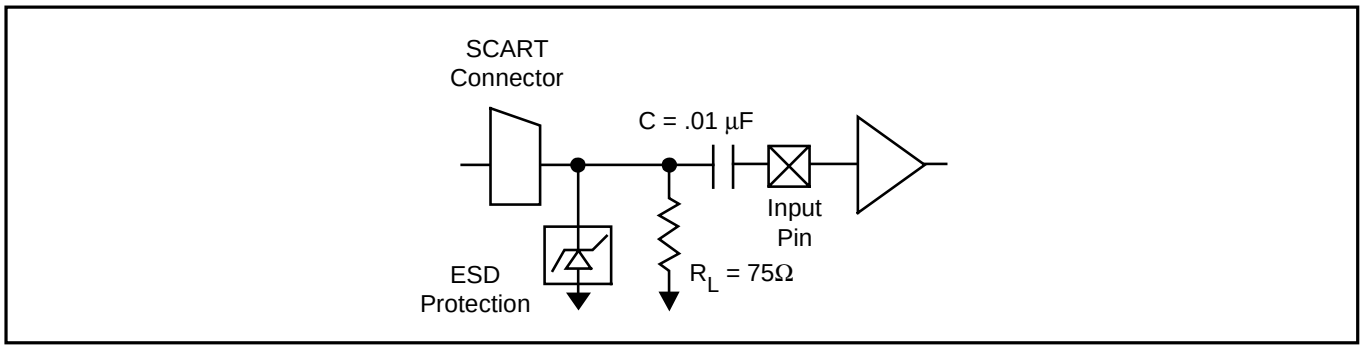
TV Function Switching (Typical)



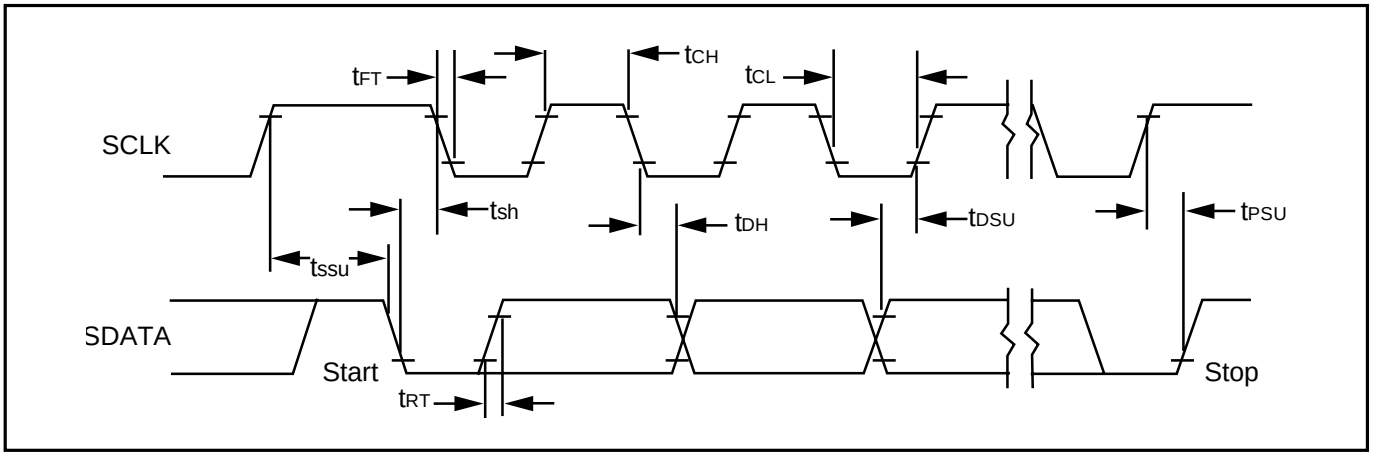
VCR/AUX Function Switching Input (Typical)



SCART Audio Input (Typical)



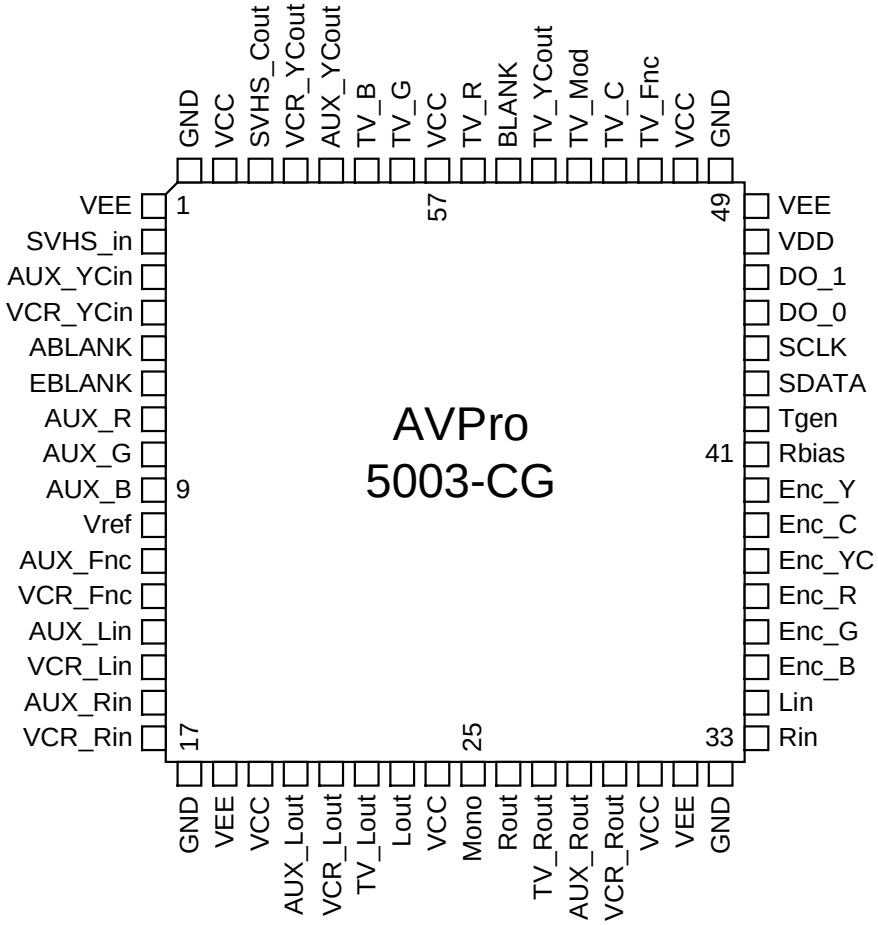
Video Input (Typical)



Serial Port Timing (Typical)

PACKAGE PIN DESIGNATIONS

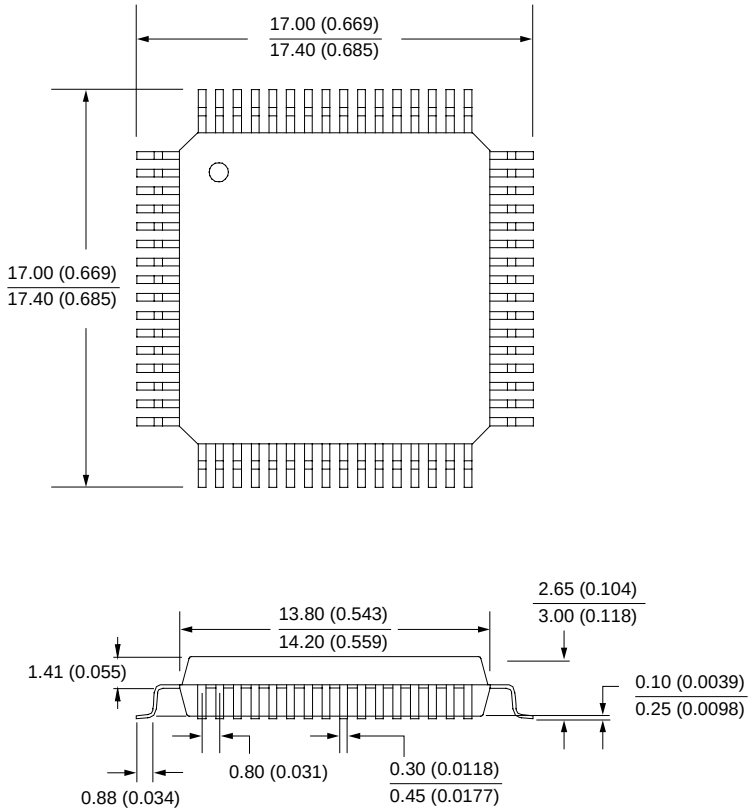
(Top View)



64-Lead Quad Flatpack (MQFP)
AVPro® 5003

MECHANICAL DRAWING

64-Lead QFP



ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PACKAGE MARK
AVPro® 5003 Triple audio/video switch	AVPro 5003-CG	AVPro® 5003-CG

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