

# DATA SHEET

## **PMBF170**

**N-channel enhancement mode  
vertical D-MOS transistor**

Product specification  
File under Discrete Semiconductors, SC13b

April 1995

# N-channel enhancement mode vertical D-MOS transistor

**PMBF170**

## DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. Designed for use as a Surface Mounted Device (SMD) in thin and thick-film circuits with applications in relay, high-speed and line transformer drivers.

## FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

## QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$I_D$	max.	250 mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	300 mW
Drain-source on-resistance $I_D = 200\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DS(on)}$	typ.	2.5 $\Omega$
		max.	5.0 $\Omega$
Transfer admittance $I_D = 200\text{ mA}; V_{DS} = 10\text{ V}$	$ Y_{fs} $	min.	100 mS
		typ.	200 mS

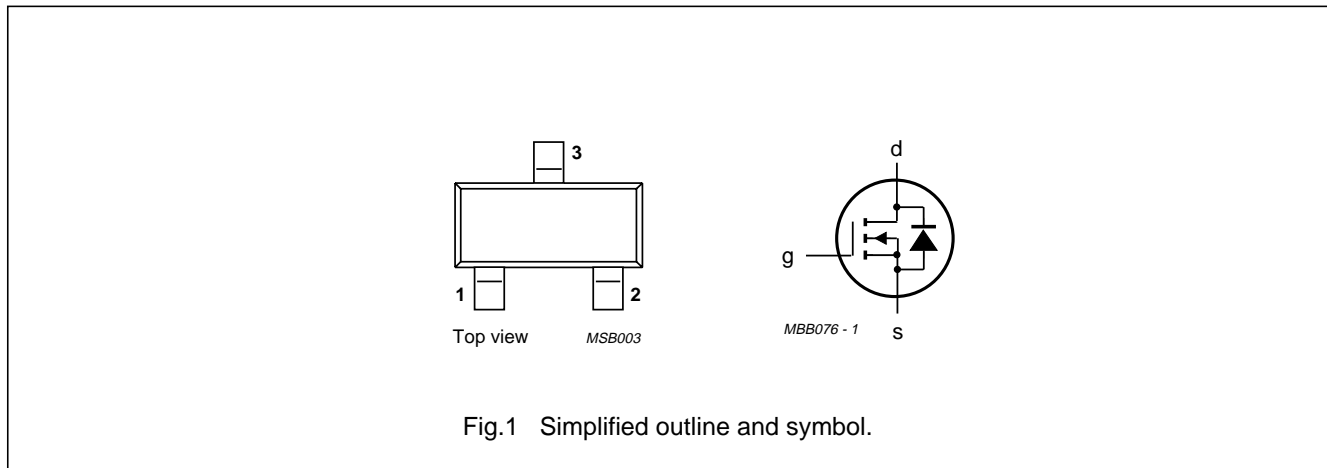
## PINNING - SOT23

- 1 = gate
- 2 = source
- 3 = drain

Marking code:

PMBF170 = PKX

## PIN CONFIGURATION



## N-channel enhancement mode vertical D-MOS transistor

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### RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$I_D$	max.	250 mA
Drain current (peak)	$I_{DM}$	max.	500 mA
Total power dissipation up to $T_{amb} = 25\text{ °C}$ (note 1)	$P_{tot}$	max.	300 mW (note 1)
		max.	250 mW (note 2)
Storage temperature range	$T_{stg}$		-65 to +150 °C
Junction temperature	$T_j$	max.	150 °C

### THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j-a}$	=	430 K/W
From junction to ambient (note 2)	$R_{th\ j-a}$	=	500 K/W

### Notes

1. Mounted on ceramic substrate measuring 10 mm × 8 mm × 0.7 mm.
2. Mounted on printed-circuit board.

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### CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified

Drain-source breakdown voltage

$I_D = 10\text{ }\mu\text{A}; V_{GS} = 0$

$V_{(BR)DSS}$	min.	60 V
	typ.	90 V

Drain-source leakage current

$V_{DS} = 25\text{ V}; V_{GS} = 0$

$I_{DSS}$	max.	500 nA
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$V_{DS} = 48\text{ V}; V_{GS} = 0$

$I_{DSS}$	max.	1 $\mu\text{A}$
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Gate-source leakage current

$V_{GS} = 15\text{ V}; V_{DS} = 0$

$I_{GSS}$	max.	10 nA
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Gate-source cut-off voltage

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

$V_{GS(th)}$	min.	0.8 V
	max.	3.0 V

Drain-source on-resistance

$I_D = 200\text{ mA}; V_{GS} = 10\text{ V}$

$R_{DS(on)}$	typ.	2.5 $\Omega$
	max.	5.0 $\Omega$

Transfer admittance

$I_D = 200\text{ mA}; V_{DS} = 10\text{ V}$

$ Y_{fs} $	min.	100 mS
	typ.	200 mS

Input capacitance

$V_{DS} = 10\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

$C_{iss}$	typ.	25 pF
	max.	40 pF

Output capacitance

$V_{DS} = 10\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

$C_{oss}$	typ.	22 pF
	max.	30 pF

Feedback capacitance

$V_{DS} = 10\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

$C_{rss}$	typ.	6 pF
	max.	10 pF

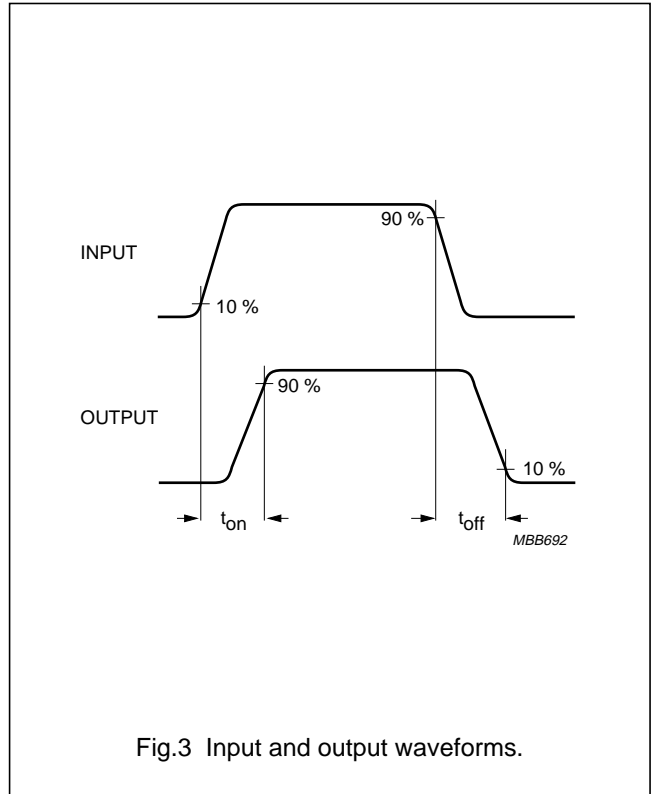
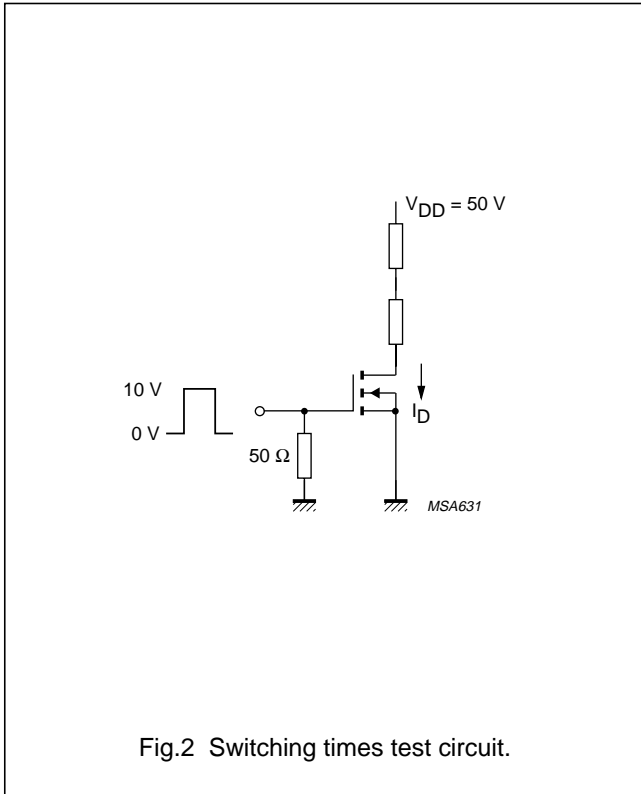
Switching times

$V_{GS} = 0\text{ to }10\text{ V}; I_D = 200\text{ mA}; V_{DD} = 50\text{ V}$

$t_{on}$	max.	10 ns
$t_{off}$	max.	15 ns

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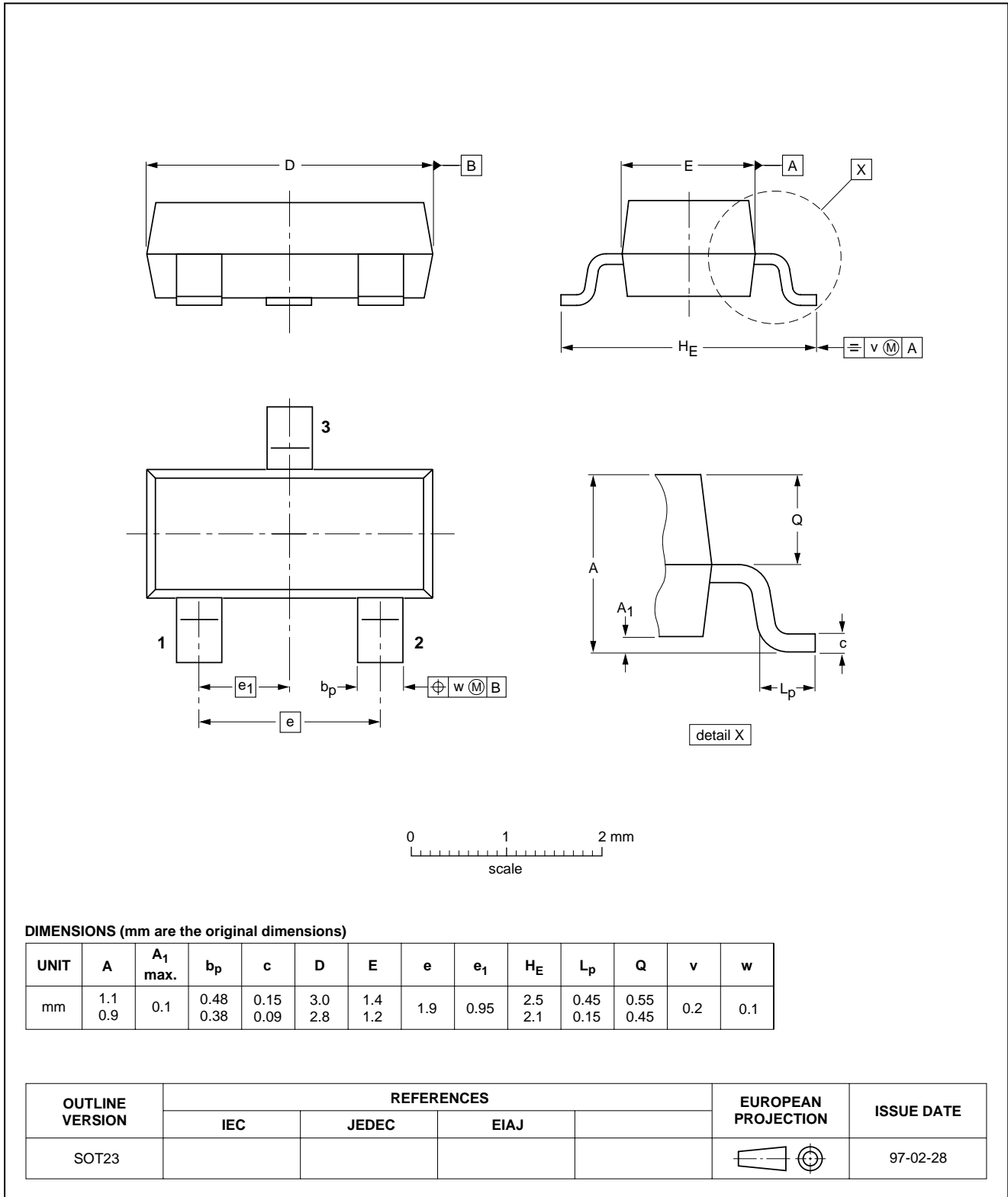
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## PACKAGE OUTLINES

Plastic surface mounted package; 3 leads

SOT23



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**PMBF170****DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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