NEC

MOS INTEGRATED CIRCUIT

μPD161643

176-OUTPUT TFT-LCD GATE DRIVER

DESCRIPTION

The μPD161643 is a TFT-LCD gate driver. Because this gate driver has a level shift circuit for logic input, it can output a high gate scanning voltage in response to a CMOS-level input.

FEATURES

- High-withstanding-voltage output (V_T-V_{EE} = 42 V MAX.)
- 3.0 V CMOS level input
- Number of output: 176

ORDERING INFORMATION

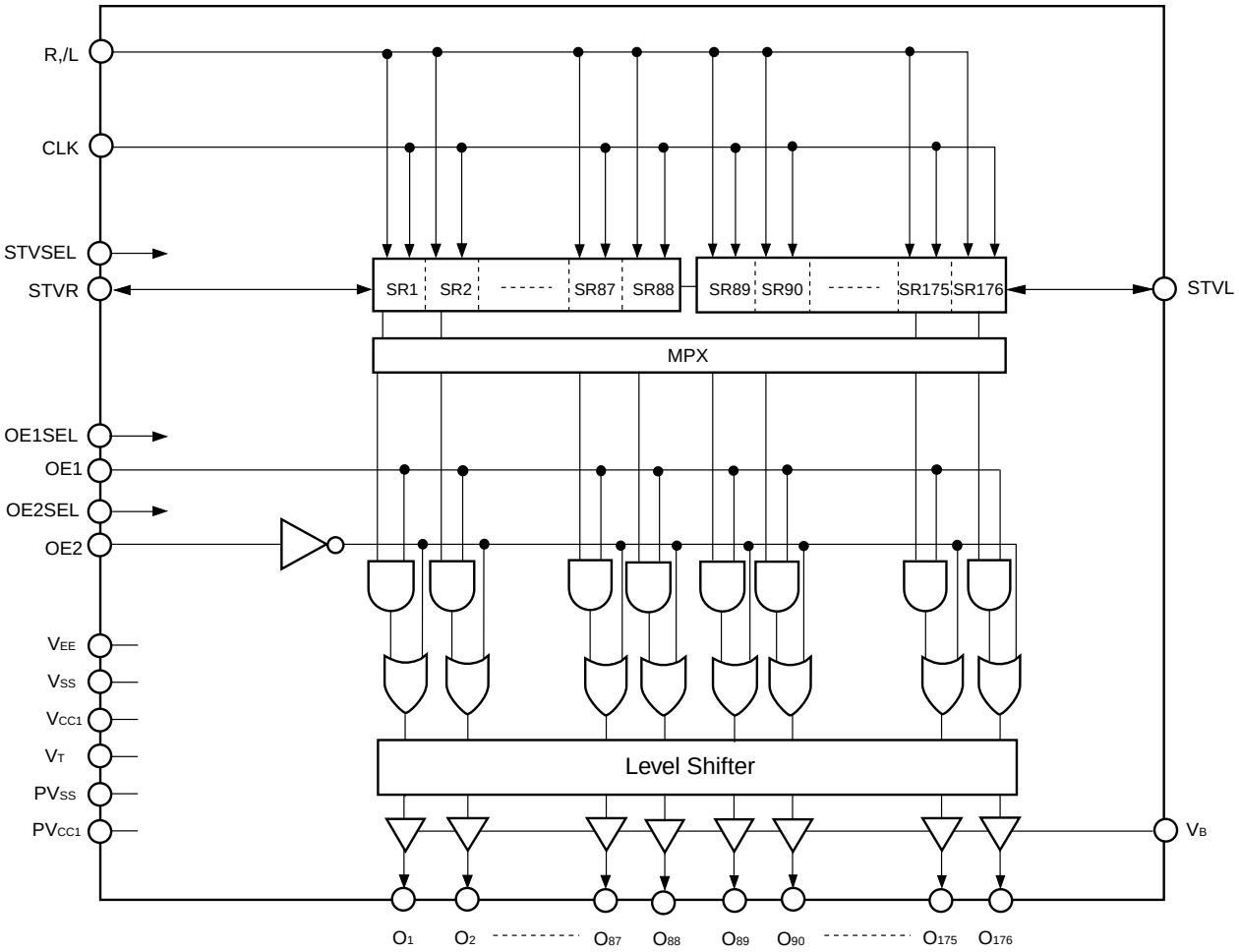
	Part number	Package
★	μPD161643P	Chip

Remark Purchasing the above chip entails the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representatives.

Document No. S15796EJ1V0DS00 (1st edition)
Date Published February 2003 NS CP(K)
Printed in Japan

The mark ★ shows major revised points.

1. BLOCK DIAGRAM



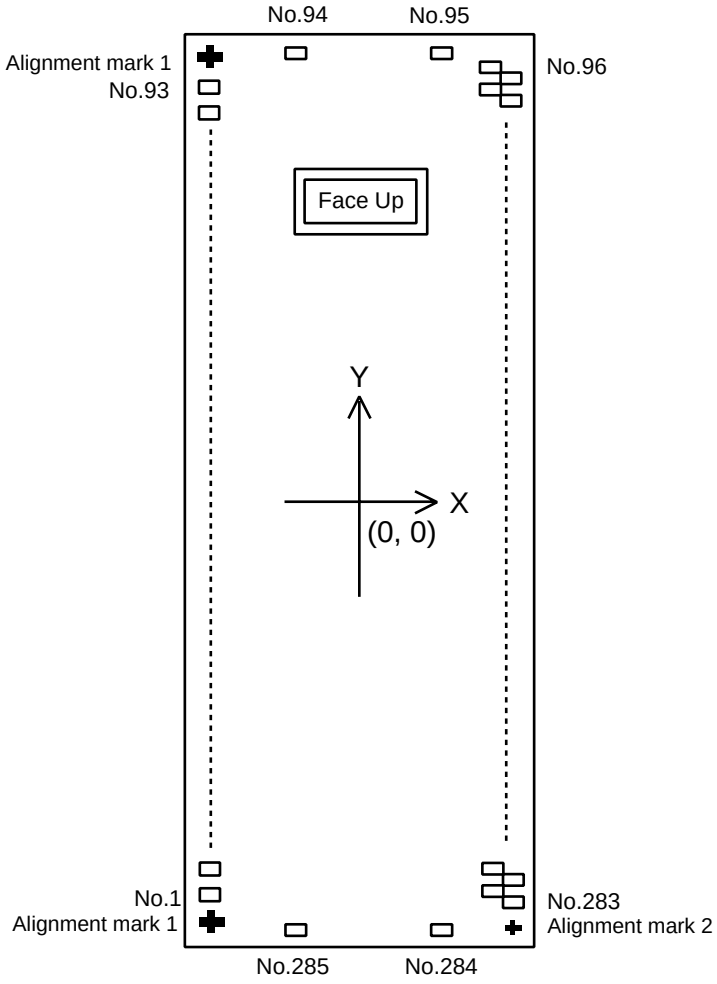
Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (PAD LAYOUT)

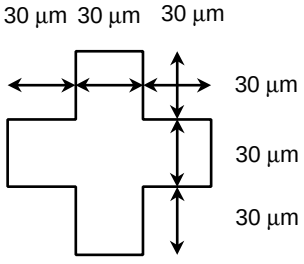
Chip size: 2.3 x 7.05 mm^2

Bump size: INPUT/LEFT/RIGHT (include INPUT/OUTPUT/RIGHT side DUMMY): 49 x 85 μm^2

OUTPUT (include OUTPUT side DUMMY): 35 x 94 μm^2



Alignment mark 1



Alignment mark 2

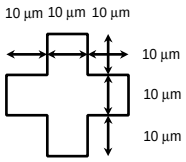


Table 2–1. Pad Layout (1/4)

Gate Inputs 70 μm pitch			
Pad No.	Pad Name	X [mm]	Y [mm]
-	Alignment Mark1	-0.9995	-3.3745
1	DUMMY	-0.9995	-3.2200
2	DUMMY	-0.9995	-3.1500
3	DUMMY	-0.9995	-3.0800
4	DUMMY	-0.9995	-3.0100
5	DUMMY	-0.9995	-2.9400
6	DUMMY	-0.9995	-2.8700
7	DUMMY	-0.9995	-2.8000
8	DUMMY	-0.9995	-2.7300
9	DUMMY	-0.9995	-2.6600
10	DUMMY	-0.9995	-2.5900
11	DUMMY	-0.9995	-2.5200
12	DUMMY	-0.9995	-2.4500
13	DUMMY	-0.9995	-2.3800
14	DUMMY	-0.9995	-2.3100
15	DUMMY	-0.9995	-2.2400
16	DUMMY	-0.9995	-2.1700
17	DUMMY	-0.9995	-2.1000
18	DUMMY	-0.9995	-2.0300
19	DUMMY	-0.9995	-1.9600
20	DUMMY	-0.9995	-1.8900
21	DUMMY	-0.9995	-1.8200
22	DUMMY	-0.9995	-1.7500
23	DUMMY	-0.9995	-1.6800
24	DUMMY	-0.9995	-1.6100
25	DUMMY	-0.9995	-1.5400
26	DUMMY	-0.9995	-1.4700
27	DUMMY	-0.9995	-1.4000
28	PVCC1	-0.9995	-1.3300
29	OE1SEL	-0.9995	-1.2600
30	OE1SEL	-0.9995	-1.1900
31	PVSS	-0.9995	-1.1200
32	OE2SEL	-0.9995	-1.0500
33	OE2SEL	-0.9995	-0.9800
34	PVCC1	-0.9995	-0.9100
35	STVSEL	-0.9995	-0.8400
36	STVSEL	-0.9995	-0.7700
37	PVSS	-0.9995	-0.7000
38	R,/L	-0.9995	-0.6300
39	R,/L	-0.9995	-0.5600
40	PVCC1	-0.9995	-0.4900
41	DUMMY	-0.9995	-0.4200
42	DUMMY	-0.9995	-0.3500
43	VT	-0.9995	-0.2800
44	VT	-0.9995	-0.2100
45	VT	-0.9995	-0.1400
46	VT	-0.9995	-0.0700
47	VT	-0.9995	0.0000
48	DUMMY	-0.9995	0.0700
49	DUMMY	-0.9995	0.1400
50	VCC1	-0.9995	0.2100
51	VCC1	-0.9995	0.2800
52	VCC1	-0.9995	0.3500
53	VCC1	-0.9995	0.4200
54	VCC1	-0.9995	0.4900
55	DUMMY	-0.9995	0.5600
56	DUMMY	-0.9995	0.6300
57	VSS	-0.9995	0.7000
58	VSS	-0.9995	0.7700
59	VSS	-0.9995	0.8400
60	VSS	-0.9995	0.9100
61	VSS	-0.9995	0.9800
62	DUMMY	-0.9995	1.0500
63	DUMMY	-0.9995	1.1200
64	VEE	-0.9995	1.1900
65	VEE	-0.9995	1.2600

Gate Inputs 70 μm pitch			
Pad No.	Pad Name	X [mm]	Y [mm]
66	VEE	-0.9995	1.3300
67	VEE	-0.9995	1.4000
68	VEE	-0.9995	1.4700
69	DUMMY	-0.9995	1.5400
70	DUMMY	-0.9995	1.6100
71	VB	-0.9995	1.6800
72	VB	-0.9995	1.7500
73	VB	-0.9995	1.8200
74	VB	-0.9995	1.8900
75	VB	-0.9995	1.9600
76	DUMMY	-0.9995	2.0300
77	DUMMY	-0.9995	2.1000
78	STVR	-0.9995	2.1700
79	STVR	-0.9995	2.2400
80	DUMMY	-0.9995	2.3100
81	STVL	-0.9995	2.3800
82	STVL	-0.9995	2.4500
83	DUMMY	-0.9995	2.5200
84	CLK	-0.9995	2.5900
85	CLK	-0.9995	2.6600
86	DUMMY	-0.9995	2.7300
87	OE1	-0.9995	2.8000
88	OE1	-0.9995	2.8700
89	DUMMY	-0.9995	2.9400
90	OE2	-0.9995	3.0100
91	OE2	-0.9995	3.0800
92	DUMMY	-0.9995	3.1500
93	DUMMY	-0.9995	3.2200
-	Alignment Mark1	-0.9995	3.3745

Table 2–1. Pad Layout (2/4)

Gate Outputs 35 μm pitch			
Pad No.	Pad Name	X [mm]	Y [mm]
96	DUMMY	0.8650	3.2725
97	DUMMY	0.9950	3.2375
98	DUMMY	0.8650	3.2025
99	DUMMY	0.9950	3.1675
100	DUMMY	0.8650	3.1325
101	DUMMY	0.9950	3.0975
102	O176	0.8650	3.0625
103	O175	0.9950	3.0275
104	O174	0.8650	2.9925
105	O173	0.9950	2.9575
106	O172	0.8650	2.9225
107	O171	0.9950	2.8875
108	O170	0.8650	2.8525
109	O169	0.9950	2.8175
110	O168	0.8650	2.7825
111	O167	0.9950	2.7475
112	O166	0.8650	2.7125
113	O165	0.9950	2.6775
114	O164	0.8650	2.6425
115	O163	0.9950	2.6075
116	O162	0.8650	2.5725
117	O161	0.9950	2.5375
118	O160	0.8650	2.5025
119	O159	0.9950	2.4675
120	O158	0.8650	2.4325
121	O157	0.9950	2.3975
122	O156	0.8650	2.3625
123	O155	0.9950	2.3275
124	O154	0.8650	2.2925
125	O153	0.9950	2.2575
126	O152	0.8650	2.2225
127	O151	0.9950	2.1875
128	O150	0.8650	2.1525
129	O149	0.9950	2.1175
130	O148	0.8650	2.0825
131	O147	0.9950	2.0475
132	O146	0.8650	2.0125
133	O145	0.9950	1.9775
134	O144	0.8650	1.9425
135	O143	0.9950	1.9075
136	O142	0.8650	1.8725
137	O141	0.9950	1.8375
138	O140	0.8650	1.8025
139	O139	0.9950	1.7675
140	O138	0.8650	1.7325
141	O137	0.9950	1.6975
142	O136	0.8650	1.6625
143	O135	0.9950	1.6275
144	O134	0.8650	1.5925
145	O133	0.9950	1.5575
146	O132	0.8650	1.5225
147	O131	0.9950	1.4875
148	O130	0.8650	1.4525
149	O129	0.9950	1.4175
150	O128	0.8650	1.3825
151	O127	0.9950	1.3475
152	O126	0.8650	1.3125
153	O125	0.9950	1.2775
154	O124	0.8650	1.2425
155	O123	0.9950	1.2075
156	O122	0.8650	1.1725
157	O121	0.9950	1.1375
158	O120	0.8650	1.1025
159	O119	0.9950	1.0675
160	O118	0.8650	1.0325

Gate Outputs 35 μm pitch			
Pad No.	Pad Name	X [mm]	Y [mm]
161	O117	0.9950	0.9975
162	O116	0.8650	0.9625
163	O115	0.9950	0.9275
164	O114	0.8650	0.8925
165	O113	0.9950	0.8575
166	O112	0.8650	0.8225
167	O111	0.9950	0.7875
168	O110	0.8650	0.7525
169	O109	0.9950	0.7175
170	O108	0.8650	0.6825
171	O107	0.9950	0.6475
172	O106	0.8650	0.6125
173	O105	0.9950	0.5775
174	O104	0.8650	0.5425
175	O103	0.9950	0.5075
176	O102	0.8650	0.4725
177	O101	0.9950	0.4375
178	O100	0.8650	0.4025
179	O99	0.9950	0.3675
180	O98	0.8650	0.3325
181	O97	0.9950	0.2975
182	O96	0.8650	0.2625
183	O95	0.9950	0.2275
184	O94	0.8650	0.1925
185	O93	0.9950	0.1575
186	O92	0.8650	0.1225
187	O91	0.9950	0.0875
188	O90	0.8650	0.0525
189	O89	0.9950	0.0175
190	O88	0.8650	-0.0175
191	O87	0.9950	-0.0525
192	O86	0.8650	-0.0875
193	O85	0.9950	-0.1225
194	O84	0.8650	-0.1575
195	O83	0.9950	-0.1925
196	O82	0.8650	-0.2275
197	O81	0.9950	-0.2625
198	O80	0.8650	-0.2975
199	O79	0.9950	-0.3325
200	O78	0.8650	-0.3675
201	O77	0.9950	-0.4025
202	O76	0.8650	-0.4375
203	O75	0.9950	-0.4725
204	O74	0.8650	-0.5075
205	O73	0.9950	-0.5425
206	O72	0.8650	-0.5775
207	O71	0.9950	-0.6125
208	O70	0.8650	-0.6475
209	O69	0.9950	-0.6825
210	O68	0.8650	-0.7175
211	O67	0.9950	-0.7525
212	O66	0.8650	-0.7875
213	O65	0.9950	-0.8225
214	O64	0.8650	-0.8575
215	O63	0.9950	-0.8925
216	O62	0.8650	-0.9275
217	O61	0.9950	-0.9625
218	O60	0.8650	-0.9975
219	O59	0.9950	-1.0325
220	O58	0.8650	-1.0675
221	O57	0.9950	-1.1025
222	O56	0.8650	-1.1375
223	O55	0.9950	-1.1725
224	O54	0.8650	-1.2075
225	O53	0.9950	-1.2425

Table 2–1. Pad Layout (3/4)

Gate Outputs 35 μm pitch			
Pad No.	Pad Name	X [mm]	Y [mm]
226	O52	0.8650	-1.2775
227	O51	0.9950	-1.3125
228	O50	0.8650	-1.3475
229	O49	0.9950	-1.3825
230	O48	0.8650	-1.4175
231	O47	0.9950	-1.4525
232	O46	0.8650	-1.4875
233	O45	0.9950	-1.5225
234	O44	0.8650	-1.5575
235	O43	0.9950	-1.5925
236	O42	0.8650	-1.6275
237	O41	0.9950	-1.6625
238	O40	0.8650	-1.6975
239	O39	0.9950	-1.7325
240	O38	0.8650	-1.7675
241	O37	0.9950	-1.8025
242	O36	0.8650	-1.8375
243	O35	0.9950	-1.8725
244	O34	0.8650	-1.9075
245	O33	0.9950	-1.9425
246	O32	0.8650	-1.9775
247	O31	0.9950	-2.0125
248	O30	0.8650	-2.0475
249	O29	0.9950	-2.0825
250	O28	0.8650	-2.1175
251	O27	0.9950	-2.1525
252	O26	0.8650	-2.1875
253	O25	0.9950	-2.2225
254	O24	0.8650	-2.2575
255	O23	0.9950	-2.2925
256	O22	0.8650	-2.3275
257	O21	0.9950	-2.3625
258	O20	0.8650	-2.3975
259	O19	0.9950	-2.4325
260	O18	0.8650	-2.4675
261	O17	0.9950	-2.5025
262	O16	0.8650	-2.5375
263	O15	0.9950	-2.5725
264	O14	0.8650	-2.6075
265	O13	0.9950	-2.6425
266	O12	0.8650	-2.6775
267	O11	0.9950	-2.7125
268	O10	0.8650	-2.7475
269	O9	0.9950	-2.7825
270	O8	0.8650	-2.8175
271	O7	0.9950	-2.8525
272	O6	0.8650	-2.8875
273	O5	0.9950	-2.9225
274	O4	0.8650	-2.9575
275	O3	0.9950	-2.9925
276	O2	0.8650	-3.0275
277	O1	0.9950	-3.0625
278	DUMMY	0.8650	-3.0975
279	DUMMY	0.9950	-3.1325
280	DUMMY	0.8650	-3.1675
281	DUMMY	0.9950	-3.2025
282	DUMMY	0.8650	-3.2375
283	DUMMY	0.9950	-3.2725

Table 2–1. Pad Layout (4/4)

Gate Left 600 μm pitch			
Pad No.	Pad Name	X [mm]	Y [mm]
94	DUMMY	-0.3000	3.3925
95	DUMMY	0.3000	3.3925

Gate Right 600 μm pitch			
Pad No.	Pad Name	X [mm]	Y [mm]
284	DUMMY	0.3000	-3.3925
285	DUMMY	-0.3000	-3.3925

Pad No.	Pad Name	X [mm]	Y [mm]
-	Alignment Mark2	0.9950	-3.3925

3. PIN FUNCTIONS

(1/2)

Symbol	Pin Name	Pad No.	I/O	Function
O_1 to O_{176}	Driver output	277 to 102	Output	Scan signal output pins that drive the gate electrode of a TFT-LCD. The status of each output pin changes in synchronization with the rising edge of shift clock. The output voltage of the driver is V_T-V_B.
STVR, STVL	Start pulse input/output	78, 79, 81, 82	I/O	Input/output pin of the internal shift register. Read of start pulse signal is set at rising (or falling) edge of shift clock, and outputs a scanning signal from a driver output pin. In addition, the effective level of a STVR/STVL pin is determined by setup of STVSEL pin. Moreover, an input/output level is V_{CC1}-V_{SS} (logic level). STVSEL = L: Start pulse is set to low level by the 176th falling edge of shift clock, and is set to a high level by the 177th falling edge.
STVSEL	Start pulse input effective level selection	35, 36	Input	The effective level of the start pulse signal inputted into STVR/STVL is selected. STVSEL = L: Low level STVSEL = H: High level
CLK	Shift clock input	84, 85	Input	Shift clock input for the internal shift register. The contents of internal shift register is shifted at the rising edge of CLK. Connect to GCLK pin of source driver.
R,/L	Shift direction switching input	38, 39	Input	Shift direction switching input pin of the internal shift register. R,/L = H (right shift): STVR → O_1 → O_2 ··· O_{175} → O_{176} → STVL R,/L = L (left shift): STVL → O_{176} → O_{175} ··· O_2 → O_1 → STVR
OE1	Enable input	87, 88	Input	Input of the level selected by OE1SEL fixes a driver output to a low level (input of a low level fixes driver output to low level at the time of OE1SEL = L). However, shift register is not cleared. Moreover, output enable operation is asynchronous on a clock. Connect with GOE1 pin of sauce driver.
OE1SEL	OE1 effective level selection	29, 30	Input	This pin selects effective level of OE1 pin. OE1SEL = L: Low level OE1SEL = H: High level
OE2	Enable input	90, 91	Input	Input of the level selected by OE2SEL fixes a driver output to a high level (input of a low level fixes driver output to high level at the time of OE2SEL = L). However, shift register is not cleared. Moreover, output enable operation is asynchronous on a clock. Connect with GOE2 pin of sauce driver.
OE2SEL	OE2 effective level selection	32, 33	Input	This pin selects effective level of OE2 pin. OE2SEL = L: Low level OE2SEL = H: High level

(2/2)

Symbol	Name	Pad No.	I/O	Function
V_T	Positive power supply for driver	43 to 47	–	Positive power supply for level shifter and output buffer. Positive power supply for Liquid crystal.
V_{EE}	Negative power supply for logic	64 to 68	–	Negative power supply for level shifter.
V_B	Negative power supply for driver	71 to 75	–	Negative power supply for output buffer. Negative power supply for Liquid crystal.
V_{CC1}	Positive power supply for logic	50 to 54	–	Positive power supply for logic circuit.
V_{SS}	Ground	57 to 61	–	Connect to the system ground.
PV_{CC1}	Pull-up power supply	28, 34, 40	–	Pull-up power supply for mode setting pins (R,/L, STVSEL, OE1SEL, OE2SEL).
PV_{SS}	Pull-down power supply	31, 37	–	Pull-down power supply for mode setting pins (R,/L, STVSEL, OE1SEL, OE2SEL).

4. MODE DESCRIPTION

Output Mode Selection

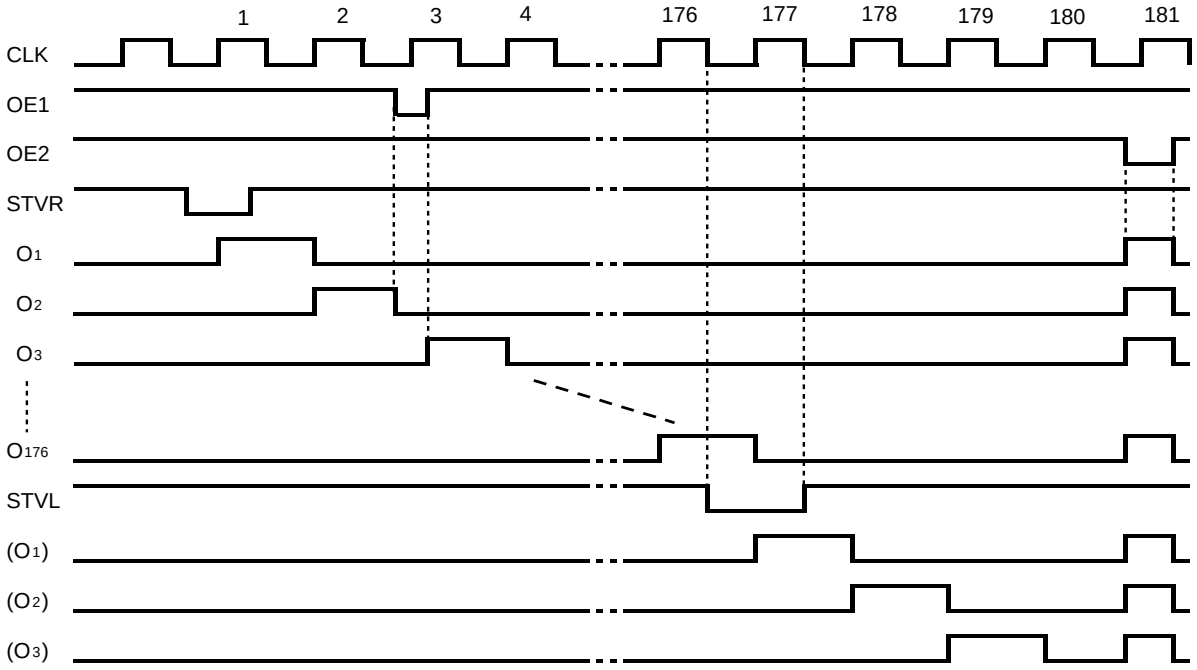
R,/L	STVR	STVL	Scan Direction
H	Input	Output	1 → 176
L	Output	Input	176 → 1

Remark H: V_{CC1}, L: V_{SS}

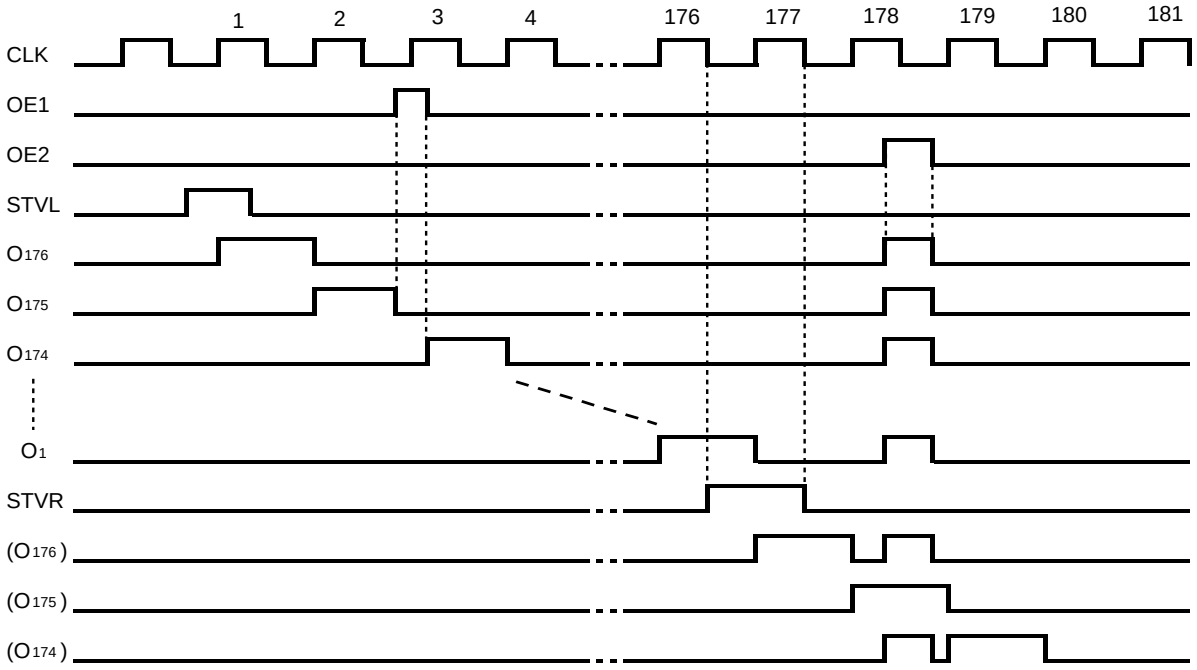
5. TIMING CHART

The timing chart in each condition is shown as follows.

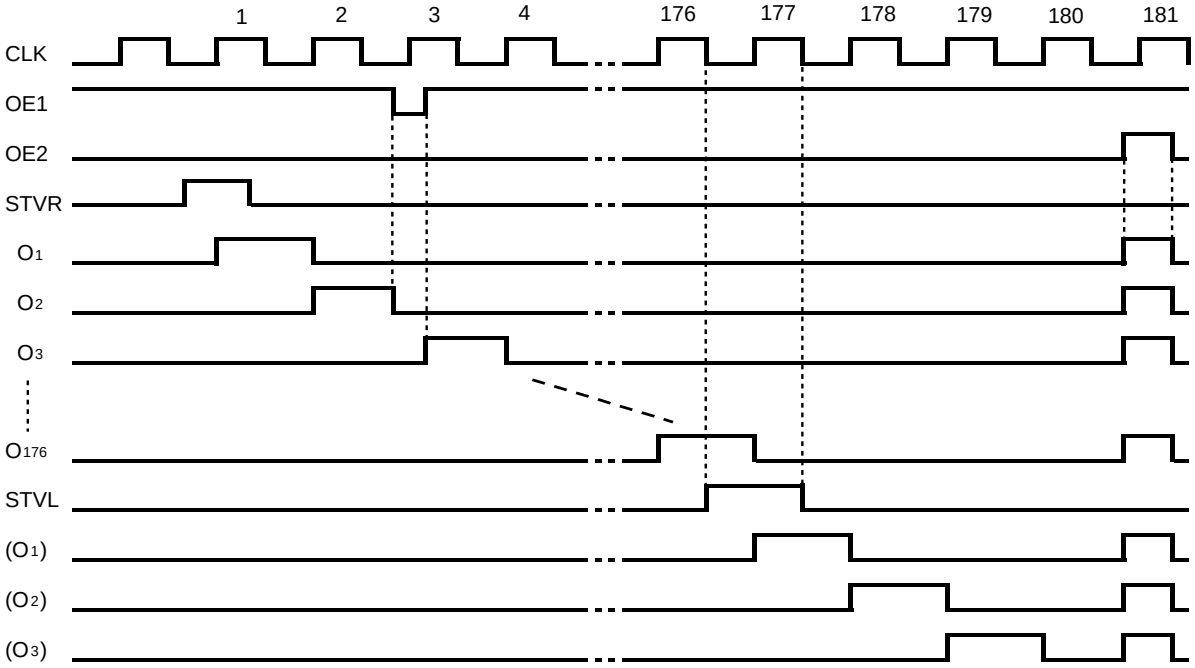
R,/L = H, STVSEL = L, OE1SEL = L, OE2SEL = L



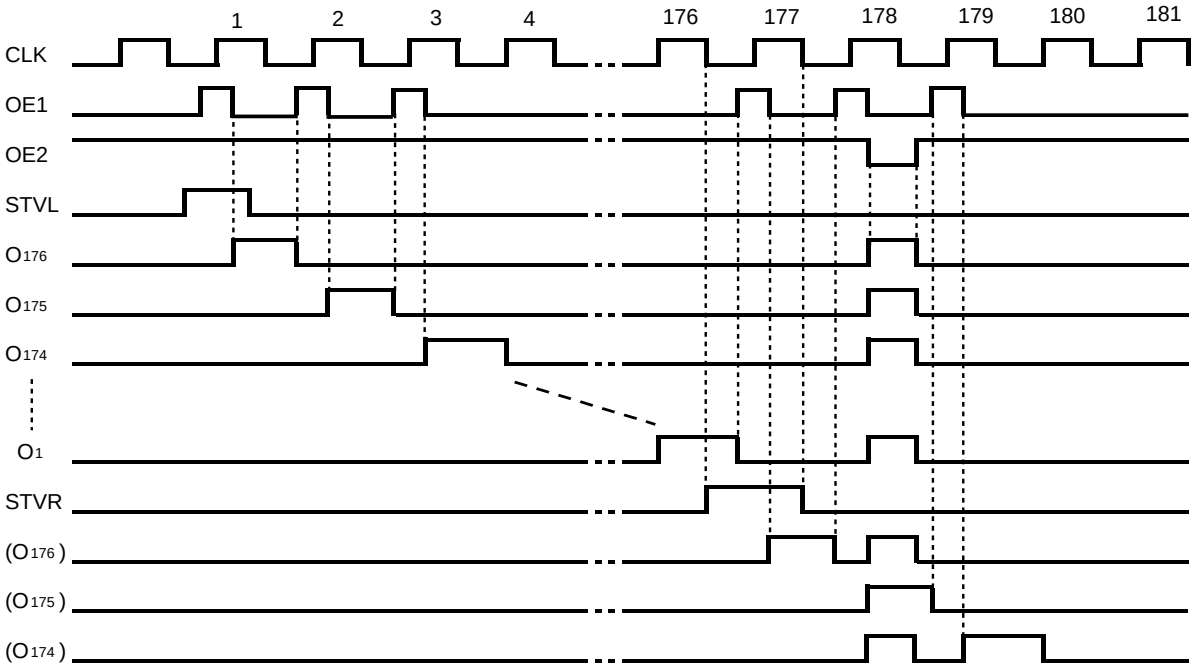
R,/L = L, STVSEL = H, OE1SEL = H, OE2SEL = H



R,/L = H, STVSEL = H, OE1SEL = L, OE2SEL = H



R,/L = L, STVSEL = H, OE1SEL = H, OE2SEL = L



6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_T	–0.5 to +30	V
Supply Voltage	V_{CC1}	–0.5 to +6.5	V
Supply Voltage	V_T-V_{EE}	–0.5 to +45	V
Supply Voltage	V_{EE}	–25 to +0.5	V
Supply Voltage	V_B	V_{EE} – 0.5 to +0.5	V
Input Voltage Note	V_I	–0.5 to V_{CC1} + 0.5	V
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–55 to +150	°C

Note R,/L, CLK, STVR, STVL, OE1, OE2, STVSEL, OE1SEL, OE2SEL

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_T	10	15	25	V
Supply Voltage	V_{EE}	–20	–15	–10	V
Supply Voltage	V_B	V_{EE}	–15	–6.5	V
Supply Voltage	V_T-V_{EE}	20	30	42	V
Supply Voltage	V_{CC1}	2.5	3.0	3.6	V
Input Voltage Note	V_I	0		V_{CC1}	V

Note R,/L, CLK, STVR, STVL, OE1, OE2, STVSEL, OE1SEL, OE2SEL

Electrical Characteristics (T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.6 V, V_T = 15 V, V_{EE} = V_B = –15 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High Level Input Voltage	V_{IH1}	R,/L, CLK, STVR, STVL, OE1, OE2,	0.8 V_{CC1}		V_{CC1}	V
Low Level Input Voltage	V_{IL1}	STVSEL, OE1SEL, OE2SEL	0		0.2 V_{CC1}	V
High Level Output Voltage	V_{OH}	STVR, STVL, I_{OH} = –40 μA	V_{CC1} – 0.4		V_{CC1}	V
Low Level Output Voltage	V_{OL}	STVR, STVL, I_{OH} = +40 μA	0		0.4	V
Output ON Resistance	R_{ON1}	O_1 to O_{176}, V_{OUT} = V_T – 0.5 V		5.0	7.5	kΩ
	R_{ON2}	O_1 to O_{176}, V_{OUT} = V_{EE} + 0.5 V		5.0	7.5	kΩ
Input Current	I_{I1}	Logic input pin			±1.0	μA
Dynamic Current 1	I_{CC1}	V_{CC1}, **Note**			200	μA
Dynamic Current 2	I_T	V_T, **Note**			100	μA
Dynamic Current 3	I_{EE}	V_{EE}, **Note**			100	μA
Static Current **Note**	I_{SS}	V_{CC1}, V_T in stand-by mode			10	μA

Note f_{CLK} = 20 kHz, frame frequency = 60 Hz, output no load

Switching Characteristics (T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.6 V, V_T = 15 V, V_{EE} = V_B = –15 V, V_{SS} = 0 V)

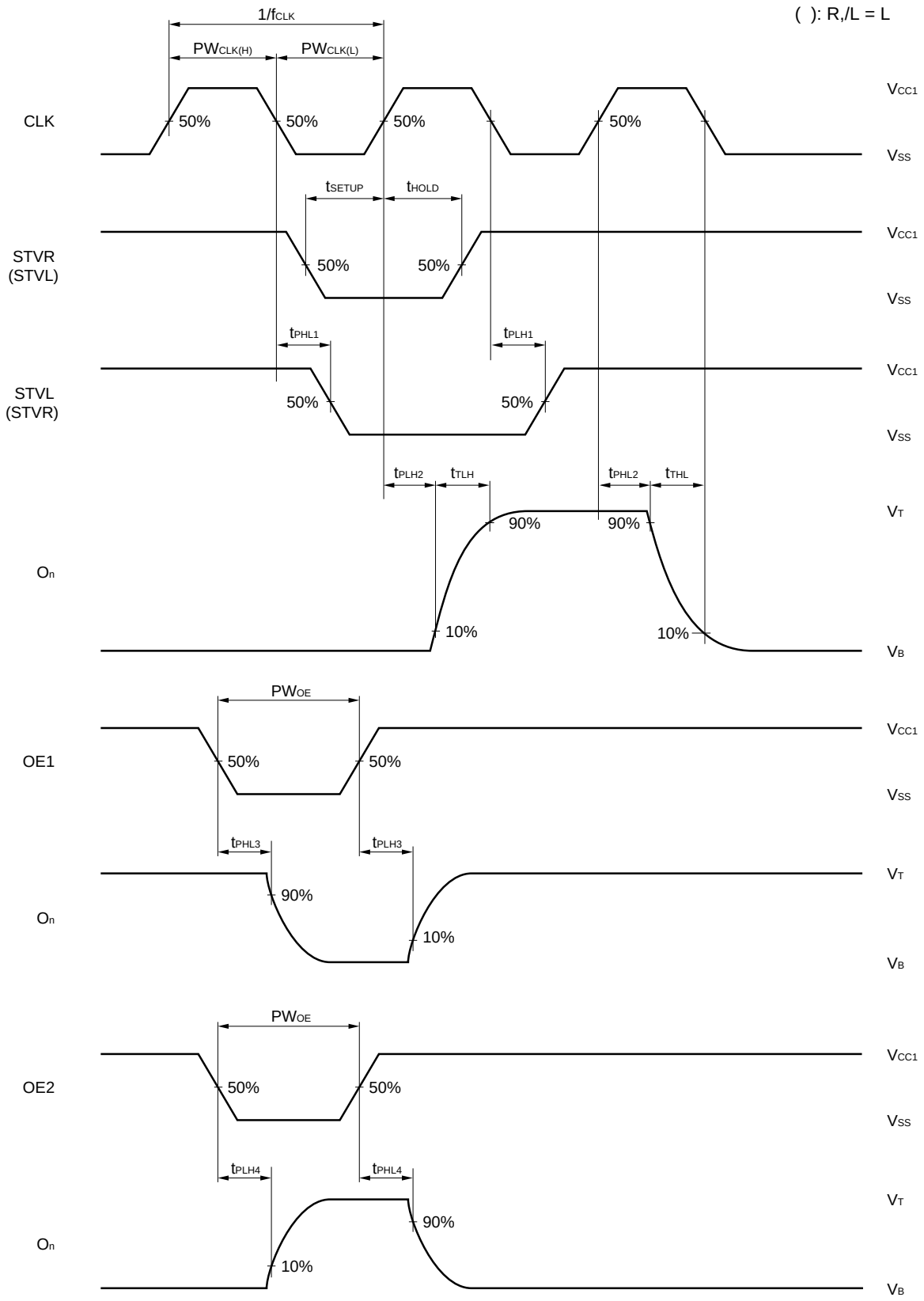
	Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
	Cascade Output Delay Time	t_{PHL1}	C_L = 20 pF,			800	ns
		t_{PLH1}	CLK → STVL (STVR)			800	ns
★	Driver Output Delay Time 1	t_{PHL2}	C_L = 50 pF,			1.5	μs
		t_{PLH2}	CLK → O_n			1.5	μs
★	Driver Output Delay Time2	t_{PHL3}	C_L = 50 pF,			1.5	μs
		t_{PLH3}	OE1 → On			1.5	μs
★	Driver Output Delay Time 3	t_{PHL4}	C_L = 50 pF,			1.5	μs
		t_{PLH4}	OE2 → On			1.5	μs
★	Output Rise Time	t_{TLH}	C_L = 50 pF			1.5	μs
	Output Fall Time	t_{THL}				1.5	μs
	Input Capacitance	C_I	T_A = 25°C			15	pF
	Clock Frequency	f_{CLK}	When connected in cascade		20	100	kHz

Timing Requirement (T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.6 V, V_T = 15 V, V_{EE} = V_B = –15 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse High Period	$PW_{CLK(H)}$		500			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		500			ns
Enable Pulse High Period	PW_{OE}	OE1, OE2	1			μs
Data Setup Time	t_{SETUP}	STVR (STVL) ↓ → CLK ↑	200			ns
Data Hold Time	t_{HOLD}	CLK ↑ → STVR (STVL) ↑	200			ns

Remark The rise and fall times of logic input must be t_r = t_f = 20 ns (10 to 90%)

★ **Switching Characteristics Waveform (R,/L = H, STVSEL = L, OE1SEL = L, OE2SEL = L)**



NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.