Advanced Power MOSFET

SSH7N80A

FEATURES
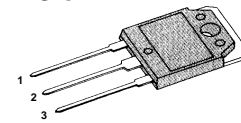
- ■ Avalanche Rugged Technology
- ■ Rugged Gate Oxide Technology
- ■ Lower Input Capacitance
- ■ Improved Gate Charge
- ■ Extended Safe Operating Area
- ■ Lower Leakage Current : 25 μA (Max.) @ V_{DS} = 800V
- ■ Low $R_{DS(ON)}$: 1.472 Ω (Typ.)

BV_{DSS} = 800 V

$R_{DS(on)}$ = 1.8 Ω

I_D = 7 A

TO-3P

1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	800	V
I_D	Continuous Drain Current (T_C=25 ℃)	7	A
	Continuous Drain Current (T_C=100 ℃)	4.4	
I_{DM}	Drain Current-Pulsed ①	28	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy ②	523	mJ
I_{AR}	Avalanche Current ①	7	A
E_{AR}	Repetitive Avalanche Energy ①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.0	V/ns
P_D	Total Power Dissipation (T_C=25 ℃)	200	W
	Linear Derating Factor	1.59	W/℃
T_J , T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	℃
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	0.63	℃/W
$R_{\theta CS}$	Case-to-Sink	0.24	--	
$R_{\theta JA}$	Junction-to-Ambient	--	40	

Electrical Characteristics $(T_C=25℃$ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	800	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.93	--	$V/℃$	$I_D=250\mu A$ **See Fig 7**
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	3.5	V	$V_{DS}=5V, I_D=250\mu A$
I_{GSS}	Gate-Source Leakage , Forward	--	--	100	nA	$V_{GS}=30V$
	Gate-Source Leakage , Reverse	--	--	-100		$V_{GS}=-30V$
I_{DSS}	Drain-to-Source Leakage Current	--	--	25	μA	$V_{DS}=800V$
		--	--	250		$V_{DS}=640V, T_C=125℃$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	1.8	Ω	$V_{GS}=10V, I_D=0.85A$ ④*
g_{fs}	Forward Transconductance	--	4.95	--	Ω	$V_{DS}=50V, I_D=0.85A$ ④
C_{iss}	Input Capacitance	--	1500	1950	pF	$V_{GS}=0V, V_{DS}=25V, f=1MHz$ **See Fig 5**
C_{oss}	Output Capacitance	--	140	165		
C_{rss}	Reverse Transfer Capacitance	--	57	66		
$t_{d(on)}$	Turn-On Delay Time	--	23	55	ns	$V_{DD}=400V, I_D=2A,$ $R_G=16 \Omega$ **See Fig 13** ④⑤
t_r	Rise Time	--	40	90		
$t_{d(off)}$	Turn-Off Delay Time	--	92	195		
t_f	Fall Time	--	34	80		
Q_g	Total Gate Charge	--	67	88	nC	$V_{DS}=640V, V_{GS}=10V,$ $I_D=2A$ **See Fig 6 & Fig 12** ④⑤
Q_{gs}	Gate-Source Charge	--	11.2	--		
Q_{gd}	Gate-Drain("Miller") Charge	--	29.6	--		

Source-Drain Diode Ratings and Characteristics

| Symbol	Characteristic		Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current		--	--	7	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current	①	--	--	28		
V_{SD}	Diode Forward Voltage	④	--	--	1.4	V	$T_J=25 ℃, I_S=7A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time		--	520	--	ns	$T_J=25 ℃, I_F=7A$
Q_{rr}	Reverse Recovery Charge		--	6.66	--	μC	$di_F/dt=100A/\mu s$ ④

Notes ;

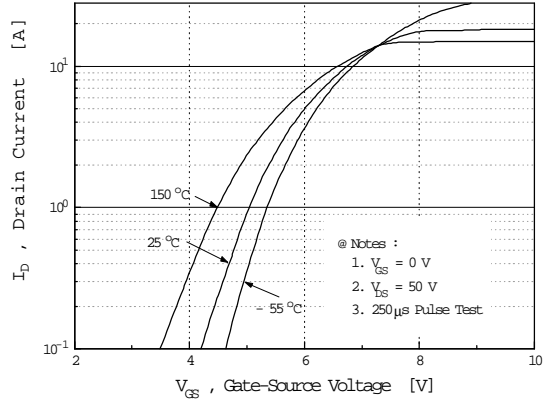① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature

② L=20mH, $I_{AS}=7A, V_{DD}=50V, R_G=27\Omega$, Starting $T_J=25 ℃$

③ $I_{SD} \leq 7A$, di/dt $\leq 150A/\mu s, V_{DD} \leq BV_{DSS}$, Starting $T_J=25 ℃$

④ Pulse Test : Pulse Width = 250 μs, Duty Cycle $\leq 2\%$

⑤ Essentially Independent of Operating Temperature

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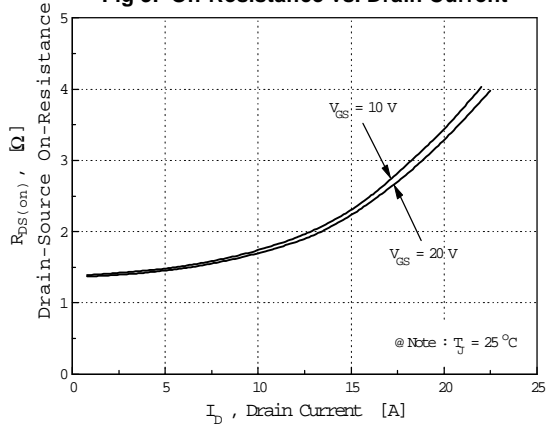
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Fig 1. Output Characteristics
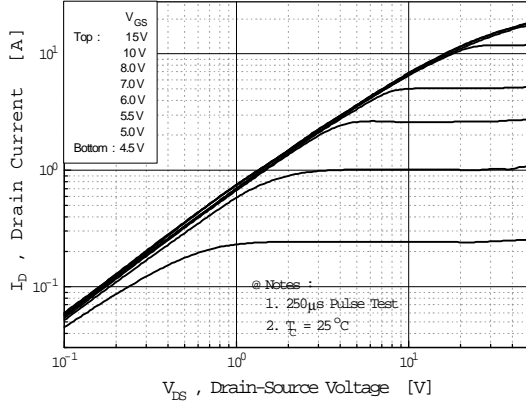
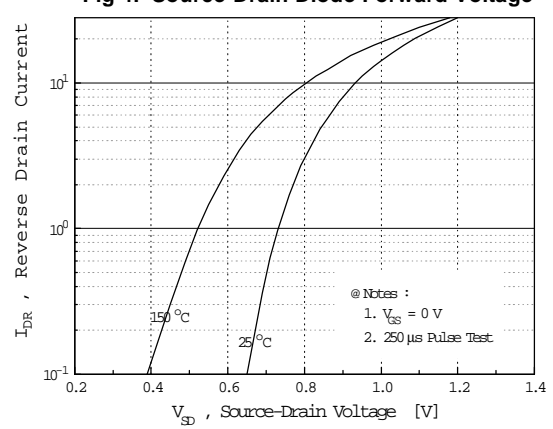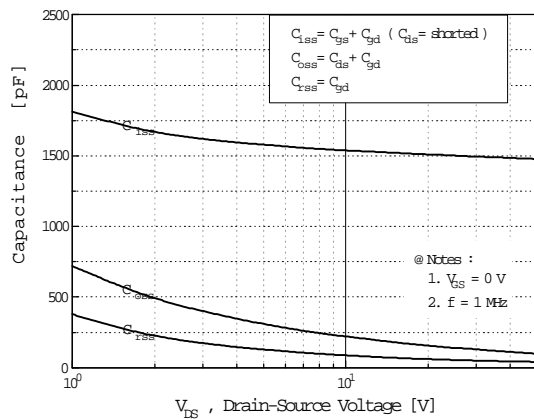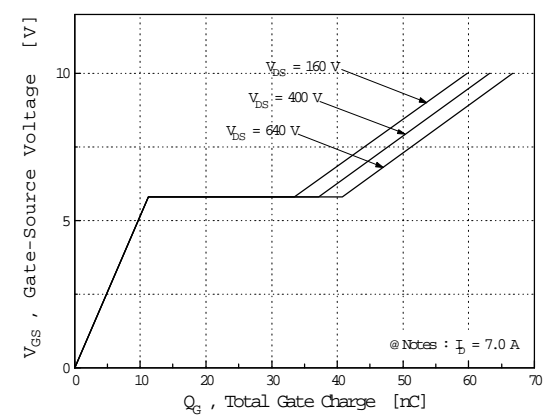### Fig 2. Transfer Characteristics

Fig 3. On-Resistance vs. Drain Current
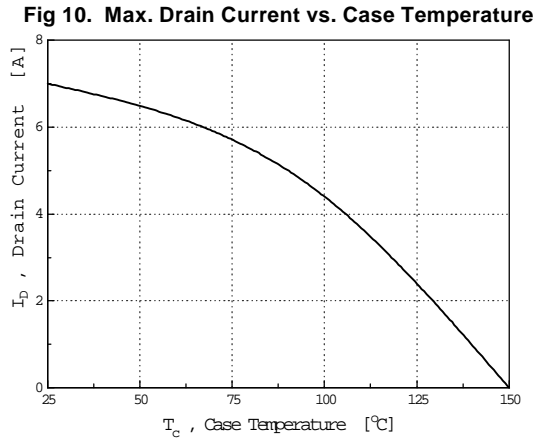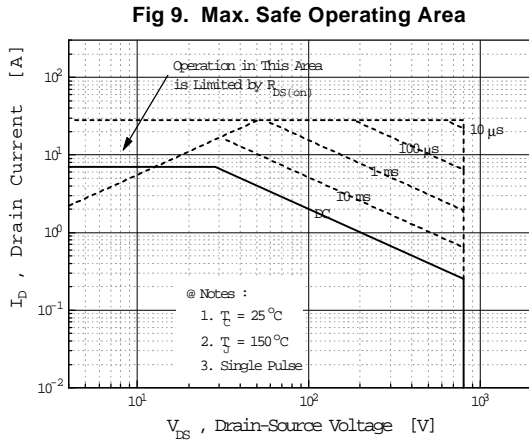

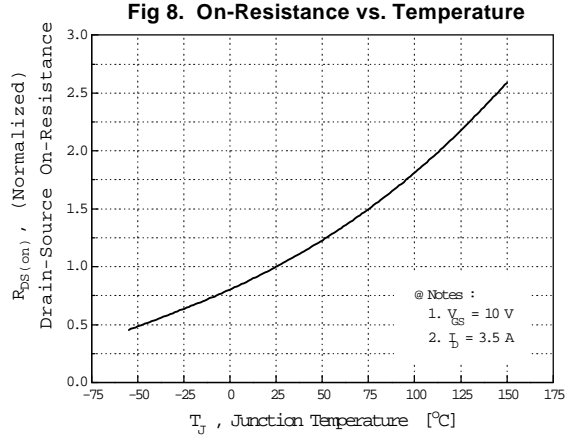
Fig 4. Source-Drain Diode Forward Voltage

Fig 5. Capacitance vs. Drain-Source Voltage

Fig 6. Gate Charge vs. Gate-Source Voltage

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Fig 7. Breakdown Voltage vs. Temperature

@ Notes :
1. V_{GS} = 0 V
2. I_D = 250 μA

Fig 8. On-Resistance vs. Temperature

@ Notes :
1. V_{GS} = 10 V
2. I_D = 3.5 A

Fig 9. Max. Safe Operating Area

Operation in This Area
is Limited by $R_{DS(on)}$

10 μs
100 μs
1 ms
10 ms
DC

@ Notes :
1. T_C = 25 °C
2. T_J = 150 °C
3. Single Pulse

Fig 10. Max. Drain Current vs. Case Temperature

Fig 11. Thermal Response

D=0.5
0.2
0.1
0.05
0.02
0.01

single pulse

@ Notes :
1. $Z_{\theta JC}(t)$=0.63 °C/W Max.
2. Duty Factor, D=t_1/t_2
3. T_{JM} - T_C = P_{DM} * $Z_{\theta JC}(t)$
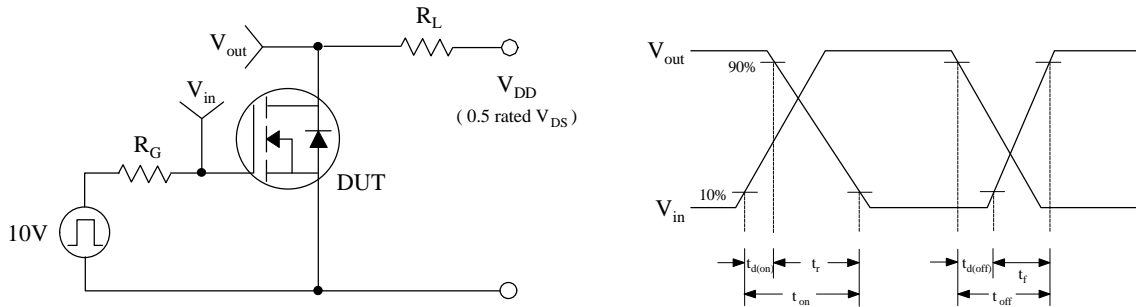
P_{DM}
t_1
t_2

Fig 12. Gate Charge Test Circuit & Waveform
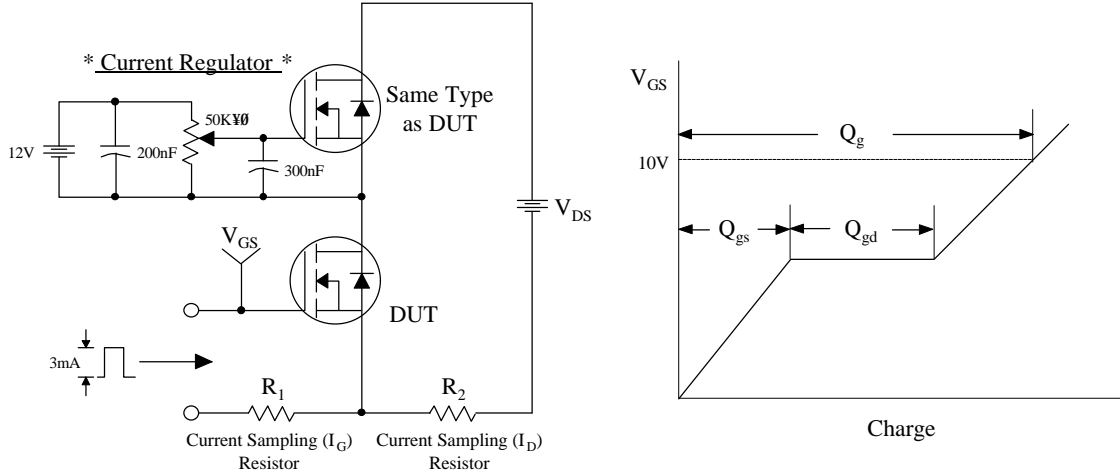
Fig 13. Resistive Switching Test Circuit & Waveforms

Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

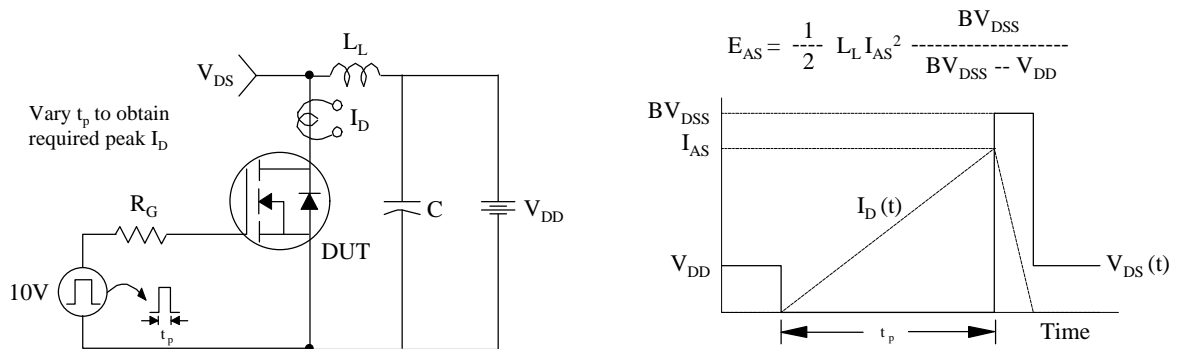$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

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Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

+

--

I_S

L

V_{GS}

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by "R_G"
• I_S controlled by Duty Factor "D"

V_{GS}
(**Driver**)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_S
(**DUT**)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(**DUT**)

Body Diode Recovery dv/dt

V_f

V_{DD}

Body Diode
Forward Voltage Drop