UMC

UM82C88

Bus Controller

Features

- Pin compatible with bipolar 8288
- Provides advanced commands for multimaster busses
- 3-state command outputs
- Bipolar drive capability
- Fully TTL compatible
- High performance HCMOS process
- Single 5V power supply
- Low power operation

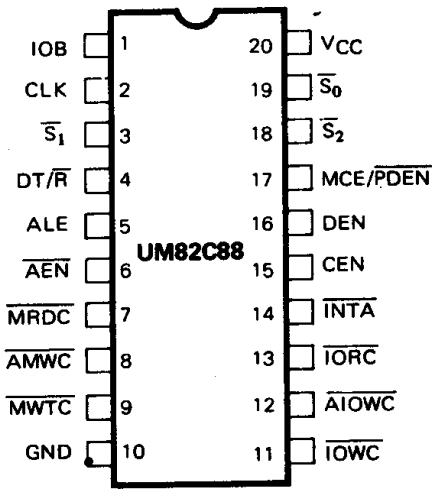
  I_{CCSB} – 10μA

  I_{CCOP} – 1mA/MHz

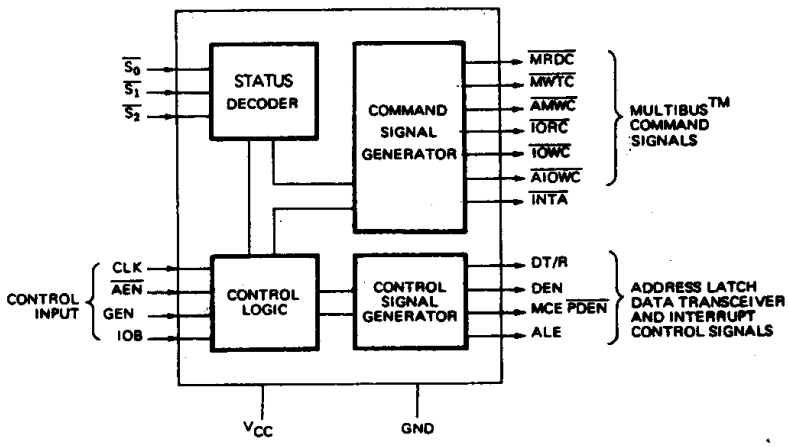
General Description

The UM82C88 is a high performance CMOS Bus Controller manufactured using a self-aligned silicon gate CMOS process. The UM82C88 provides the control and command timing signals for 80C86 and 8086/88 systems. The high output drive capability of the UM82C88 eliminates the need for additional bus drivers. High speed and industry standard configuration make the UM82C88 compatible with microprocessors such as the 80C86, 8086, 8088, 8089, 80186, and 80188.

Pin Configuration



Block Diagram



*TM Multibus is an INTEL Corp trademark

Absolute Maximum Ratings*

Supply Voltage . . . . . +8.0 Volts
Operating Voltage Range . . . . . +4V to +7V
Input Voltage Applied . . . . . GND −2.0V to +6.5V
Output Voltage Applied . . . . . GND −0.5V to V_{CC} +0.5V
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C
Maximum Power Disipation . . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Electrical Characteristics

(V_{CC} = 5.0V ±10%; T_A = 0°C to +70°C)

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{IH}	Logic One Input Voltage	2.0		V V	
V_{IL}	Logic Zero Input Voltage		0.8	V	
V_{IHC}	LCK Logical One Input Voltage	0.7 V_{CC}		V	
V_{ILC}	CLK Logical Zero Input Voltage		0.2 VCC	V	
V_{OH}	Output High Voltage Command Outputs	3.0 VCC−0.4		V V	I_{OH} = −8.0mA I_{OH} = −2.5mA
	Output High Voltage Control Outputs	3.0 VCC−0.4		V V	I_{OH} = −4.0mA I_{OH} = −2.5mA
V_{OL}	Output Low Voltage Command Outputs		0.5	V	I_{OL} = +20.0mA
	Output Low Voltage Control Outputs		0.4	V	I_{OL} = +8.0mA
I_{IL}	Input Leakage Current	−1.0	1.0	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$ except $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$
I_{BHH}	Input Leakage Current-Status Bus	−50	−300	μA	V_{IN} = 2.0V $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ (see Note 1)
I_O	Output Leakage Current	−10.0	10.0	μA	$0V \leqslant V_O \leqslant V_{CC}$
I_{CCSB}	Standby Power Supply		10	μA	V_{CC} = 5.5V V_{IN} = V_{CC} or GND Outputs Open
I_{CCOP}	Operating Power Supply Current		1	mA/MHz	V_{CC} = 5.5V Outputs Open

Capacitance

(T_A = 25°C; V_{CC} = GND = OV; V_{IN} = +5V or GND)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		5	pf	FREQ = 1MHz Unmeasured pins returned to GND
C_{OUT}*	Output Capacitance		16	pf	

*Guaranteed and sampled, but not 100% tested

A.C. Characteristics

(V_{CC} = +5V ±10%, GND = 0V; T_A = 0°C to 70°C)

TIMING REQUIREMENTS

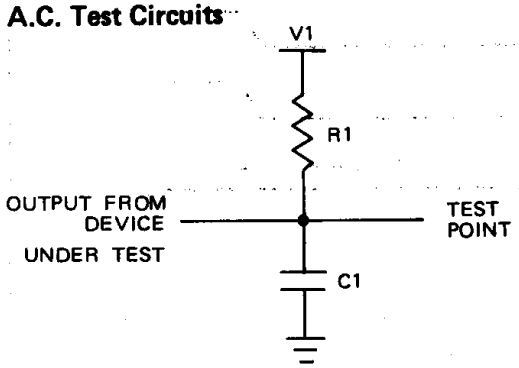
Symbol	Parameter	Min.	Max.	Unit	Conditions
T_{CLCL}	CLK Cycle Period	125		ns	
T_{CLCH}	CLK Low Time	66		ns	
T_{CHCL}	CLK High Time	40		ns	
T_{SVCH}	Status Active Setup Time	35		ns	
T_{CHSV}	Status Active Hold Time	10		ns	
T_{SHCL}	Status Inactive Setup Time	35		ns	
T_{CLSH}	Status Inactive Hold Time	10		ns	

TIMING RESPONSES

Symbol	Parameter	Min.	Max.	Unit	Conditions
T_{CVNV}	Control Active Delay	5	45	ns	1
T_{CVNX}	Control Inactive Delay	10	45	ns	1
T_{CLLH}	ALE Active Delay (from CLK)		20	ns	1
T_{CLMCH}	MCE Active Delay (from CLK)		25	ns	1
T_{SVLH}	ALE Active Delay (from Status)		20	ns	1
T_{SVMCH}	MCE Active Delay (from Status)		30	ns	1
T_{CHLL}	ALE Inactive Delay	4	22	ns	1
T_{CLML}	Command Active Delay	5	35	ns	2
T_{CLMH}	Command Inactive Delay	5	35	ns	2
T_{CHDTL}	Direction Control Active Delay		50	ns	1
T_{CHDTH}	Direction Control Inactive Delay		30	ns	1
T_{AELCH}	Command Enable Time[1]		40	ns	3
T_{AEHCZ}	Command Disable Time[2]		40	ns	4
T_{AELCV}	Enable Delay Time	110	250	ns	2
T_{AEVNV}	$\overline{AEN}$ to DEN		25	ns	1
T_{CEVNV}	CEN to DEN, $\overline{PDEN}$		25	ns	1
T_{CELRH}	CEN to Command		TCLML +10	ns	2
T_{LHLL}	ALE High Time	TCLCH −10		ns	1

Note: 1. T_{AELCH} measurement is between 1.5V and 2.5V.
2. T_{AEHCZ} measured at 0.5V change in VO.

A.C. Test Circuits

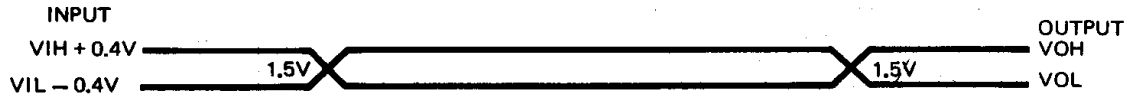


*Includes stray and jig capacitance

Test Conditions	IOH	IOL	V_1	R_1	C_1
1	−4.0mA	+ 8.0mA	2.13V	220Ω	80pf
2	−8.0mA	+20.0mA	2.29V	91Ω	300pf
3	−8.0mA	–	1.50V	187Ω	300pf
4	−8.0mA	–	1.50V	187Ω	50pf

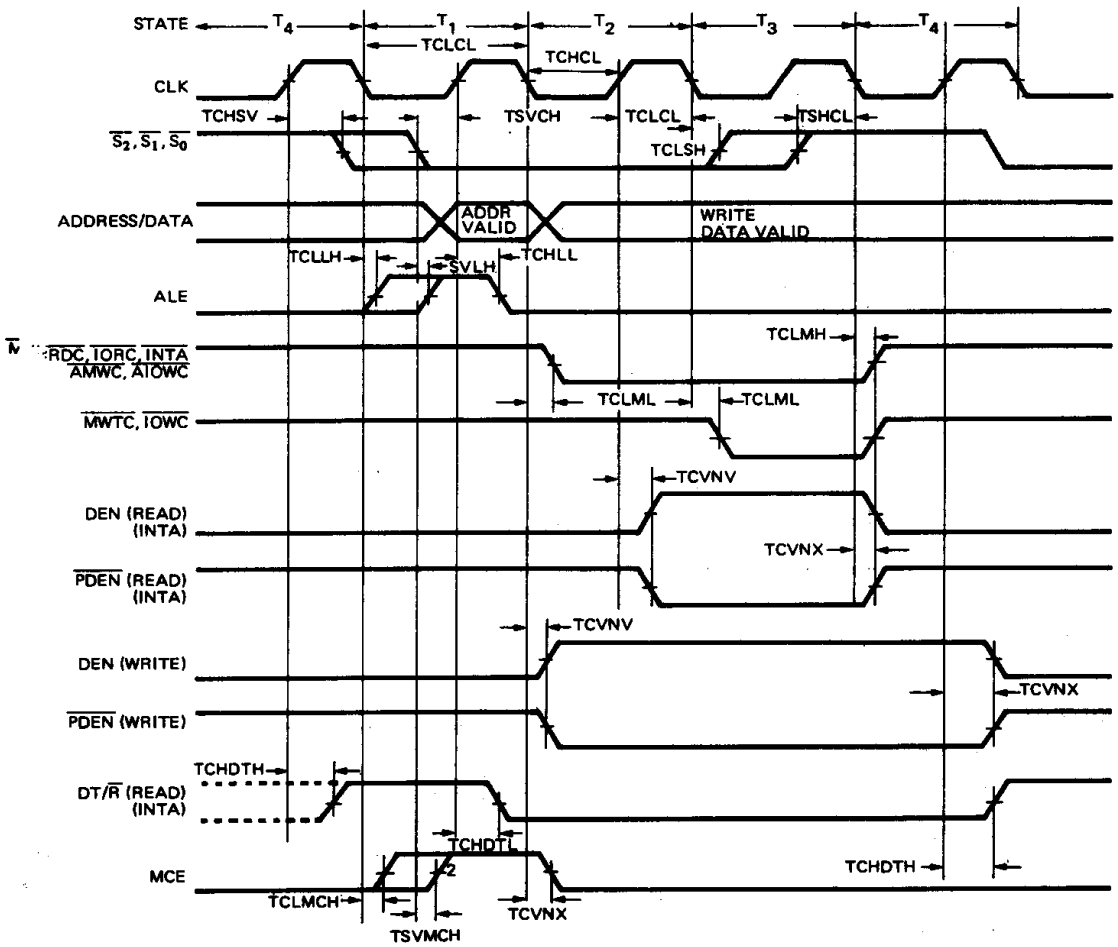
Test Condition Definition Table

A.C. Testing Input, Output Waveform



A.C. Testing: All input signals (other than CLK) must switch between VIL –0.4V and VIH +0.4V. CLK must switch between 0.4V and 3.9V. T_R and T_F must be less than or equal to 15ns.

Waveforms

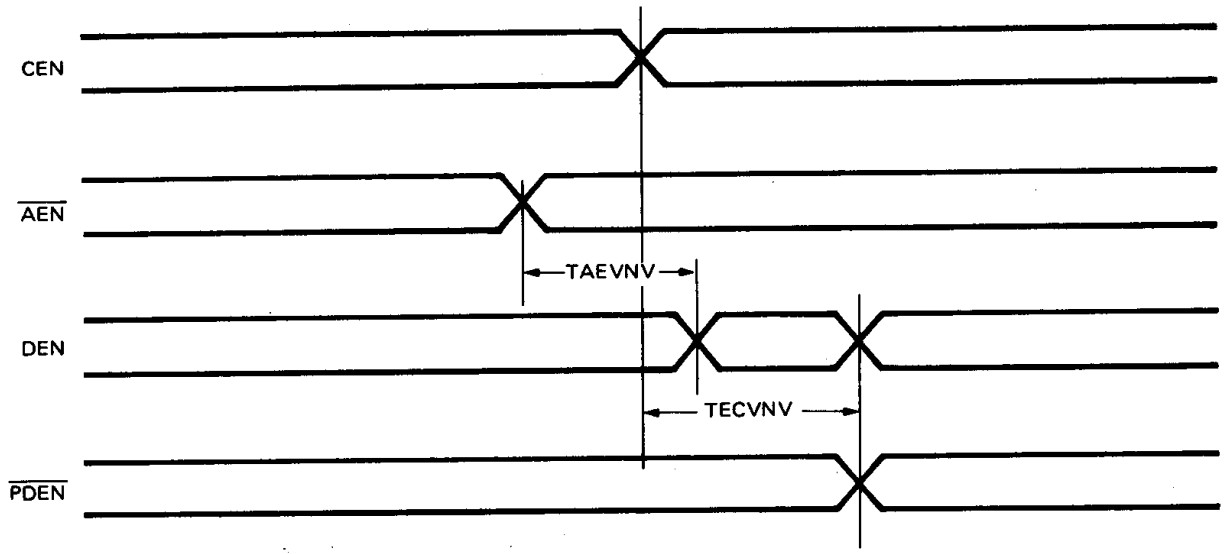


Notes:

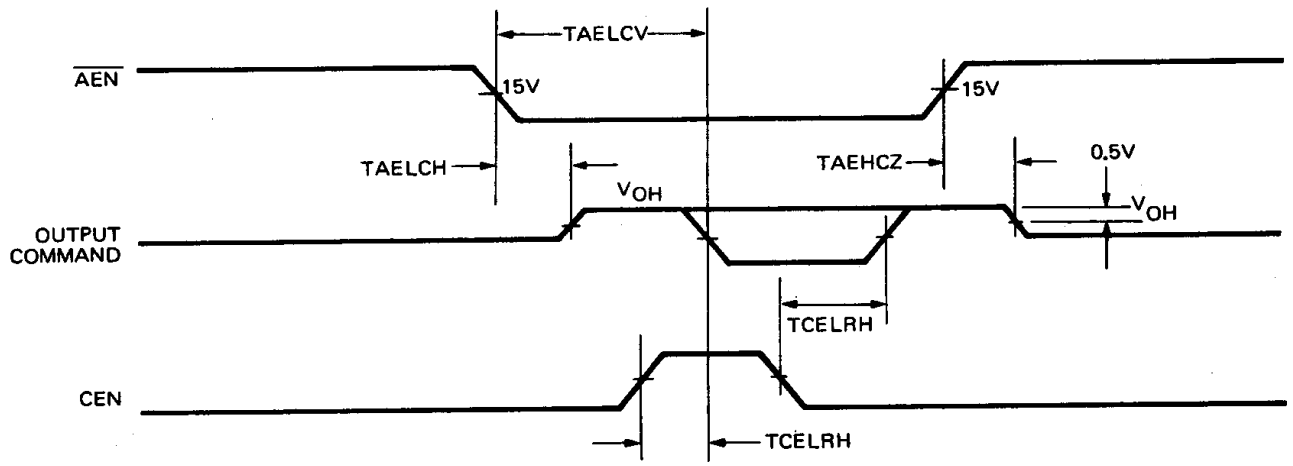
1 Address/data bus is shown only for reference purposes
2 Leading edge of ale and mce is determined by the falling edge of CLK or status going active whichever occurs last
3 All timing me asurements are made at 15V unless specified otherwise

Waveforms (Continued)

DEN, $\overline{PDEN}$ QUALIFICATION TIMING



ADDRESS ENABLE ($\overline{AEN}$) TIMING (3-STATE ENABLE/DISABLE)



Note:
CEN must be low or valid prior to T_2 to prevent the command from being generated.

Pin Description

Symbol	Pin Number	Type	Functions
V_{CC}	20	O	+5V power supply
GND	10		Ground
$\overline{S_0}$ $\overline{S_1}$ $\overline{S_2}$	19, 3, 18	I	Status input pins: These pins are the input pins from the 80C86, 8086/88/8089 processors. The UM82C88 decodes these inputs to generate command and control signals at the appropriate time. When Status pins are not in use (passive), command outputs are held HIGH (See Table 1.)
CLK	2	I	Clock: This is a CMOS compatible input which receives a clock signal from the UM82C84A clock generator and serves to establish when command/control signals are generated.
ALE	5	O	Address Latch Enable: This signal serves to strobe an address into the address latches. This signal is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches, such as the 82C82.
DEN	16	O	Data Enable: This signal serves to enable data transceivers onto either the local or system data bus. This signal is active HIGH.
DT/$\overline{R}$	4	O	Data Transmit/Receive: This signal establishes the direction of data flow through the transceivers. A HIGH on this line indicates Transmit (write to I/O or memory) and a LOW indicates Transmit (write to I/O or memory) and a LOW indicates Receive (Read).
$\overline{AEN}$	6	I	Address Enable: $\overline{AEN}$ enables command outputs of the UM82C88 Bus Controller a minimum of 110ns (250ns maximum) after it becomes active (LOW). $\overline{AEN}$ going inactive immediately 3-states the command output drivers. $\overline{AEN}$ does not affect the I/O command lines if the UM82C88 is in the I/O Bus mode (IOB tied HIGH).
CEN	15	I	Command Enable: When this signal LOW all UM82C88 command outputs and the DEN and PDEN control outputs are forced to their inactive state. When this signal is HIGH, these same outputs are enabled.
IOB	1	I	Input/Output Bus Mode: When the IOB is strapped HIGH the UM82C88 functions in the I/O Bus mode. When it is strapped LOW, the UM82C88 functions in the System Bus mode (See I/O Bus and System Bus sections).
$\overline{AIOWC}$	12	O	Advanced I/O Write Command: The $\overline{AIOWC}$ issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AIOWC}$ is active LOW.
$\overline{IOWC}$	11	O	I/O Write Command: This command line instructs an I/O device to read the data on the data bus. The signal is active LOW.
$\overline{IORC}$	13	O	I/O Read Command: This command line instructs an I/O device to drive its data onto the data bus. This signal is active LOW.
$\overline{AMWC}$	8	O	Advanced Memory Write Command: The $\overline{AMWC}$ issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AMWC}$ is active LOW.
$\overline{MWTC}$	9	O	Memory Write Command: This command line instructs the memory to record the data present on the data bus. This signal is active LOW.
$\overline{MRDC}$	7	O	Memory Read Command: This command line instructs the memory to drive its data onto the data bus. $\overline{MRDC}$ is active LOW.
$\overline{INTA}$	14	O	Interrupt Acknowledge: This command line tells an interrupting device that its interrupt has been acknowledged and that it should drive vectoring information onto the data bus. This signal is active LOW.
MCE/$\overline{PDEN}$	17	O	This is a dual function pin. MCE (IOB is tied LOW): Master Cascade Enable occurs during an interrupt sequence and serves to read a Cascade Address from a master UM82C59A Priority Interrupt Controller onto the data bus. The MCE signal is active HIGH. $\overline{PDEN}$ (IOB is tied HIGH): Peripheral Data Enable enables the data bus transceiver for the I/O bus that DEN performs for the system bus. $\overline{PDEN}$ is active LOW.

Functional Description

Command and Control Logic

The command logic decodes the three 80C86, 8086, 8088 or 8089 status lines ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) to determine what command is to be issued (see Table 1).

Table 1. Command Decode Definition

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Processor State	UM82C88 Command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

I/O BUS Mode

The UM82C88 is in the I/O Bus mode if the IOB pin is strapped HIGH. In the I/O Bus mode, all I/O command lines ($\overline{IORC}$, $\overline{ILWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (i.e., not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the UM82C88 immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one UM82C88 Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal mermory access requires a "Bus Ready" signal ($\overline{AEN}$ LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.

System BUS Mode

The UM82C88 is in the System Bus Mode if the IOB pin is strapped LOW. In this mode, no command is issued until a specified time period after the AEN line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the AEN line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

Command Outputs

The advanced writer commands are made available to initiate write procedures early in the machine cycle. This signal can be used to prevent the processor from entering an unnecessary wait state.

The command outputs are:

- $\overline{MRDC}$ – Memory Read Command
- $\overline{MWTC}$ – Memory Write Command
- $\overline{IORC}$ – I/O Read Command
- $\overline{IOWC}$ – I/O Write Command
- $\overline{AMWC}$ – Advanced Memory Write Command
- $\overline{AIOWC}$ – Advanced I/O Write Command
- $\overline{INTA}$ – Interrupt Acknowledge

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

Control Outputs

The control outputs of the UM82C88 are Data Enable (DEN), Data Transmit/Receive (DT/$\overline{R}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{PDEN}$). The Den signal determines when the external bus should be enabled onto the local bus and the DT/R determines the direction of data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/$\overline{PDEN}$ pin changes function with the two modes of the UM82C88. When the UM82C88 is in the IOB mode (IOB HIGH), the $\overline{PDEN}$ signal serves as a dedicated data enable signal for the I/O or Peripheral System bus.

Interrupt Acknowledge and MCE

The MCE signal is used during an interrupt acknowledge cycle if the UM82C88 is in the System Bus mode (IOB LOW). During any interrupt sequence, there are two interrupt acknowledge cycles that occur back to back. During the first interrupt cycle no data or address transfers take place. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle, the addressed slave PIC gates an interrupt vector onto the system data bus where it is ready by the processor.

If the system contains only one PIC, the MCE signal is not used. In this case, the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

Address Latch Enable and Halt

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe the current address into the 82C82 address latches. ALE also serves to strobe the status ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) into a latch for halt state decoding.

Command Enable

The Command Enable (CEN) input acts as a command qualifier for the UM82C88. If the CEN pin is high, the UM82C88 functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.