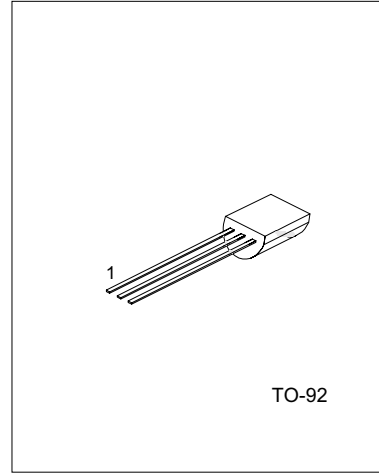


**SENSITIVE GATE SILICON
CONTROLLED RECTIFIERS
REVERSE BLOCKING
THYRISTORS**

DESCRIPTION

PNPN devices designed for high volume, line-powered consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.



1:CATHODE 2:GATE 3:ANODE

DESCRIPTION

- *Sensitive Gate Allows Triggering by Micro controllers and Other Logic circuits
- *Blocking Voltage to 600V
- *On-State Current Rating of 0.8A RMS at 80°C
- *High Surge Current Capability – 10A
- *Minimum and Maximum Values of IGT, VGT and IH Specified for Ease of Design
- *Immunity to dV/dt – 20V/ μ sec Minimum at 110°C
- *Glass-Passivated Surface for Reliability and Uniformity

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	MAX	UNIT
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Lead Solder Temperature ($<1/16$ " from case, 10 secs max)	T_L	260	°C

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MAX	UNIT
Peak Repetitive Off-State Voltage(note) ($T_J = -40$ to 110°C , Sine Wave, 50 to 60Hz; Gate Open)	V_{DRM}, V_{RRM}		V
MCR100-4		200	
MCR100-6		400	
MCR100-8		600	
On-State RMS Current ($T_c = 80^\circ\text{C}$) 180° Condition Angles	$I_T(\text{RMS})$	0.8	A
Peak Non-Repetitive Surge Current (1/2 cycle, Sine Wave, 60Hz, $T_J = 25^\circ\text{C}$)	I_{TSM}	10	A

PARAMETER	SYMBOL	MAX	UNIT
Circuit Fusing Considerations (t=8.3 ms)	I^2t	0.415	A ² s
Forward Peak Gate Power (T _A =25°C, Pulse Width ≤1.0μs)	PGM	0.1	W
Forward Average Gate Power (T _A =25°C, t=8.3ms)	PG(AV)	0.1	W
Peak Gate Current – Forward (T _A =25°C, Pulse Width≤1.0μs)	IGM	1	A
Peak Gate Voltage – Reverse (T _A =25°C, Pulse Width≤1.0μs)	VGRM	5	V
Operating Junction Temperature Range @ Rated V _{RRM} and V _{DRM}	T _J	-40 to +110	°C
Storage Temperature Range	T _{stg}	-40 to +150	°C

Note: V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

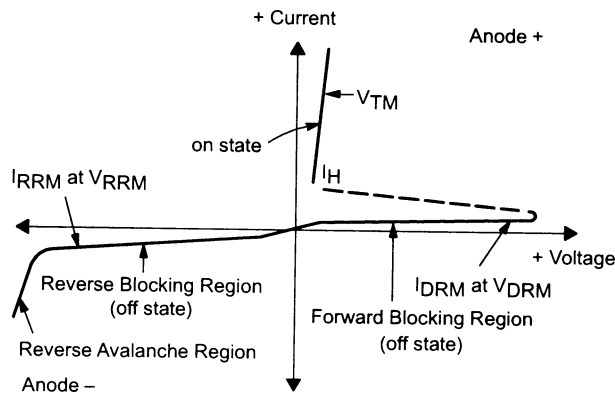
ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise stated)

PARAMETER	TEST CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Peak Forward or Reverse Blocking Current T _C =25°C T _C =125°C	V _D =Rated V _{DRM} and V _{RRM} ; R _{GK} =1kΩ	I _{DRM} , I _{RRM}			10 100	μA μA
ON CHARACTERISTICS						
Peak Forward On-State Voltage (Note1)	I _{TM} =1A Peak @ T _A =25°C	V _{TM}			1.7	V
Gate Trigger Current (Continuous dc)(note2)	V _{AK} =7Vdc, R _L =100Ω, T _C =25°C	I _{GT}		40	200	μA
Holding Current (note 3) T _C =25 °C T _C =-40 °C	V _{AK} =7Vdc, initiating current=20mA	I _H		0.5	5 10	mA
Latch Current T _C =25 °C T _C =-40 °C	V _{AK} =7V, I _g =200μA	I _L		0.6	10 15	mA
Gate Trigger Current (continuous dc) (Note 2) T _C =25 °C T _C =-40 °C	V _{AK} =7Vdc, R _L =100Ω	V _{GT}		0.62	0.8 1.2	V
DYNAMIC CHARACTERISTICS						
Critical Rate of Rise of Off-State Voltage	V _D =Rated V _{DRM} , Exponential Waveform, R _{GK} =1000Ω, T _J =110°C	dV/dt	20	35		V/μs
Critical Rate of Rise of On-State Current	I _{PK} =20A; P _w =10μsec; diG/dt=1A/μsec, I _{gt} =20mA	di/dt			50	A/μs

Notes: 1. Indicates Pulse Test Width≤1.0ms, duty cycle ≤1%
 2. R_{GK}=1000Ω included in measurement.
 3. Does not include R_{GK} in measurement.

VOLTAGE CURRENT CHARACTERISTIC OF SCR

SYMBOL	PARAMETER
V_{DRM}	Peak Repetitive Off Stat Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak On State Voltage
I_H	Holding Current



CLASSIFICATION OF I_{GT}

RANK	B	C	AA	AB	AC	AD
RANGE	50-100 μ A	100-200 μ A	8-15 μ A	15-20 μ A	20-25 μ A	25-50 μ A

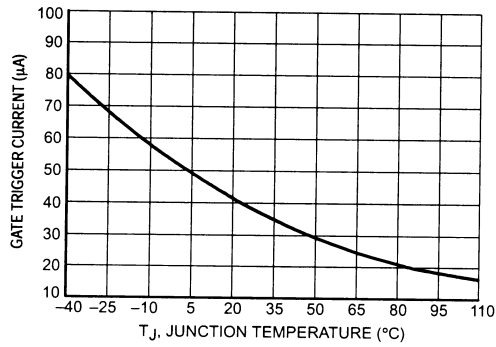


Figure 1. Typical Gate Trigger Current versus Junction Temperature

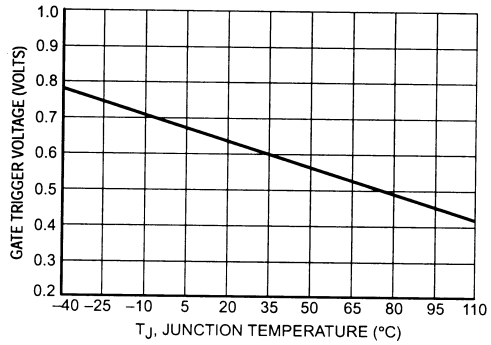


Figure 2. Typical Gate Trigger Voltage versus Junction Temperature

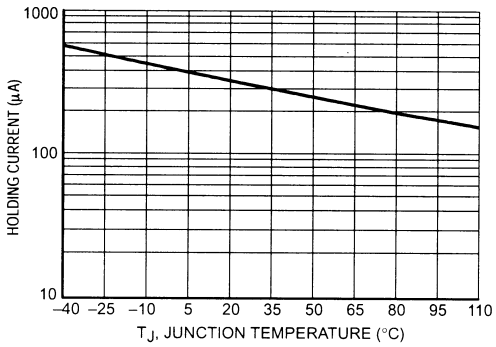


Figure 3. Typical Holding Current versus Junction Temperature

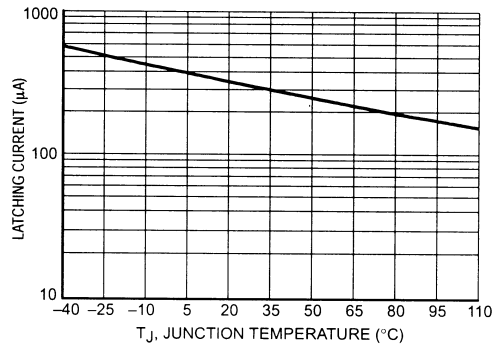


Figure 4. Typical Latching Current versus Junction Temperature

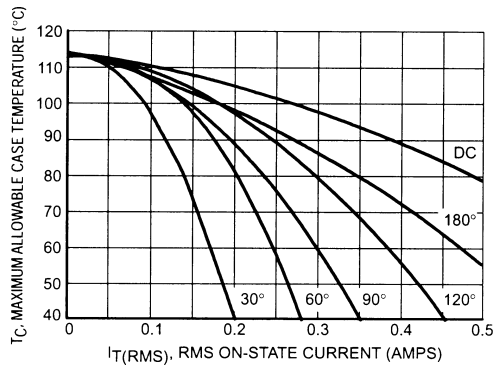


Figure 5. Typical RMS Current Derating

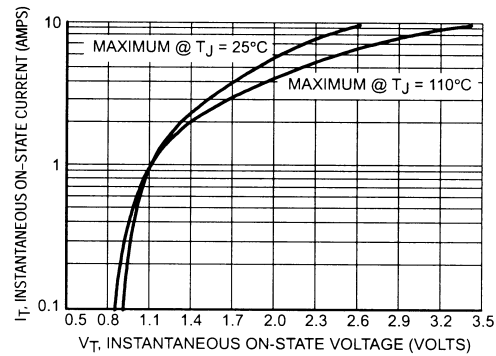


Figure 6. Typical On-State Characteristics