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## NTE1739 Integrated Circuit TV Horizontal/Vertical Countdown Digital Sync System

**Features:**

- Horizontal Oscillator
- Vertical Countdown
- Composite Blanking Output
- Burst-Gate Output
- Horizontal Ramp Generator
- Internal Shunt Regulator

**Description:**

The NTE1739 is a video sync system in a 16-Lead DIP type package designed for use in television, monitor or video display products. The NTE1739 contains a horizontal phase-locked oscillator and vertical countdown. It also features composite blanking and burst-gate outputs which, when externally summed, produce the sandcastle pulse necessary for the operation of most chroma/luma circuits.

The NTE1739 is intended for use in 525-line systems and operates with standard or nonstandard input signals. An automatic mode-recognition circuit forces operation into the nonsynchronous mode for nonstandard sync input signals.

**Absolute Maximum Ratings:**

DC Supply Current, Pin7 .....	50mA
Input Voltage (All Inputs) .....	-1V to V+ + 1V
Device Dissipation ( $T_A \leq +85^\circ\text{C}$ ) .....	900mW
Derate Linearly Above 85°C .....	14mW/°C
Operating Ambient Temperature Range .....	-40° to +85°C
Storage Temperature Range .....	-65° to +150°C
Lead Temperature (During Soldering, 1/16 ± 1/32 in. (1.59 ± 0.79mm) from case, 10s max) ...	+265°C

**Circuit Operation**

The master oscillator operates at 8 times the horizontal rate, fH, as determined by the external LC connected between Pin5 and Pin6. The master oscillator is divided by 2, 4, and 8 and is then fed to the horizontal output amplifier and also to a 10-stage vertical countdown circuit. Horizontal AFC is performed by comparing the horizontal ramp input signal on Pin2, derived from the flyback pulse, to the horizontal sync signal on Pin3, producing correction voltage. The correction voltage then is applied to the master oscillator to phase lock the system.

The divide by 2 and 4 outputs are used to drive a 10-stage counter for the vertical circuits. The use of the countdown system and associated logic circuits assures good noise immunity and the deletion of the vertical hold control.

### **Circuit Operation (Cont'd)**

The Gain/Window switch input on Pin10 is a logic input which controls the digital window in which the system looks for the occurrence of a vertical sync pulse: it also adjusts the phase detector gain for the two corresponding vertical windows. The 464th (Pin10 = low) or the 512th (Pin10 = high) clock pulse (at 2fH) from the horizontal divider is used to set the start of the vertical sync window. The end of the sync window occurs at the 592nd (Pin10 = low) or the 568th (Pin10 = High) clock pulse. If the incoming vertical sync pulse occurs regularly at the same time the 525th clock pulse occurs, it is used to generate the start of the vertical blanking and vertical sweep; the system is in the standard sync mode. If the incoming vertical sync pulse is absent (removed by noise, for example), the 10-stage counter will continue to provide an output pulse at the 525th clock pulse; a 3-bit counter will count the number of fields where no sync pulse occurred coincident with the 525th clock pulse. If no coincidence is detected in 8 sequential fields, the 3-bit counter energizes the toggle which shifts the mode of operation from standard sync to nonstandard sync.

In the nonstandard sync mode vertical scan is initiated by the incoming vertical sync pulse. Non standard sync operation results when the incoming vertical sync pulse occurs regularly within the vertical sync window; 464 to 592 counts (Pin10 = low) or 512 to 568 counts (Pin10 = high) but not at the 525th count (Standard Sync Mode). In the nonstandard sync mode if no sync pulse is present, the system will free run at a frequency determined by the 592 (Pin10 = low) or 568 (Pin10 = high) count.

The NTE1739 generates a composite blanking signal and a burst-gate (key pulse) which, when summed externally, produce the sandcastle pulse necessary for the operation of most Chrom/Luminance integrated circuits.

### **Electrical Characteristics:** ( $T_A = +25^\circ$ to $+70^\circ\text{C}$ unless otherwise specified)

Parameter	Pin	Test Conditions	Min	Typ	Max	Unit
Supply Current	7	Adjust 24V Supply for 7V on Pin7	7	–	14	mA
Regulator Voltage	7		7.0	–	8.6	V
Saturation Voltages						
Horizontal Output	8		0	–	0.4	V
Inverted Horizontal Output	13		0	–	0.4	V
Vertical Output	11		0	–	0.2	V
Blanking Output	12		0	–	0.175	V
Horizontal Ramp Output	15		0	–	0.175	V
Horizontal VCO Free Running Freq.	8	No Sync Applied $S_1 = B$	15547	–	15854	Hz
Horizontal VCO Oscillator Pull-In	8	For 15734 $\pm 1\text{Hz}$	–300	–	+300	Hz
Horizontal Blanking Width	12	Std NTSC Sync Applied	9.5	–	10.5	$\mu\text{s}$
Vertical Blanking Width	12	Std NTSC Sync Applied	1140	–	1148	$\mu\text{s}$
Burst Gate Width	16	Std NTSC Sync Applied	2.98	–	3.42	$\mu\text{s}$
Burst Gate Delay	16	From End of Horizontal Sync (Pin3) to Start of Burst Gate (Pin16)	20	–	215	ns
Horizontal Pulse Width	8	Std NTSC Sync Applied	31.4	–	32.1	$\mu\text{s}$
Vertical Pulse Width	11	Std NTSC Sync Applied	504	–	516	$\mu\text{s}$
Horizontal Sync Input	–		–	10	–	$V_{P-P}$
Vertical Sync Input	–		–	10	–	$V_{P-P}$

### Pin Connection Diagram

